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Panasonic

AN44071A

37V/1.0A&1.7A
Dual Microstepping Motor Driver

FEATURES

- 2-channel stepping motor driver
  A signal driver controls 2 stepping motors
- Built-in decoder for micro steps (2-phase, half step, 1-2 phase, W1-2 phase and 2W1-2 phase excitation)
  Stepping motor can be driven by only external clock signal.
- PWM can be driven by built-in CR (3-value can be selected during PWM OFF period.)
  The selection of PWM OFF period enables the best PWM drive.
- Mix Decay control (4-value can be selected for Fast Decay ratio)
  Mix Decay control can improve accuracy of motor current waveform.
- Built-in over-current protection (OCP)
  If the current flows to motor output more than the setup value due to ground-fault etc., the OCP operates and all motor outputs are turned OFF.
- Built-in under voltage lockout (UVLO)
  If supply voltage falls to less than the operating supply voltage range, the UVLO operates and all motor outputs are turned OFF.
- Built-in thermal protection (TSD)
  If chip junction temperature rises and reaches to the setup temperature, all motor outputs are turned OFF.
- Built-in abnormal detection output function
  If OCP or TSD operates, an abnormal detection signal is output.
- Built-in standby function
  The operation of standby function can lower current consumption of this LSI.
- Built-in Home Position function
  Home Position function can detect the position of motor.
- Built-in step detection output function
  If step detection output function detects clock input signal, it outputs a signal.
- Built-in 5 V power supply (accuracy : ±5%)
- 56 pin Plastic Small Outline Package With Heat Sink (SOP Type)

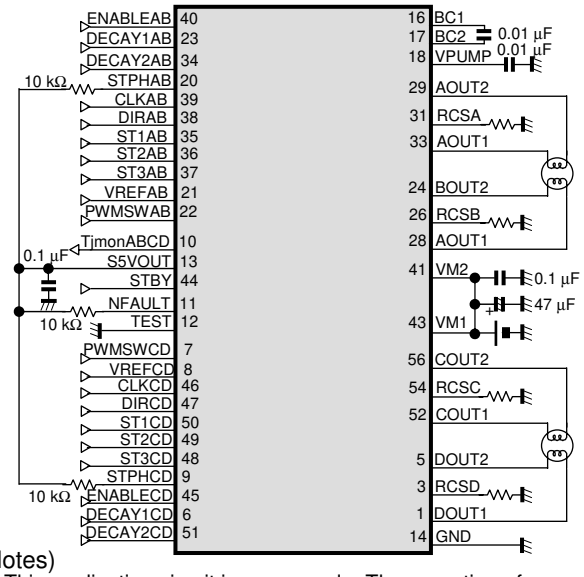
APPLICATIONS

- LSI for stepping motor drives

DESCRIPTION

AN44071A is a quad channel H-bridge driver LSI. Two bipolar stepping motor can be controlled by a single driver LSI. Interface control is 1CLK_type, it can be selected 2-phase excitation, half- step, 1-2 phase excitation, W1-2 phase excitation and 2W1-2 phase excitation.

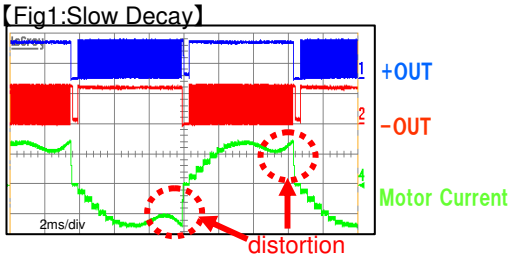
SIMPLIFIED APPLICATION



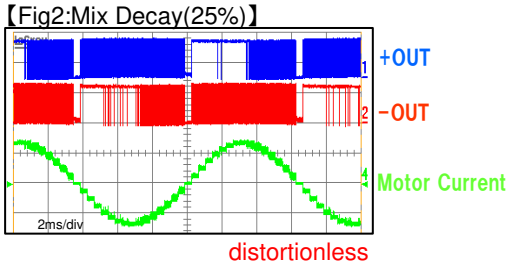
Notes)
This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

Mix Decay effect for Motor current

【Fig1:Slow Decay】



【Fig2:Mix Decay(25%)】



Condition:
excitation mode :2W1-2 phase drive
fig1 DECAY1=L DECAY2=L
fig2 DECAY1=L DECAY2=H

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage (Pin 41, 43)	V_M	37	V	*1
Power dissipation	P_D	448	mW	*2
Operating ambient temperature	T_{opr}	–20 to +85	°C	*3
Operating junction temperature	T_j	–20 to + 150	°C	*3
Storage temperature	T_{stg}	–55 to +150	°C	*3
Output pin voltage (Pin 1, 5, 24, 28, 29, 33, 52, 56)	V_{OUT}	37	V	*4
Motor drive current 1 (Pin 24, 28, 29, 33)	I_{OUT1}	±1.0	A	*5
Motor drive current 2 (Pin 1, 5, 52, 56)	I_{OUT2}	±1.7	A	*5
Flywheel diode current 1(Pin 24, 28, 29, 33)	I_{f1}	±1.0	A	*5
Flywheel diode current 2 (Pin 1, 5, 52, 56)	I_{f2}	±1.7	A	*5
Input Voltage Range	V_{RCSA},V_{RCSB},V_{RCSC},$V_{RCSD;}$	2.5	V	—
	$V_{DECAY2CD}$,$V_{DECAY2AB}$ $V_{DECAY1CD}$,$V_{DECAY1AB}$	-0.3 to 6	V	—
	$V_{PWMSWAB}$,$V_{PWMSWCD}$	-0.3 to 6	V	—
	V_{VREFAB},V_{VREFCD}	-0.3 to 6	V	—
	V_{STPHAB},V_{STPHCD}	-0.3 to 6	V	*6
	V_{NFAULT}	-0.3 to 6	V	*6
	V_{TEST}	-0.3 to 6	V	—
	V_{BC2}	(VM-1) to 43	V	*7
	V_{VPUMP}	(VM-2) to 43	V	*7
	V_{ST1AB},V_{ST2AB},V_{ST3AB} V_{ST1CD},V_{ST2CD},V_{ST3CD}	-0.3 to 6	V	—
	V_{DIRAB},V_{DIRCD}	-0.3 to 6	V	—
	V_{CLKAB},V_{CLKCD}	-0.3 to 6	V	—
	$V_{ENABLEAB}$,$V_{ENABLECD}$	-0.3 to 6	V	—
	V_{STBY}	-0.3 to 6	V	—
	I_{STPHAB},I_{STPHCD}	2	mA	*6
	I_{NFAULT}	2	mA	*6
	I_{S5VOUT}	-7 to 0	mA	—
ESD	HBM (Human Body Model)	±2	kV	—
	CDM (Charge Device Model)	±1	kV	—

Notes). This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.

When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : The power dissipation shown is the value at T_a = 85°C for the independent (unmounted) LSI package without a heat sink. When using this LSI, refer to the P_D-T_a diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

ABSOLUTE MAXIMUM RATINGS (continued)

Notes) *4 :This is a rated value of output voltage, and do not apply input voltage from outside to these pins. Set not to exceed the allowable range at any time.

*5 :Do not apply external current to any pin specially mentioned. For circuit currents, (+) denotes current flowing into the LSI and (–) denotes current flowing out of the LSI.

*6 :This pin is connected to open drain circuit inside. Connect a resistor in series with power supply.Do not exceed the rated value at any time. Refer to page 4 for the recommended value.

*7 :External voltage must not be applied to this pin. Do not exceed the rated value at any time.

POWER DISSIPATION RATING

Condition	θ_{JA}	PD (Ta=25 °C)	PD (Ta=85 °C)
Mount on PWB *1	79.5 °C/W	1572mW	818mW
Without PWB	144.9°C/W	863mW	448mW

Note). For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, supply voltage, load and ambient temperature conditions to ensure that there is enough margin follow the power and the thermal design does not exceed the allowable value.

*1: Glass-Epoxy: 50×50×0.8 (mm) , heat dissipation fin: Dai-pad , the state where it does not mount.

CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VM1,VM2	10	24	34	V	*1
Input Voltage Range	$V_{DECAY2CD}$,$V_{DECAY2AB}$ $V_{DECAY1CD}$,$V_{DECAY1AB}$	0	-	5.5	V	—
	$V_{PWMSWAB}$,$V_{PWMSWCD}$	0	-	5.5	V	—
	V_{VREFAB},V_{VREFCD}	0	-	5	V	—
	V_{TEST}	0	-	5.5	V	—
	V_{ST1AB},V_{ST2AB},V_{ST3AB} V_{ST1CD},V_{ST2CD},V_{ST3CD}	0	-	5.5	V	—
	V_{DIRAB},V_{DIRCD}	0	-	5.5	V	—
	V_{CLKAB},V_{CLKCD}	0	-	5.5	V	—
	$V_{ENABLEAB}$,$V_{ENABLECD}$	0	-	5.5	V	—
	V_{STBY}	0	-	5.5	V	—
External Constants	C_{BC}	-	0.01	-	µF	—
	C_{VPUMP}	-	0.01	-	µF	—
	C_{S5VOUT}	-	0.1	-	µF	—
Operating ambient temperature	Ta^{opr}	-20	-	85	°C	—
Operating junction temperature	Tj^{opr}	-	-	120	°C	—

Note) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

ELECRTRICAL CHARACTERISTICS

VM=24V, T_a = 25°C±2°C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Power block							
Output saturation voltage 1 High	V_{OH1}	I = –0.5 A (Pin 24, 28, 29, 33)	VM – 0.5	VM – 0.3	—	V	—
Output saturation voltage 1 Low	V_{OL1}	I = 0.5 A (Pin 24, 28, 29, 33)	—	0.48	0.75	V	—
Output saturation voltage 2 High	V_{OH2}	I = –0.8 A (Pin 1, 5, 52, 56)	VM – 0.55	VM – 0.35	—	V	—
Output saturation voltage 2 Low	V_{OL2}	I = 0.8 A (Pin 1, 5, 52, 56)	—	0.64	0.97	V	—
Flywheel diode forward voltage 1	V_{DI1}	I = 0.5 A (Pin 24, 28, 29, 33)	0.5	1	1.5	V	—
Flywheel diode forward voltage 2	V_{DI2}	I = 0.8 A (Pin 1, 5, 52, 56)	0.5	1	1.5	V	—
Upper-side output OFF current	$I_{OUTOFF1}$	V_M = 37 V, V_{RCS} = 0 V, OUT = 0 V	-10	—	—	µA	*1
Lower-side output OFF current	$I_{OUTOFF2}$	V_M = 37 V, V_{RCS} = 0 V, OUT = 37 V	—	—	100	µA	*1
Supply current							
Supply current (Active)	I_M	ENABLEAB = ENABLECD = Low, STBY = High	—	10	19	mA	—
Supply current (STBY)	I_{MSTBY}	STBY = Low	—	22	40	µA	—
I/O Block							
STBY High-level input voltage	V_{STBYH}	—	2.1	—	5.5	V	—
STBY Low-level input voltage	V_{STBYL}	—	0	—	0.6	V	—
STBY High-level input current	I_{STBYH}	STBY = 5 V	25	50	100	µA	—
STBY Low-level input current	I_{STBYL}	STBY = 0 V	– 2	—	2	µA	—
CLK High-level input voltage	V_{CLKH}	—	2.1	—	5.5	V	*2
CLK Low-level input voltage	V_{CLKL}	—	0	—	0.6	V	*2
CLK High-level input current	I_{CLKH}	CLK = 5 V	25	50	100	µA	*2
CLK Low-level input current	I_{CLKL}	CLK = 0 V	– 2	—	2	µA	*2
CLK maximum input frequency	f_{CLK}	—	50	—	—	kHz	*2
ENABLE High-level input voltage	$V_{ENABLEH}$	—	2.1	—	5.5	V	*3
ENABLE Low-level input voltage	$V_{ENABLEL}$	—	0	—	0.6	V	*3
ENABLE High-level input current	$I_{ENABLEH}$	ENABLE = 5 V	25	50	100	µA	*3
ENABLE Low-level input current	$I_{ENABLEL}$	ENABLE = 0 V	– 2	—	2	µA	*3

Notes) *1 :OUT represents AOUT1, AOUT2, BOUT1, BOUT2, COUT1, COUT2, DOUT1 and DOUT2.
*2 :CLK represents CLKAB and CLKCD.
*3 :ENABLE represents ENABLEAB and ENABLECD.

ELECRTRICAL CHARACTERISTICS (continued)

VM=24V, T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I/O Block (Continued)							
PWMSW High-level input voltage	V_{PWMSWH}	—	2.3	—	5.5	V	*4
PWMSW Middle-level input voltage	V_{PWMSWM}	—	1.3	—	1.7	V	*4
PWMSW Low-level input voltage	V_{PWMSWL}	—	0	—	0.6	V	*4
PWMSW High-level input current	I_{PWMSWH}	PWMSW = 5 V	40	83	150	µA	*4
PWMSW Low-level input current	I_{PWMSWL}	PWMSW = 0 V	–70	–36	–18	µA	*4
PWMSW open voltage	V_{PWMSWO}	—	1.3	1.5	1.7	V	*4
DECAY High-level input voltage	V_{DECAYH}	—	2.1	—	5.5	V	*5
DECAY Low-level input voltage	V_{DECAYL}	—	0	—	0.6	V	*5
DECAY High-level input current	I_{DECAYH}	DECAY = 5 V	25	50	100	µA	*5
DECAY Low-level input current	I_{DECAYL}	DECAY = 0 V	– 2	—	2	µA	*5
DIR High-level input voltage	V_{DIRH}	—	2.1	—	5.5	V	*6
DIR Low-level input voltage	V_{DIRL}	—	0	—	0.6	V	*6
DIR High-level input current	I_{DIRH}	DIR = 5 V	25	50	100	µA	*6
DIR Low-level input current	I_{DIRL}	DIR = 0 V	– 2	—	2	µA	*6
ST High-level input voltage	V_{STH}	—	2.1	—	5.5	V	*7
ST Low-level input voltage	V_{STL}	—	0	—	0.6	V	*7
ST High-level input current	I_{STH}	ST = 5 V	25	50	100	µA	*7
ST Low-level input current	I_{STL}	ST = 0 V	– 2	—	2	µA	*7
Torque Control Block							
Input bias current 1	I_{REFH}	V_{REFAB} = V_{REFCD} = 5 V	– 2	—	2	µA	—
Input bias current 2	I_{REFL}	V_{REFAB} = V_{REFCD} = 0 V	– 2	—	2	µA	—
PWM OFF time 1	T_{OFF1}	PWMSW = Low	16.8	28	39.2	µs	*4
PWM OFF time 2	T_{OFF2}	PWMSW = High	9.1	15.2	21.3	µs	*4
PWM OFF time 3	T_{OFF3}	PWMSW = Middle	4.9	8.1	11.3	µs	*4
Pulse blanking time	T_B	V_{REFAB} = V_{REFCD} = 0 V	0.4	0.7	1.0	µs	—
Comp threshold	VT_{CMP}	V_{REFAB} = V_{REFCD} = 5 V	475	500	525	mV	—
Reference voltage block							
Reference voltage	V_{S5VOUT}	I_{S5VOUT} = 0 mA	4.75	5.0	5.25	V	—
Output impedance	Z_{S5VOUT}	I_{S5VOUT} = –7 mA	—	—	10	Ω	—

Notes) *4 : PWMSW represents PWMSWAB and PWMSWCD.
*5 : DECAY represents DECAY1AB, DECAY2AB, DECAY1CD and DECAY2CD.
*6 : DIR represents DIRAB and DIRCD.
*7 : ST represents ST1AB, ST2AB, ST3AB, ST1CD, ST2CD and ST3CD.

ELECRTRICAL CHARACTERISTICS（continued）

VM=24V,T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Abnomal detection output block							
NFAULT pin output Low-level voltage	$V_{NFAULTL}$	I_{NFAULT} = 1 mA	—	—	0.2	V	—
NFAULT pin output leak current	$I_{NFAULT(leak)}$	V_{NFAULT} = 5 V	—	—	5	µA	—
Home Position/ STEP detection output block							
STPH pin output Low-level voltage	V_{STPHL}	I_{STPH} = 1 mA	—	—	0.2	V	*8
STPH pin output leak current	$I_{STPH(leak)}$	V_{STPH} = 5 V	—	—	5	µA	*8
Test input block							
TEST High-level input voltage	V_{TESTH}	—	4.0	—	5.5	V	—
TEST Low-level input voltage	V_{TESTL}	—	0	—	0.6	V	—
TEST High-level input current	I_{TESTH}	TEST = 5 V	25	50	100	µA	—
TEST High-level input current	I_{TESTL}	TEST = 0 V	– 2	—	2	µA	—

*8 : STPH represents STPHAB and STPHCD.

ELECRTRICAL CHARACTERISTICS（continued）

VM=24V,T_a = 25°C±2°C unless otherwise noted.

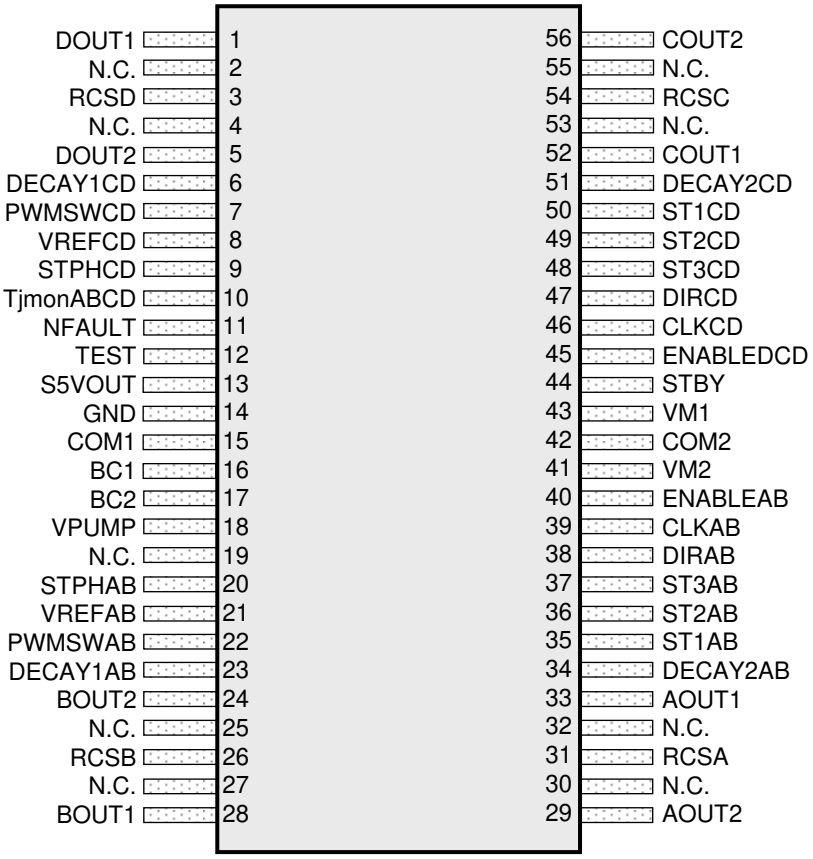
Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Output block							
Output slew rate 1	VT_r	At the rising edge of output voltage, sink side of motor current	—	350	—	V/µs	*9 *10
Output slew rate 2	VT_f	At the falling edge of output voltage, sink side of motor current	—	-400	—	V/µs	*9 *10
Dead time	T_D	—	—	0.8	—	µs	*9 *10
Thermal shutdown protection							
Thermal shutdown protection operating temperature	TSD_{on}	—	—	150	—	°C	*10
Under voltage lockout							
Protection start voltage	V_{UVLO1}	—	—	7.5	—	V	*10
Protection stop voltage	V_{UVLO2}	—	—	8.5	—	V	*10

*9 :The characteristics of all outputs of AOUT1, AOUT2, BOUT1, BOUT2, COUT1, COUT2, DOUT1 and DOUT2 are shown.

*10 :Typical Value checked by design.

PIN CONFIGURATION

Top View



PIN FUNCTIONS

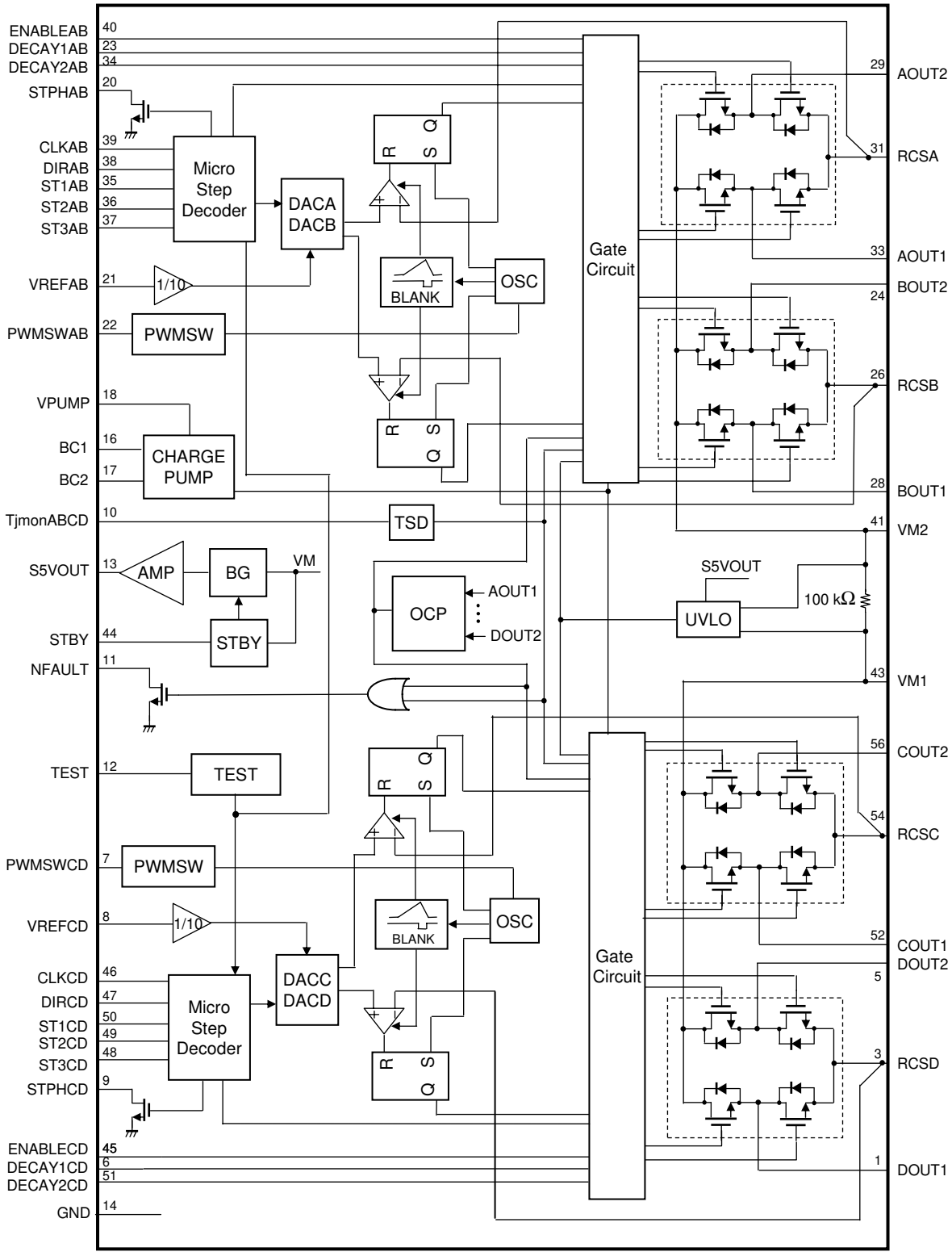
Pin No.	Pin name	Type	Description
1	DOUT1	Output	Phase D motor drive output 1
2, 4,19, 25, 27,30, 32,53, 55	N.C.	—	N.C.
3	RCSD	Input/Output	Phase D motor current detection
5	DOUT2	Output	Phase D motor drive output 2
6	DECAY1CD	Input	Phase C/D Mix Decay setup 1
7	PWMSWCD	Input	Phase C/D PWM OFF period selection input
8	VREFCD	Input	Phase C/D Torque reference voltage input
9	STPHCD	Output	Phase C/D Home Position / Step detection signal output
10	TjmonABCD	Output	Phase A/B, C/D VBE monitor
11	NFAULT	Output	Abnormal detection output
12	TEST	Input	Test mode setup
13	S5VOUT	Output	Internal reference voltage (output 5 V)
14	GND	Ground	Ground
15	COM1	—	Die pad ground 1
16	BC1	Output	Capacitor connection 1 for charge pump
17	BC2	Output	Capacitor connection 2 for charge pump
18	VPUMP	Output	Charge pump circuit output
20	STPHAB	Output	Phase A/B Home Position / Step detection signal output
21	VREFAB	Input	Phase A/B Torque reference voltage input
22	PWMSWAB	Input	Phase A/B PWM OFF period selection input
23	DECAY1AB	Input	Phase A/B Mix Decay setup 1
24	BOUT2	Output	Phase B motor drive output 2
26	RCSB	Input/Output	Phase B motor current detection
28	BOUT1	Output	Phase B motor drive output 1

PIN FUNCTIONS (continued)

Pin No.	Pin name	Type	Description
29	AOUT2	Output	Phase A motor drive output 2
31	RCSA	Input/Output	Phase A motor current detection
33	AOUT1	Output	Phase A motor drive output 1
34	DECAY2AB	Input	Phase A/B Mix Decay setup 2
35	ST1AB	Input	Phase A/B excitation selection 1
36	ST2AB	Input	Phase A/B excitation selection 2
37	ST3AB	Input	Phase A/B excitation selection 3
38	DIRAB	Input	Phase A/B rotation direction setup
39	CLKAB	Input	Phase A/B clock input
40	ENABLEAB	Input	Phase A/B Enable / disable CTL
41	VM2	Power supply	Power supply 2 for motor
42	COM2	—	Die pad ground 2
43	VM1	Power supply	Power supply 1 for motor
44	STBY	Input	Standby
45	ENABLECD	Input	Phase C/D Enable / disable CTL
46	CLKCD	Input	Phase C/D clock input
47	DIRCD	Input	Phase C/D rotation direction setup
48	ST3CD	Input	Phase C/D excitation selection 3
49	ST2CD	Input	Phase C/D excitation selection 2
50	ST1CD	Input	Phase C/D excitation selection 1
51	DECAY2CD	Input	Phase C/D Mix Decay setup 2
52	COUT1	Output	Phase C motor drive output 1
54	RCSC	Input/Output	Phase C motor current detection
56	COUT2	Output	Phase C motor drive output 2

Notes) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

FUNCTIONAL BLOCK DIAGRAM



Note) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

OPERATION

1. Control mode

Note) * is AB or CD.

1) Truth table (Excitation select)

ENABLE*	DIR*	ST1*	ST2*	ST3*	Output excitation mode	
Low	—	—	—	—	—	Output OFF
High	Low	Low	Low	Low	Phase B/D 90° delay to phase A/C	2-phase excitation drive (4-step sequence)
High	Low	Low	High	Low		Half step drive (8-step sequence)
High	Low	High	Low	Low		1-2 phase excitation drive (8-step sequence)
High	Low	High	High	Low		W1-2 phase excitation drive (16-step sequence)
High	Low	—	—	High		2W1-2 phase excitation drive (32-step sequence)
High	High	Low	Low	Low	Phase B/D 90° advance to phase A/C	2-phase excitation drive (4-step sequence)
High	High	Low	High	Low		Half step drive (8-step sequence)
High	High	High	Low	Low		1-2 phase excitation drive (8-step sequence)
High	High	High	High	Low		W1-2 phase excitation drive (16-step sequence)
High	High	—	—	High		2W1-2 phase excitation drive (32-step sequence)

2) Truth table (Control / Charge pump circuit)

STBY	ENABLE*	Control / Charge pump circuit	Output transistor
Low	—	OFF	All channel output : OFF
High (*3)	Low	ON	OFF (*4)
High (*3)	High	ON	ON

3) Truth table (PWM OFF period selection)

PWMSW*	PWM OFF period (*5)
Low	28.0 µ s
Middle	8.1 µ s
High	15.2 µ s

4) Truth table (Decay selection)

DECAY1*	DECAY2*	Decay control (*6)
Low	Low	Slow Decay
Low	High	25%
High	Low	50%
High	High	100%

Note) The above rate is applied to Fast Decay every PWM OFF period.

5) Truth table (STPH output selection)

TEST	STPH* output
Low	STEP detection output
High	Home Position output

6) Truth table (NFAULT output)

TSD (*1)	OCP (*2)	NFAULT	Output transistor
Thermal shutdown protection start	—	Low	All channel output : OFF
—	Over-current detection start	Low	All channel output : OFF
Thermal shutdown protection stop	Over-current detection stop	Hi-Z	ON

Notes) *1 : TSD is a latch type protection

→ The protection operation starts at 150°C. (All motor outputs are turned off , and latched.) / The latch is released by Standby or UVLO.

*2 : OCP is a latch type protection

→ All motor outputs are turned off by over-current detection, and be latched. / The latch is released by Standby or UVLO. In addition, All motor outputs are turned off at under UVLO.

*3 : Input external signals to STBY pin in order to set STBY signal to High-level. Because, STBY pin cannot be set to High-level when it is connected to S5VOUT(Pin13).

*4 : The output transistors of AB/CD channel are controlled by ENABLEAB/CD respectively.

*5 : The PWM OFF intervals of AB/CD channel are set by PWMSWAB/CD respectively.

*6 : The Decay controls of AB/CD channel are set by DECAY1AB/CD (DECAY2AB/CD) respectively.

OPERATION (continued)

2. Each phase current value

1) 1-2 phase, W1-2 phase, 2W1-2 phase DIRAB / DIRCD = Low

Note) The definition of Phase A, B, C and D current "100%" : (VREFAB(VREFCD) × 0.1) / Motor current detection resistance

1-2 phase (8-Step)	W1-2 phase (16- Step)	2W1-2 phase (32-Step)	A/C phase current (%)	B/D phase current (%)
1	1	1	70.7	–70.7
—	—	2	83.2	–55.6
—	2	3	92.4	–38.3
—	—	4	98.1	–19.5
2	3	5	100	0
—	—	6	98.1	19.5
—	4	7	92.4	38.3
—	—	8	83.2	55.6
3	5	9	70.7	70.7
—	—	10	55.6	83.2
—	6	11	38.3	92.4
—	—	12	19.5	98.1
4	7	13	0	100
—	—	14	–19.5	98.1
—	8	15	–38.3	92.4
—	—	16	–55.6	83.2
5	9	17	–70.7	70.7
—	—	18	–83.2	55.6
—	10	19	–92.4	38.3
—	—	20	–98.1	19.5
6	11	21	–100	0
—	—	22	–98.1	–19.5
—	12	23	–92.4	–38.3
—	—	24	–83.2	–55.6
7	13	25	–70.7	–70.7
—	—	26	–55.6	–83.2
—	14	27	–38.3	–92.4
—	—	28	–19.5	–98.1
8	15	29	0	–100
—	—	30	19.5	–98.1
—	16	31	38.3	–92.4
—	—	32	55.6	–83.2

OPERATION (continued)

2. Each phase current value (continued)

2) 1-2 phase, W1-2 phase, 2W1-2 phase DIRAB / DIRCD = High

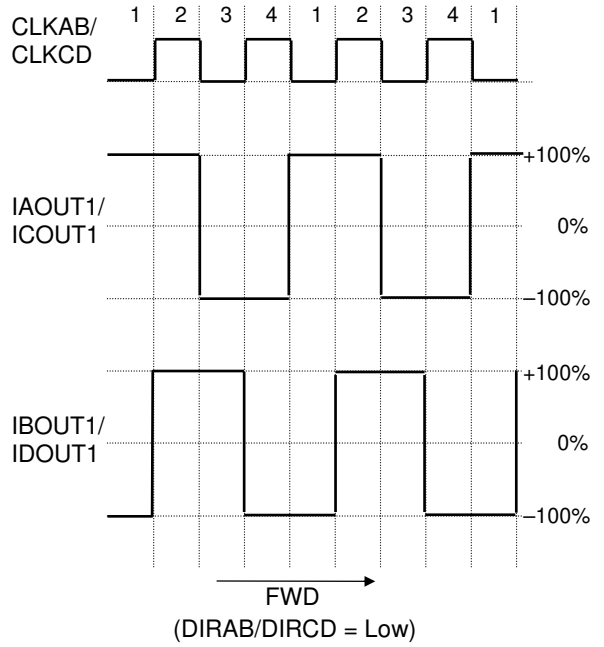
Note) The definition of Phase A, B, C and D current "100%" : (VREFAB(VREFCD) × 0.1) / Motor current detection resistance

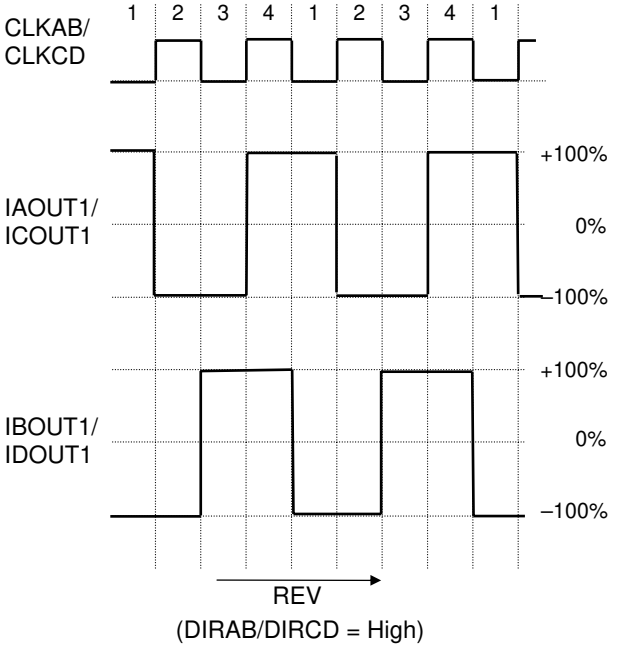
1-2 phase (8-Step)	W1-2 phase (16-Step)	2W1-2 phase (32-Step)	A/C phase current (%)	B/D phase current (%)
1	1	1	70.7	–70.7
—	—	2	55.6	–83.2
—	2	3	38.3	–92.4
—	—	4	19.5	–98.1
2	3	5	0	–100
—	—	6	–19.5	–98.1
—	4	7	–38.3	–92.4
—	—	8	–55.6	–83.2
3	5	9	–70.7	–70.7
—	—	10	–83.2	–55.6
—	6	11	–92.4	–38.3
—	—	12	–98.1	–19.5
4	7	13	–100	0
—	—	14	–98.1	19.5
—	8	15	–92.4	38.3
—	—	16	–83.2	55.6
5	9	17	–70.7	70.7
—	—	18	–55.6	83.2
—	10	19	–38.3	92.4
—	—	20	–19.5	98.1
6	11	21	0	100
—	—	22	19.5	98.1
—	12	23	38.3	92.4
—	—	24	55.6	83.2
7	13	25	70.7	70.7
—	—	26	83.2	55.6
—	14	27	92.4	38.3
—	—	28	98.1	19.5
8	15	29	100	0
—	—	30	98.1	–19.5
—	16	31	92.4	–38.3
—	—	32	83.2	–55.6

OPERATION (continued)

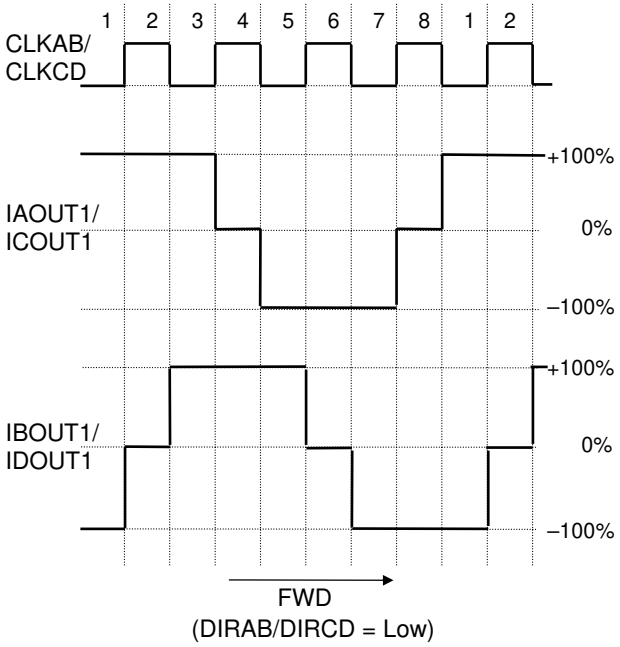
3. Each phase current value(Timing chart)

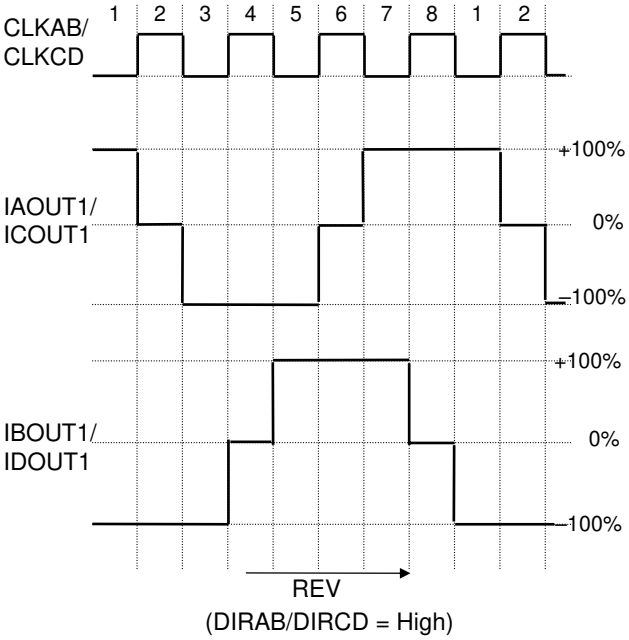
1) 2-phase excitation drive (4-step sequence)
(ST1AB/ST1CD = Low, ST2AB/ST2CD = Low, ST3AB/ST3CD = Low)





2) Half step drive (8-step sequence)
(ST1AB/ST1CD = Low, ST2AB/ST2CD = High, ST3AB/ST3CD = Low)

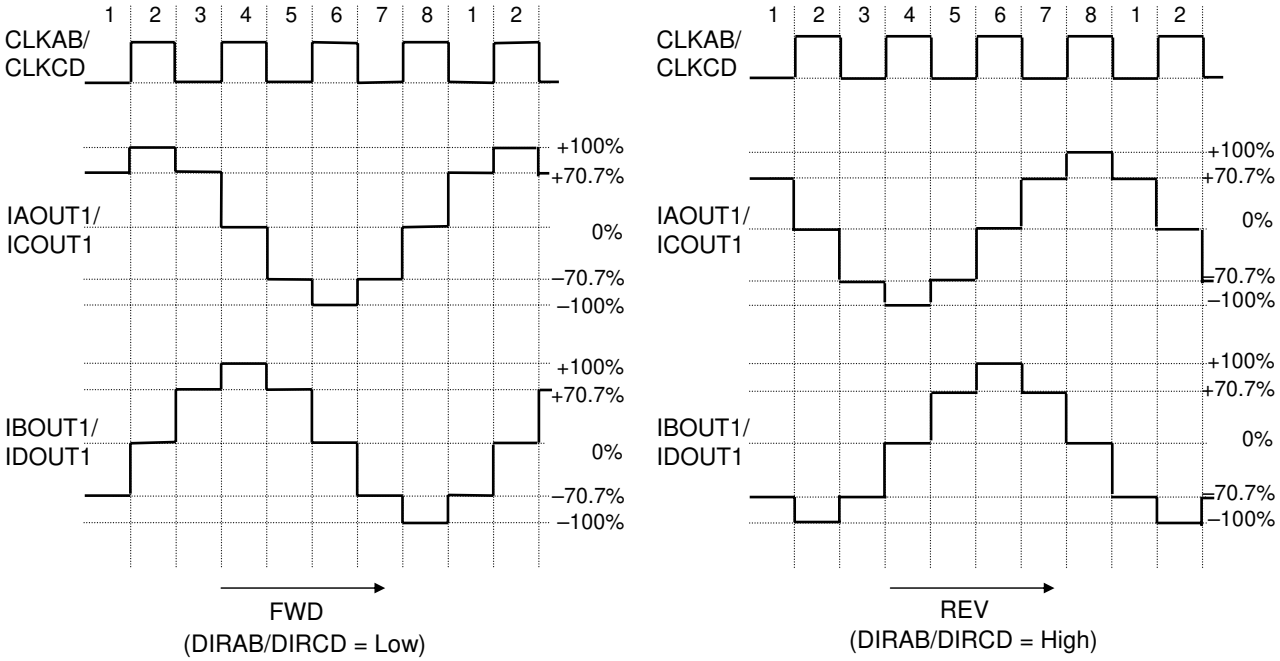




OPERATION (countinued)

3. Each phase current value (Timing chart) (continued)

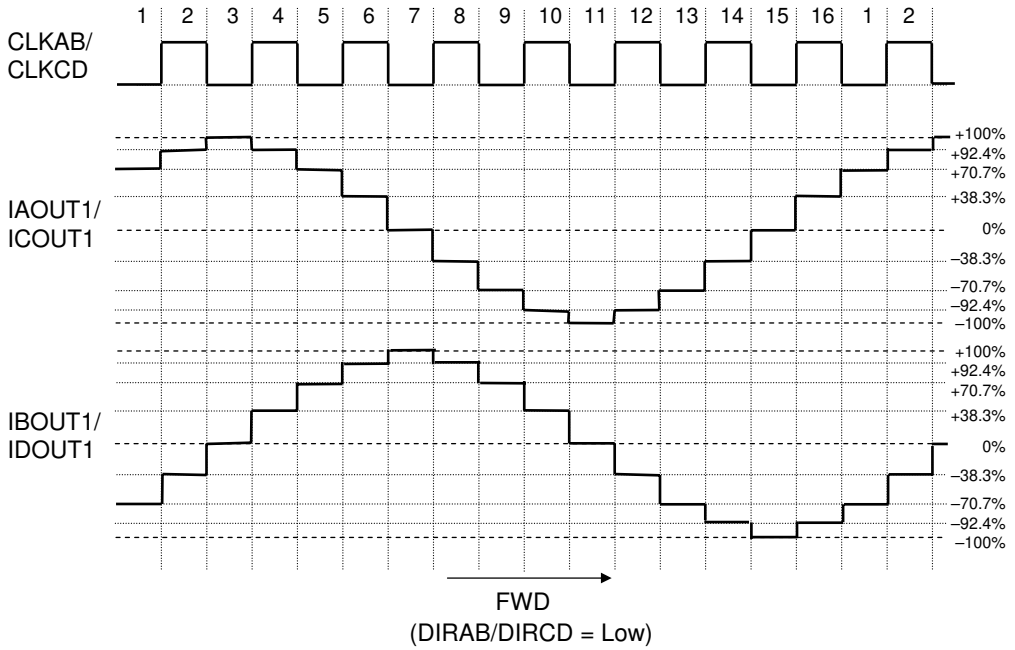
3) 1-2-phase excitation (8-step sequence)
(ST1AB/ST1CD = High, ST2AB/ST2CD = Low, ST3AB/ST3CD = Low)

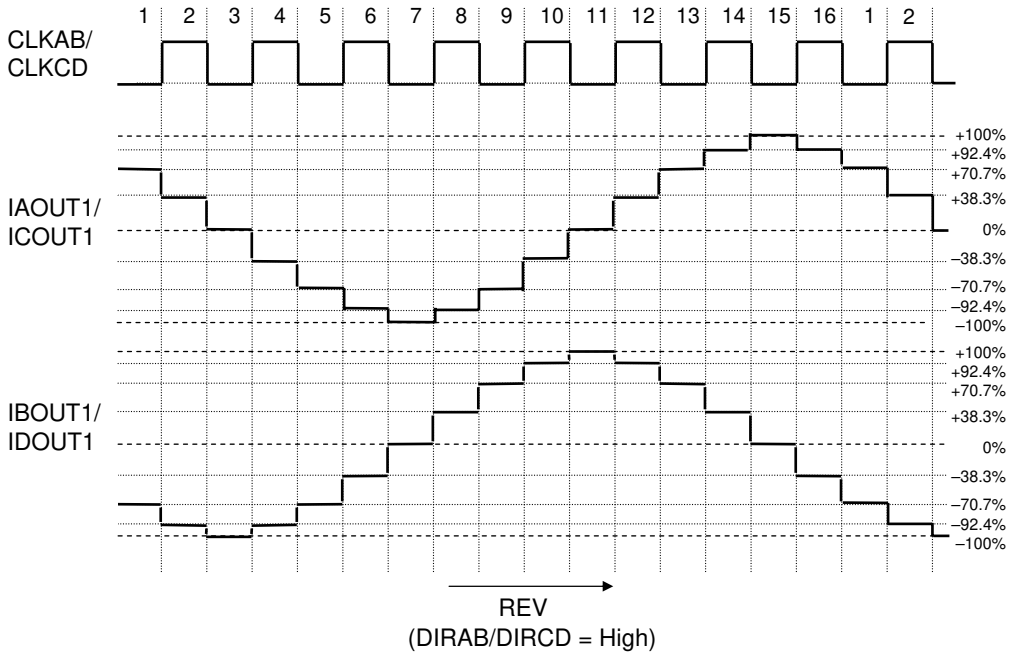


OPERATION (countinued)

3. Each phase current value (Timing chart) (continued)

4) W1-2-phase excitation (16-step sequence)
(ST1AB/ST1CD = High, ST2AB/ST2CD = High, ST3AB/ST3CD = Low)

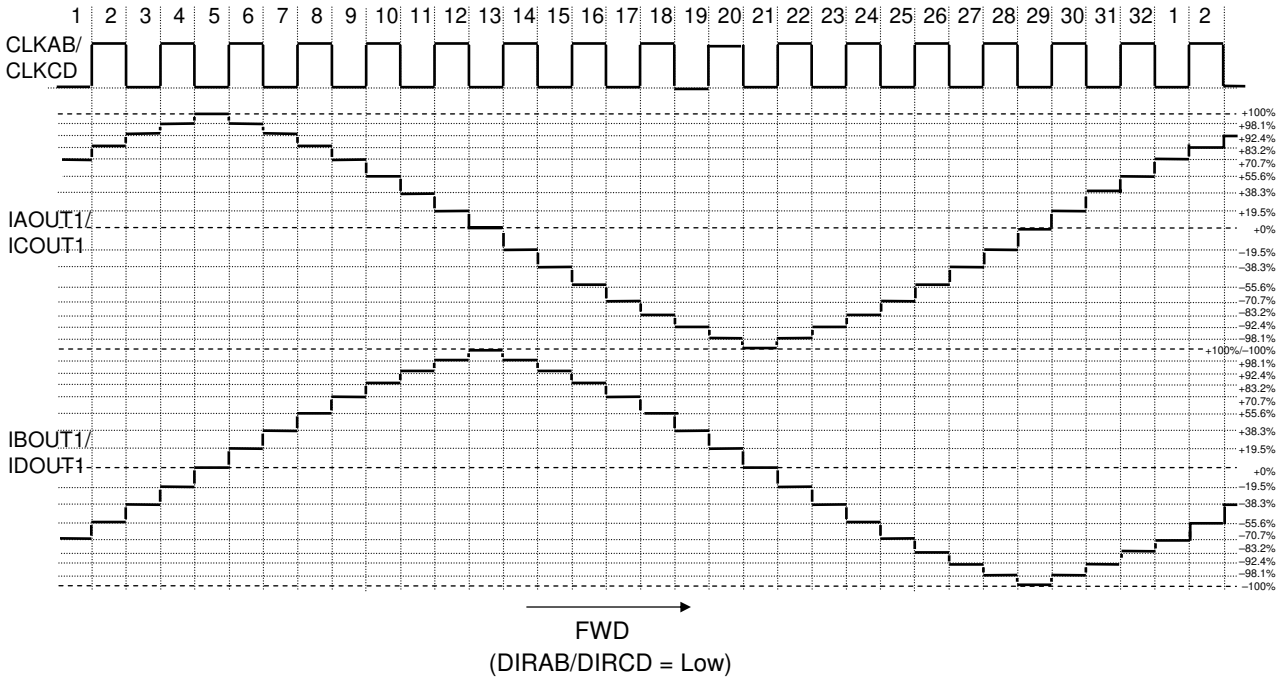




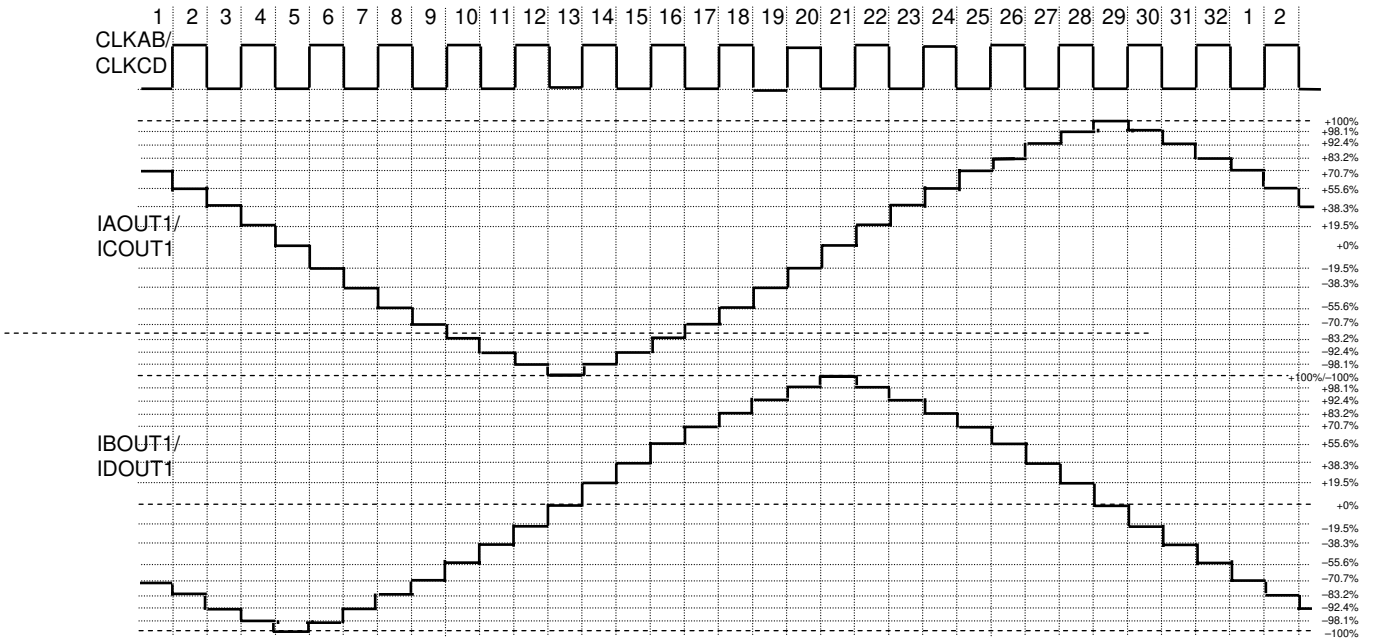
OPERATION (continued)

3. Each phase current value (Timing chart) (continued)

5) 2W1-2-phase excitation (32-step sequence)
(ST3AB/ST3CD = High)



FWD
(DIRAB/DIRCD = Low)

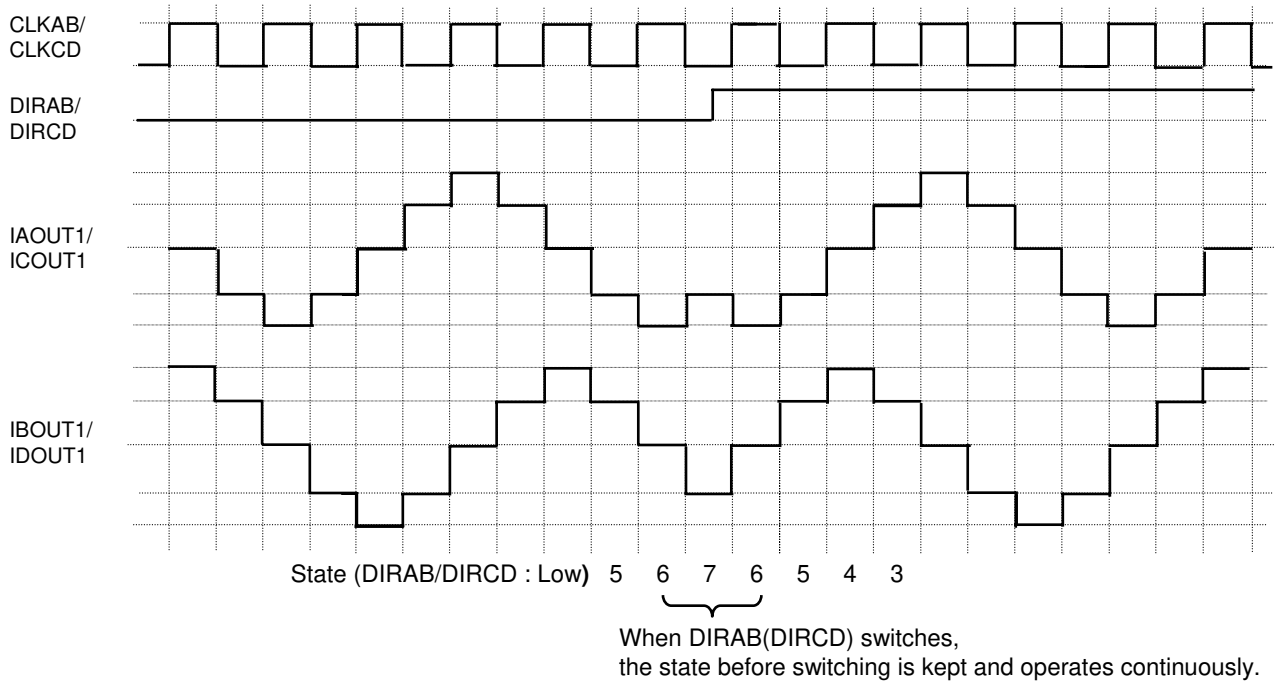


REV
(DIRAB/DIRCD = High)

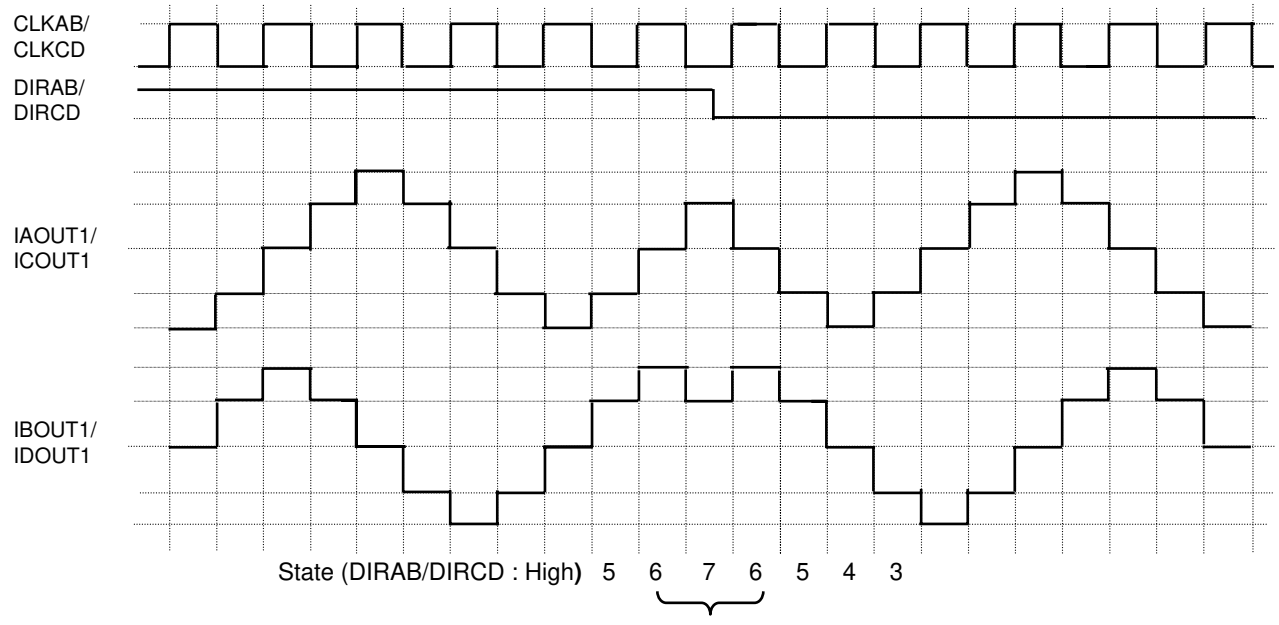
OPERATION (continued)

4. Timing chart when DIR switches

(Example 1) Timing chart at 1-2-phase excitation (DIRAB/DIRCD : Low → High)



(Example 2) Timing chart at 1-2-phase excitation (DIRAB/DIRCD : High → Low)



OPERATION (continued)

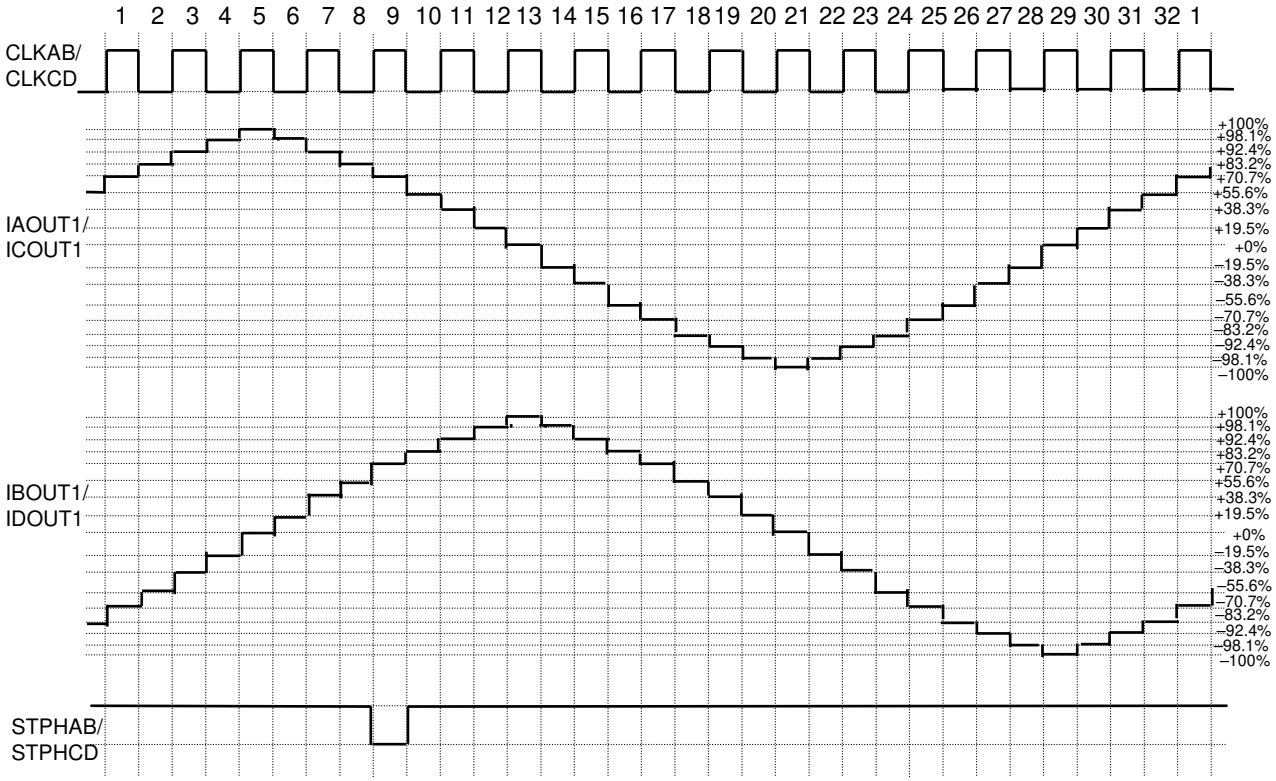
5. Home Position function (TEST=High)

This LSI has built-in Home Position function to reduce the displacement of motor current state at the change of excitation mode during motor drive. Low-level voltage is output to STPHAB pin and STPHCD pin at the timing when the displacement of motor current state doesn't occur at the change of excitation mode. The timing when Low-level voltage is output to STPHAB pin and STPHCD pin is as follows. The Home Position function becomes valid by setting TEST pin to High.

Connect pull-up resistor to power supply (recommendation : S5VOUT), because STPHAB pin and STPHCD pin are composed by open drain circuit. The recommended value of pull-up resistor is 10 kΩ.

Home Position output timing chart (DIRAB / DIRCD = Low)

1) 2W1-2-phase excitation

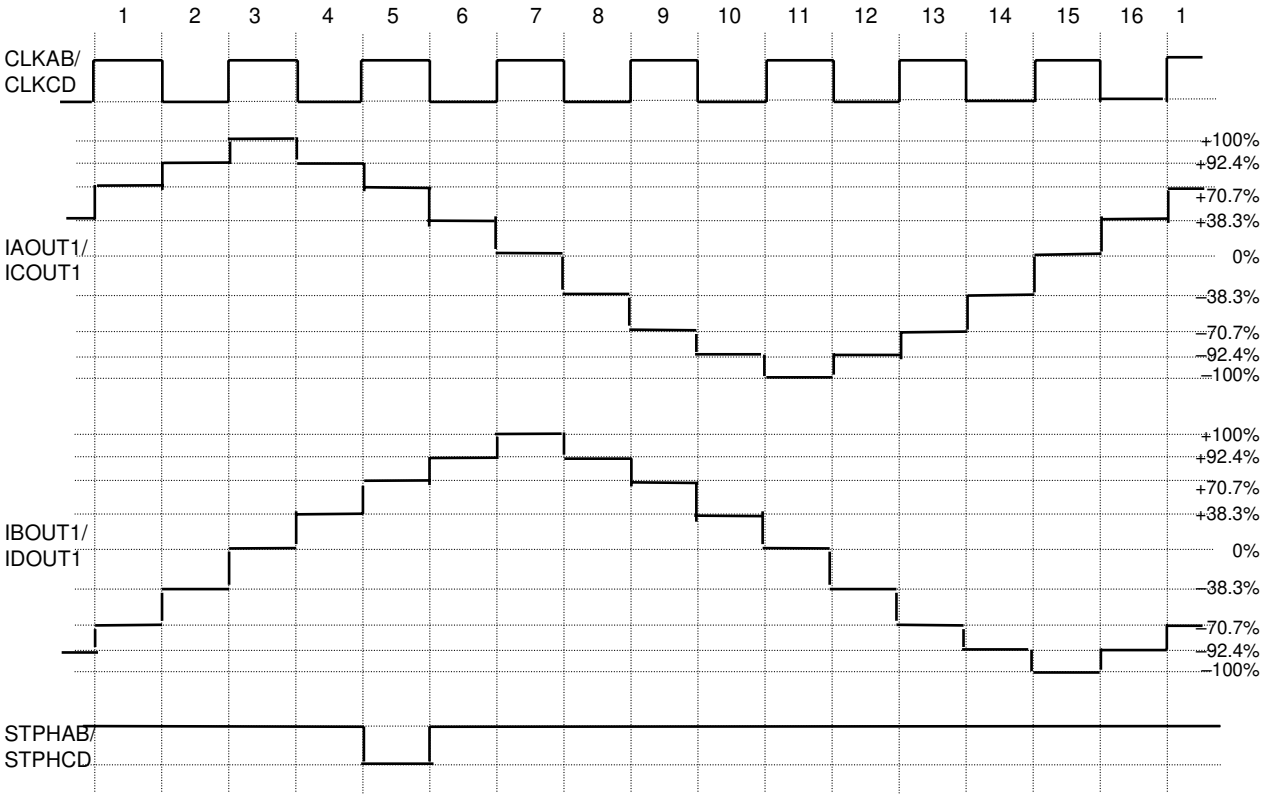


OPERATION (continued)

5. Home Position function(TEST=High)(continued)

Home Position output timing chart (DIRAB / DIRCD = Low) (continued)

2) W1-2-phase excitation

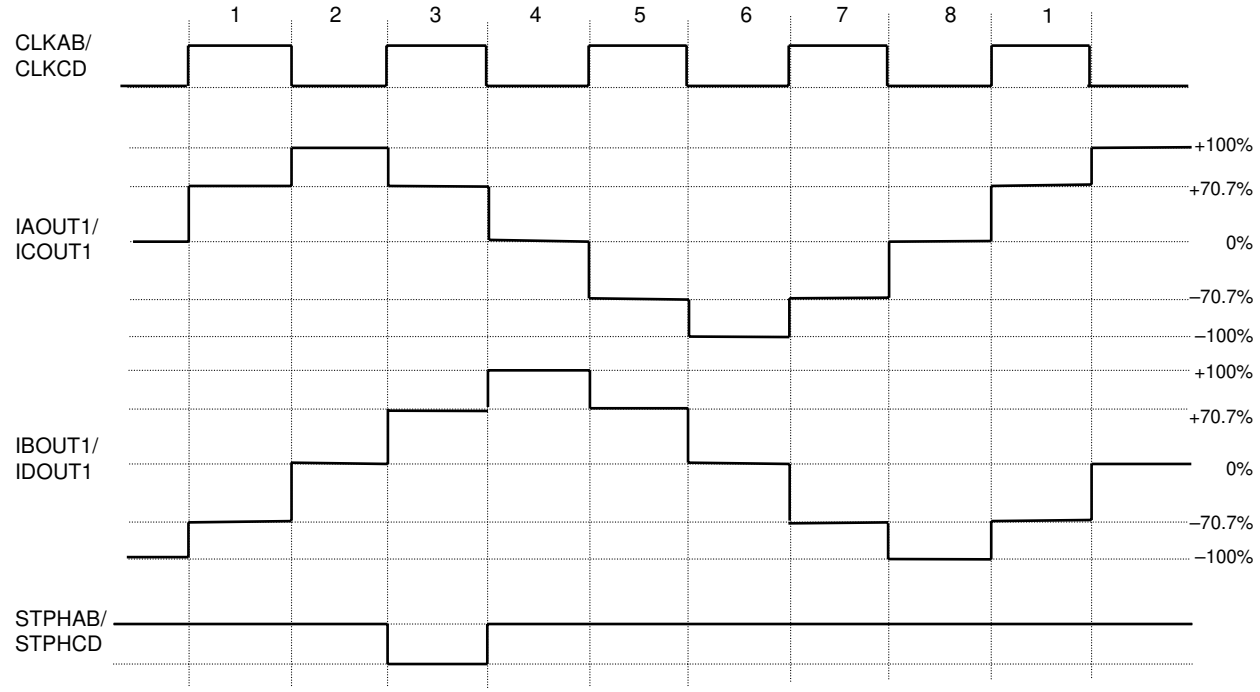


OPERATION (continued)

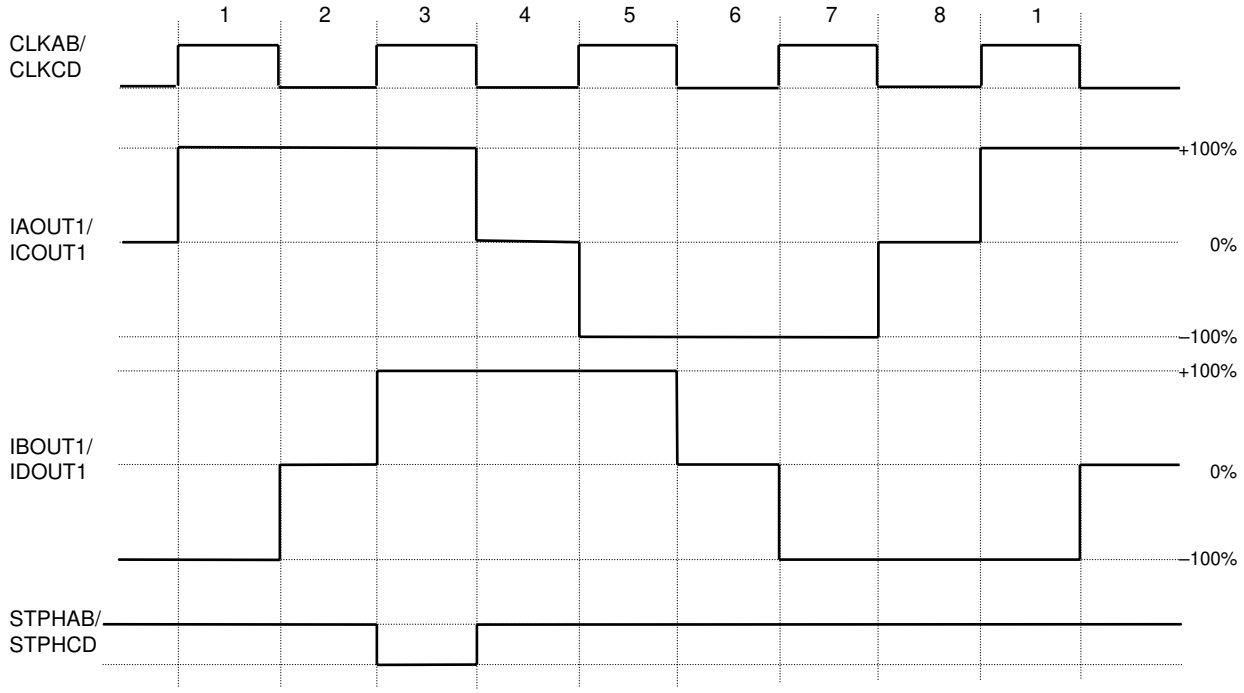
5. Home Position function (TEST=High) (continued)

Home Position output timing chart (DIRAB / DIRCD = Low)(continued)

3) 1-2-phase excitation



4) Half step

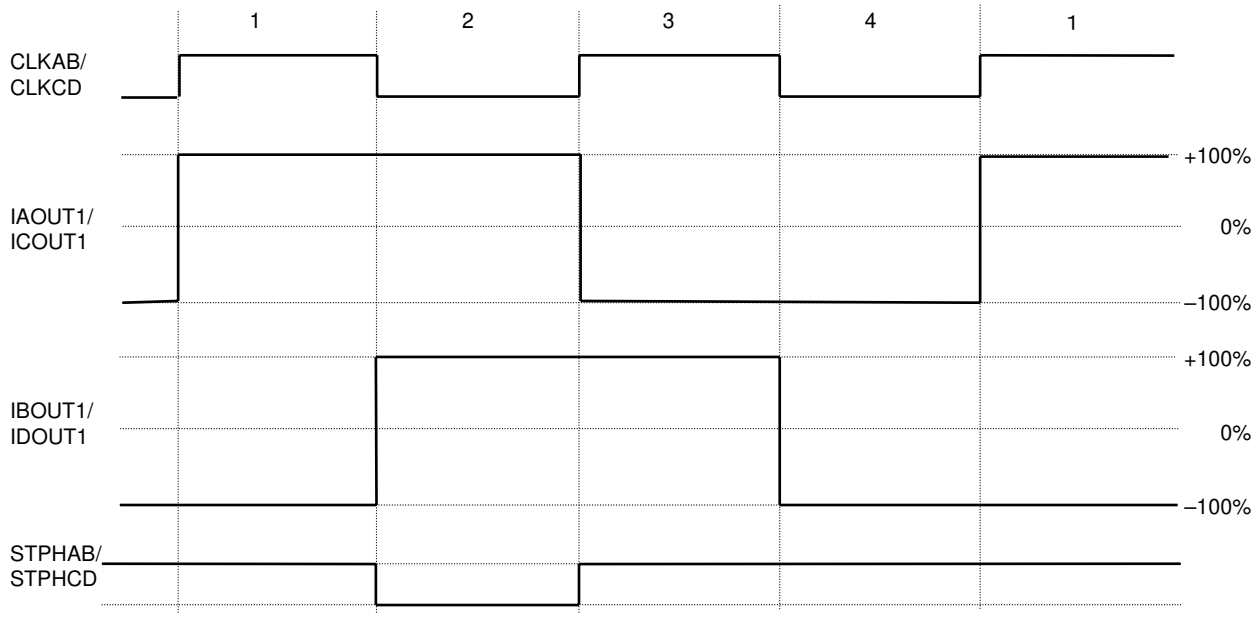


OPERATION (continued)

5. Home Position function (TEST=High) (continued)

Home Position output timing chart (DIRAB / DIRCD = Low) (continued)

5) 2-phase excitation



OPERATION (continued)

6. STEP detection output function (TEST = Low)

Whenever edges signal is input into clock input pins, this LSI outputs Low pulse signal from step detection output pins. The Low pulse width depend on each excitation mode. Refer to the below table. The STEP detection function becomes valid by setting TEST pin to Low. Connect pull-up resistor to supply voltage (Recommendation : S5VOUT), because STPHAB pin and STPHCD pin are composed by open drain circuit. The recommended value of pull-up resistor is 10 kΩ.

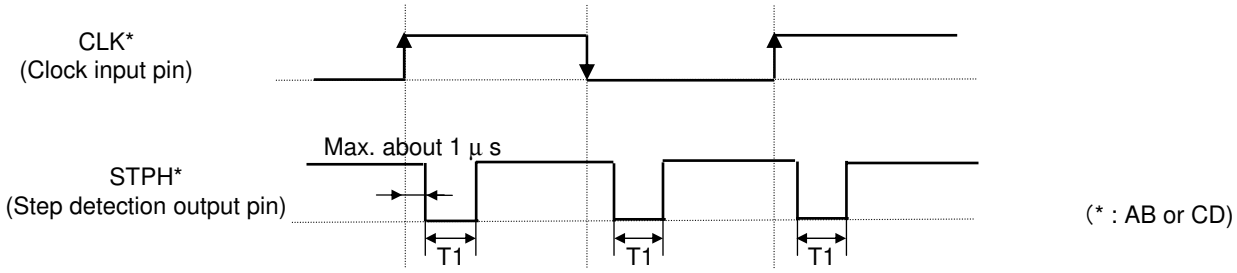


Table Step detection output pulse width

	2-phase excitation	Half step / 1-2 phase excitation	W1-2-phase excitation	2W1-2-phase excitation
Pulse width (T1)	About 20 µs	About 20 µs	About 10 µs	About 5 µs

7. Over-current protection function

This LSI has over-current protection (OCP) circuit to protect from the ground-fault etc. of the motor output. When motor current more than setting value flows to power MOS for about 3.8 µ s (Typ.) due to the ground-fault, all motor outputs are turned OFF by latch operation. OCP is canceled by STBY = Low or UVLO (Under-voltage lockout) operation. However, the OCP circuit do not guaranteed the protection circuit of set. Therefore, do not use the OCP function of this LSI to protect a set. Note that this LSI might break before the protection function operates when it instantaneously exceeds the safe operation area and the maximum rating. When the inductor element is large due to the length of wiring at ground-fault, note that this LSI might break. Because the motor output voltage falls on a negative voltage or excessively rises after motor current excessively flows to motor outputs. The setup current of the OCP (reference) is as follows.

Table Over-current protection setup current (Typ. value)

	A/Bch motor output	C/Dch motor output
Setup current	2.2 A	3.3 A

8. About inputting the supply voltage to IF pins when VM power supply is not applied.

This LSI does the measures of error for inputting voltage to IF pins when VM power supply is not applied.

IF pin : ENABLE*, DIR*, ST1*, ST2*, ST3*, CLK*, STBY, VREF* (* : AB or CD)

Therefore, this LSI doesn't break and it doesn't cause error operation by the input voltage to the IF pins when VM supply voltage is not supplied.

APPLICATIONS INFORMATION

1. Notes

1) Pulse blanking time
This LSI has pulse blanking time (0.7 µs/Typ. value) to prevent erroneous current detection caused by noise. Therefore, the motor current value will not be less than current determined by pulse blanking time. Pay attention at the time of low current control. The relation between pulse blanking time and minimum current value is shown as Chart 1. In addition, increase-decrease of motor current value is determined by L value, wire wound resistance, induced voltage and PWM on Duty inside a motor.

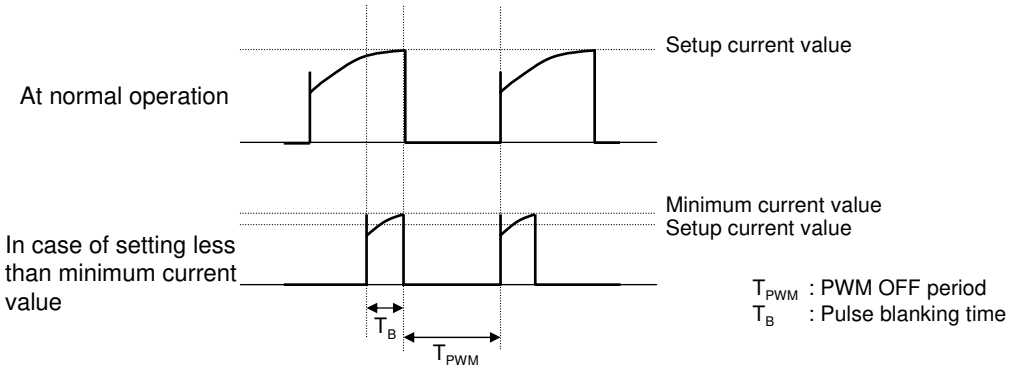


Chart 1. RCS current waveform

2) VREF voltage
When VREF* voltage is set to Low-level, erroneous detection of current might be caused by noise because threshold of motor current detection comparator becomes low (= VREF/10 × motor current ratio [%] .
Use this LSI after confirming no misdetection with setup VREF* voltage.
If VREF* pin is open, input voltage might be irregular and rise, a large current might flow to the output. Therefore do not use on condition that VREF* pin is open.

3) Notes on interface
Absolute maximum of Pin 6 to 8, Pin 12, Pin 21 to 23, Pin 34 to 40 and Pin 44 to 51 is –0.3 V to 6 V. When the setup current for a motor is large and lead line of GND is long, GND pin potential might rise. Take notice that interface pin potential is negative to difference in potential between GND pin reference and interface pin in spite of inputting 0 V to the interface pin. At that time, pay attention allowable voltage range must not be exceeded.

4) Notes on test mode
When inputting voltage of above 0.6 V and below 4.0 V to TEST (Pin 12), this LSI might become test mode. When disturbance noise etc. makes this LSI test mode, motor might not operate normally. Therefore, use this LSI on condition that TEST pin is shorted to GND or S5VOUT at normal motor operation.