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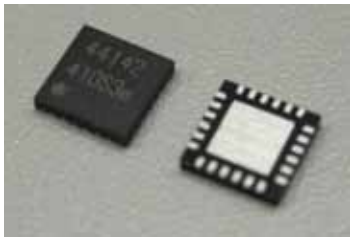
Panasonic

AN44142A

Driver IC for 3-phase Brushless Motor

FEATURES



- Supply voltage range: 4.5 V ~ 26.4 V
- Built-in 5-V regulator
- 3-phase full-wave sine-wave PWM drive by 1-Hall-sensor
- Selectable Input Mode: Either linear voltage input or PWM input through VSP pin
- Controllable lower limit for linear voltage input mode through VSPL pin
- Conduction angle auto driver phase shift correction
- Rotation direction selectable (Forward/Reverse)
- FG pulse divide selectable
- Sleep mode
- Various protection functions:
  Under Voltage Lock Out (UVLO), Over Voltage Lock Out (OVLO), Thermal protection, Over Load Protection, and Over Current Protection

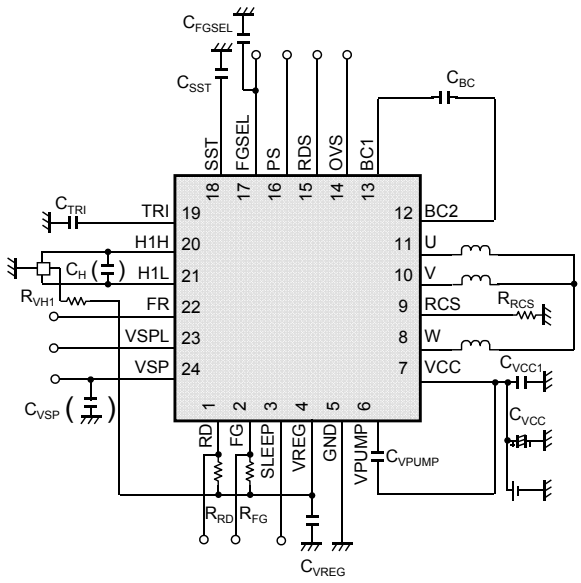
DESCRIPTION

- AN44142A is a driver IC for 3-phase brushless motor optimized for fan motors.
  By employing the rotor position detector and sine wave PWM drive by 1-Hall-sensor, this IC achieves component reduction and miniaturization of motor set as well as motor drive at low noise, low vibration and low power consumption.

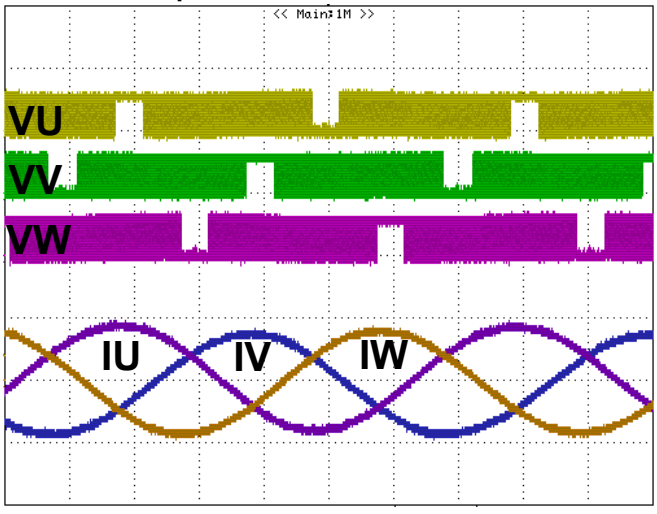
APPLICATIONS

- Driver IC for 3-phase brushless fan motor

TYPICAL APPLICATION



AN44142A 3-phase full-wave sine-wave PWM drive



Condition:
V_{CC} = 12 V, V_{FR} = 0 V, V_{VSP} = PWM mode (60kHz,Duty60%)

Notes: The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

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CONTENTS

- FEATURES 1
- DESCRIPTION 1
- APPLICATIONS 1
- TYPICAL APPLICATION 1
- TYPICAL CHARACTERISTICS 1
- CONTENTS 2
- ABSOLUTE MAXIMUM RATINGS 3
- POWER DISSIPATION RATING 3
- RECOMMENDED OPERATING CONDITIONS 4
- ELECTRICAL CHARACTERISTICS 5
- PIN FUNCTIONS 9
- PIN CONFIGURATION 9
- FUNCTIONAL BLOCK DIAGRAM 10
- OPERATION 11
- AREA OF SAFE OPERATION 33
- PIN EQUIVALENT CIRCUIT 34
- PACKAGE INFORMATION 41
- IMPORTANT NOTICE 44
- USAGE PRECAUTIONS 46

Established : 2014-05-14
Revised : 2014-07-08

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{CC}	28	V	*1
Operating ambient temperature	T_{opr}	– 40 ～ + 95	°C	*2
Storage temperature	T_{stg}	– 55 ～ +150	°C	*2
Input Voltage Range	V_{VREG}	– 0.3 ～ 6.0	V	*3
	V_{SLEEP},V_{H1H},V_{H1L},V_{FGSEL}, V_{VSP},V_{VSPL},V_{FR},V_{RDS},V_{PS},V_{OVS}	– 0.3 ～ 6.0	V	—
	V_{TRI} ,V_{SST}	– 0.3 ～ 6.0	V	—
Output Voltage Range	V_{FG},V_{RD}	– 0.3 ～ 6.0	V	—
	V_{VREG}	– 0.3 ～ 6.0	V	—
	V_{RCS}	– 0.3 ～ 6.0	V	*4
	V_{BC1}	28	V	*4
	V_{BC2},V_{pump}	37	V	*4
Output Current Range	I_{Udc}, I_{Vdc}, I_{Wdc}	± 600	mA	*5
	I_{Upeak}, I_{Vpeak}, I_{Wpeak}	± 2200	mA	*5, *6
	I_{FG},I_{RD}	5	mA	—
	I_{VREG}	−10	mA	—
ESD	HBM	2	kV	—

Notes: This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25°C.

*3: Applying external voltage to this pin is possible only when this pin and VCC pin is connected.
When applying external voltage to this pin, do not exceed the stated ratings even in transient state.

*4: Applying external voltage into these pins is prohibited. Do not exceed the stated ratings even in transient state.

*5: Applying external voltage into these pins is prohibited. Do not exceed the stated ratings even in transient state.

*6: For VCC≧5.6 V, output current of ±2200 mA is only allowed within 100µs.
For VCC＜5.6 V, output current of ±1500 mA is only allowed within 100µs.

POWER DISSIPATION RATING

Package	$\theta_{j\text{-}a}$	$\theta_{j\text{-}c}$	P_D (T_a=25 °C)	P_D (T_a=70 °C)
24 pin Plastic Quad Flat Non-leaded Package (QFN type)	56.1 °C/W	4.4 °C/W	2.22 W	1.42 W

Notes: For the actual usage, please refer to the P_D-T_a characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

*1: Glass-Epoxy Substrate (2 Layers) : 50 x 50 x 0.8t (mm), Heat dissipation fin: Die-pad, Soldered. (Heat dissipation via 2 layer board)

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply voltage range	V_{CC}	4.5	—	26.4	V	—
Input voltage range	V_{SLEEP}	0	—	V_{VREG}	V	*1
	V_{H1H}	0	—	V_{VREG}	V	*1
	V_{H1L}	0	—	V_{VREG}	V	*1
	V_{PS}	0	—	V_{VREG}	V	*1
	V_{RDS}	0	—	V_{VREG}	V	*1
	V_{OVS}	0	—	V_{VREG}	V	*1
	V_{FGSEL}	0	—	V_{VREG}	V	*1
	V_{VSP}	0	—	V_{VREG}	V	*1
	V_{VSPL}	0	—	V_{VREG}	V	*1
	V_{FR}	0	—	V_{VREG}	V	*1
External constants	C_{VCC}	4.7µ	—	—	F	*2,*3
	C_{VCC1}	—	0.1µ	—	F	*2,*3
	C_{VREG}	—	0.1µ	—	F	*2,*4
	C_{SST}	22p	1800p	—	F	*2,*5
	C_{BC}	—	0.1µ	—	F	*2,*4
	C_{VPUMP}	—	0.1µ	—	F	*2,*4
	C_{TRI}	220p	390p	1300p	F	*2,*5
	R_{RCS}	0.15	0.22	—	Ω	*2,*5,*6
	R_{VH}	—	1k	—	Ω	*2,*5
	C_{FGSEL}	—	0.01µ	—	F	*2,*7
	C_{VSP}	—	0.1µ	—	F	*2,*8

Note: *1: For setting range of input control voltage, refer to Electrical Characteristics (page 5 - 8) and Operation (page 11 - 32).
*2: Operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set.
*3: Please perform sufficient evaluation and verification to ensure that VCC pin voltage ripple is reduced.
*4: It is recommended to use the values indicated.
*5: Please choose the setting according to the usage. Please refer to the Electrical Characteristics (page 5 - 8) and Operation (page 11 - 32).
*6: Do not use resistor of value smaller than this. When using value smaller than the minimum value, latch-up function which is used to prevent thermal damage may operate due to external factors (PCB heat dissipation, metal impedance, etc...) or internal factors (threshold change, etc...).
*7: When using with FGSEL pin open, please connect capacitor to the FGSEL pin to prevent noise and carry out sufficient evaluation and verification.
*8: When VSP pin is used for DC input, it is recommended to insert a capacitor to the VSP pin.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 12.0 V, V_{VREG} = 5.0 V

Note: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Circuit Current							
V_{CC} current	I_{CC1}	—	3.0	5.6	9.0	mA	—
V_{CC} current at sleep mode	I_{CC3}	V_{SLEEP} = H	—	—	50	μA	—
Regulator Block							
VREG voltage	V_{VREG}	—	4.7	5	5.3	V	—
Output impedance	Z_{VREG}	I_{VREG} = −10 mA	—	—	10	Ω	—
FG Block							
FG output (low voltage)	V_{FGL}	I_{FG} = 1.0 mA	—	0.1	0.3	V	—
RD Block							
RD output (low voltage)	V_{RDL}	I_{RD} = 1.0 mA	—	0.1	0.3	V	—
Power Block							
On resistance	R_{ONHL}	I = 400 mA	0.5	1.0	1.5	Ω	—
On resistance (Vcc=4.5V)	R_{ONHL}	Vcc = 4.5V I = 400 mA	—	1.25	2.05	Ω	—
Diode forward voltage	V_{DI}	I = 400 mA	0.6	0.8	1	V	—
Motor Lock Protection							
Lock detection time	t_{LOCK1}	—	0.35	0.5	0.65	s	—
Lock release time	t_{LOCK2}	—	3.5	5	6.5	s	—
Lock protection ratio	PR_{RATIO}	—	9	10	11	—	—
Over Current Protection							
Over current detection level	V_{CL1}	—	0.225	0.250	0.275	V	—
Hall Block							
Input dynamic range	V_{HALL}	—	0	—	VREG - 2.0V	V	—
Pin current	I_{HALL}	—	– 2	0	2	μA	—
Input offset voltage for H1H−H1L drop	V_{HOFS}	—	-6	0	6	mV	—
Min. input amplitude voltage	V_{HA}	—	25	—	—	mV	—
Hysteresis width	V_{HHYS}	—	7.5	10	13	mV	—
SLEEP							
Low-level input voltage	V_{SLL}	—	—	—	0.5	V	—
High-level input voltage	V_{SLH}	—	2.5	—	—	V	—
Open-circuit voltage	V_{SLZ}	—	—	0	0.3	V	—
Input impedance	Z_{SL}	—	70	100	130	kΩ	—

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ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 12.0 V, V_{VREG} = 5.0 V

Note: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
VSP							
Pin current	I_{VSP}	V_{VSP}=5.0V	—	15	45	μA	—
VSP DC Input Control							
Stop control VSP input	V_{VSPDCL}	—	0.9	1.0	1.1	V	—
Max. speed VSP input	V_{VSPDCH}	—	3.6	4.0	4.4	V	—
VSP PWM Input Control							
Stop control VSP input	$V_{VSPPWML}$	V_{VREG}=V_{OSC}=5.0V	2	3	4	%	*1,*2 *3
Max. speed VSP input	$V_{VSPPWMH}$	V_{VREG}=V_{OSC}=5.0V	—	100	—	%	*1,*2 *5
Low-level input voltage during PWM input	V_{VSPLL}	V_{VREG}=V_{OSC}=5.0V	—	—	1.0	V	*1,*2
High-level input voltage during PWM input	V_{VSPHL}	V_{VREG}=V_{OSC}=5.0V	2.0	—	—	V	*1,*2
PWM input frequency range	F_{PWM}	—	15	—	100	kHz	*1,*2
VSPL DC Input Control							
VSPL enabled input voltage range	V_{VSPL}	—	1.3	—	3.0	V	—
Pin current	I_{VSPL}	V_{VSPL}=5.0V	—	5	15	μA	—
Internal Oscillation Frequency							
Internal oscillation frequency	f_{OSC}	—	17.5	25	32.5	MHz	—
Triangle Wave Oscillator for PWM Waveform (TRI pin)							
Amplitude	V_{TRI}	—	1.36	1.53	1.70	Vpp	—
External capacitor charging current	I_{TRI1}	V_{TRI} =0.5V	−83.5	−64.5	−45.5	μA	—
External capacitor discharging current	I_{TRI2}	V_{TRI} =2.0V	45.5	64.5	83.5	μA	—
TRI pin input voltage during PWM control	V_{TRITH}	—	2.9	—	—	V	*2
Triangle Wave Oscillator during Soft Start (SST pin)							
Amplitude	V_{SST}	—	0.75	1.0	1.25	Vpp	—
External capacitor charging current	I_{SST1}	V_{SST} =0.6V	−6.0	−4.0	−2.0	μA	—
External capacitor discharging current	I_{SST2}	V_{SST} =1.6V	2.0	4.0	6.0	μA	—
SST pin input voltage when Soft Start not used	V_{SSTTH}	—	2.9	—	—	V	*4

Note: *1: During PWM control, VSPL pin must be connected to GND.
*2: During PWM control setting, TRI pin must be connected to VREG pin.
*3: It is recommended to input 0% Duty (Low input) when input STOP.
*4: When Soft Start is not in used, SST pin must be connected to VREG pin.
*5: Typical Design Value.

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ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 12.0 V, V_{VREG} = 5.0 V

Note: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
FR (3-State Input circuit)							
Low-level input voltage	V_{FRL}	—	—	—	0.8	V	—
Mid-level input voltage	V_{FRM}	—	1.3	—	2.0	V	—
High-level input voltage	V_{FRH}	—	2.5	—	—	V	—
Open-circuit voltage	V_{FRZ}	—	1.4	1.65	1.9	V	—
Pin current	I_{INFR}	V_{FR} = 0 V	- 40	- 20	—	µA	—
FGSEL (3-State Input circuit)							
Low-level input voltage	V_{FGSELL}	—	—	—	1.0	V	—
High-level input voltage	V_{FGSELH}	—	4.0	—	—	V	*1
Open-circuit voltage	V_{FGSELZ}	—	1.8	2.4	2.8	V	*2
Pin current	I_{INFG}	V_{FGSEL} = 0 V	- 40	- 20	—	µA	—
PS (2-State Input circuit)							
Low-level input voltage	V_{PSL}	—	—	—	1.0	V	—
High-level input voltage	V_{PSH}	—	4.0	—	—	V	*1
Open-circuit voltage	V_{PSZ}	—	—	0.0	0.5	V	—
Pin current	I_{INPS}	V_{PS} = 5.0 V	—	5	15	µA	—
RDS (2-State Input circuit)							
Low-level input voltage	V_{RDSL}	—	—	—	1.0	V	—
High-level input voltage	V_{RDSH}	—	4.0	—	—	V	*1
Open-circuit voltage	V_{RDSZ}	—	—	0.0	0.5	V	—
Pin current	I_{INRDS}	V_{RDS} = 5.0 V	—	5	15	µA	—
OVS (2-State Input circuit)							
Low-level input voltage	V_{OVSL}	—	—	—	1.0	V	—
High-level input voltage	V_{OVSH}	—	4.0	—	—	V	*1
Open-circuit voltage	V_{OVSZ}	—	—	0.0	0.5	V	—
Pin current	I_{INOVS}	V_{OVS} = 5.0 V	—	5	15	µA	—

Note: *1: During High level setting, please ensure to connect to VREG pin.
*2: Please connect a capacitor to FGSEL pin when it is open during use to prevent noise. To ensure the noise prevention, please perform sufficient evaluation and verification.

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ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 12.0 V, V_{VREG} = 5.0 V

Note: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Design value			Unit	Note
			Min	Typ	Max		
Thermal Protection							
Protection operating temperature	TSD_{ON}	—	—	160	—	°C	*1
Hysteresis width	TSD_{HYS}	—	—	25	—	°C	*1
Output Block							
Output slew rate at source current	V_{TRSO}	—	—	300	—	V/µs	*1
Output slew rate at source current	V_{TFSO}	—	—	300	—	V/µs	*1
Output slew rate at sink current	V_{TRSI}	—	—	300	—	V/µs	*1
Output slew rate at sink current	V_{TFSI}	—	—	300	—	V/µs	*1
Triangle Wave Oscillator for PWM Waveform (TRI pin)							
Oscillation frequency range	f_{TRI}	—	15	—	100	kHz	*2
Standard oscillation frequency	F_{TRI}	C_{TRI} = 390 pF	—	55.4	—	kHz	*1
Triangle Wave Oscillator during Soft Start (SST pin)							
Standard oscillation frequency	F_{SST}	C_{SST} = 1800 pF	—	1.13	—	kHz	*1
Maximum Rotating Speed							
Minimum hall cycle	T_{HMIN}	—	—	173	—	µs	*1
Under Voltage Lock Out							
Protection operating voltage	V_{LVON}	—	—	3.55	—	V	*1
Protection release voltage	V_{LVOFF}	—	—	3.75	—	V	*1
Over Voltage Lock Out							
Protection operating voltage 1	V_{OVON1}	V_{OVS} = VREG	15.0	16.0	17.0	V	*1
Protection operating voltage 2	V_{OVON2}	V_{OVS} = 0V	26.4	27.2	28.0	V	*1

Note: *1: Typical Design Value.
*2: These are values checked by design but not production tested.

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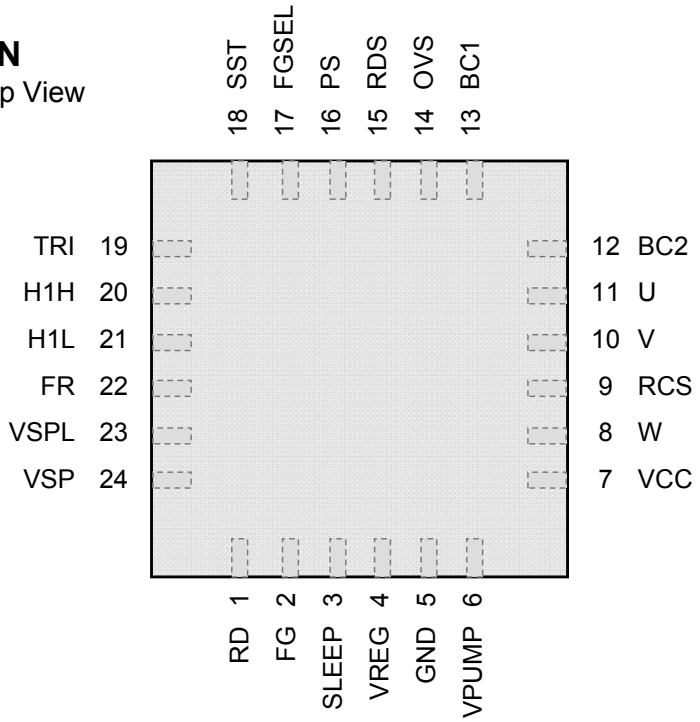
PIN CONFIGURATION

Top View



PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	RD	Output	Over load protection
2	FG	Output	FG external output
3	SLEEP	Input	Sleep setting
4	VREG	Output	Internal reference voltage
5	GND	Ground	Ground
6	VPUMP	Output	Charge pump circuit output
7	VCC	Power	Supply voltage for motor
8	W	Output	W-phase output
9	RCS	Output	Motor current detector
10	V	Output	V-phase output
11	U	Output	U-phase output
12	BC2	Output	Capacitor connection pin 2 for charge pump
13	BC1	Output	Capacitor connection pin 1 for charge pump
14	OVS	Input	Over voltage detection selectable threshold. High for 16V detection, Low for 27.2V detection
15	RDS	Input	Selectable Release of Motor lock protection. High to use the release of lock protection. Low to disable the release of lock protection.
16	PS	Input	Selectable phase shift mode. High to enable Auto Phase FB shift mode. Low to enable constant phase shift mode.
17	FGSEL	Input	FG pulse count select
18	SST	Input / Output	Capacitor connection pin for Soft Start triangle wave oscillator frequency setting
19	TRI	Input / Output	Capacitor connection pin for PWM triangle wave oscillator frequency setting
20	H1H	Input	Hall amplifier input (+)
21	H1L	Input	Hall amplifier input (-)
22	FR	Input	Rotation direction select (Forward/Reverse)
23	VSPL	Input	Voltage input for setting low rotating speed during DC input mode
24	VSP	Input	Voltage input for setting rotating speed

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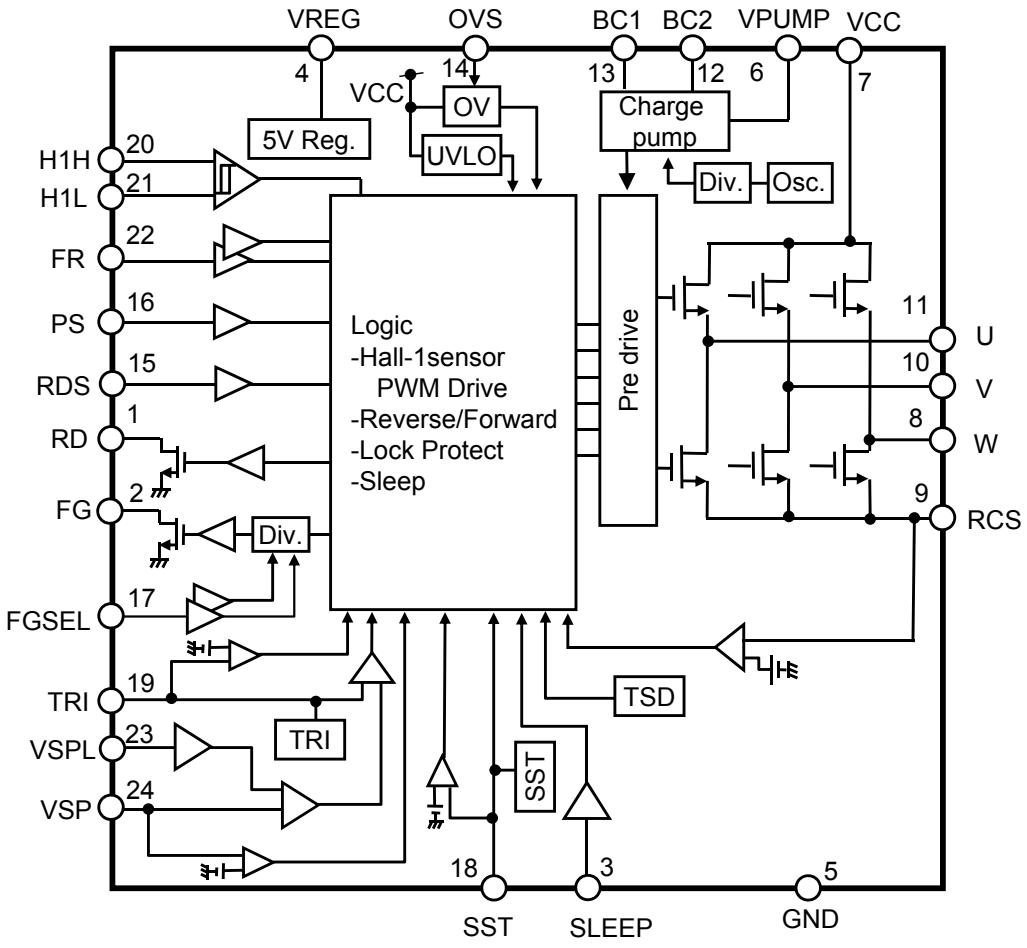
FUNCTIONAL BLOCK DIAGRAM



Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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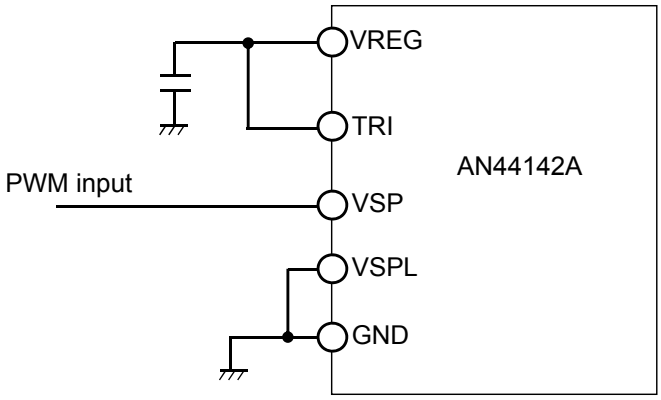
OPERATION

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

1. VSP input configuration

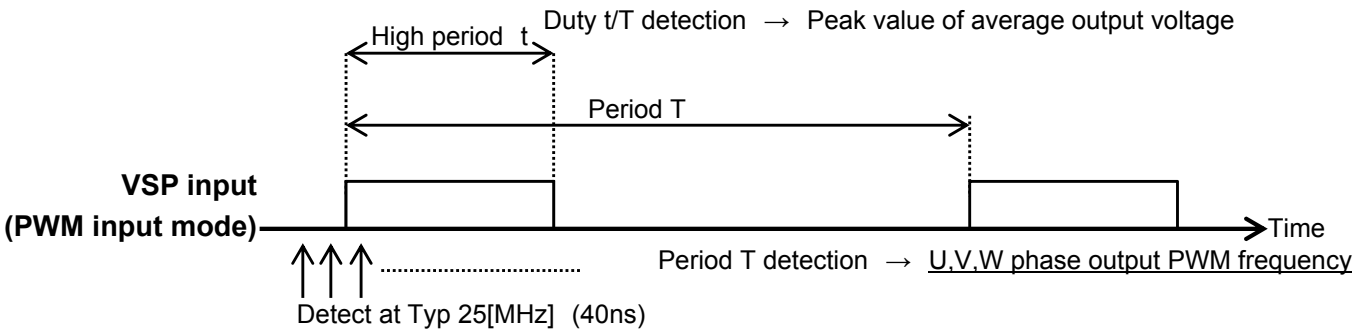
1-1. PWM input mode

PWM input control or DC input control are used as the input controls to VSP pin.
When using PWM input control, please ensure to connect TRI pin to VREG pin. VSPL pin shall be open or connected to GND pin (It is recommended to connect to GND.).



PWM input control signal detection

The below periodic signal T and Duty signal t/T is detected when PWM is input to VSP pin.
Periodic signal T respond to output PWM frequency and Duty signal t/T respond to speed signal.



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OPERATION (Continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

1. VSP input configuration (Continued)

1-1. PWM input mode (Continued)

Points to note when using PWM input mode

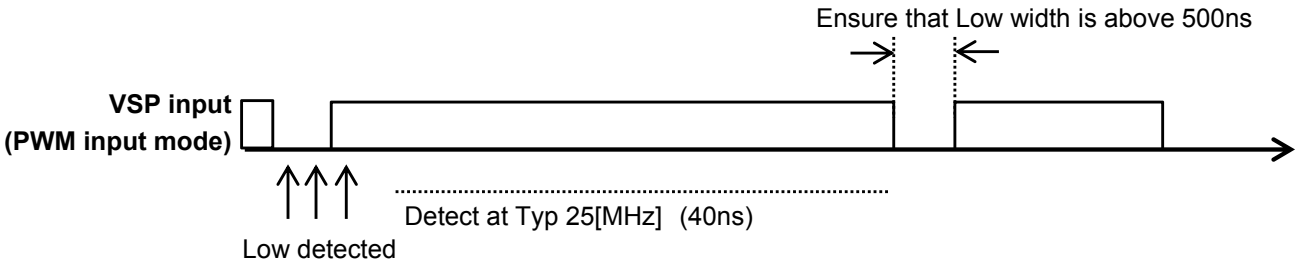
Operation when input at VSP=100%duty

During output, when the VSP PWM input duty changes from below 100% to 100% duty, the frequency (period t) that is being input will halt and 100% input will be detected.
Therefore, output frequency will become 1/t. (However, this will be reflected in the output about 7t later, after signal is changed to 100% duty.)

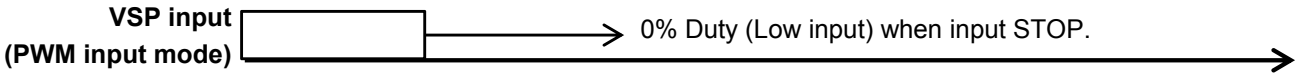
When VSP pin is already input with 100% duty during power or SLEEP start-up, operation is at output frequency of about 58kHz.
After which, when PWM signal is input to the VSP pin and frequency signal is detected, output frequency will follow the frequency that is being input to VSP pin.

Maximum pulse width when VSP below 100% is input

VSP input resolution under PWM input mode is typ 25MHz(40ns period).
Therefore, input pulse below 40ns may not be detected.
This is especially when input is near to 100% duty, period T signal many not be correctly detected.
Therefore to ensure that normal signal can be detected, please ensure that input to VSP pin at Low is above 500ns and more.



It is recommended to input 0% Duty (Low input) when input STOP.



Under PWM input mode, please ensure that PWM signal is input to the VSP pin.

Established : 2014-05-14
Revised : 2014-07-08

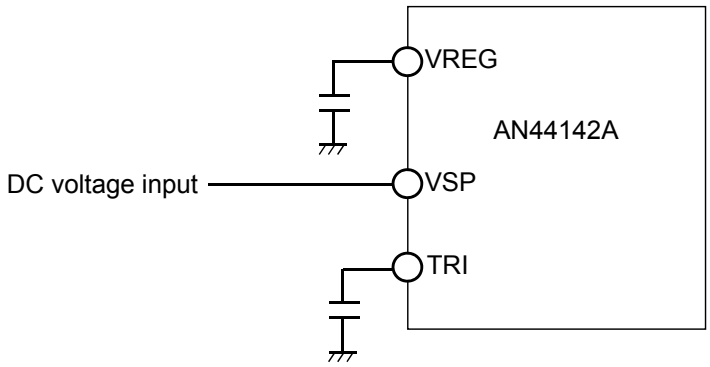
OPERATION (Continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

1. VSP input configuration (Continued)

1-2. VSP input mode

PWM input control or DC input control are used as the input controls to VSP pin.
When using DC input control, please ensure to connect a capacitor between TRI pin and GND pin.



Signal during DC input mode

During DC input mode, PWM signal is generated by the comparison between the TRI pin triangle waveform and the VSP pin input DC voltage.
Peak value of average output voltage is dependent on VSP pin voltage and output PWM frequency is dependent on TRI pin triangle waveform frequency.

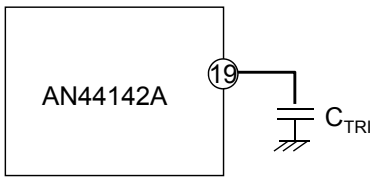
TRI pin triangle wave oscillator frequency

The triangle wave oscillator frequency input into TRI pin is calculated using the below formula.

Triangle wave oscillator frequency

$$f_{TRI} = \frac{A}{2 \times C_{TRI} \times V_{TRI}}$$

V_{TRI} : Triangle waveform amplitude (Under typ.1.53 V)
A : 64.5 μA (Under typ.)



Lower limit control using VSPL pin

During DC input control, lower limit of the VSP input voltage can be controlled by inputting DC voltage to the VSPL pin.
When not controlling the lower limit, please ensure to connect VSPL pin to GND pin during use.

Established : 2014-05-14
Revised : 2014-07-08

OPERATION (Continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

2. VSP input voltage and average output voltage

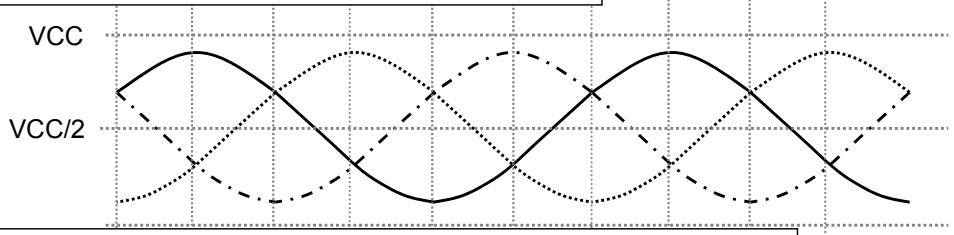
Values in this page are all Typ values. In addition, these are where our recommended TRI value is used, under DC input mode.

○Hall Voltage Difference
HU = H1H-H1L

○FG Voltage

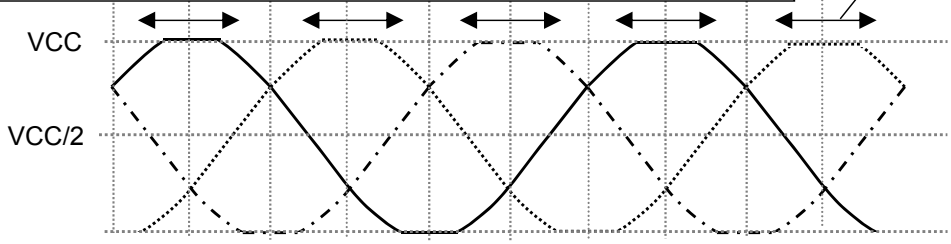
○Average Output Voltage

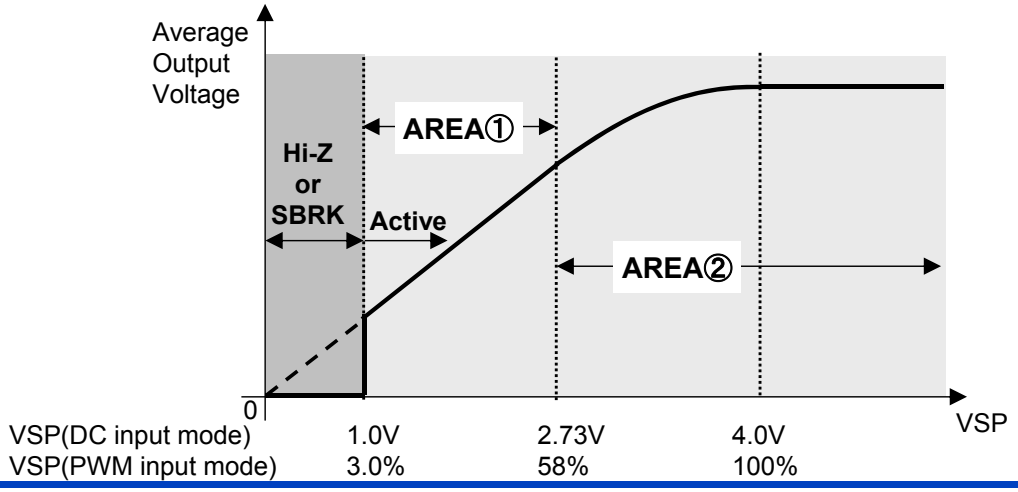
AREA① Output Duty is linearly dependent on VSP input
・VSP(DC input mode) ≒ 1.0V ~ 2.73 V
・VSP(PWM input mode) = 3.0% ~ 58 %



AREA② Output Duty is non-linear dependent on VSP as average voltage is distorted by VCC
・VSP(DC input mode) ≒ 2.73V ~ 4.0 V
・VSP(PWM input mode) = 58% ~ 100 %
Output Duty is a fixed value, not dependent on VSP
・ VSP(DC input mode) > 4.3 V
・VSP(PWM input mode) = 100%

Distorted area is increased due to VSP dependence





Established : 2014-05-14
Revised : 2014-07-08

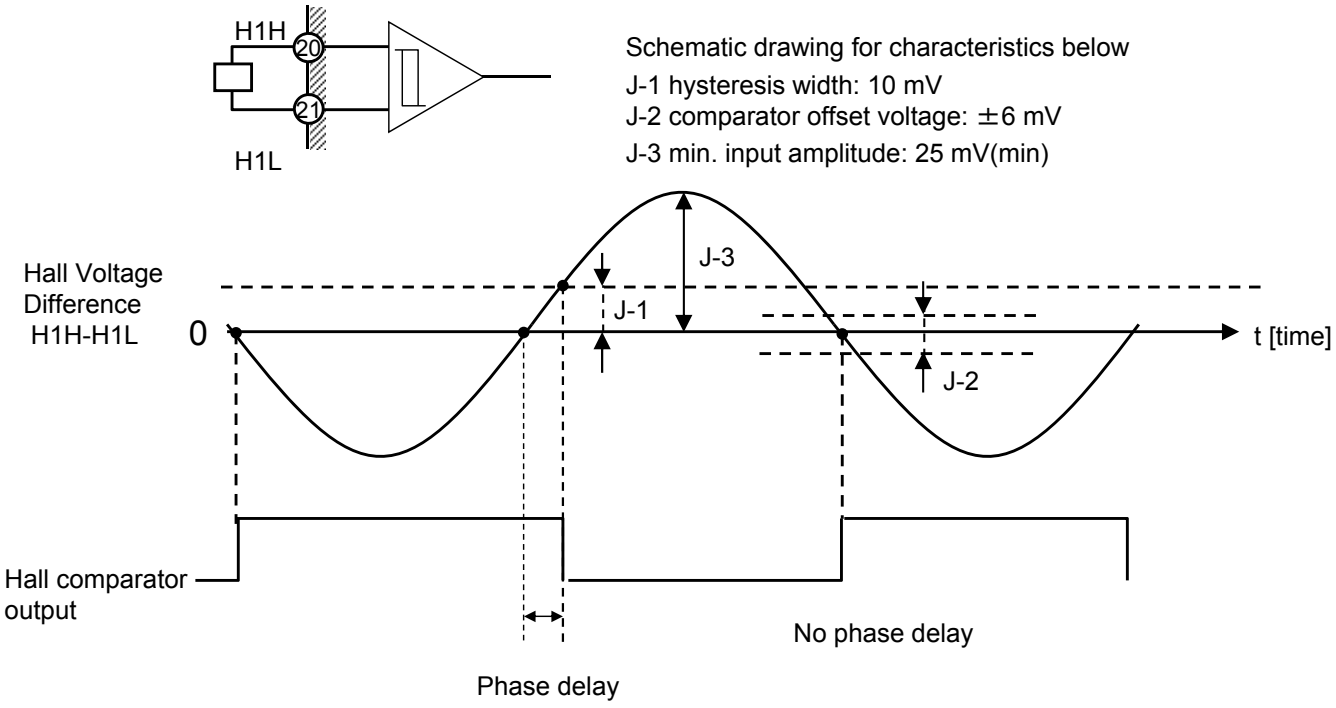
OPERATION (Continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

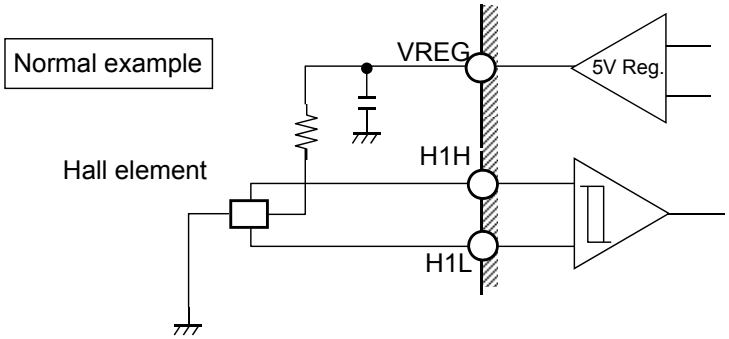
3. Hall Input Specification

3.1. System to detect hall signal

The motor position is detected by the Hall hysteresis comparator. If the amplitude of sine wave is small, phase delay of comparator output will be very prominent. Therefore, please make the amplitude of the sine wave larger. When chattering occurs to Hall element, insert a capacitor between H1H (pin 20) and H1L (pin 21).



For the biased source of the Hall element, please construct by externally shorting to VREG pin.



Established : 2014-05-14
Revised : 2014-07-08

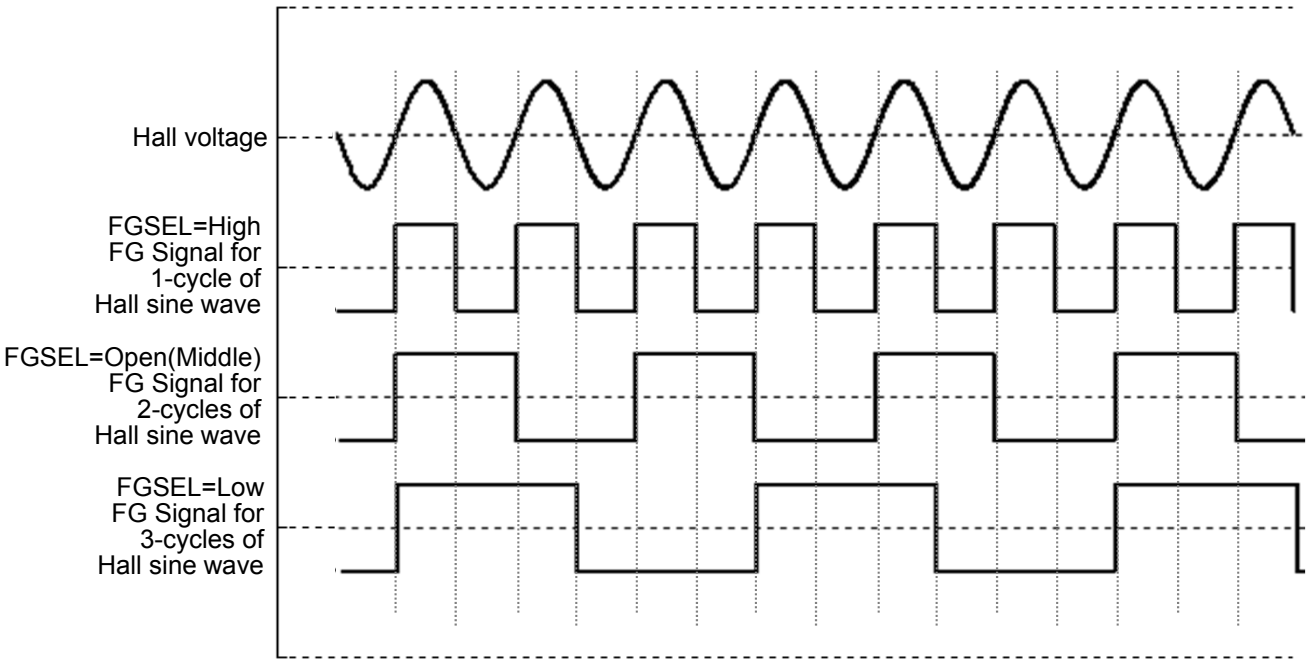
OPERATION (Continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

3. Hall Input Specification (Continued)

3.2. The Relation between Hall Voltage and FGSEL

1-cycle FG signal, which is equivalent to 1-cycle/2-cycle/3-cycle of Hall sine wave (selected by FGSEL), is output.



Established : 2014-05-14
Revised : 2014-07-08

OPERATION (Continued)

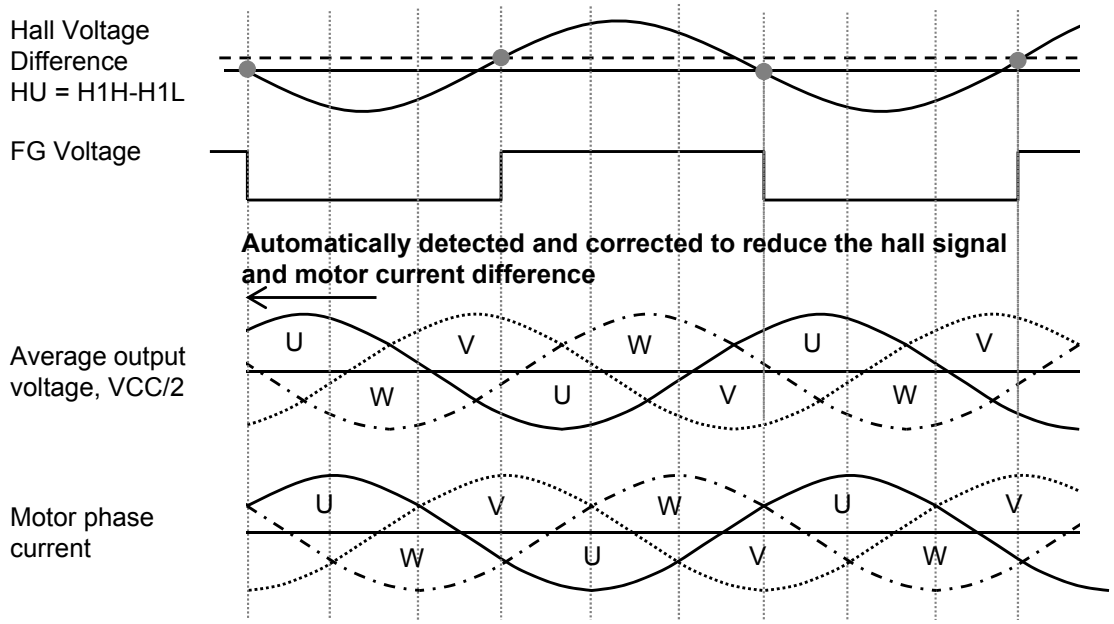
Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

3. Hall Input Specification (Continued)

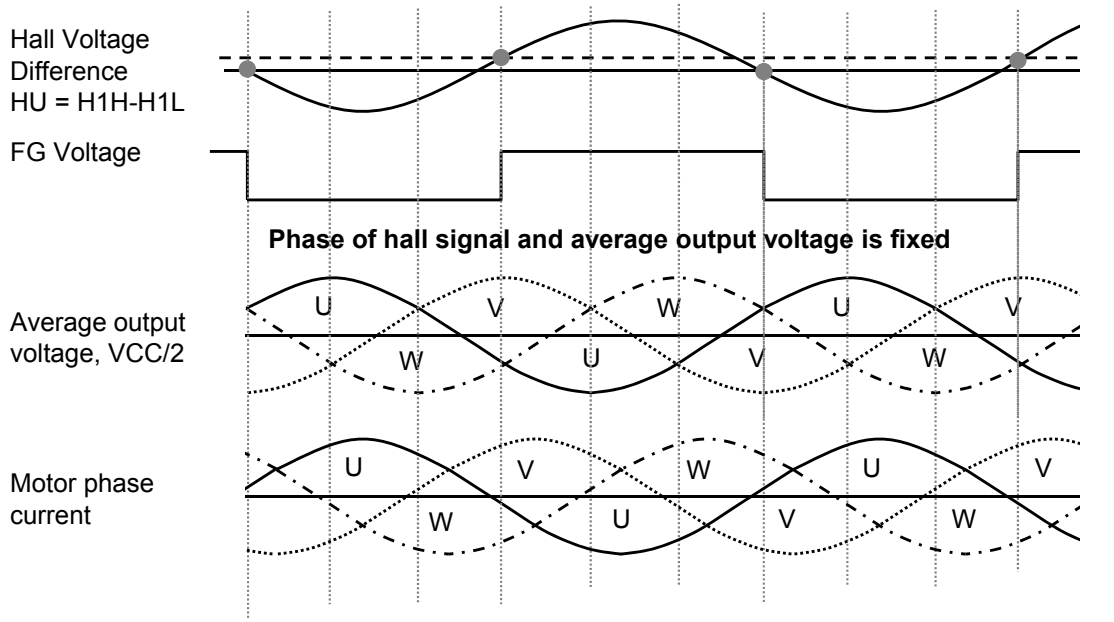
3.3. Drive Phase Shift Control

Automatic drive phase shift control when PS=Low. The hall signal phase with respect to the conduction angle detects the IC's own phase difference and automatically correct it to the most optimum phase. The example for U-phase output voltage is shown below.

Automatic drive phase shift control when PS=Low



Fixed to 0 deg when PS=High



Established : 2014-05-14
Revised : 2014-07-08

OPERATION (Continued)

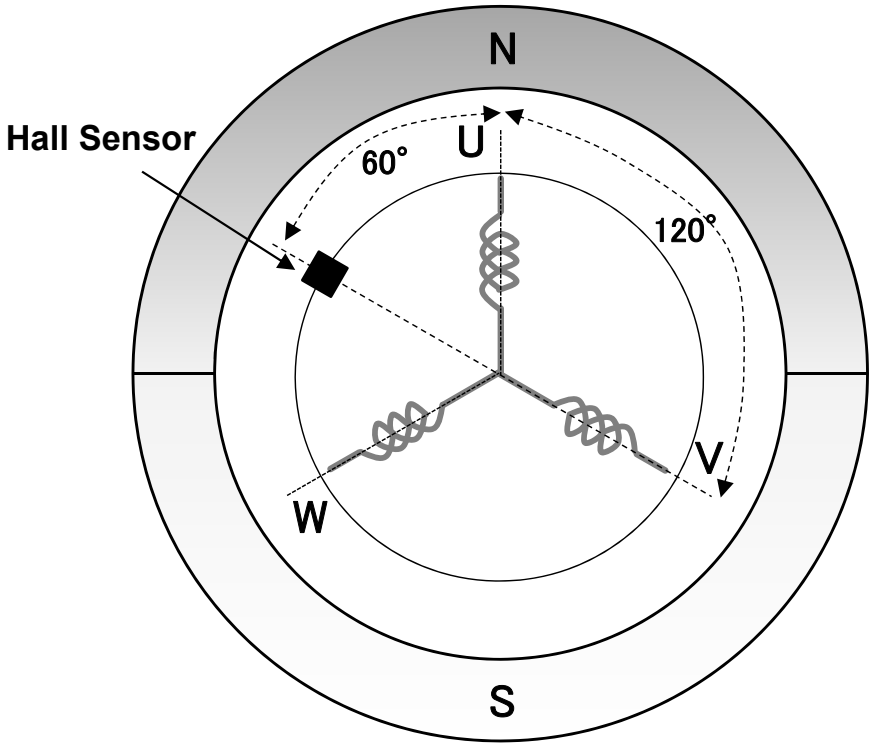
Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

3. Hall Input Specification (Continued)

3.4. Hall Sensor Placement

This IC uses only 1 hall sensor.
Please use the U-phase hall sensor for 3 phase 3 sensor motor

The diagram below shows the hall placement for a 2 pole 3 slots motor



Example placement for the hall sensor
(2 pole 3 slot motor)

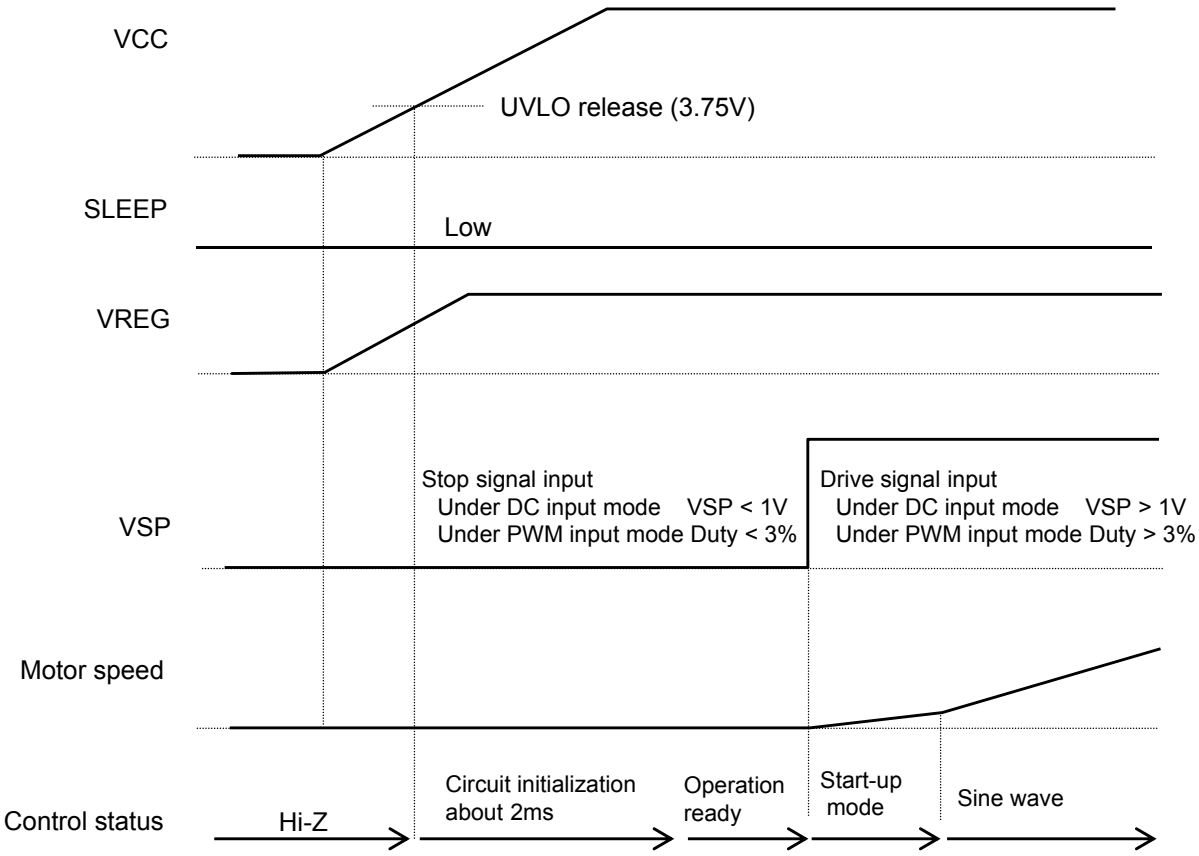
Established : 2014-05-14
Revised : 2014-07-08

OPERATION (Continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

4. Start / Stop control

Start-up by rising VCC pin voltage



- After UVLO is released, circuit initialization is required for about 2ms and output signal is stopped. When circuit is under initialization, no signal is output even when VSP drive signal is inputted. Output of signal starts after initialization completes.
- Start up mode is within 4 cycles hall signal input. During this period, no FG signal is output.

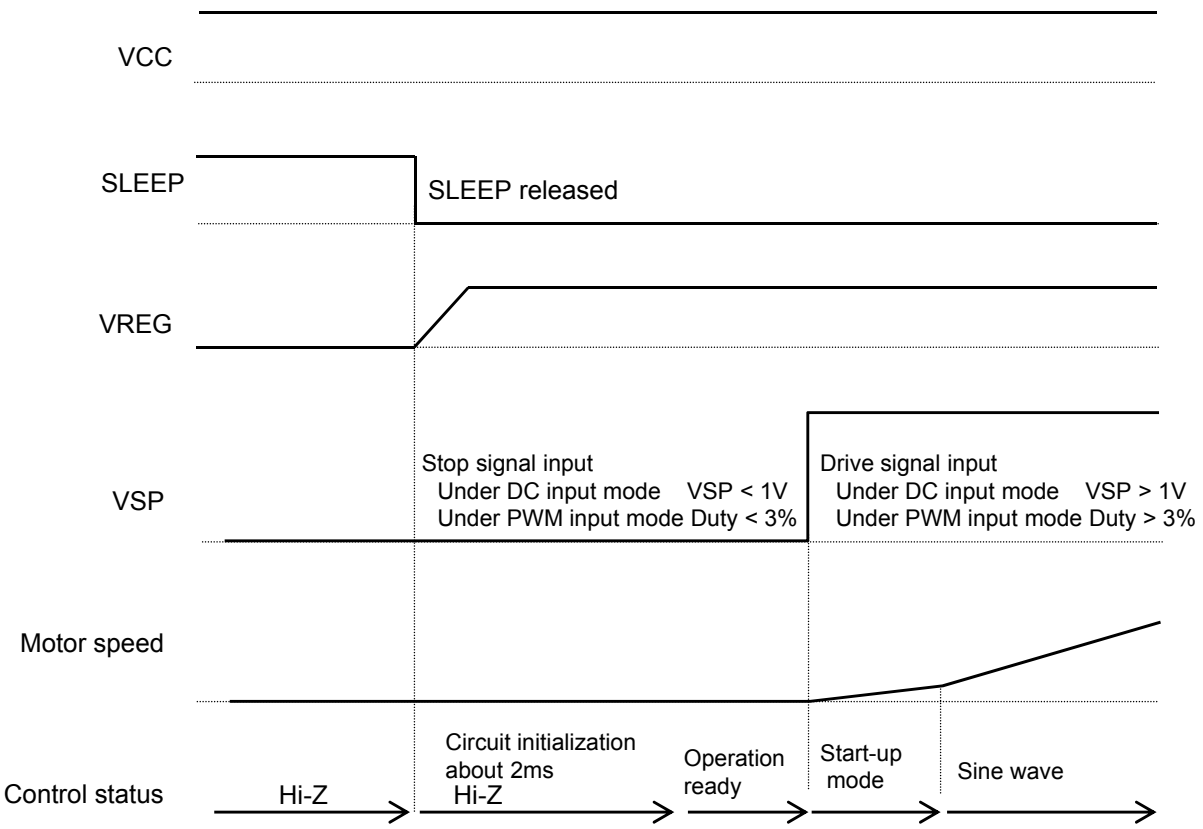
Established : 2014-05-14
Revised : 2014-07-08

OPERATION (Continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

4. Start / Stop control (Continued)

Start-up by SLEEP signal release



- After SLEEP mode is released, circuit initialization is required for about 2ms and output signal is stopped. When circuit is under initialization, no signal is output even when VSP drive signal is inputted. Output of signal starts after initialization completes.
- Start up mode is within 4 cycles hall signal input. During this period, no FG signal is output.

Established : 2014-05-14
Revised : 2014-07-08

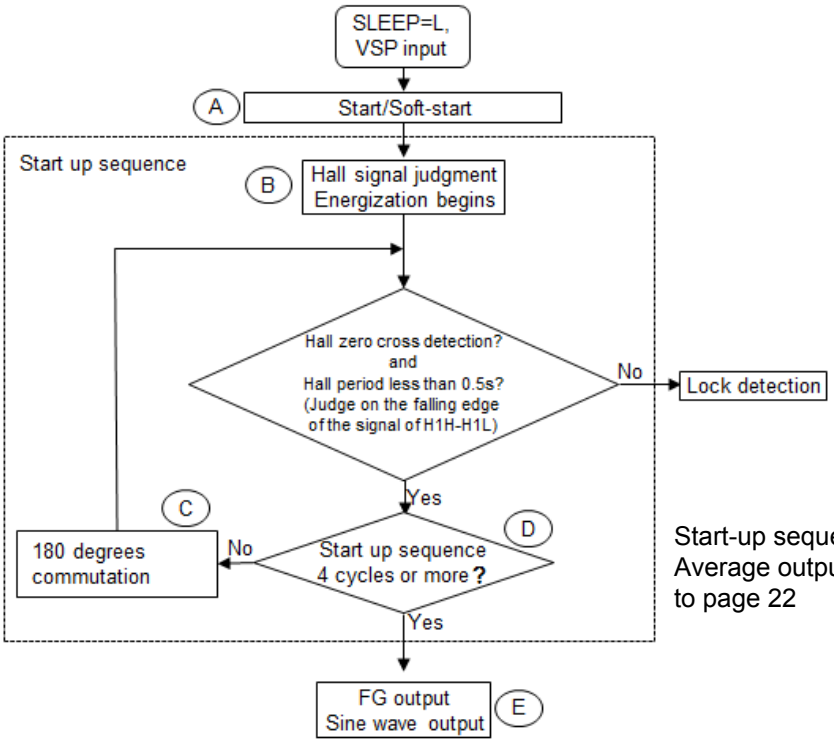
OPERATION (Continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

4. Start / Stop control (Continued)

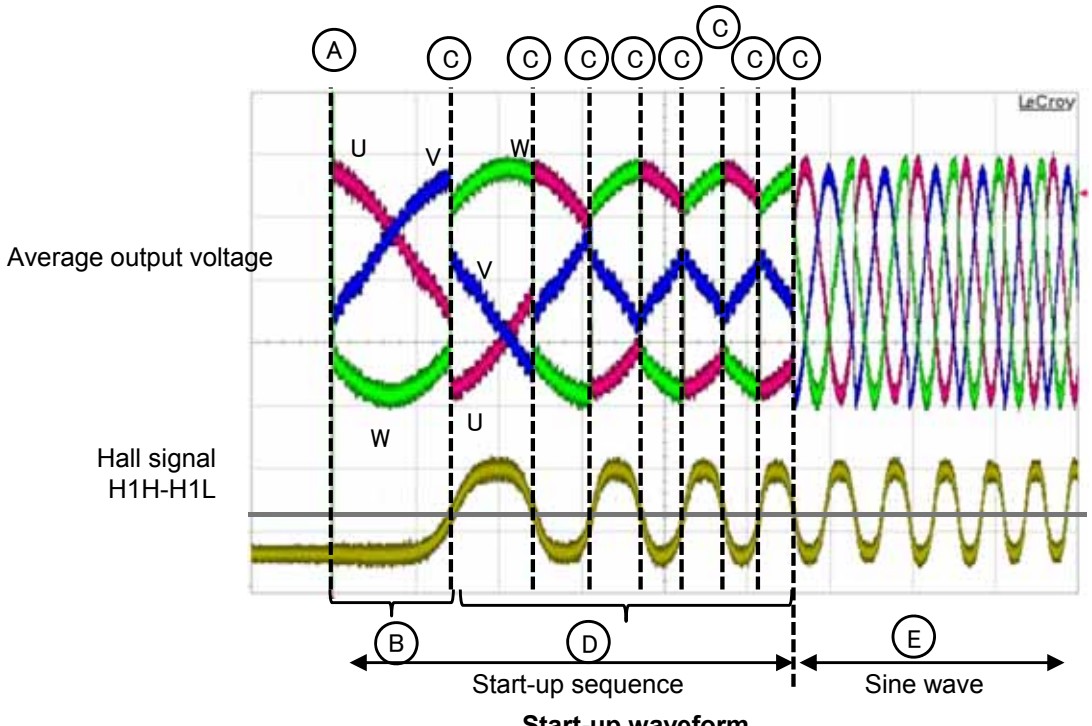
Start-up sequence

The flow chart below illustrates the start-up sequence.



Start-up sequence
Average output voltage waveforms refer to page 22

Start-up sequence flow chart



Start-up waveform

Established : 2014-05-14
Revised : 2014-07-08

OPERATION (Continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

4. Start / Stop control (Continued)

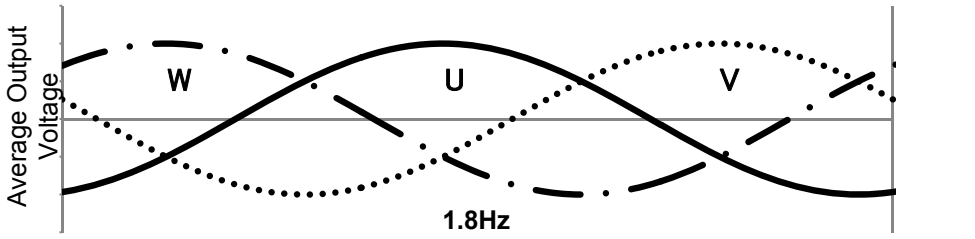
Start-up sequence (Continued)

Start-up sequence average output voltage.

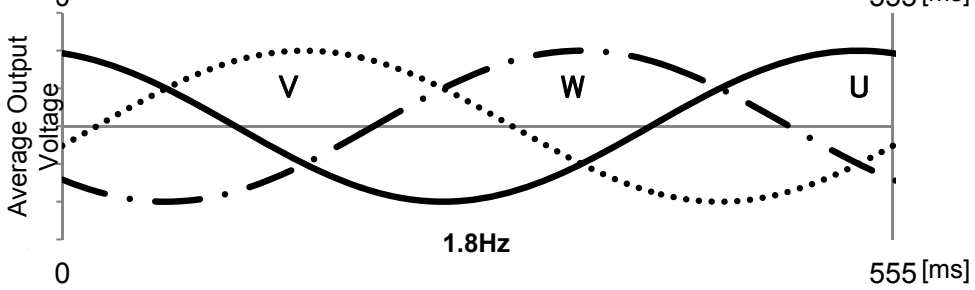
The following waveforms illustrates the average output for different hall zero crossing detection, H1H-H1L at start-up.

Forward (FR=L)

H1H-H1L>0

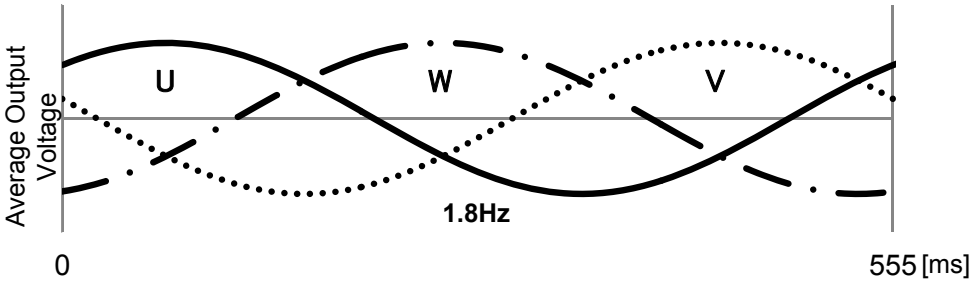


H1H-H1L<0

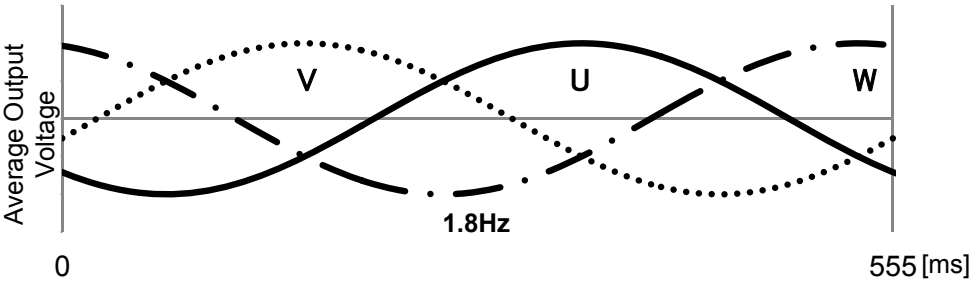


Reverse (FR=H)

H1H-H1L>0



H1H-H1L<0



- Due to the initial position of the rotor, the starting torque differs slightly during start-up. For motor type that requires large inertia force to turn, please ensure that sufficient starting current is available for the motor. Please perform sufficient testing and evaluations to ensure this.

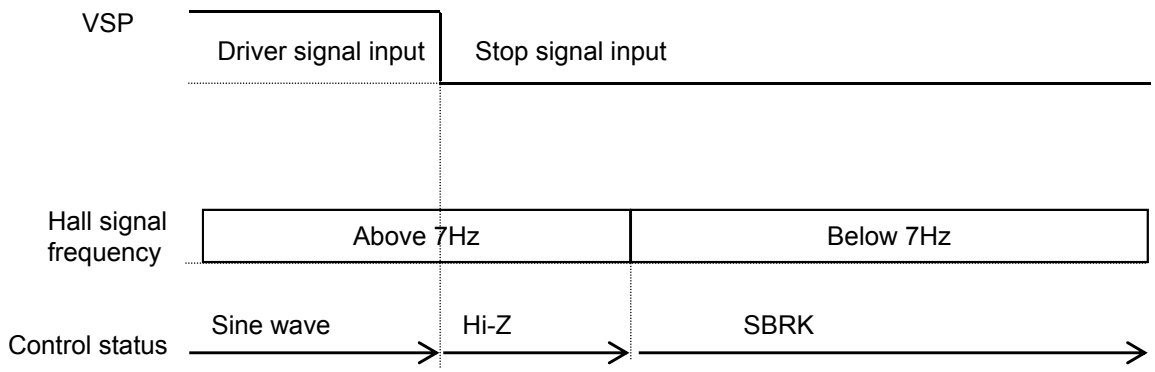
Established : 2014-05-14
Revised : 2014-07-08

OPERATION (Continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

4. Start / Stop control (Continued)

Stop



- When stop signal is input to VSP, hall signal frequency above 7Hz will result in Hi-Z at output and below 7Hz will result in SBRK at output.

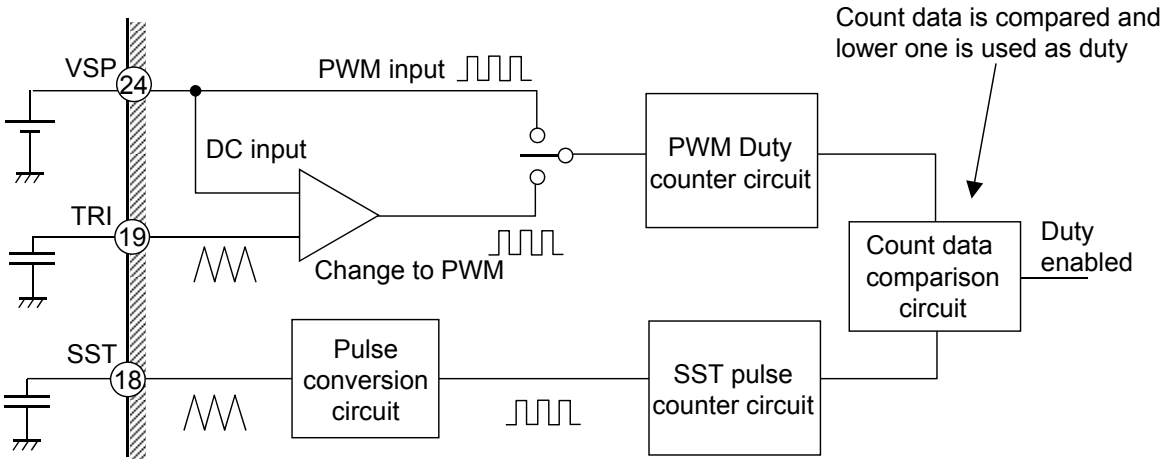
Established : 2014-05-14
Revised : 2014-07-08

OPERATION (Continued)

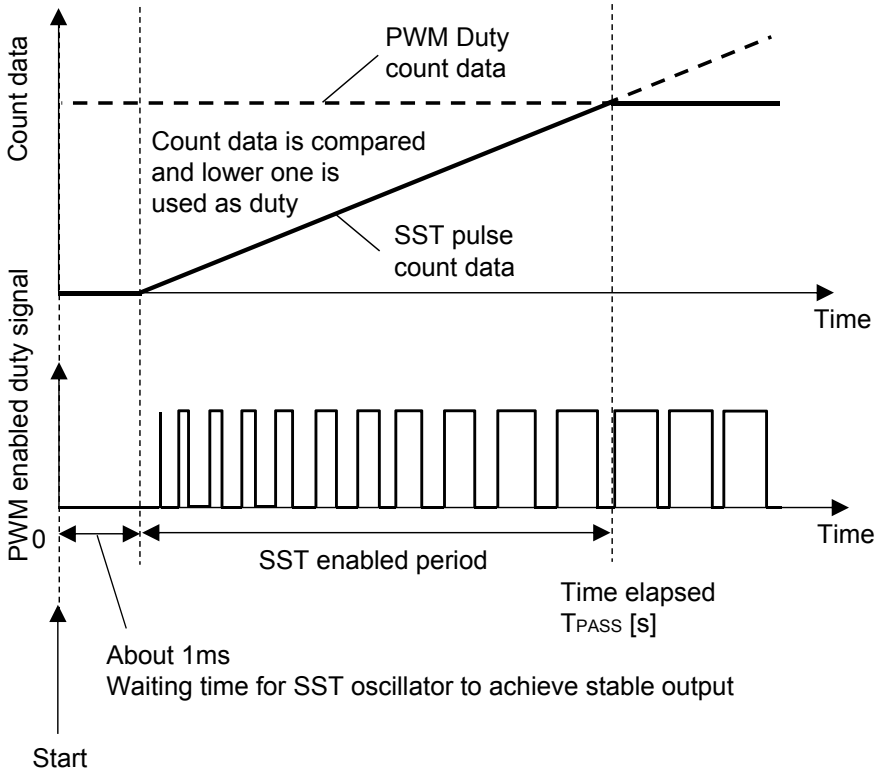
Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

5. Soft Start Function and PWM Specification

By connecting a capacitor to the SST pin, soft start control is performed by the start-up mode conditions during the mode transition. The period for soft start control is determined by the formula shown on the next page. When soft start control is not required, ensure to connect SST pin to VREG pin.



Below shows the correlation timing chart of count data and PWM enabled duty for VSP and SST.



・Notes on the use of the soft-start function.
With the increase in soft-start time, the motor current will also increase slowly . Therefore if the soft-start timing is too long, it will result in the motor not having enough starting torque and lock protection detection will be triggered if soft start timing is more than 0.5s (typ). This will cause the motor to be unable to start. Please evaluate and check this condition thoroughly when using this function.

Established : 2014-05-14
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OPERATION (Continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

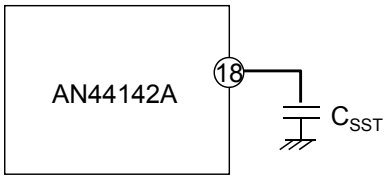
5. Soft Start Function and PWM Specification (Continued)

The triangle wave oscillator frequency output by SST pin is determined by the below formula. Soft Start timing is generated by comparing the VSP pin input PWM frequency and this triangle waveform frequency.

Triangle wave oscillator frequency

$$f_{SST} = \frac{A}{2 \times C_{SST} \times V_{SST}}$$

V_{SST} : Triangle waveform amplitude (At typ. 1 V)
A : Current flowing in/out SST pin (At typ. 4 μA)



The PWM enabled duty reflected in the output, at the time elapsed T_{PASS} within the SST enabled timing is determined by the below formula:

$$\text{PWM duty} = \frac{T_{PASS} \times T_{OSC}}{T_{SST} \times T_{PWM}}$$

T_{PWM} : Input PWM cycle [s]
T_{OSC} : Oscillation cycle of internal oscillator $40*10^{-9}$ [s]
T_{SST} : SST triangle wave oscillation cycle[s]
T_{PASS} : Time elapsed [s]

T_{PASS} at the end of the SST timing can be determined by the below formula:

$$T_{PASS} = \frac{T_{PWM} \times D \times T_{SST}}{T_{OSC}}$$

D : Input PWM duty [%]

Input PWM duty during the DC input can be determined by the below formula:

$$D = \left(\frac{97}{3} \times V_{VSP} - \frac{88}{3} \right) \times 0.01$$

Under DC input, V_{VSP}=1V～4V

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