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AN8018SA

1.8-volt 2-channel step-up, step-down, or inverting DC-DC converter control IC

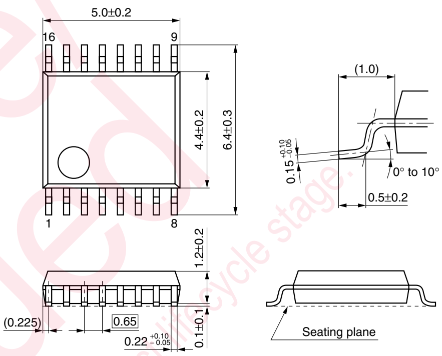
■ Overview

The AN8018SA is a two-channel PWM DC-DC converter control IC that features low-voltage operation.

This IC can obtain the step-up, step-down and inverting voltages with a small number of external components.

The minimum operating voltage is as low as 1.8 V so that it can operate with two dry batteries. In addition, since it uses the 16-pin surface mounting type package with 0.65 mm pitch, it is suitable for miniaturized highly efficient potable power supply.

Unit: mm



SSOP016-P-0225A

Note) The package of this product will be changed to lead-free type (SSOP016-P-0225E). See the package dimensions section later of this datasheet.

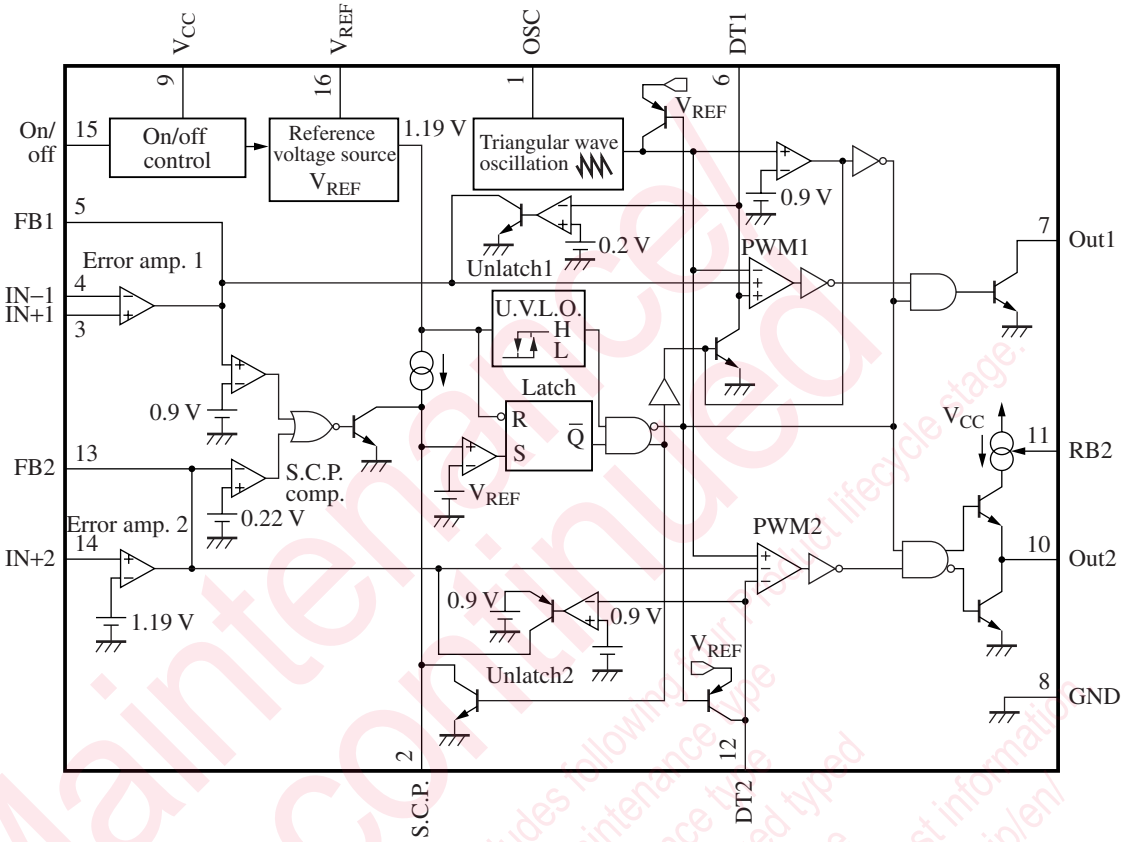
■ Features

- Wide operating supply voltage range (1.8 V to 14 V)
- Incorporating a high precision reference voltage circuit (allowance: ± 2%)
- Control in a wide output frequency range is possible (20 kHz to 1 MHz).
- Built-in wideband error amplifier (single gain bandwidth 10 MHz typical)
- Built-in timer latch short-circuit protection circuit (charge current 1.1 µA typical)
- Incorporating the under-voltage lock-out circuit (U.V.L.O.) (circuit operation-starting voltage 1.67 V typical)
- Dead-time is variable.
- Flatness of switching current can be obtained by staggering the turn-on timing of each channel.
- Built-in unlatch function
  When DT1 pin is low level, or DT2 pin is high level, independent turn-off is possible.
- Incorporating a on/off control function (active-high control input, standby mode current: 5 µA maximum)
- Parallel operation is possible.
- Output block
  - Totem pole 1 output
    - Output source-current: −50 mA maximum (Constant current output with a less supply voltage fluctuation is possible by connecting an external resistor to pin 11)
    - Output sink-current: +80 mA maximum
  - Open-collector 1 output
    - Output current: 50 mA maximum

■ Applications

- LCD displays, digital still cameras, and PDAs

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Description
1	OSC	Pin for oscillation timing resistor and capacitor connection
2	S.C.P.	Pin for connecting the time constant setting capacitor for short-circuit protection
3	IN+1	Error amplifier 1 block noninverting input pin
4	IN−1	Error amplifier 1 block inverting input pin
5	FB1	Output pin of error amplifier 1 block
6	DT1	PWM1 block dead-time setting pin
7	Out1	Out1 block open-collector type output pin

Pin No.	Symbol	Description
8	GND	Grounding pin
9	V_{CC}	Power supply voltage application pin
10	Out2	Out2 block push-pull type output pin
11	RB2	Out2 block output source current setting resistor connection pin
12	DT2	PWM2 block dead-time setting pin
13	FB2	Output pin of error amplifier 2 block
14	IN+2	Error amplifier 2 block inverting input pin
15	Off	On/off control pin
16	V_{REF}	Reference voltage output pin

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	15	V
Off terminal allowable application voltage	V_{OFF}	15	V
IN+1 terminal allowable application voltage *2	V_{IN+1}	6	V
IN−1 terminal allowable application voltage *2	V_{IN-1}	6	V
IN+2 terminal allowable application voltage *2	V_{IN+2}	6	V
Out1 terminal allowable application voltage	V_{OUT}	15	V
Supply current	I_{CC}	—	mA
Out1 terminal output current	I_O	+50	mA
Out2 terminal source current	$I_{SO(OUT)}$	−50	mA
Out2 terminal sink current	$I_{SI(OUT)}$	+80	mA
Power dissipation *1	P_D	135	mW
Operating ambient temperature	T_{opr}	−30 to +85	°C
Storage temperature	T_{stg}	−55 to +150	°C

Note) 1. Do not apply external currents or voltages to any pins not specifically mentioned.
For the circuit currents, '+' denotes current flowing into the IC, and '−' denotes current flowing out of the IC.
2. Except for the power dissipation, operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.
3. ∗1: T_a = 85 °C. For the independent IC without a heat sink. Note that applications must observe the derating curve for the relationship between the IC power consumption and the ambient temperature.
∗2: V_{IN-1} , V_{IN-1} , $V_{IN+2} = V_{CC}$ when V_{CC} < 6 V.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	1.8 to 14	V
Off control terminal application voltage	V_{OFF}	0 to 14	V
Output source current	$I_{SO(OUT)}$	−40 (minimum)	mA
Output sink current	$I_{SI(OUT)}$	70 (maximum)	mA
Timing resistance	R_T	1 to 51	kΩ
Timing capacitance	C_T	100 to 10 000	pF
Oscillation frequency	f_{OUT}	20 to 1 000	kHz
Short-circuit protection time constant setting capacitance	C_{SCP}	1 000 (minimum)	pF
Output current setting resistance	R_B	180 to 15 000	Ω

■ Electrical Characteristics at V_{CC} = 2.4 V, C_{REF} = 0.1 µF, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference voltage block						
Reference voltage	V_{REF}	I_{REF} = − 0.1 mA	1.166	1.19	1.214	V
Input regulation with input fluctuation	Line	V_{CC} = 1.8 V to 14 V	—	15	30	mV
Load regulation	Load	I_{REF} = − 0.1 mA to −1 mA	−20	−5	—	mV

■ Electrical Characteristics at V_{CC} = 2.4 V, C_{REF} = 0.1 µF, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
U.V.L.O. block						
Circuit operation start voltage	V_{UON}		1.59	1.67	1.75	V
Error amplifier 1 block						
Input offset voltage	V_{IO}		–6	—	+6	mV
Common-mode input voltage range	V_{ICR}		0.3	—	0.7	V
Input bias current 1	I_{B1}		– 0.6	– 0.2	—	µA
High-level output voltage 1	V_{EH1}		0.83	0.93	1.03	V
Low-level output voltage 1	V_{EL1}		—	—	0.2	V
Output source current 1	$I_{SO(FB)1}$		–61	–47	–33	µA
Output sink current 1	$I_{SI(FB)1}$		33	47	61	µA
Error amplifier 2 block						
Input threshold voltage	V_{TH}		1.16	1.19	1.22	V
Input bias current 2	I_{B2}		—	0.2	0.8	µA
High-level output voltage 2	V_{EH2}		0.83	0.93	1.03	V
Low-level output voltage 2	V_{EL2}		—	—	0.2	V
Output source current 2	$I_{SO(FB)2}$		–61	–47	–33	µA
Output sink current 2	$I_{SI(FB)2}$		33	47	61	µA
Oscillator block						
Output off threshold voltage	$V_{TH(OSC)}$		0.8	0.9	1.0	V
Output 1 block						
Oscillation frequency 1	f_{OUT1}	R_T = 12 kΩ, C_T = 330 pF	185	205	225	kHz
Output duty ratio 1	Du_1		75	80	85	%
Output saturation voltage	$V_{O(SAT)}$	I_O = 30 mA	—	—	0.5	V
Output leak current	I_{OLE}	V_{CC} = 14 V	—	—	1	µA
Output 2 block						
Oscillation frequency 2	f_{OUT2}	R_T = 12 kΩ, C_T = 330 pF	185	205	225	kHz
Output duty ratio 2	Du_2		72	77	82	%
High-level output voltage	V_{OH}	I_O = –10 mA, R_B = 820 Ω	1.4	—	—	V
Low-level output voltage	V_{OL}	I_O = 10 mA, R_B = 820 Ω	—	—	0.2	V
Output source current	$I_{SO(OUT)}$	V_O = 0.7 V, R_B = 820 Ω	–40	–30	–20	mA
Output sink current	$I_{SI(OUT)}$	V_O = 0.7 V, R_B = 820 Ω	20	—	—	mA
Pull-down resistance	R_O		20	30	40	kΩ
PWM1 block						
Output full-off input threshold voltage 1	V_{T0-1}	Duty = 0%	—	0.28	0.30	V
Output full-on input threshold voltage 1	V_{T100-1}	Duty = 100%	0.65	0.72	—	V
Input current 1	I_{DT1}	V_{DT1} = 0.4 V	–1.1	– 0.5	—	µA

■ Electrical Characteristics at V_{CC} = 2.4 V, C_{REF} = 0.1 µF, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PWM2 block						
Output full-off input threshold voltage 2	V_{T0-2}	Duty = 0%	0.65	0.72	—	V
Output full-on input threshold voltage 2	V_{T100-2}	Duty = 100%	—	0.28	0.30	V
Input current 2	I_{DT2}	V_{DT2} = 0 V	−1.1	− 0.5	—	µA
Unlatch circuit 1 block						
Input threshold voltage 1	V_{THUL1}		0.15	0.20	0.25	V
Unlatch circuit 2 block						
Input threshold voltage 2	V_{THUL2}		0.8	0.9	1.0	V
Short-circuit protection circuit block						
Input standby voltage	V_{STBY}		—	60	120	mV
Input threshold voltage 1	V_{THPC1}		0.8	0.9	1.0	V
Input threshold voltage 2	V_{THPC2}		0.17	0.22	0.27	V
Input latch voltage	V_{IN}		—	60	120	mV
Charge current	I_{CHG}	V_{SCP} = 0 V	−1.43	−1.1	− 0.77	µA
On/off control block						
Input threshold voltage	$V_{ON(TH)}$		0.8	1.0	1.3	V
Whole device						
Output off consumption current	$I_{CC(OFF)}$	R_B = 820 Ω, duty = 0%	—	5.7	8.0	mA
Latch mode consumption current	$I_{CC(LA)}$	R_B = 820 Ω	—	5.6	7.8	mA
Standby current	$I_{CC(SB)}$		—	—	1	µA

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference voltage block						
V_{REF} temperature characteristics	V_{REFdT}	T_a = −30°C to +85°C	−1	—	+1	%
Over-current protection drive current	I_{OC}		—	−11	—	mA
U.V.L.O. block						
Reset voltage	V_R		—	0.8	—	V
Error amplifier 1/2 blocks						
V_{TH} temperature characteristics	V_{THdT}	T_a = −30°C to +85°C	− 0.3	—	+ 0.3	mV/°C
Open-loop gain	A_V		—	57	—	dB
Single gain bandwidth	f_{BW}		—	10	—	MHz
Output 1/2 blocks						
Frequency supply voltage characteristics	f_{dV}		−1	—	+1	%
Frequency temperature characteristics	f_{dT}		−3	—	+3	%

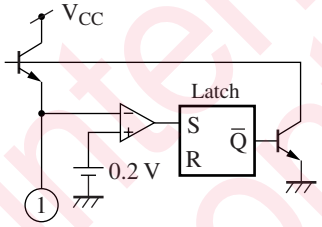
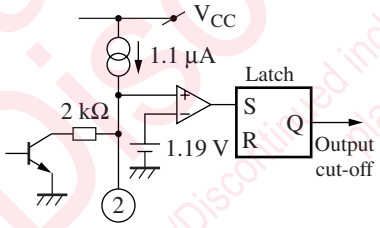
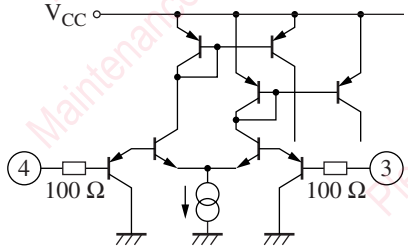
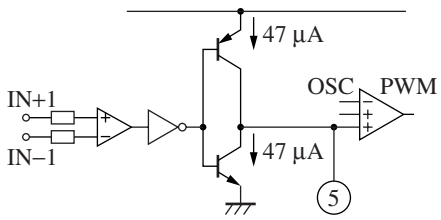
■ Electrical Characteristics at V_{CC} = 2.4 V, C_{REF} = 0.1 µF, T_a = 25°C (continued)

• Design reference data (continued)

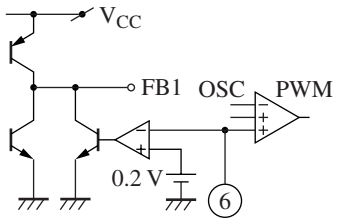
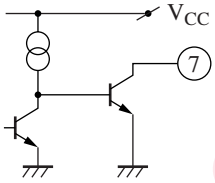
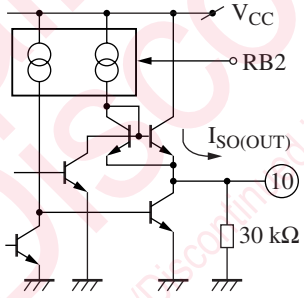
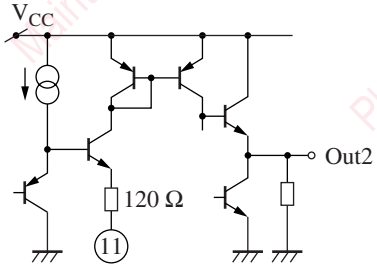
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output 2 block						
RB terminal voltage	V_B		—	0.36	—	V
Short-circuit protection block						
Comparator threshold voltage	V_{THL}		—	1.19	—	V
On/off control block						
Off terminal current	I_{OFF}		—	23	—	µA

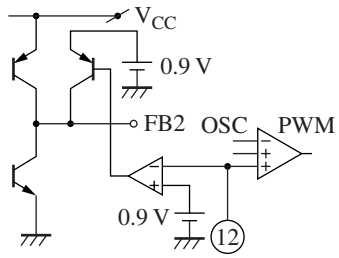
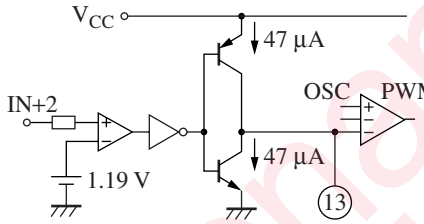
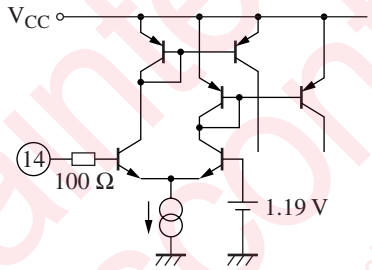
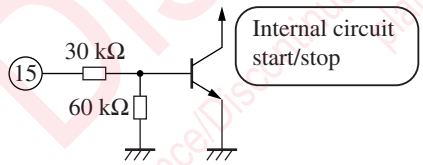
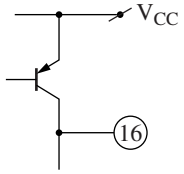
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	I/O
1		OSC: The terminal used for connecting a timing capacitor/resistor to set oscillation frequency. Use a capacitance value within the range of 100 pF to 10 000 pF and a resistance value within the range of 3 kΩ to 30 kΩ. Use an oscillation frequency in the range of 20 kHz to 1 MHz. When operating the circuit in parallel and synchronously, the channel 2 output stops when this pin becomes 0.9 V or more. (Refer to the "Application Notes, [7]" section.)	O
2		S.C.P.: The terminal for connecting a capacitor to set the time constant of the timer latch short-circuit protection circuit. Use a capacitance value in the range of 1 000 pF or more. The charge current I_{CHG} is 1.1 µA typical.	O
3		IN+1: The noninverting input pin for error amplifier 1 block.	I
4		IN−1: The inverting input pin for error amplifier 1 block.	I
5		FB1: The output pin for error amplifier 1 block. The source current is –47 µA and the sink current is 47 µA. Correct the frequency characteristics of the gain and the phase by connecting a resistor and a capacitor between this terminal and GND.	O

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
6		DT1: The pin for setting channel 1 output maximum duty ratio. If this terminal is set at a voltage of 0.20 V or less, FB1 terminal becomes low-level voltage and the protective function for channel 1 output short-circuit will stop (Unlatch function).	I
7		Out1: The pin is open-collector type output terminal. The absolute maximum rating of output current is +50 mA.	O
8		GND: Grounding terminal	—
9		V_{CC}: The supply voltage application terminal Use the operating supply voltage in the range of 1.8 V to 14 V.	—
10		Out2: The pin is push-pull type output terminal. The absolute maximum rating of output source current is −50 mA. The absolute maximum rating of output sink current is +80 mA. A constant current output with less fluctuation with power supply voltage and dispersion can be obtained by the resistor externally attached to RB2 pin. $I_{SO(OUT)2} = 68 \times \frac{V_{RB2}}{R_{B2}}$ [A]	O
11		RB2: The pin for connecting a resistor for setting channel 2 output current. Use a resistance value in the range of 180 Ω to 15 kΩ. The terminal voltage is 0.36 V (at R_{B2} = 820 Ω). Please refer to the "Usage Notes [2]", if you intend to directly drive a n-channel MOSFET from this pin.	I

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
12		DT2: The pin for setting channel 2 output maximum duty ratio. If this terminal is set at a voltage of 0.9 V or more, FB2 terminal becomes high-level voltage and the protective function for channel 2 output short-circuit will stop (Unlatch function).	I
13		FB2: The output pin for error amplifier 2 block. The source current is –47 µA and the sink current is 47 µA. Correct the frequency characteristics of the gain and the phase by connecting a resistor and a capacitor between this terminal and GND.	O
14		IN+2: The noninverting input pin for error amplifier 2 block.	I
15		Off: The terminal for on/off control. High-level input: Normal operation (V_{OFF} > 1.3 V) Low-level input: Standby state (V_{OFF} < 0.8 V) The total current consumption in the standby state can be suppressed to a value 1 µA or less.	I
16		V_{REF}: The output terminal for the internal reference voltage. The reference voltage is 1.19 V (allowance: ± 2%) at V_{CC} = 2.4 V and I_{REF} = – 0.1 mA. Connect a capacitor of 0.01 µF or more between V_{REF} and GND for phase compensation.	O

■ Usage Notes

[1] The loss P of this IC increases in proportion to the supply voltage. Use the IC so as not to exceed the allowable power dissipation of package P_D .

Reference formula:

$P = V_{O(SAT)1} \times I_{OUT1} \times Du_1 + (V_{CC} - V_{BEQ2}) \times I_{SO(OUT)} \times Du_2 + V_{CC} \times I_{CC} < P_D$

$V_{O(SAT)1}$: Out1 terminal saturation voltage (0.5 V maximum at I_{OUT1} = 30 mA)

I_{OUT1} : Out1 terminal output current (= $\{V_{CC} - V_{BEQ1} - V_{O(SAT)1}\} / R_{O1}$)

Du_1 : Output1 duty ratio

V_{BEQ2} : Base-emitter voltage of npn transistor Q2

$I_{SO(OUT)}$: Out2 terminal output source current (set by RB, $I_{SO(OUT)}$ = 40 mA maximum at RB2 = 820 Ω)

Du_2 : Output2 duty ratio

I_{CC} : V_{CC} terminal current (8.0 mA maximum but at V_{CC} = 2.4 V)

[2] Since the output 2 of the AN8018SA is assuming the bipolar transistor driving, it is necessary to pay attention to the following points when directly driving n-channel MOSFET.

1. Select an n-channel MOSFET having a low input capacitance

   The AN8018SA is of the constant-current (50 mA maximum) output source-current type circuit assuming the bipolar transistor driving. Also, its sink current capability is around 80 mA maximum. For those reason, it is necessary to pay attention to the increase of loss due to the extension of the output rise time and the output fall time.

   If any problem arises, there is a method to solve it by amplifying with inverters as shown in figure 1.

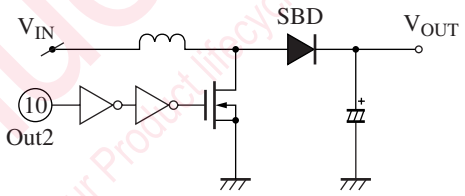


Figure 1. Output bootstrap circuit example

2. Select an n-channel MOSFET having a low gate threshold value

   The output high-level voltage of Out2 pin of the AN8018SA is V_{CC} −1.0 V minimum, so that it is necessary to select a low V_T MOSFET having a sufficiently low on-state resistance in accordance with the using operating supply voltage.

   If a larger V_{GS} is desired, there is a method to apply the double-voltage of the input to the IC's V_{CC} pin by using the transformer as shown in figure 2.

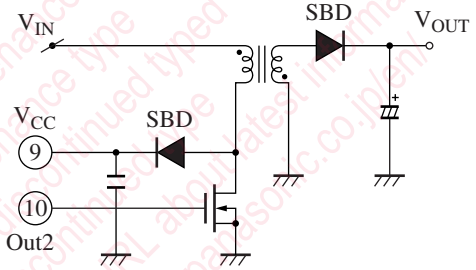


Figure 2. Gate drive voltage increasing method

[3] In order to realize a low noise and high efficiency, a care should be taken in the following points in designing the board layout.

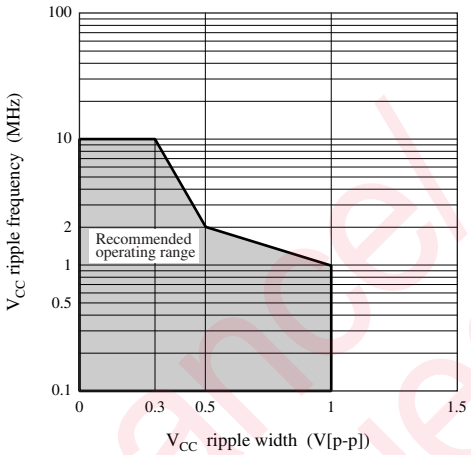
1. The wiring for ground line should be taken as wide as possible and grounded separately from the power system.
2. The input filter capacitor should be arranged in a place as close to V_{CC} and GND pin as possible so as not to allow switching noise to enter into the IC inside.
3. The wiring between the Out terminal and switching device (transistor or MOSFET) should be as short as possible to obtain a clean switching waveform.
4. In wiring the detection resistor of the output voltage, the wiring for the low impedance side should be longer.

[4] There is a case in which this IC does not start charging to the S.C.P. capacitor when the output is short-circuited due to the malfunction of U.V.L.O. circuit biased by V_{CC} that has ripples generated by turning on and off of the switching transistor. The allowable range of the V_{CC} ripple is as shown in the following figure. Reduce the V_{CC} ripple by inserting a capacitor near the V_{CC} terminal and GND terminal of this IC so that the V_{CC} ripple is in this allowable range. However, this allowable range is design reference value and not the guaranteed value.

■ Usage Notes (continued)

[4] (continued)

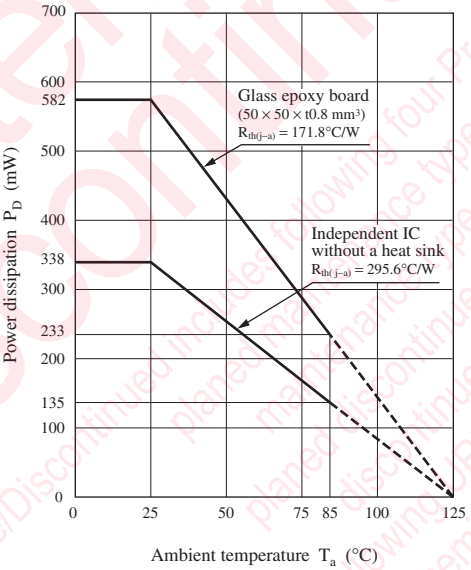
V_{CC} ripple allowable range



■ Application Notes

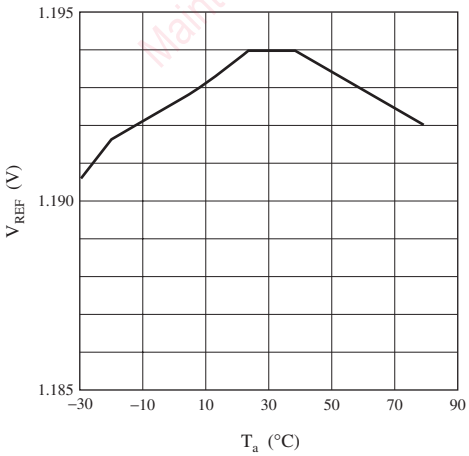
[1] P_D — T_a curves of SSOP016-P-0225A

P_D — T_a

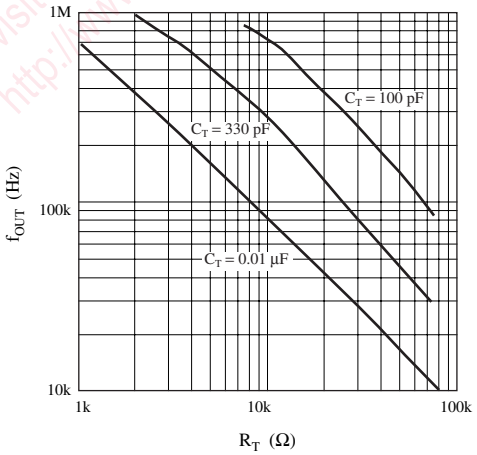


[2] Main characteristics

V_{REF} temperature characteristics



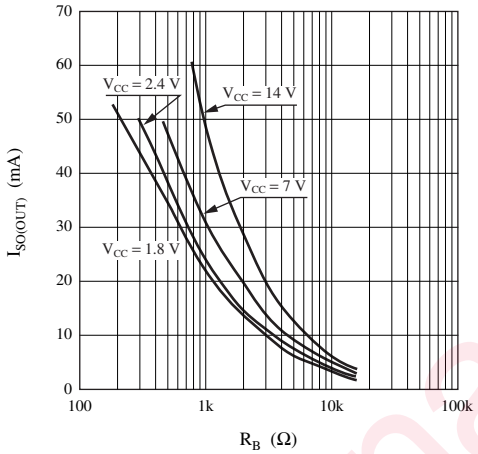
Frequency characteristics



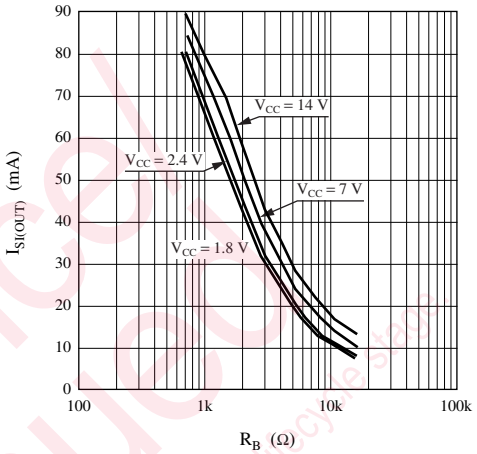
■ Application Notes (continued)

[2] Main characteristics (continued)

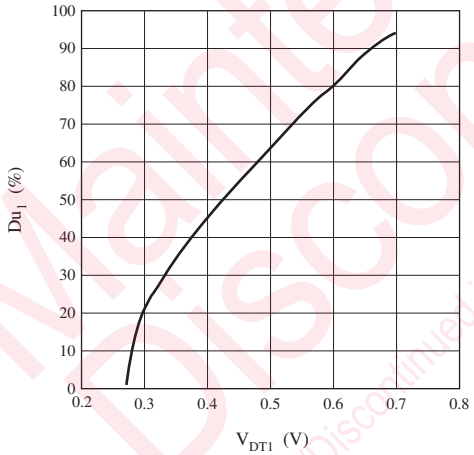
$I_{SO(OUT)}$ — R_B



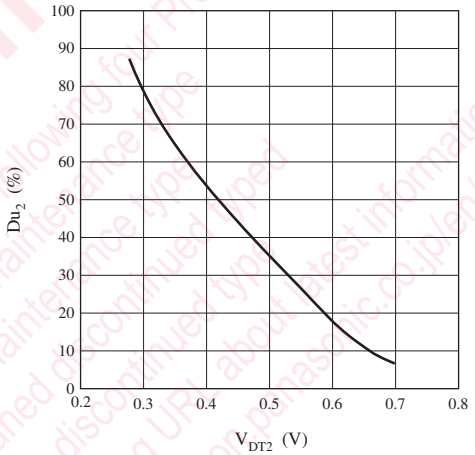
$I_{SI(OUT)}$ — R_B



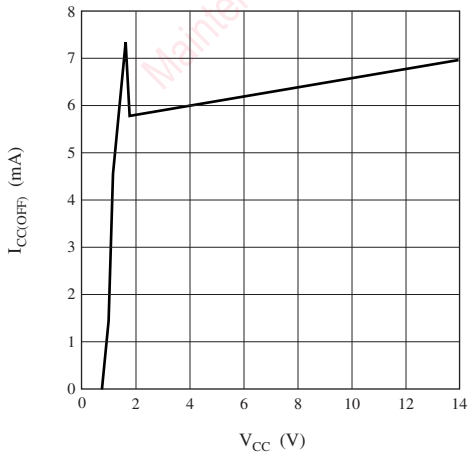
Du_1 — V_{DT1}



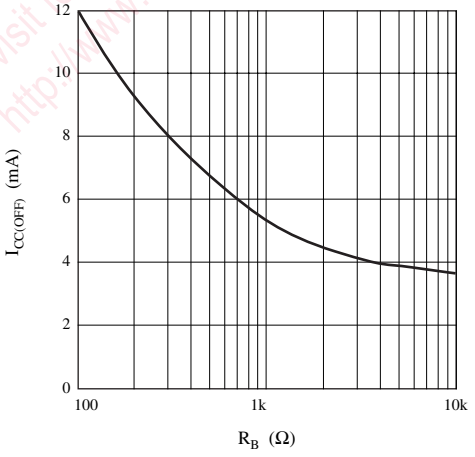
Du_2 — V_{DT2}



$I_{CC(OFF)}$ — V_{CC}

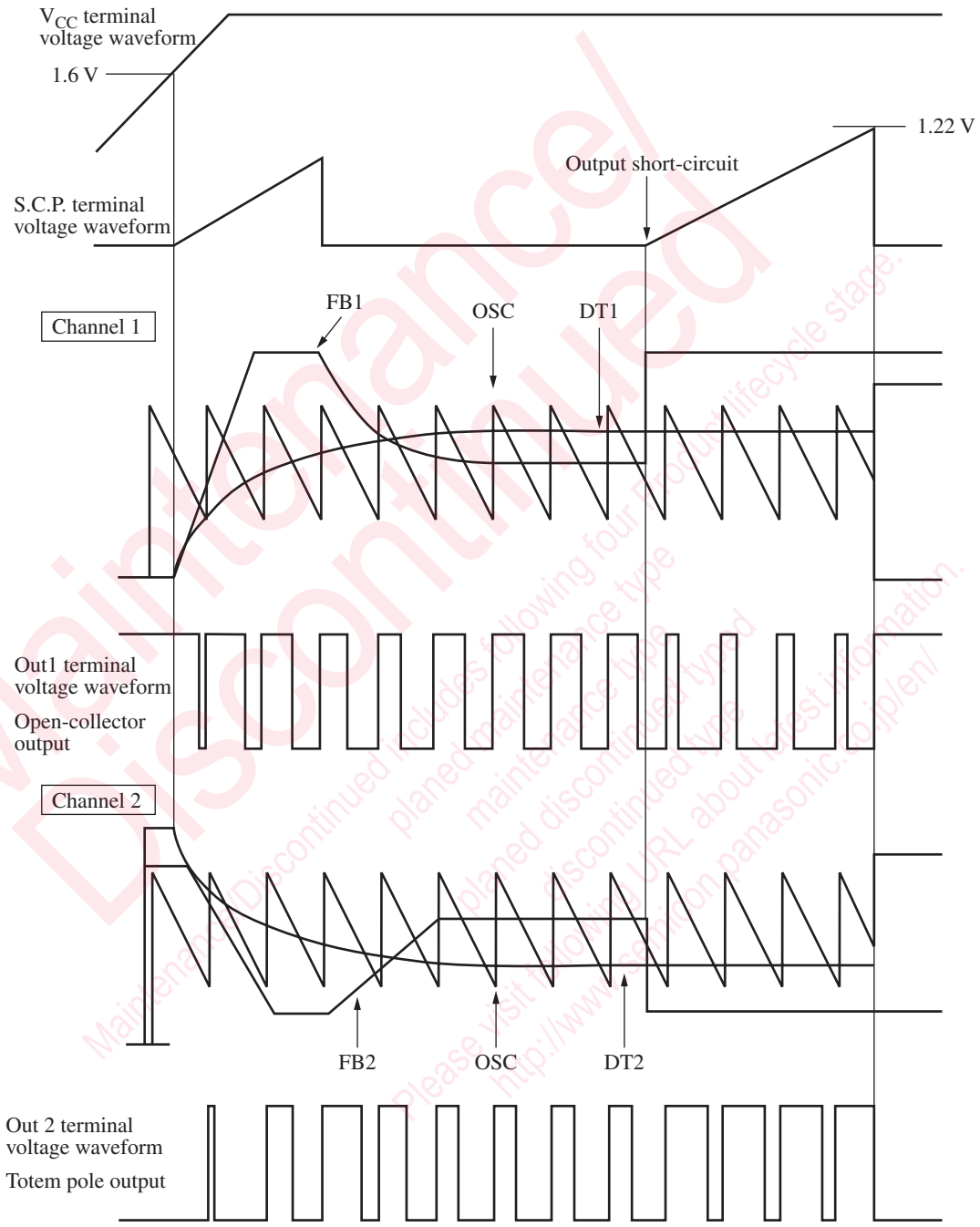


$I_{CC(OFF)}$ — R_B



■ Application Notes (continued)

[3] Timing chart (inside waveform)



■ Application Notes (continued)

[4] Function descriptions

1. Reference voltage block

   This block is composed of the band gap circuit, and outputs the temperature compensated 1.19 V reference voltage. The reference voltage is stabilized when the supply voltage is 1.8 V or more. The reference voltage is also used as the reference voltage for the error amplifier 2 block.

2. Triangular wave oscillation block

   The sawtooth-waveform-like triangular wave having a peak of approximately 0.7 V and a trough of approximately 0.2 V can be generated by connecting the timing capacitor C_T and resistor R_T to the OSC terminal (pin 1). The oscillation frequency can be freely set by the value of C_T and R_T to be connected externally. The usable oscillation frequency is from 20 kHz to the maximum 1 MHz. The triangular wave is connected with the inverting input of PWM comparator for channel 1 side and the noninverting input of PWM comparator for channel 2 side within the IC inside. Rough calculation of oscillation frequency can be calculated by the following equation.

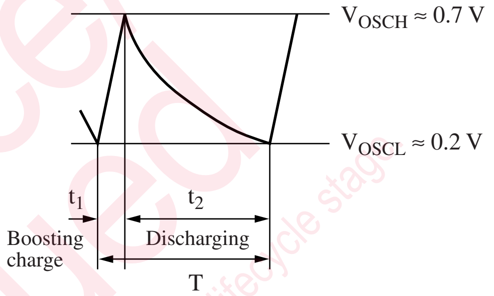


Figure 1. Triangular wave oscillation waveform

$$f_{OSC} \approx -\frac{1}{C_T \times R_T \times \ln \dfrac{V_{OSCL}}{V_{OSCH}}} \approx 0.8 \times \frac{1}{C_T \times R_T} \text{ [Hz]}$$

   However, boosting charge time, over-shoot and under shoot quantities are not considered in the above equation. And refer to the experimentally determined graph of the frequency characteristics provided in the main characteristics section.

3. Error amplifier 1 block

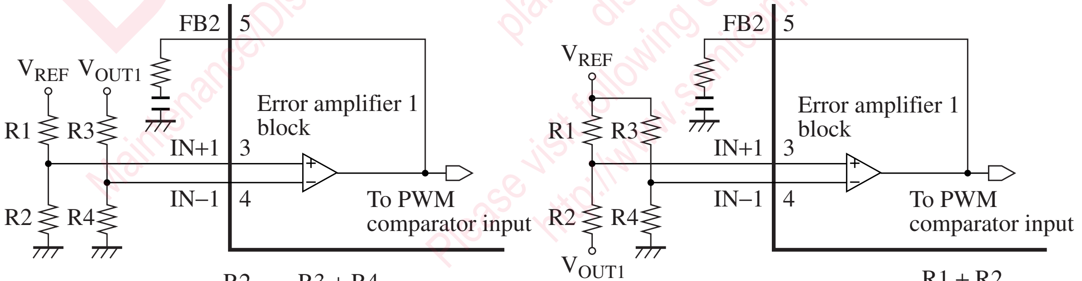
   The output voltage of DC-DC converter is detected by the pnp-transistor-input type error-amplifier and the amplified signal is input to the PWM comparator.

   Also, it is possible to perform the gain setting and the phase compensation arbitrarily by connecting a resistor and a capacitor from the FB1 terminal (pin 5) to GND in series.

   The output voltage V_{OUT1} can be set by making connection as shown in figure 2.

Case of step-up output

Case of inverting output



$$V_{OUT1} = \frac{R2}{R1 + R2} \cdot \frac{R3 + R4}{R4} \cdot V_{REF}$$

$$V_{OUT1} = -(V_{REF} - V_{IN-1}) \cdot \frac{R1 + R2}{R1} + V_{REF}$$

$$V_{IN-1} = V_{REF} \cdot \frac{R4}{R3 + R4}$$

Figure 2. Connection method of error amplifier 1 block

4. Error amplifier 2 block

   The output voltage of DC-DC converter is detected by the npn-transistor-input type error-amplifier and the amplified signal is input to the PWM comparator. The internal reference voltage 1.19 V is given to the noninverting input.

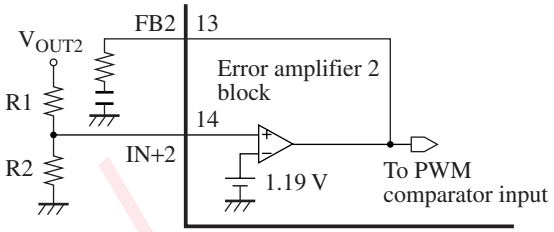
■ Application Notes (continued)

[4] Function descriptions (continued)

4. Error amplifier 2 block (continued)

Also, it is possible to perform the gain setting and the phase compensation arbitrarily by connecting a resistor and a capacitor from the FB2 terminal (pin 13) to GND in series.

The output voltage V_{OUT2} can be set by making connection as shown in figure 3.



$$V_{OUT2} = 1.19 \times \frac{R_1 + R_2}{R_2}$$

Figure 3. Connection method of error amplifier 2 block (step-up output)

5. Timer latch short-circuit protection circuit

This circuit protects the external main switching devices, flywheel diodes, and choke coils, etc. from destruction or deterioration if overload or short-circuit condition of power supply output lasts for a certain time.

The timer latch short-circuit protection circuit detects the output level of the error amplifier. When the output voltage of DC-DC converter drops and the FB1 terminal (pin 5) becomes 0.9 V or more, or the FB2 terminal (pin 13) becomes 0.22 V or less, the low-level output is given and the timer circuit is actuated to start the charge of the external protection-enable capacitor.

If the output of the error amplifier does not return to a normal voltage range by the time when the voltage of this capacitor reaches 1.19 V, it sets the latch circuit, and cuts off the output drive transistor, and sets the dead-time to 100%.

6. Low input voltage malfunction prevention circuit (U.V.L.O.)

This circuit protects the system from destruction or deterioration due to control malfunction when the supply voltage is low in the transient state of power on/off.

The low input voltage malfunction prevention circuit detects the internal reference voltage which changes according to the supply voltage level. Until the supply voltage reaches 1.67 V during its rise time, it cuts off the output drive transistor, and sets the dead-time to 100%. At the same time, it holds the S.C.P. terminal (pin 2) and DT1 terminal (pin 6) to low-level, and the OSC terminal (pin 1) and DT2 terminal (pin 12) to high-level.

7. PWM comparator block

The PWM comparator controls the on-period of the output pulse according to the input voltage. The PWM1 and PWM2 block are set in an opposite logic relation of each other and on-period of each output is staggered.

The PWM1 block turns on the output transistor during the period when the triangular wave of OSC terminal (pin 1) is lower than any lower one of the FB1 (pin 5) terminal voltage and the DT1 (pin 6) terminal voltage.

The PWM2 block turns on the output transistor during the period when the triangular wave of OSC terminal (pin 1) is higher than any higher one of the FB2 (pin 13) terminal voltage and the DT2 (pin 12) terminal voltage.

The maximum duty ratio is variable from the outside.

Also, the soft start which gradually extends on-period of the output pulse is activated by connecting a capacitor in parallel with the resistor-dividing for the maximum duty ratio setting.

8. Unlatch block

The unlatch circuit 1 block fixes the FB1 terminal (pin 5) at low level at the DT1 terminal (pin 6) is 0.20 V or less. The unlatch circuit 2 block fixes the FB2 terminal (pin 13) at high-level at the DT2 terminal (pin 12) is 0.9 V or more. Consequently, by controlling the DT1 and the DT2 terminal voltages, it is possible to operate only one channel or to start and stop each channel in any required sequence.

9. Output 1 block

This output circuit is open-collector type. The available output current is up to 50 mA. The breakdown voltage of output terminal is 15 V.

10. Output 2 block

This block uses a totem pole type output circuit. By connecting the current setting resistor to the RB2 terminal, it is possible to arbitrarily set a constant-current source-output having a small fluctuation with the supply voltage.

The available constant-current source-output is up to 50 mA.

■ Application Notes (continued)

[5] About logic of PWM block

The logic for channel 1 and channel 2 of this IC is reversed. Thereby an input current flatness is realized. At the same time, noise can be suppressed to a lower level by staggering the turn on timing.

The PWM1 block turns on the output transistor during the period when the triangular wave of the OSC terminal (pin 1) is lower than both of the FB1 (pin 5) terminal voltage and the DT1 (pin 6) terminal voltage.

The PWM2 block turns on the output transistor during the period when the triangular wave of OSC terminal (pin 1) is higher than both of the FB2 (pin 13) terminal voltage and the DT2 (pin 12) terminal voltage.

(Refer to figure 4.)

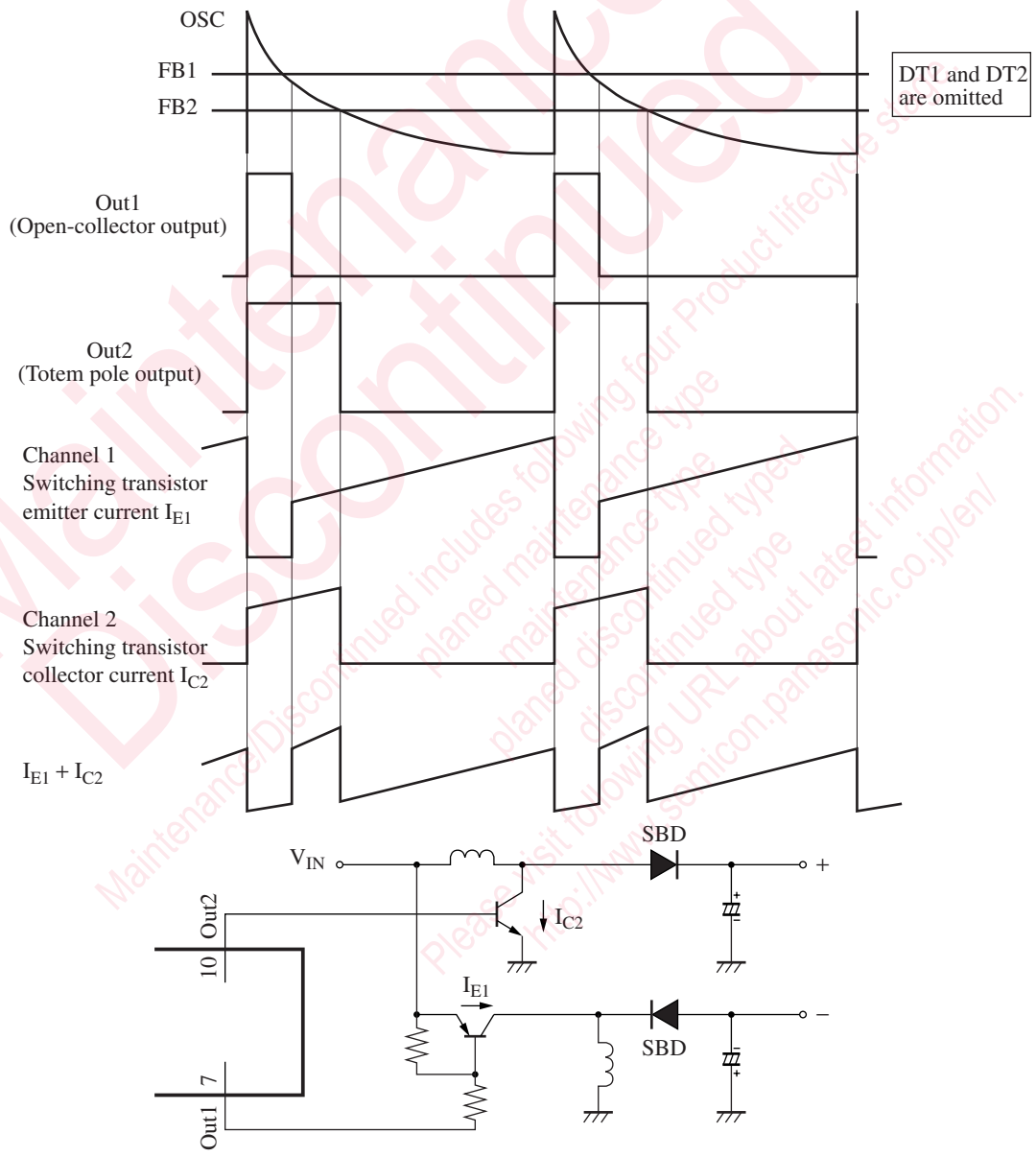


Figure 4. PWM logic explanation chart

■ Application Notes (continued)

[6] Time constant setting method for timer latch short-circuit protection circuit

The constructional block diagram of protection latch circuit is shown in figure 6. The comparator for short-circuit protection compares the error amplifier 1 output FB1 with the reference voltage of 0.9 V for channel 1 side, and the error amplifier 2 output FB2 with the reference voltage of 0.22 V for channel 2 side at all the time.

When the load conditions of DC-DC converter output is stabilized, there is no fluctuation of error amplifier output and the short-circuit protection comparator also keeps the balance. At this moment, the output transistor Q1 is in the conductive state and the S.C.P. terminal is held to approximately 60 mV.

When the load conditions for channel 1 side suddenly change and high-level signal (0.9 V or more) is input from the error amplifier 1 block to the short-circuit protection comparator, the short-circuit protection comparator outputs the low-level signal to cut off the output transistor Q1. Also, when the load conditions for channel 2 side suddenly change and low-level signal (0.22 V or less) is inputted from the error amplifier 2 block to the short-circuit protection comparator, the short-circuit protection comparator outputs the low-level signal to cut off the output transistor Q1. The capacitor C_{SCP} connected to the S.C.P. terminal starts charging. When the external capacitor C_{SCP} has been charged to approximately 1.19 V with the constant current of approximately 1.1 μA, the latch circuit is set, the output terminal is fixed to low level, and the dead-time is set to 100%. Once the latch circuit is set, the S.C.P. terminal is discharged to approximately 40 mV, However, the latch circuit is not reset unless the power for the latch circuit is turned off or restarted by the on/off control.

$$1.19\ \text{V} = I_{CHG} \times \frac{t_{PE}}{C_{SCP}}$$

$$\therefore\ t_{PE}\ [\text{s}] = 1.08 \times C_{SCP}$$

When the power supply is turned on, the output is considered to be short-circuited state so that the S.C.P. terminal voltage starts charging. It is necessary to set the external capacitor so as to start up the DC-DC converter output voltage before setting the latch circuit in the later stage. Especially, pay attention to the delay of the start-up time when applying the soft-start.

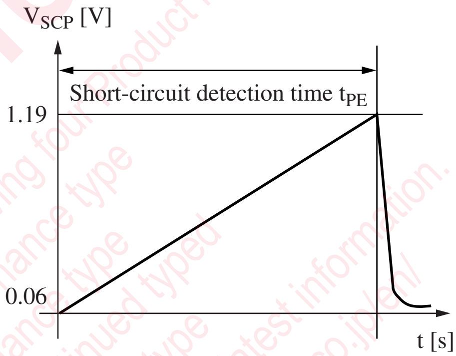


Figure 5. S.C.P. terminal charging waveform

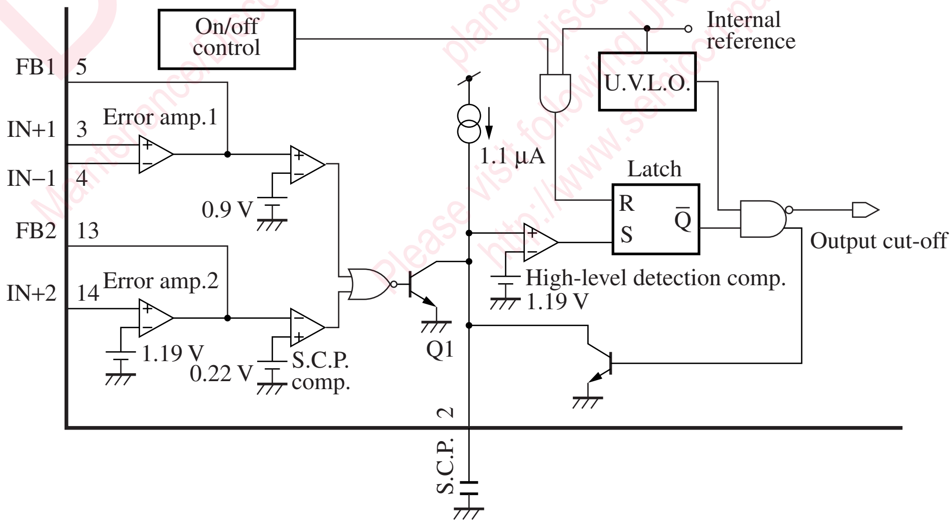


Figure 6. Short-circuit protection circuit

■ Application Notes (continued)

[7] Parallel synchronous operation of multiple ICs

Multiple instances of this IC can be operated in parallel. If the OSC terminals (pin 1) and Off terminals (pin 15) are connected to each other as shown in figure 7, the ICs will operate at the same frequency.

It is possible to operate this IC (the AN8018SA) with the two-channel totem pole output IC AN8017SA in parallel synchronous mode.

1. Usage notes
   1) The parallel synchronous operation with the single-channel AN8016SH/AN8016NSH is not possible.
   2) The remote on/off with the single IC itself is not possible. Only the simultaneous remote on/off of all ICs is possible.

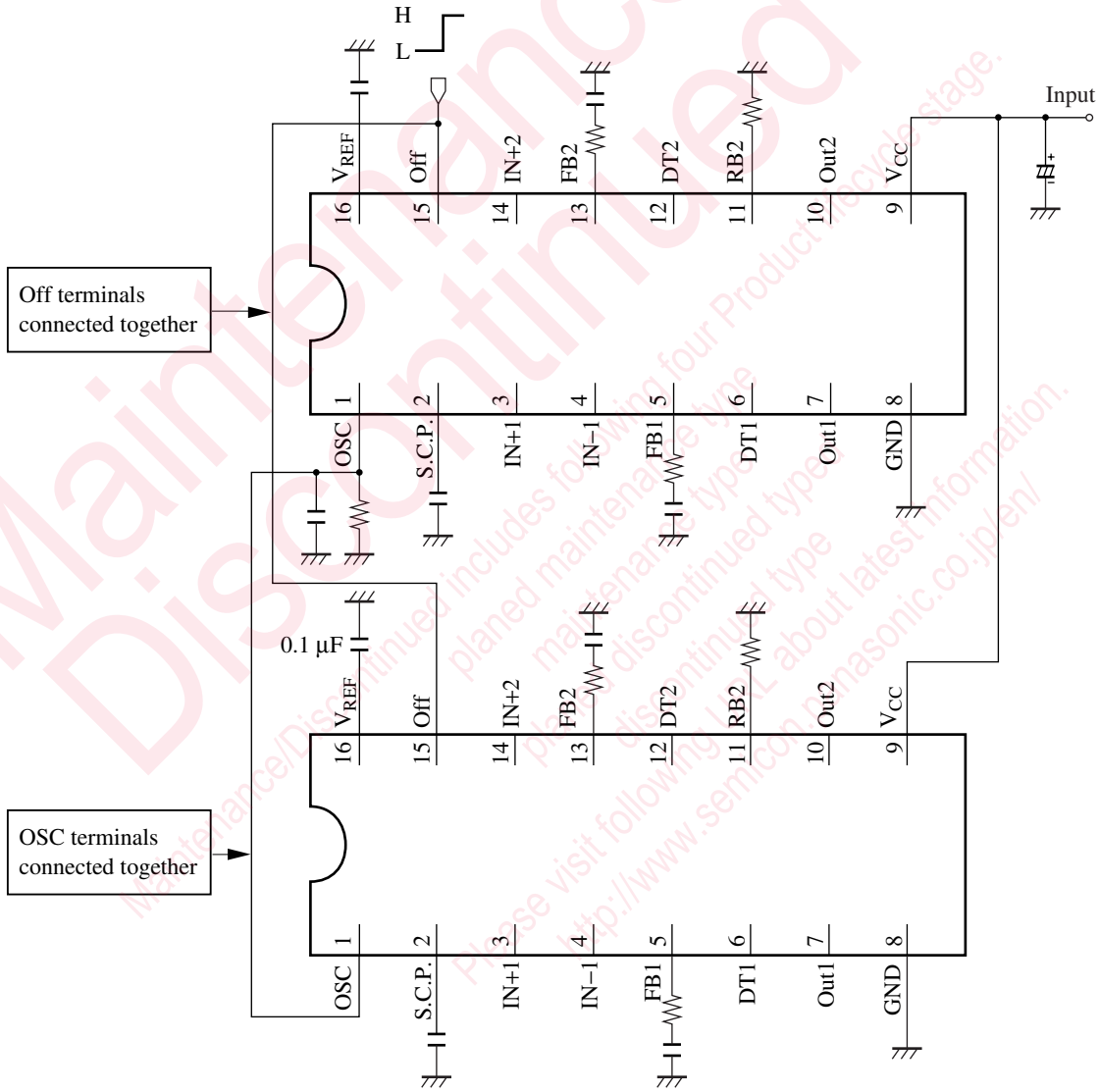


Figure 7. Slave operation circuit example

■ Application Notes (continued)

[7] Parallel synchronous operation of multiple ICs (continued)

2. About the operation of short-circuit protection at parallel synchronous operation

In the case of the operation in parallel, if the single output (or multiple outputs) of them is short-circuited and the timer latch short circuit protection of the IC is operated, the output of other ICs will be also shut down, then enter into latch mode.

In figure 8, if the IC-2 entered timer latch mode, Q1 turns on and the OSC terminal (pin 1) is fixed to approximately 1.1 V and the oscillator stops.

Then channel 1 of IC-1 becomes low level than the DT1 terminal (pin 6) voltage or high-level voltage (0.9 V) of the FB1 terminal set by terminal voltage, and then output 2 stops by PWM1 circuit of inside. The channel 2 stops output 2 by oscillator high-level detection comparator.

And then, the IC-1 becomes short-circuit state and enters latch mode after a certain time.

It becomes the same operation in case of the IC-1 enters latch mode previously.

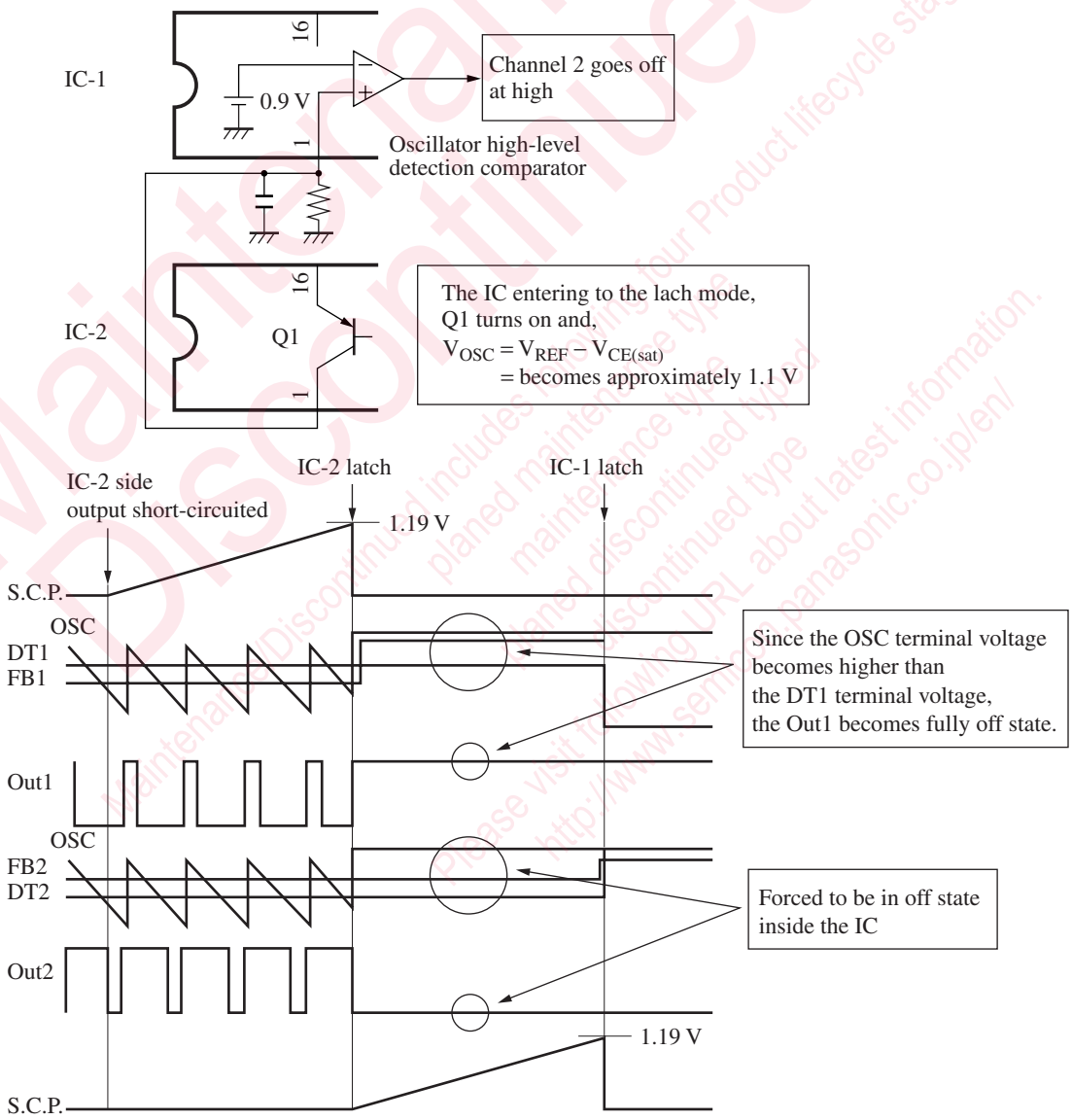


Figure 8. Operation of short-circuit protection at parallel synchronous operation

■ Application Notes (continued)

[8] Setting of Off-terminal connection resistor

The start circuit starts its operation when Q1 is turned on. In case of the resistor R_{OFF} is connected externally as shown in figure 9, the input voltage V_{CTL} at which the start circuit operates is obtained by the equation:

$V_{CTL} > V_{BEQ1} \times (R_{OFF} + R_1 + R_2) / R_2$

Therefore, R_{OFF} can be set by:

$R_{OFF} < R_2 \cdot V_{CTL} / V_{BEQ1} - R_1 - R_2$

Set the value of R_{OFF} according to above equations.

(Typical value)

$R_{OFF} < 25$ kΩ including temperature characteristics and sample to sample variations at $V_{CTL} = 3$ V.

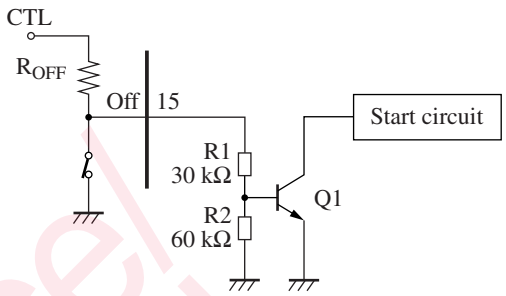


Figure 9. Off terminal peripheral circuit

[9] Sequential operation

In the case of sequential operation is necessary for each channel at IC operation, it is possible to turn on/off the output of DC-DC converter individually by turning on/off Q1 and Q2 as shown in figure 10.

In the channel 1 side, if Q1 turns on and the DT1 terminal (pin 6) becomes 0.2 V or less, the output transistor turns off due to lower voltage than the OSC terminal (pin 1). Simultaneously, unlatch circuit 1 block operates, and the timer latch short-circuit protection does not operate because the FB1 terminal (pin 5) becomes fixed to low even if output of channel 1 downs.

In the channel 2 side, if Q1 turns on and the DT2 terminal (pin 12) becomes 0.9 V or more, the output transistor turns off due to higher voltage than the OSC terminal (pin 1). Simultaneously, unlatch circuit 2 block operates, and the timer latch short-circuit protection does not operate because the FB2 terminal (pin 13) becomes fixed to high even if output of channel 2 downs.

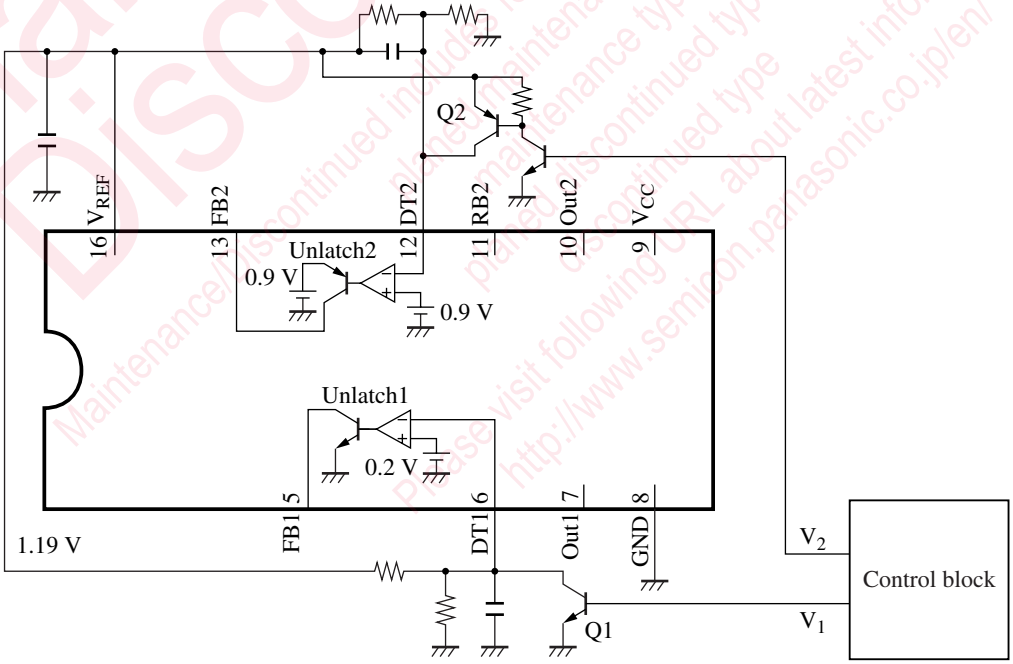
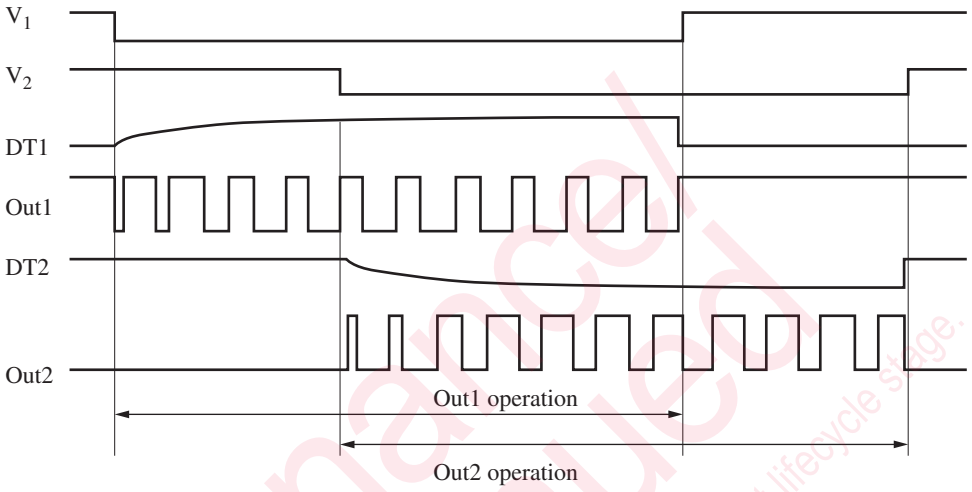


Figure 10

■ Application Notes (continued)

[9] Sequential operation (continued)



Operation when each channel single on/off

[10] Error amplifier phase-compensation setting method

The equivalent circuit of error amplifier is as shown in figure 11.

The transfer function is:

$$H = \frac{1 / \{S (C_{E1} + C_{O1})\}}{R_{E1} + 1 / \{S (C_{E1} + C_{O1})\}} = \frac{1}{SC_{O1} \cdot R_{E1} + 1} \quad (\text{from } C_{E1} << C_{O1})$$

The cut-off frequency is variable by changing the externally attached phase compensation capacitor C_{O1} .

Adjust by inserting a resistor R_{O1} between the FB1 terminal and C_{O1} in series as shown in figure 12 when it is required to have a gain on the high frequency side or desired to lead a phase.

The transfer function is:

$$H = \frac{SC_{O1} \cdot R_{O1} + 1}{SC_{O1} (R_{O1} + R_{E1}) + 1} \quad (\text{from } C_{E1} << C_{O1})$$

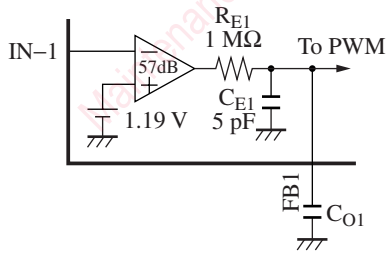


Figure 11. Error amplifier equivalent circuit

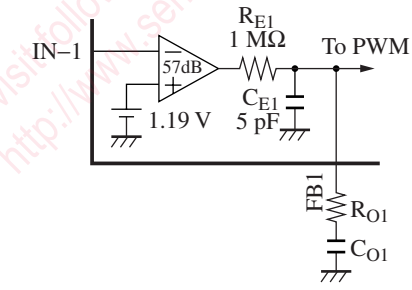
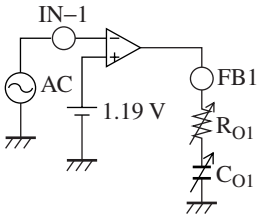
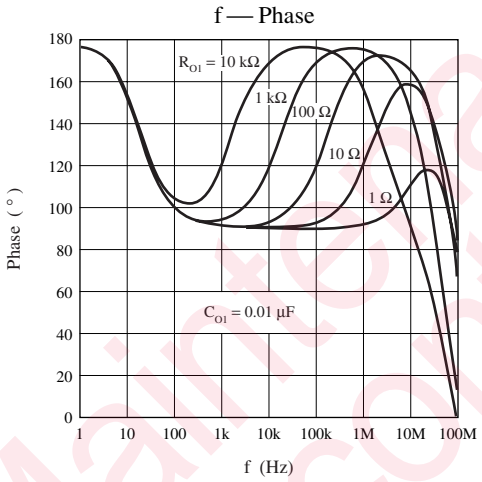


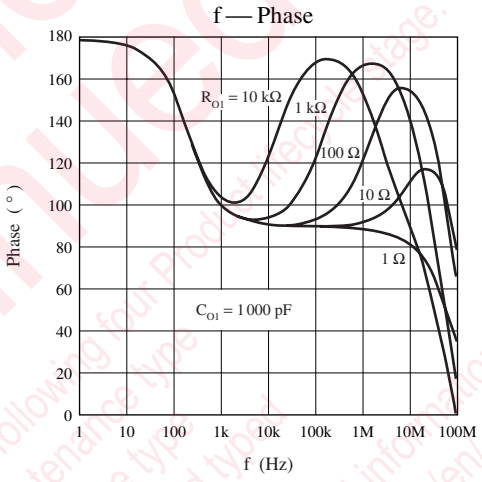
Figure 12. Error amplifier equivalent circuit (R_{O1} inserted)

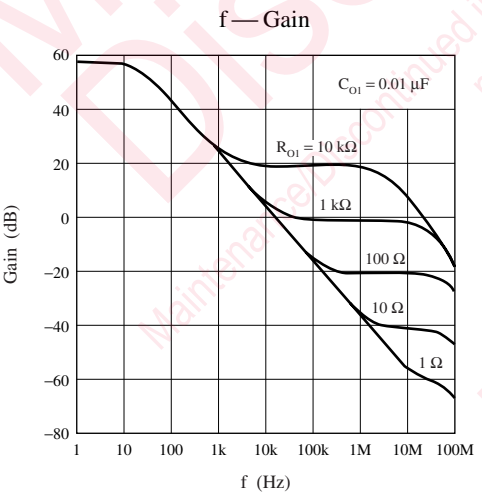
■ AC Analysis Result

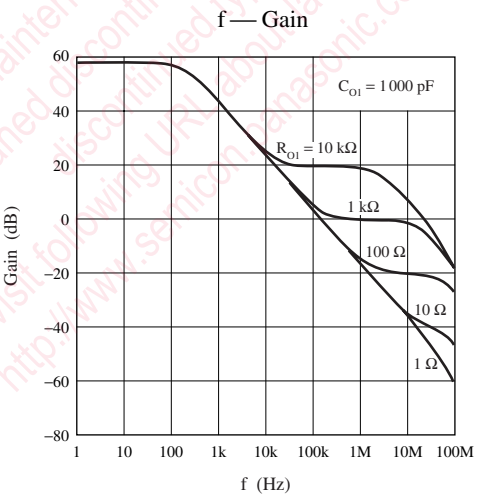
• Simulation circuit





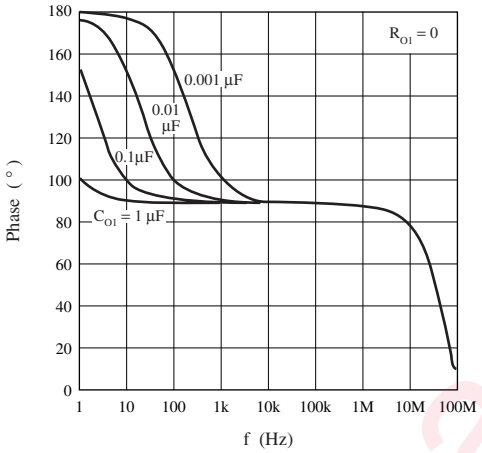




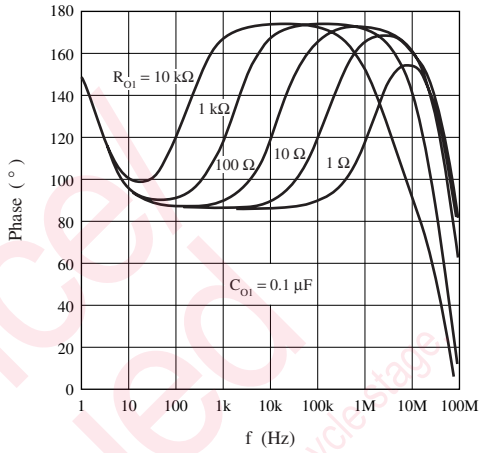


■ AC Analysis Result (continued)

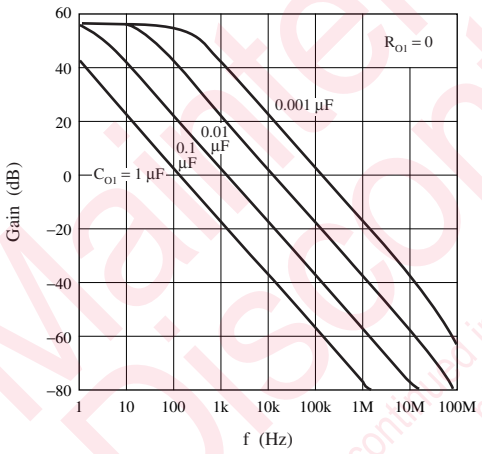
f — Phase



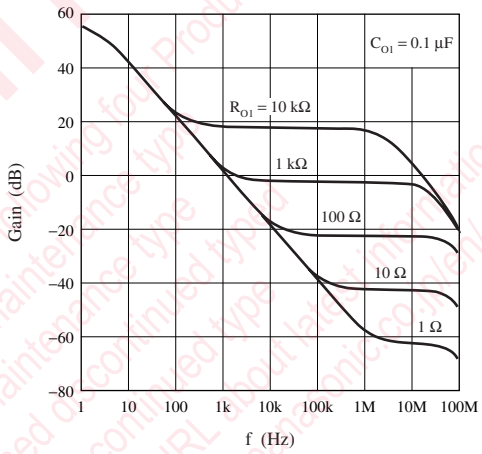
f — Phase



f — Gain

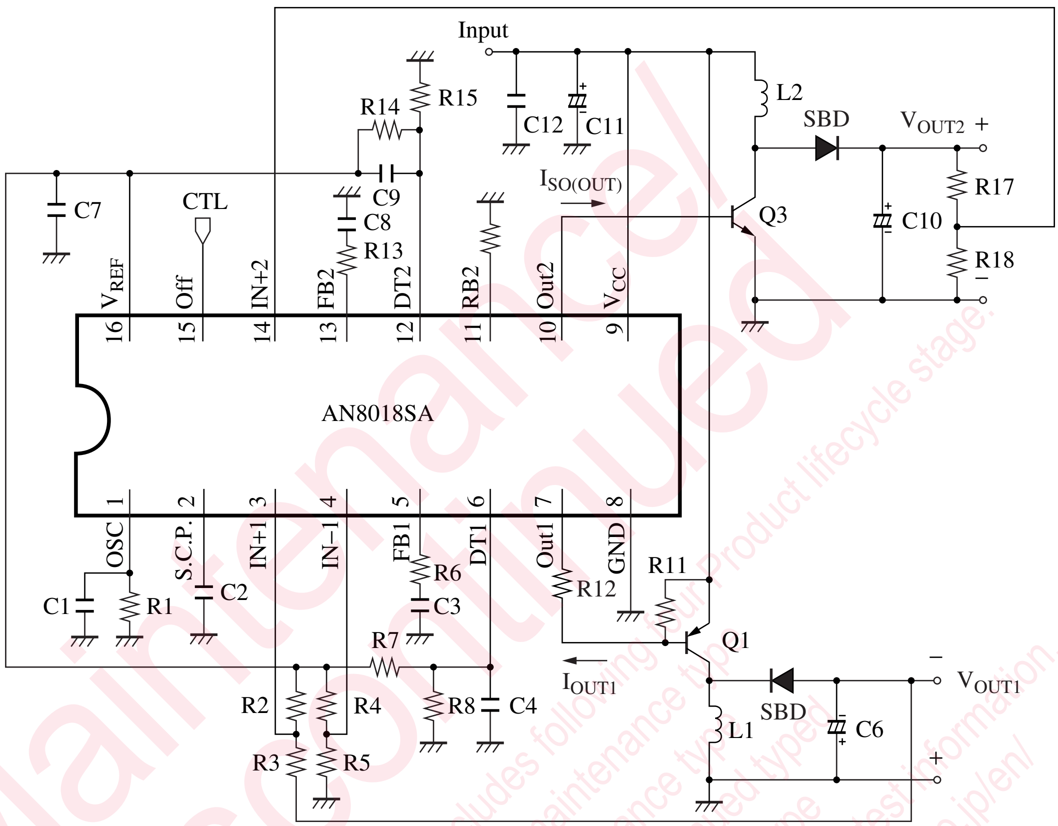


f — Gain

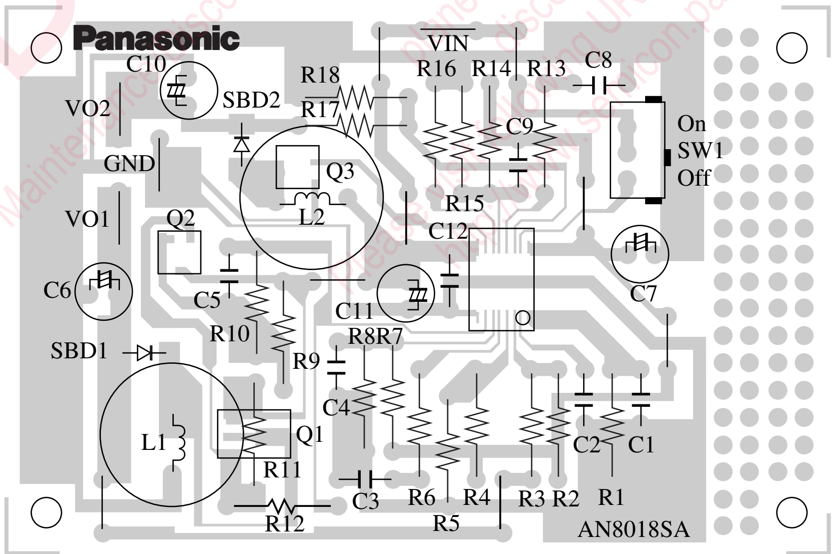


■ Application Circuit Examples

• Circuit construction for evaluation board

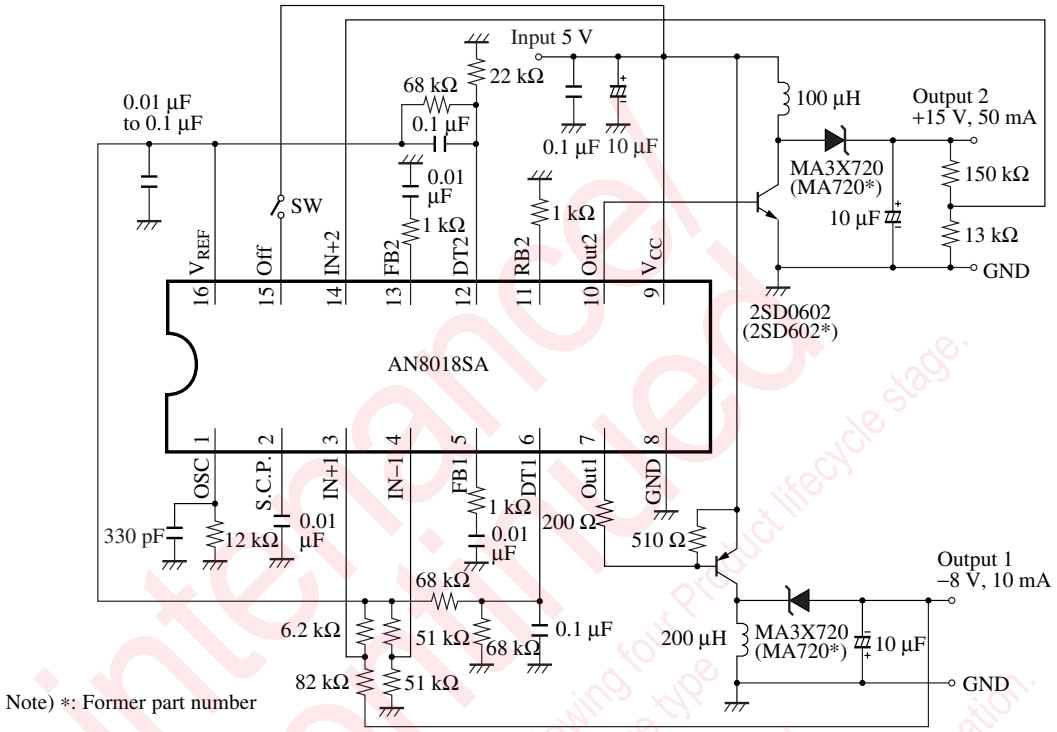


• Evaluation board



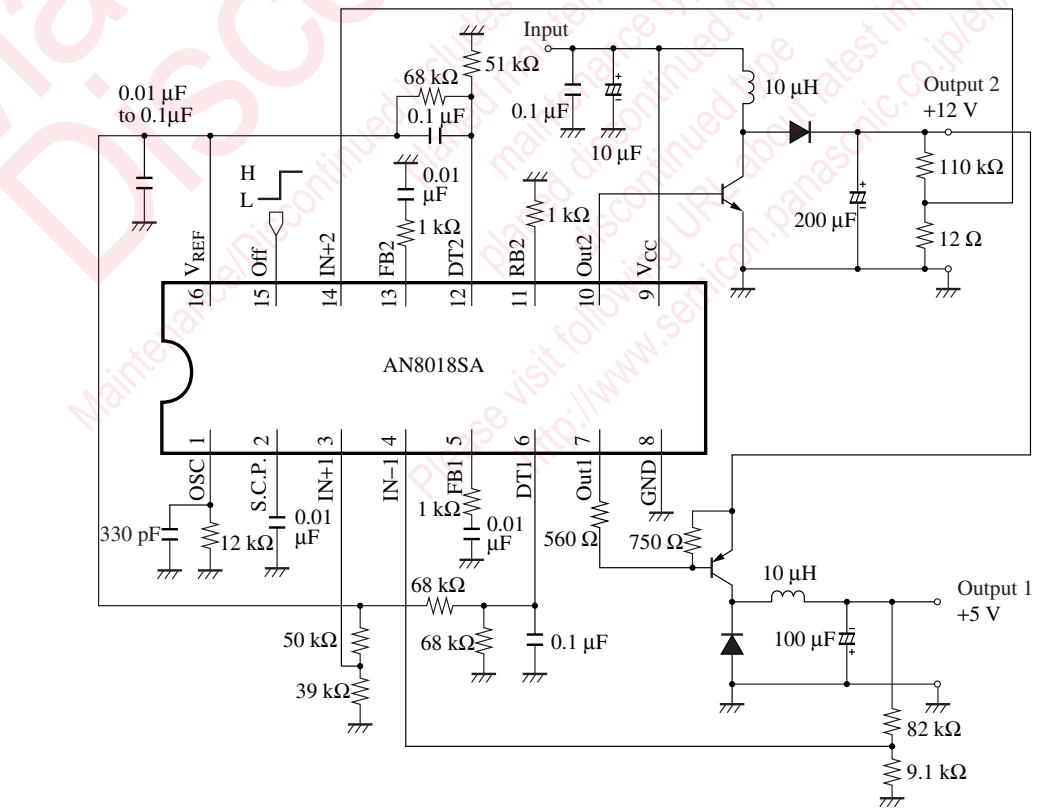
■ Application Circuit Examples (continued)

• Application circuit example 1 (Input 5 V, output 15 V/−8 V)



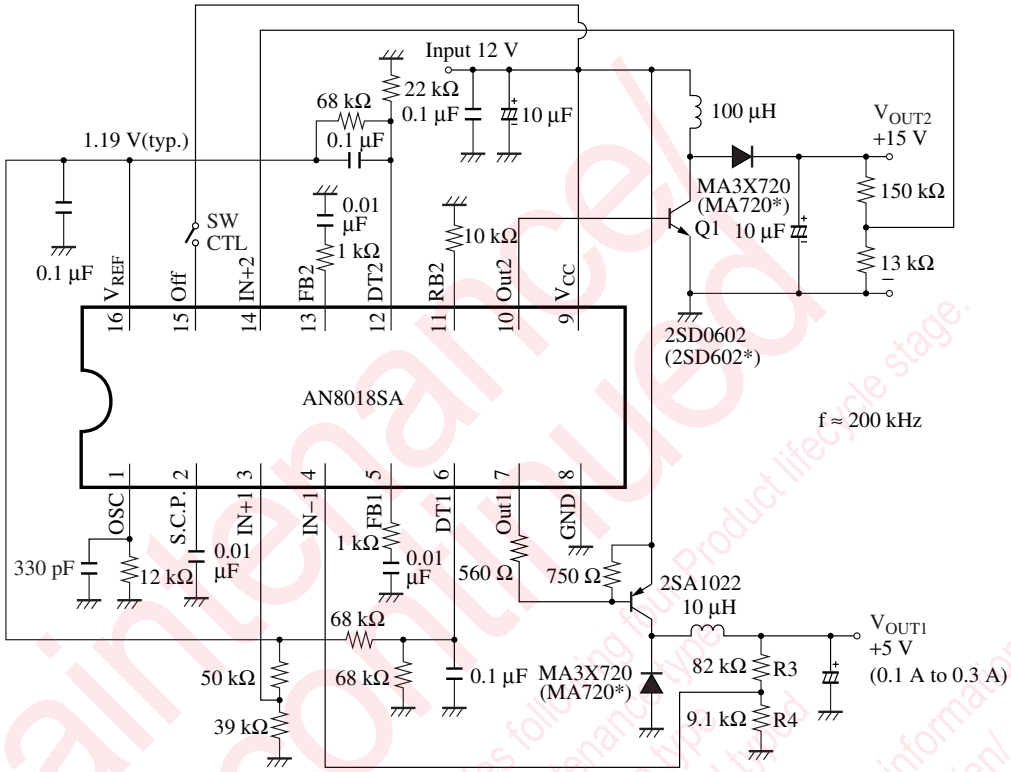
Note) ∗: Former part number

• Application circuit example 2 (Input 2.5 V to 6.5 V, output 5 V/12 V)



■ Application Circuit Examples (continued)

• Application circuit example 3 (Input 12 V, Output 5 V/15 V)



Note) *: Former part number