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# AN983B/BX

## PCI/Mini PCI-to-Ethernet LAN; PQFP - 128Pin

Communications

Never stop thinking.

**Edition 2005-12-15**

**Published by Infineon Technologies AG,**
**St.-Martin-Strasse 53,**
**81669 München, Germany**



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**Revision History: 2005-12-15, Rev. 1.81**

**Previous Version:**

| Page/Date | Subjects (major changes since last revision) |
|---|---|
| 2000-10 | Rev.0.1: Draft data sheet for review |
| 2001-02 | Rev.1.0: First release |
| 2001-03 | Rev.1.1: Add CSR15.bit28 MRXCK, Add CSR18.bit26 PMEP, Add CSR18.bit27 PMEPEN |
| 2001-09 | Rev.1.2: Add 25MHz crystal accuracy, Revise PHY registers |
| 2001-09 | Rev.1.3: Revise product logo of Pin assignment diagram |
| Page17,14/ 2001-09 | Rev.1.4:<br>1.MrxD0~D3P.23 CIOSA: 1 means enable; 0 means disable<br>2.P.14 Add LED info to pin diagram |
| Page25,40/ 2002-07 | Rev.1.5:<br>1.Offset 80h, DID default value; 0981h<br>2.CSR18[25]/PWRS_clr; 1 means PCI_reset rising will clear CR49[1:0]/PWRS |
| Page85/ 2002-07 | Rev.1.6: FIG21, FIG22, FIG23, FIG24 added for MII interface signal timing |
| Page45/ 2002-09 | Rev.1.7(B): Unicast registers added, BGA package |
| Page69/ 2003-05 | Rev.1.8(B): Modify some error statement about Loop-back Operation of transceiver |
| 2005-09-13 | Rev.1.81: when changed to the new Infineon format |
| 2005-11-30 | Minor change. Included Green package information |

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# 1 General Description

The AN983B/BX is a high performance PCI Fast Ethernet controller with a integrated physical layer interface for 10BASE-T and 100BASE-TX applications. The AN983BX is the environmentally friendly “green” package version.

The AN983B/BX was designed with advanced CMOS technology to provide a glueless 32-bit bus master interface for PCI, boot ROM interface, and CSMA/CD protocol for Fast Ethernet, as well as the physical media interface for 100BASE-TX of IEEE802.3u and 10BASE-T of IEEE802.3. The auto-negotiation function is also supported for speed and duplex detections.

The AN983B/BX can be programmed as MAC-only controller. In this mode, it provides the standard MII interface to link to an external PHY. With this mode, it can be connected to the HomePNA PHY to support the HomePNA networking solution or Homeplug PHY (Power-line solution) to support Homeplug networking solution.

The AN983B/BX provides both half-duplex and full-duplex operations, as well as supports for full-duplex flow control.

It provides long FIFO buffers for transmission and reception, and an early interrupt mechanism to enhance performance.

The AN983B/BX also supports ACPI and PCI compliant power management functions and Magic Packet wake-up event.

# 2 System Block Diagram

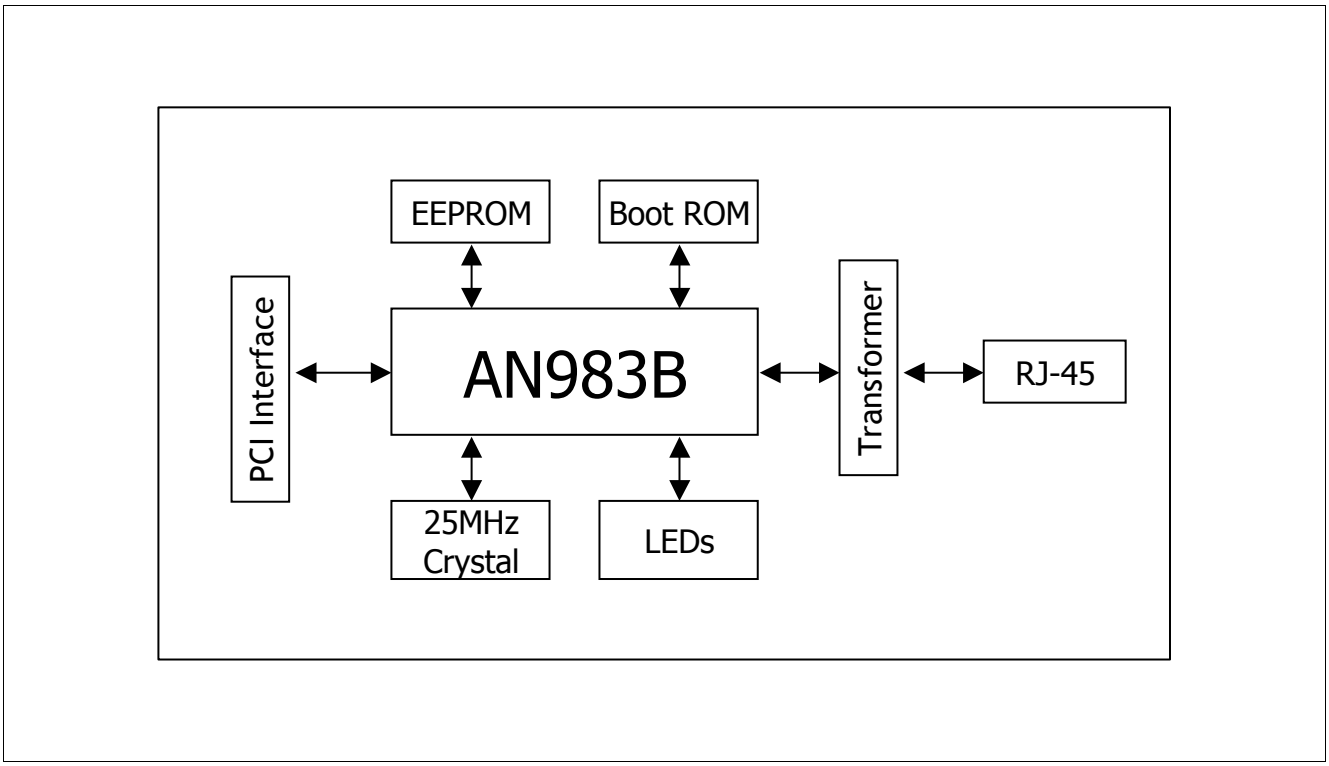


**Figure 1 System Diagram of the AN983B/BX**

# 3 Features

**Industry standard**

- IEEE802.3u 100BASE-TX and IEEE802.3 10BASE-T compliant

- Supports for IEEE802.3x flow control
- IEEE802.3u Auto-Negotiation support for 10BASE-T and 100BASE-TX
- PCI Specification 2.2 compliant
- ACPI and PCI power management Ver.1.1 compliant
- Supports PC99 wake on LAN

**FIFO**

- Provides two independent long FIFOs with 2k bytes each for transmission and receiving
- Pre-fetch up to two transmit packets to minimize inter frame gap (IFG) to 0.96 μs
- Retransmit collided packet without reload from host memory within 64 bytes
- Automatically retransmit FIFO under-run packet with maximum drain threshold until 3 times retry failure and that will not influence the registers and transmit threshold of next packet

**PCI I/F**

- Provides 32-bit PCI bus master data transfer
- Supports PCI clock with frequency from 0 Hz to 33 MHz
- Supports network operation with PCI system clock from 20 MHz to 33 MHz
- Provides performance meter, PCI bus master latency timer, for tuning the threshold to enhance the performance
- Provides burst transmit packet interrupt and transmit/receive early interrupt to reduce host CPU utilization
- Supports memory-read, memory-read-line, memory-read-multiple, memory-write, memory-write-and-invalidate command while being bus master
- Supports big or little endian byte ordering

**EEPROM/Boot ROM I/F**

- Provides write-able Flash ROM and EPROM as boot ROM with size up to 128 KB
- Provides PCI to access boot ROM by byte, word, or double word
- Re-write Flash boot ROM through I/O port by programming register
- Provides serial interface for read/write 93C46/66 EEPROM
- Automatically load device ID, vendor ID, subsystem ID, subsystem vendor ID, Maximum-Latency, and Minimum-Grand from the 64 byte contents of 93C46/66 after PCI reset de-asserted in PCI environment.

**MAC/Physical**

- Integrates the whole Physical layer functions of 100BASE-TX and 10BASE-T
- Provides Full -duplex operation on both 100 Mbit/s and 10 Mbit/s modes
- Provides Auto-negotiation (NWAY) function of full/half duplex operation for both 10 and 100 Mbit/s
- Provides transmit wave-shaper, receives filters, and adaptive equalizer
- Provides MLT-3 transceiver with DC restoration for Base-line wander compensation
- Provides MAC and Transceiver (TXCVR) loop-back modes for diagnostic
- Built in Stream Cipher Scrambler/ De-scrambler and 4B/5B encoder/decoder
- Supports external transmit transformer with turn ratio 1:1
- Supports external receive transformer with turn ratio 1:1

**LED Display**

- 3 LED displays scheme provided:
  - 100 Mbit/s (on) or Speed 10 (off)
  - Link (keeps on when link ok) or Activity (will be blinking with 10 Hz when receiving or transmitting but not collision)
  - FD (keeps on when in Full duplex mode) or Collision (will be blinking with 20 Hz when colliding)
- 4 LED displays scheme provided:
  - 100 Mbit/s and Link (keep on when link and 100 Mbit/s)
  - 10 Mbit/s and Link (keep on when link and 10 Mbit/s)
  - Activity (will be blinking with 10 Hz when receiving or transmitting but not collision)
  - FD (keeps on when in Full duplex mode) or Collision (will be blinking with 20 Hz when colliding)

**Miscellaneous**

- Provides 128-pin QFP/LQFP packages for PCI/mini-PCI interfaces
- 3.3 V power supply with 5 V/3.3 V I/O tolerance

# 4 Block Diagram

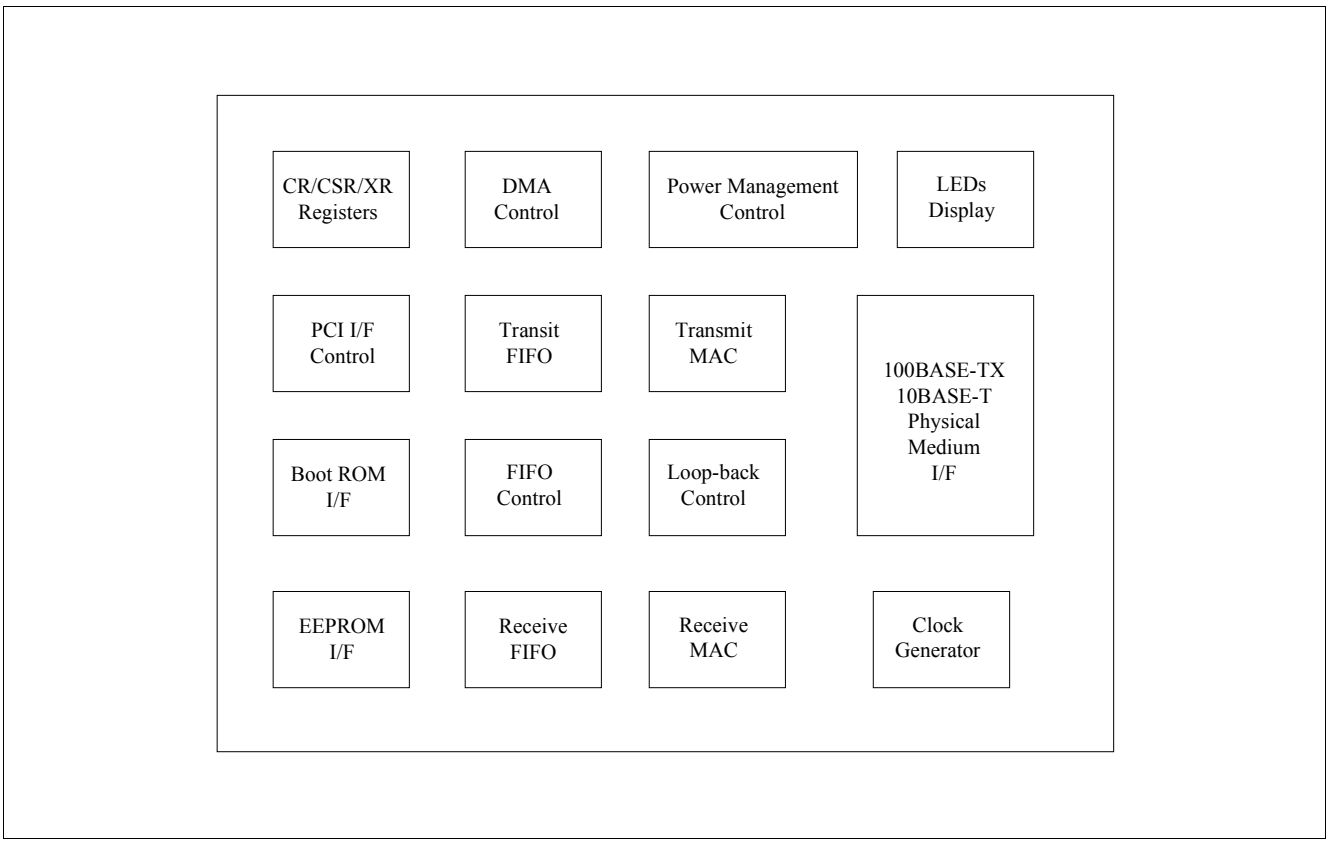


**Figure 2 Block Diagram of the AN983B/BX**

# 5 Pin Assignment Diagram

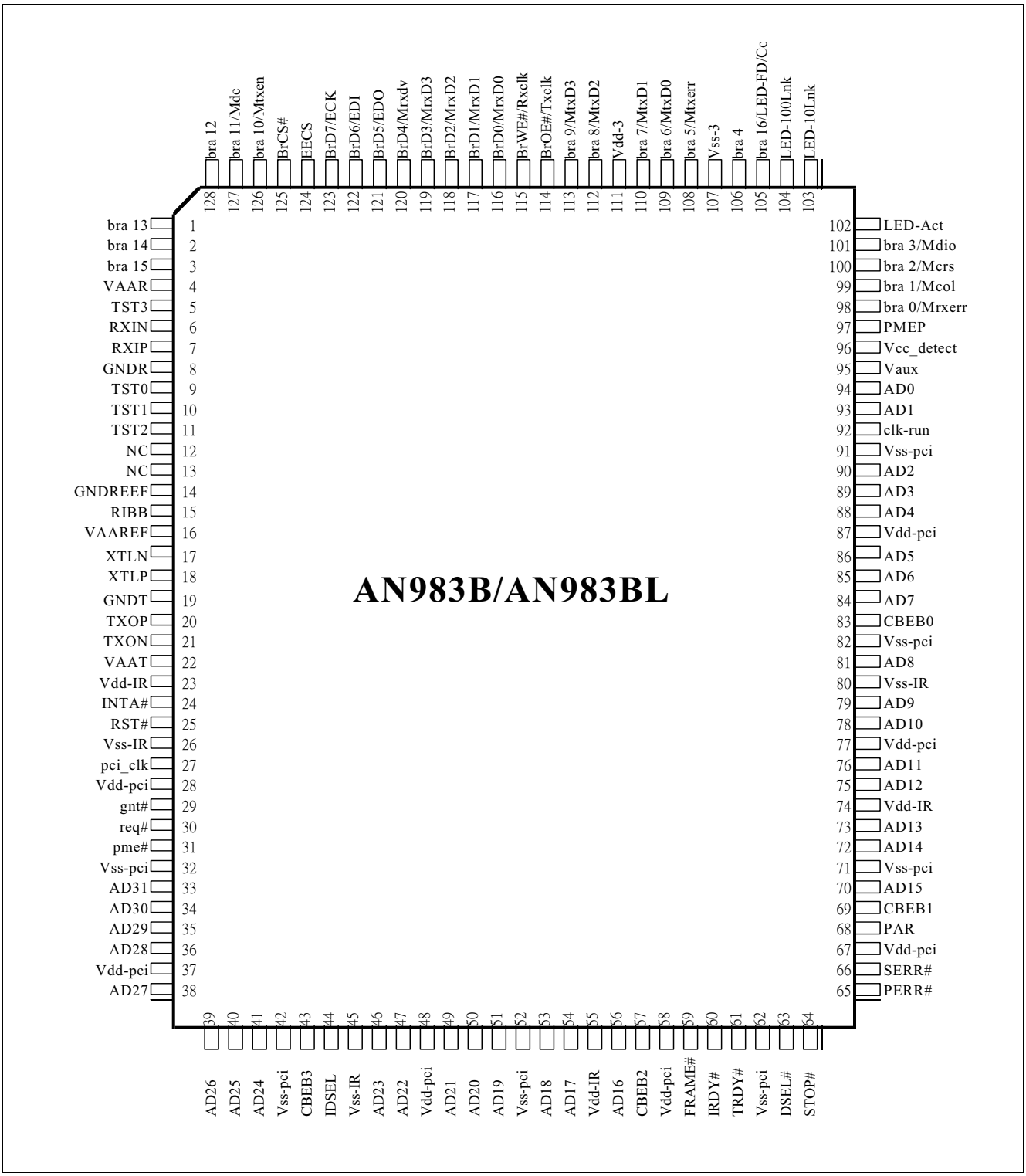


**Figure 3 Pin Assignment (top view)**

## 5.1 Pin Type and Buffer Type Abbreviations

Standardized abbreviations:

**Table 1 Abbreviations for Pin Type**

| Abbreviations | Description |
|---|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| AO | Output. Analog levels. |
| AI/O | Input or Output. Analog levels. |
| PWR | Power |
| GND | Ground |
| MCL | Must be connected to Low (JEDEC Standard) |
| MCH | Must be connected to High (JEDEC Standard) |
| NU | Not Usable (JEDEC Standard) |
| NC | Not Connected (JEDEC Standard) |

**Table 2 Abbreviations for Buffer Type**

| Abbreviations | Description |
|---|---|
| Z | High impedance |
| PU1 | Pull up, 10 kΩ |
| PD1 | Pull down, 10 kΩ |
| PD2 | Pull down, 20 kΩ |
| TS | Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance. |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource. |
| OC | Open Collector |
| PP | Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute). |
| OD/PP | Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute. |
| ST | Schmitt-Trigger characteristics |
| TTL | TTL characteristics |

# 6 Pin Description

**Table 3 Pin Definitions and Functions**

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **PCI Interface** | | | | |
| 24 | INTA# | O/D | | **PCI Interrupt Request**<br>AN983B/BX asserts this signal when one of the interrupt events occurs. |
| 25 | RST# | I | | **PCI Signal to Initialize the AN983B/BX**<br>The active reset signal should be sustained at least 100μs to guarantee that the AN983B/BX has completed the initializing activity. During the reset period, all the output pins of AN983B/BX will be set to tristate and all the O/D pins are floated. |
| 27 | PCI-CLK | I | | **This PCI Clock Inputs to AN983B/BX for PCI Relative Circuits as the Synchronized Timing Base with PCI Bus**<br>The Bus signals are recognized on rising edge of PCI-CLK. In order to let network operating properly, the frequency range of PCI-CLK is limited between 20 MHz and 33 MHz when network operating. |
| 29 | GNT# | I | | **PCI Bus Granted**<br>This signal indicates that the PCI bus request of AN983B/BX has been accepted. |
| 30 | REQ# | O | | **PCI Bus Request**<br>Bus master device want to get bus access right |
| 31 | PME# | I/O | | **Power Management Event**<br>The Power Management Event signal is an open drain, active low signal. When WOL-bit 18 of CSR 18 be set into “1”, means that the AN983B/BX is set into Wake On LAN mode. In this mode, when the AN983B/BX receives a Magic Packet frame from network then the AN983B/BX will active this signal too.In the Wake On LAN mode, when LWS-bit (bit 17) of CSR18 is set into “1” means the LAN-WAKE signal is HP-style signal, otherwise it is IBM-style signal. |

**Table 3 Pin Definitions and Functions** (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 33, 34 | AD-31, 30 | I/O | | **Multiplexed Address Data Pin of PCI Bus** |
| 35, 36 | AD-29, 28 | | | |
| 38, 39 | AD-27, 26 | | | |
| 40, 41 | AD-25, 24 | | | |
| 46, 47 | AD-23, 22 | | | |
| 49, 50 | AD-21, 20 | | | |
| 51, 53 | AD-19, 18 | | | |
| 54, 56 | AD-17, 16 | | | |
| 70, 72 | AD-15, 14 | | | |
| 73, 75 | AD-13, 12 | | | |
| 76, 78 | AD-11, 10 | | | |
| 79, 81 | AD-9, 8 | | | |
| 84, 85 | AD-7, 6 | | | |
| 86, 88 | AD-5, 4 | | | |
| 89, 90 | AD-3, 2 | | | |
| 93, 94 | AD-1, 0 | | | |
| 43 | C-BEB3 | I/O | | **Bus Command and Byte Enable** |
| 57 | C-BEB2 | | | |
| 69 | C-BEB1 | | | |
| 83 | C-BEB0 | | | |
| 44 | IDSEL | I | | **Initialization Device Select**<br>This signal is asserted when host issues the configuration cycles to the AN983B/BX. |
| 59 | FRAME# | I/O | | **Begin and Duration of Bus Access**<br>Driven by master device |
| 60 | IRDY# | I/O | | **Master Device is Ready to Data Transaction** |
| 61 | TRDY# | I/O | | **Slave Device is Ready to Data Transaction** |
| 63 | DEVSEL# | I/O | | **Device Select**<br>Device select, target is driving to indicate the address is decoded |
| 64 | STOP# | I/O | | **Stop the Current Transaction**<br>Target device request the master device to stop the current transaction |
| 65 | PERR# | I/O | | **Data Parity Error**<br>Data parity error is detected, driven by the agent receiving data |
| 66 | SERR# | O/D | | **Address Parity Error** |
| 68 | PAR | I/O | | **Parity**<br>Parity, even parity (AD [31:0] + C/BE [3:0]), master drives par for address and write data phase, target drives par for read data phase |

**Table 3 Pin Definitions and Functions** (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 92 | Clk-run | I/O | OD | **Clock Run for PCI System**<br>In the normal operation situation, Host should assert this signal to indicate AN983B/BX about the normal situation. On the other hand, when Host will deassert this signal when the clock is going down to a non-operating frequency. When AN983B/BX recognizes the deasserted status of clk-run, then it will assert clk-run to request host to maintain the normal clock operation. When clk-run function is disabled then the AN983B/BX will set clk-run in tristate. |
| **BOOTROM/EEPROM Interface** | | | | |
| 98 | BrA0 | I/O | | **ROM Data Bus**<br>Provides up to 128KB EPROM or Flash-ROM application space. |
| 99 | BrA1 | | | |
| 100 | BrA2 | | | |
| 101 | BrA3 | | | |
| 106 | BrA4 | | | |
| 108 | BrA5 | | | |
| 109 | BrA6 | | | |
| 110 | BrA7 | | | |
| 112 | BrA8 | | | |
| 113 | BrA9 | | | |
| 126 | BrA10 | | | |
| 127 | BrA11 | | | |
| 128 | BrA12 | | | |
| 1 | BrA13 | | | |
| 2 | BrA14 | | | |
| 3 | BrA15 | | | |
| 105 | BrA16 | | | |
| 116 | BrD0 | IO | | **BootROM Data Bus Bit (0~7)**<br><br>Input/Output data for AN983B/BX<br>EDO: Data Output of serial EEPROM<br>EDI: Data Input of serial EEPROM<br>ECK: Clock input of serial EEPROM<br>The AN983B/BX output clock signal to EEPROM. |
| 117 | BrD1 | | | |
| 118 | BrD2 | | | |
| 119 | BrD3 | | | |
| 120 | BrD4 | | | |
| 121 | BrD5/EDO | IO/O | | |
| 123 | BrD6/EDI<br>BrD7/ECK | IO/I<br>IO/I | | |
| 124 | EECS | O | | **Chip Select of Serial EEPROM** |
| 125 | BrCS# | O | | **BootROM Chip Select** |
| 114 | BrOE# | O | | **BootROM Read Enable for Flash ROM Application** |
| 115 | BrWE# | O | | **BootROM Write Enable for Flash ROM Application** |
| **MII Interface (Program AN983B/BX as MAC-Only Mode,Set FCH [2:0] =100B)** | | | | |
| 127 | Mdc | O | | **MII Management Data Clock** |

**Table 3 Pin Definitions and Functions** (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 128 | Mtxen | O | | **MII Transmit Enable** |
| 109 | MtxD0 | O | | **MII Transmit Data** |
| 110 | MtxD1 | | | |
| 112 | MtxD2 | | | |
| 113 | MtxD3 | | | |
| 108 | Mtxerr | O | | **MII Transmit Error** |
| 101 | Mdio | I/O | | **MII Management Data I/O** |
| 120 | Mrxdv | I | | **MII Receive Data Valid** |
| 100 | Mcrs | I | | **MII Carrier Sense** |
| 116 | MrxD0 | I | | **MII Receive Data** |
| 117 | MrxD1 | | | |
| 118 | MrxD2 | | | |
| 119 | MrxD3 | | | |
| 99 | Mcol | I | | **MII Collision** |
| 98 | Mrxerr | I | | **MII Receive Error** |
| 115 | Rxclk | I | | **MII Receive Clock** |
| 114 | Txclk | I | | **MII Transmit Clock** |
| **Physical Interface** | | | | |
| 18 | XTLP | I | | **Crystal Inputs** To be connected to a 25 MHz crystal with 50 ppm accuracy. |
| 17 | XTLN | | | |
| 6 | RXIN | I | | **Differentials Receive Inputs** The differentials receive inputs of 100BASE-TX or 10BASE-T, these pins directly input from Magnetic. |
| 7 | RXIP | | | |
| 20 | TXOP | O | | **Differential Transmit Outputs** The differential Transmit outputs of 100BASE-TX or 10BASE-T, these pins directly output to Magnetic. |
| 21 | TXON | | | |
| 15 | RIBB | I | | **Reference Bias Resistor** To be tied to an external 10.0K (1%) resistor which should be connected to the analog ground at the other end. |
| 9 | TST0 | I | | **Test Pin** |
| 10 | TST1 | | | |
| 11 | TST2 | | | |
| 5 | TST3 | | | |
| 12, 13 | NC | O | | |
| **LED Display and Miscellaneous** | | | | |

**Table 3 Pin Definitions and Functions** (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 102 | Led-Act | O | | **4 LED Mode: LED Display for Activity Status**<br>This pin will be driven on with 10 Hz blinking frequency when either effective receiving or transmitting is detected. |
| | (Led-lnk/act) | O | | **(3 LED Mode): LED Display for Link and Activity Status**<br>This pin will be driven on continually when a good Link test is detected. This pin will be driven on with 10 Hz blinking frequency when either effective receiving or transmitting is detected. |
| 103 | Led-10Lnk | O | | **4 LED Mode: LED Display for 10 Mbit/s Speed**<br>This pin will be driven on continually when the 10 Mbit/s network operating speed is detected. |
| | (Led-fd/col) | O | | **(3 LED Mode): LED Display for Full Duplex or Collision Status**<br>This pin will be driven on continually when a full duplex configuration is detected. This pin will be driven on with 20 Hz blinking frequency when a collision status is detected in the half duplex configuration. |
| 104 | Led-100Lnk | O | | **4 LED Mode: LED Display for 100 Mbit/s Speed**<br>This pin will be driven on continually when the 100 Mbit/s network operating speed is detected. |
| | (Led-speed) | O | | **(3 LED Mode): LED Display for 100 Mbit/s or 10 Mbit/s speed**<br>This pin will be driven on continually when the 100M b/s network operating speed is detected. |
| 105 | Led-Fd/Col | O | | **4 LED Mode: LED Display for Full Duplex or Collision Status**<br>This pin will be driven on continually when a full duplex configuration is detected. This pin will be driven on with 20 Hz blinking frequency when a collision status is detected in the half duplex configuration.<br>(3 LED Mode): none |
| 95 | Vaux | I | | When this pin is asserted, it indicates an auxiliary power source is supported. ACPI purpose, for detecting the auxiliary power source. This pin should be or-wired connected to:<br>1) 3.3 V when 3.3 Vaux support, or<br>2) 5 V when 5 Vaux support from 3-way switch. |
| 96 | Vcc-detect | I | | When this pin is asserted, it indicates PCI power source is supported. ACPI purpose, for detecting the main power is remained or not. This pin should be connected to PCI bus power source +5 V. |

**Table 3 Pin Definitions and Functions** (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 97 | PMEP | O | | This signal is used as the WOL pin. It provides a programmable positive or negative pulse with approximately 50 ms width. |
| **Digital Power Pins** | | | | |
| 26, 32, 42, 45, 52, 62, 71, 80, 82, 91, 107 | $V_{ss\text{-}pci}$, $V_{ss\text{-}IR}$, $V_{ss\text{-}3}$ | | | |
| 23, 28, 37, 48, 55, 58, 67, 74, 77, 87, 111 | $V_{dd\text{-}pci}$, $V_{dd\text{-}IR}$, $V_{dd\text{-}3}$ | | | **Connect to 3.3 V** |
| **Analog Power Pins** | | | | |
| 4, 16, 22 | $V_{AAR}$, $V_{AAREF}$, $V_{AAT}$, 3.3 V | | | |
| 8, 14, 19 | GNDR, GNDREF, GNDT | | | |

# 7 Functional Descriptions

## 7.1 Initialization Flow

The flow of initialize AN983B/BX is shown as below.

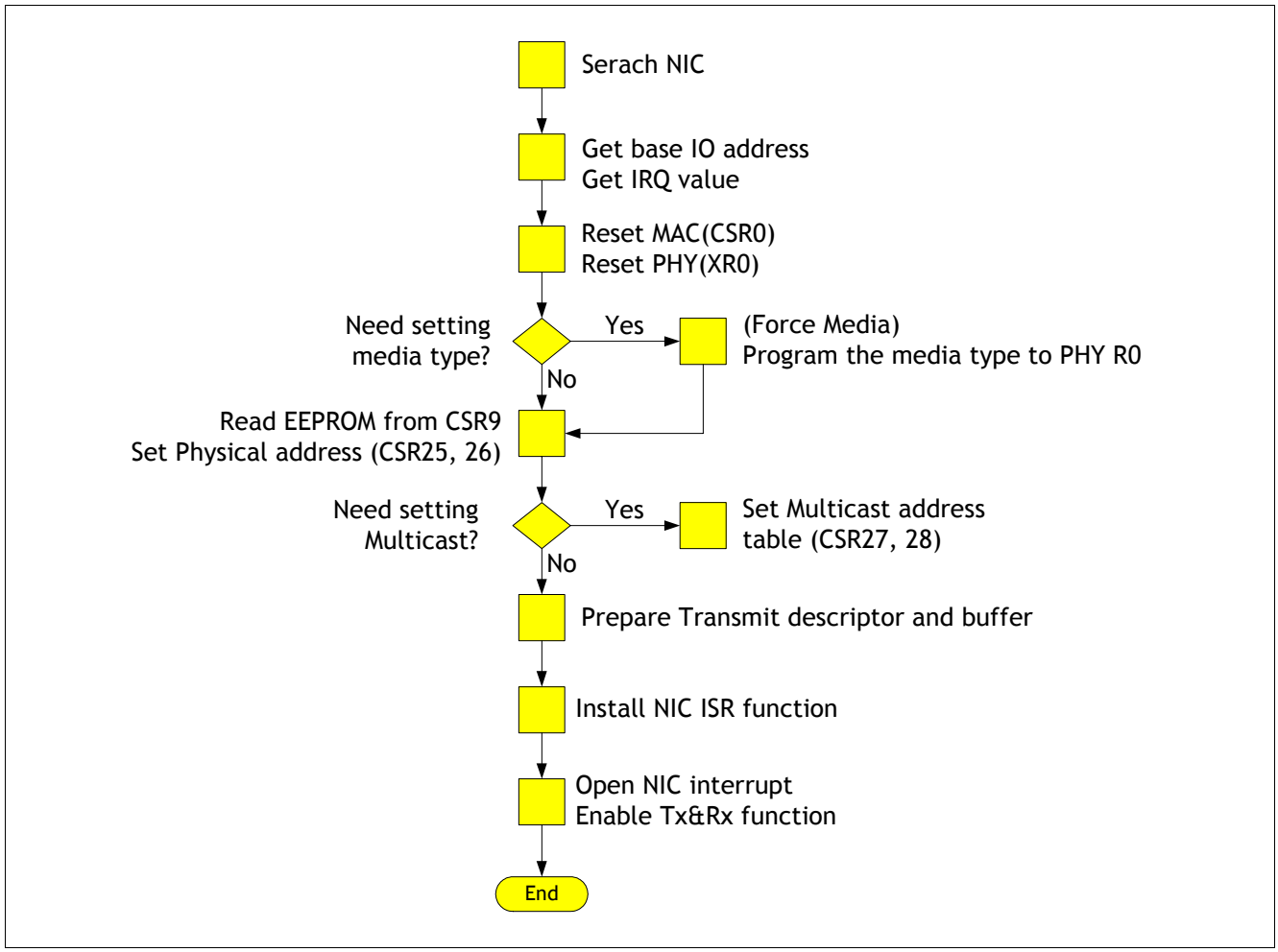


**Figure 4 Initialization Flow**

## 7.2 Network Packet Buffer Management

### 7.2.1 Descriptor Structure Types

For networking operations the AN983B/BX transmits the data packet from transmit buffers in host memory to AN983B/BX's transmit FIFO and receives the data packet from AN983B/BX's receiving FIFO to receive buffers in host memory. The descriptors that the AN983B/BX supports to build in host memory are used as the pointers of these transmit and receive buffers.

There are two structure types for the descriptor, **Ring and Chain**, supported by the AN983B/BX and are shown as below. The type selection is controlled by the bit24 of RDES1 and the bit24 of TDES1.

The transmitting and receiving buffers are physically built in host memory. Any buffer can contain either a whole packet or just parts of a packet. But it can't contain more than one packet.

- Ring structure

There are two buffers per descriptor in the ring structure. Support receives early interrupt.

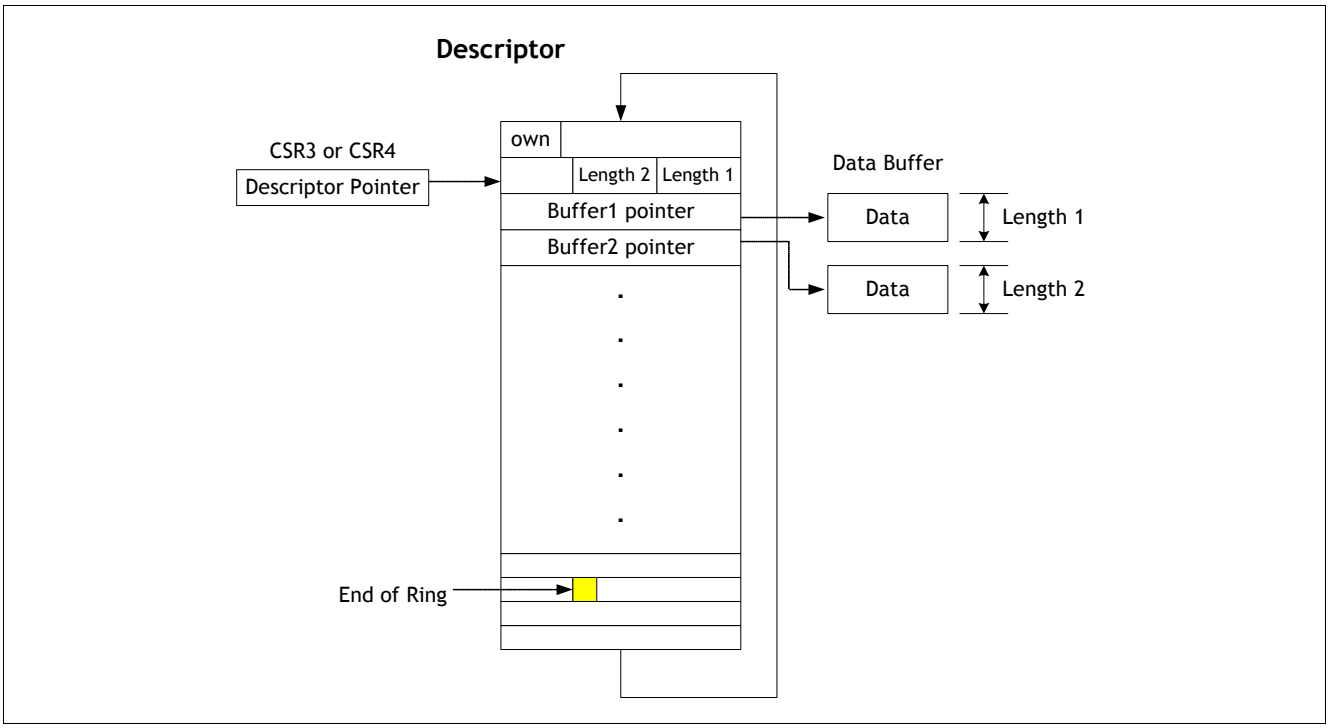


**Figure 5 Ring Structure of Frame Buffer**

- Chain structure

There is only one buffer per descriptor in chain structure.

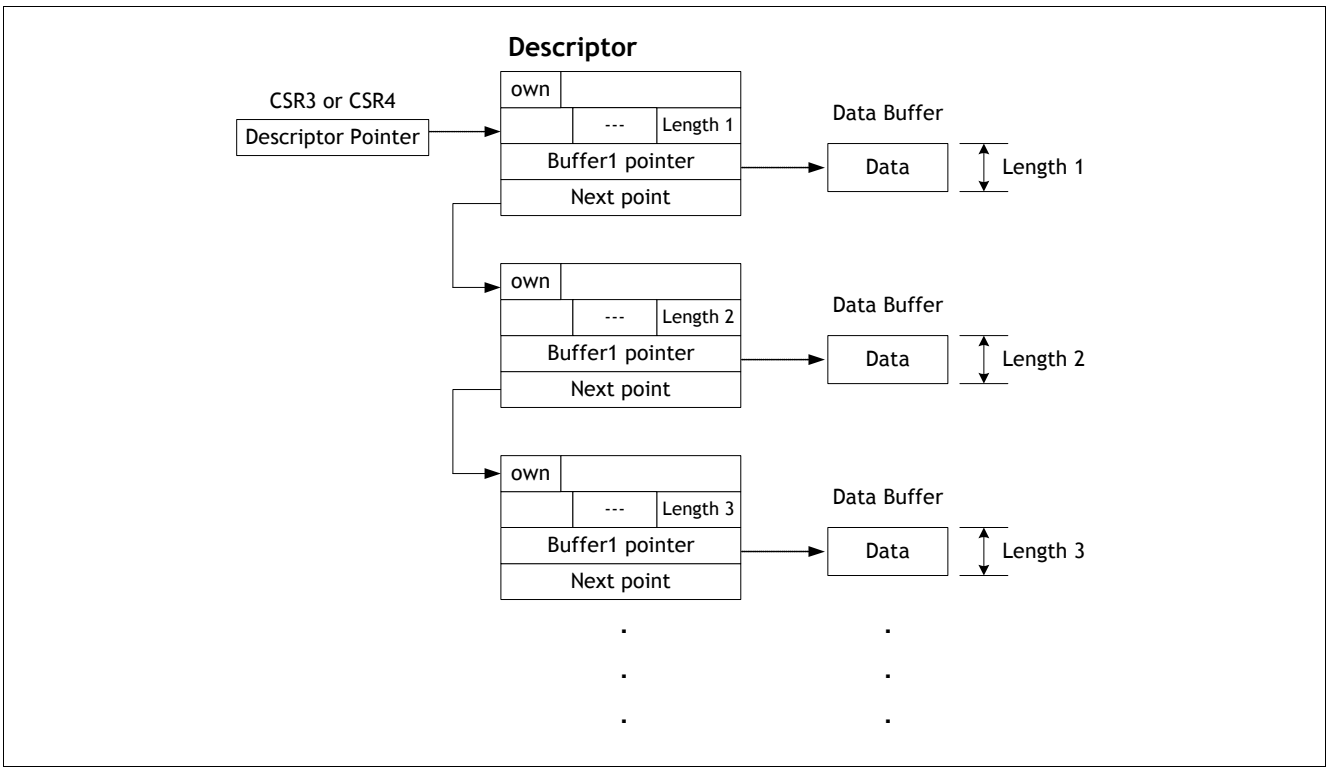


**Figure 6 Chain Structure of Frame Buffer**

### 7.2.2 The Point of Descriptor Management

OWN bit = 1, ready for network side access

OWN bit = 0, ready for host side access

- Transmit Descriptor Pointers

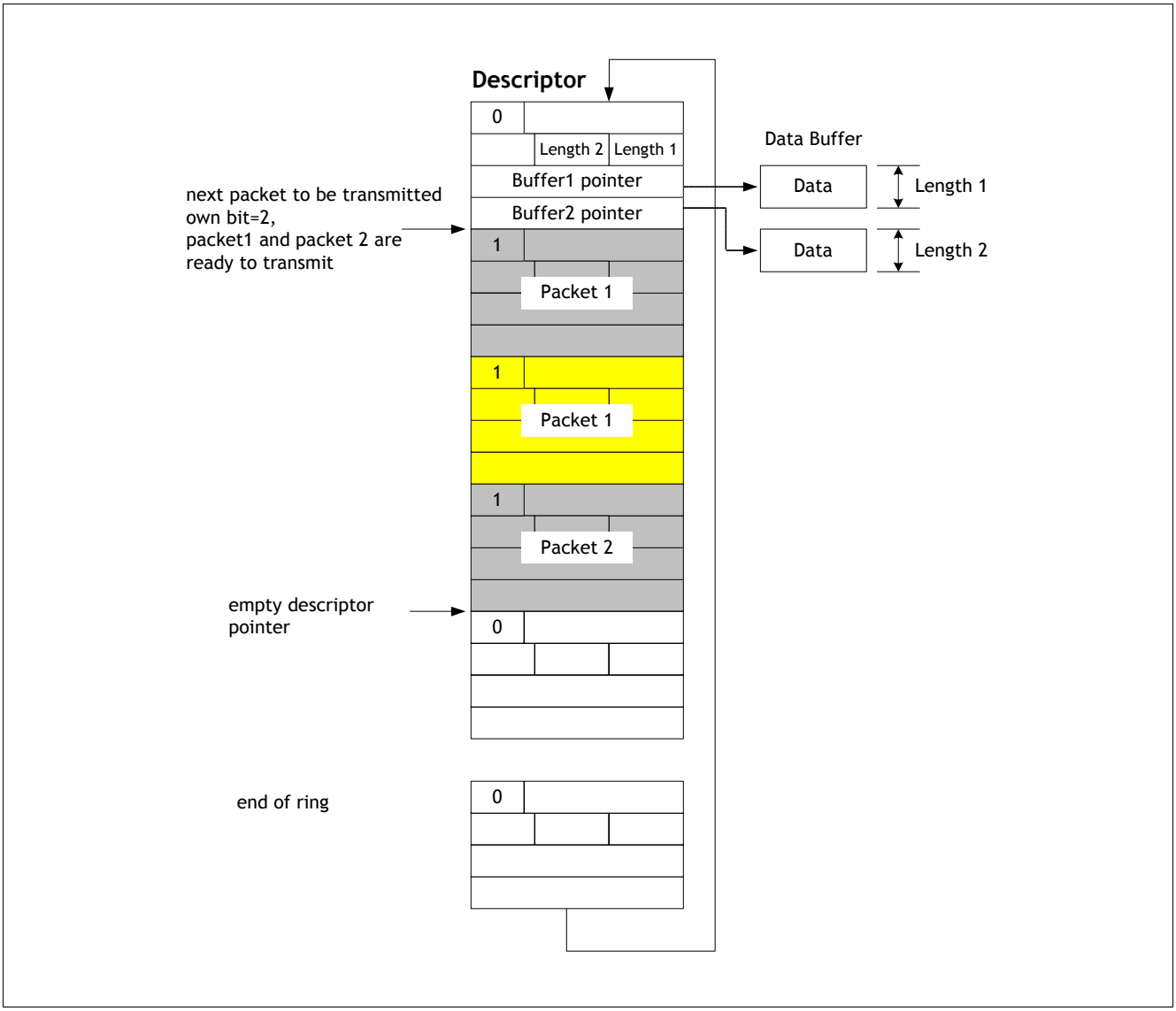


**Figure 7 Transmit Pointers for Descriptor Management**

- Receive Descriptor Pointers

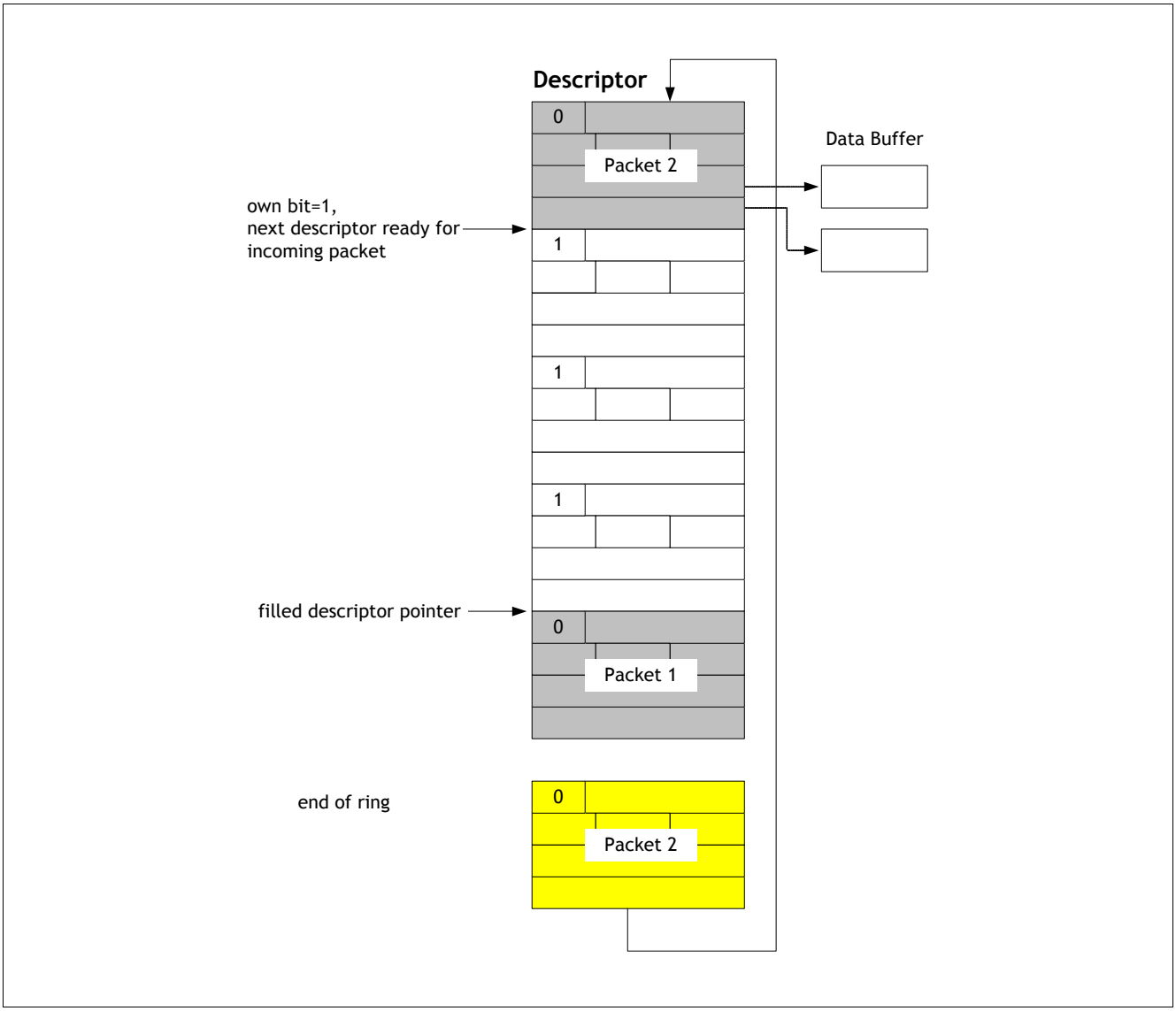


**Figure 8 Receive Pointers for Descriptor Management**

## 7.3 Transmit Scheme and Transmit Early Interrupt

### 7.3.1 Transmit Flow

The flow of packet transmit is shown as below.

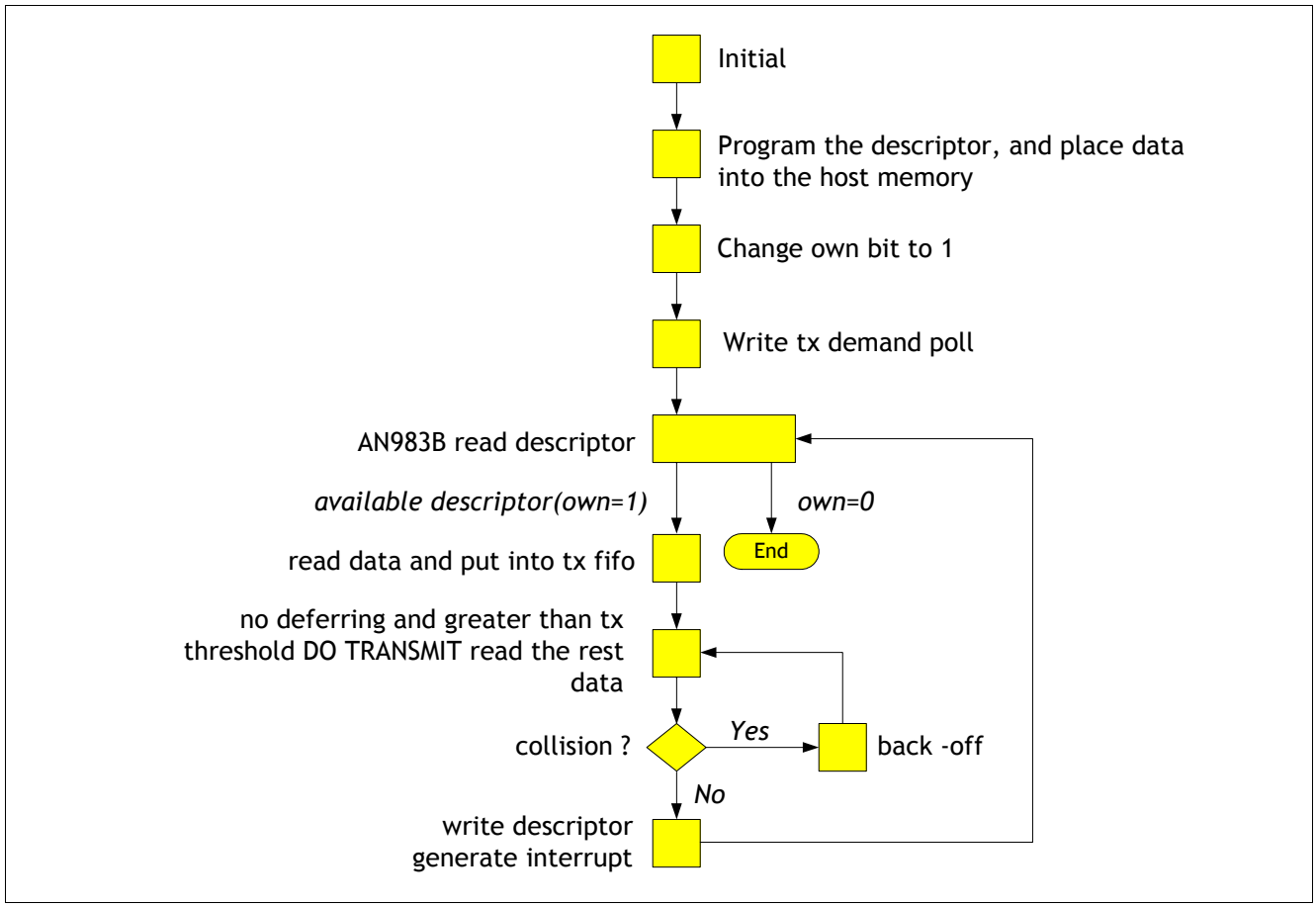


**Figure 9 Transmit Flow**

### 7.3.2 Transmit Pre-fetch Data Flow

- Transmit FIFO size = 2K-byte
- Two packets in the FIFO at the same time
- Meet the transmit min. back-to-back

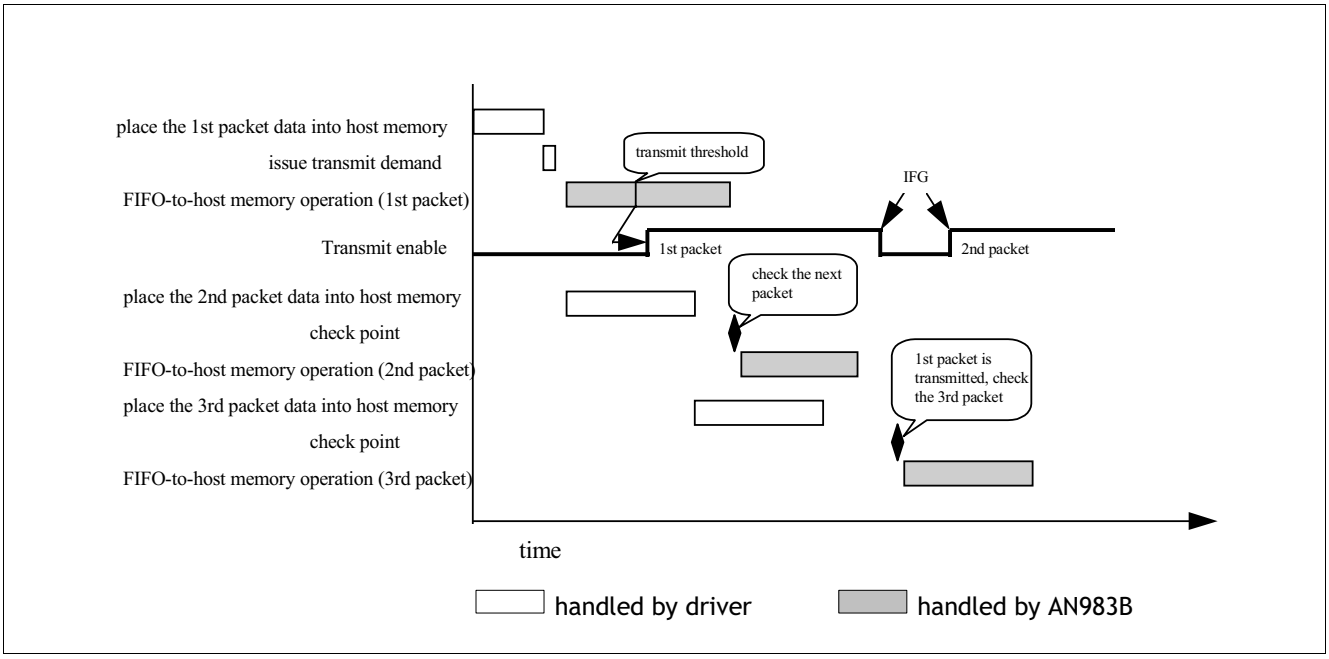


**Figure 10 Transmit Data Flow of Pre-fetch Data**

### 7.3.3 Transmit Early interrupt Scheme

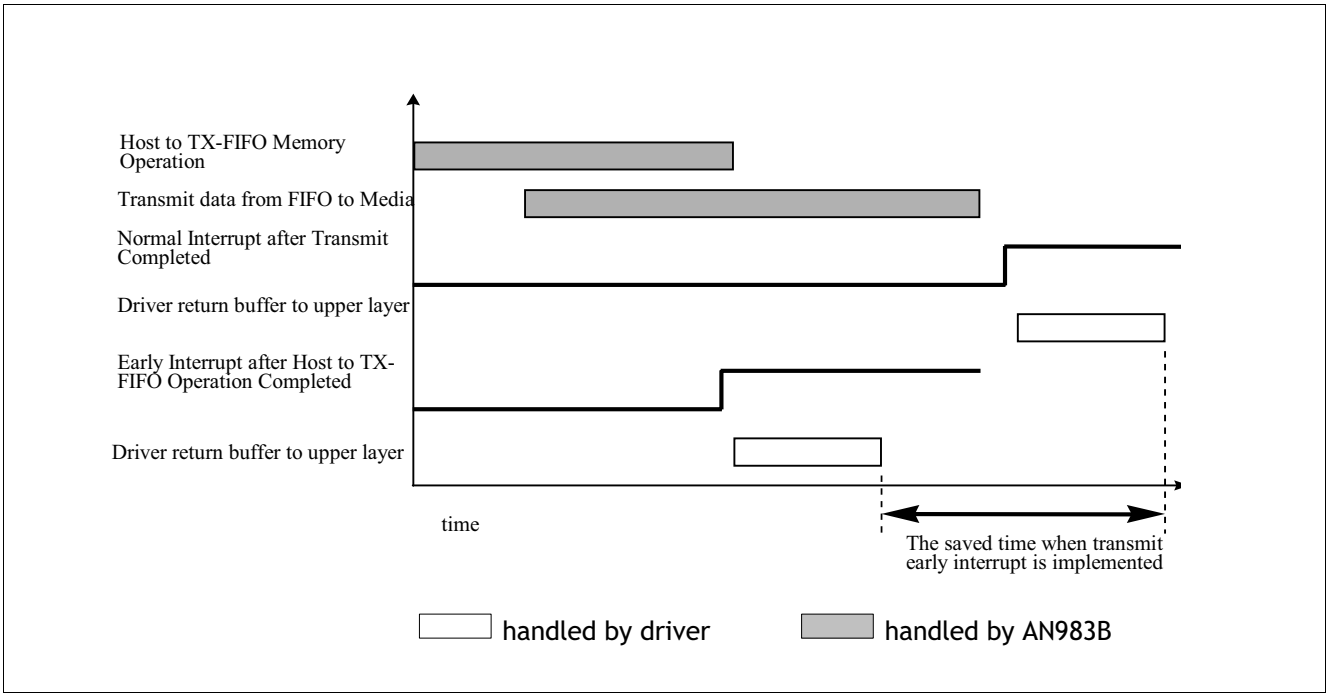


**Figure 11 Transmit Normal Interrupt and Early Interrupt Comparison**

## 7.4 Receive Scheme and Receive Early Interrupt Scheme

The following figure shows the difference of timing without early interrupt and with early interrupt.

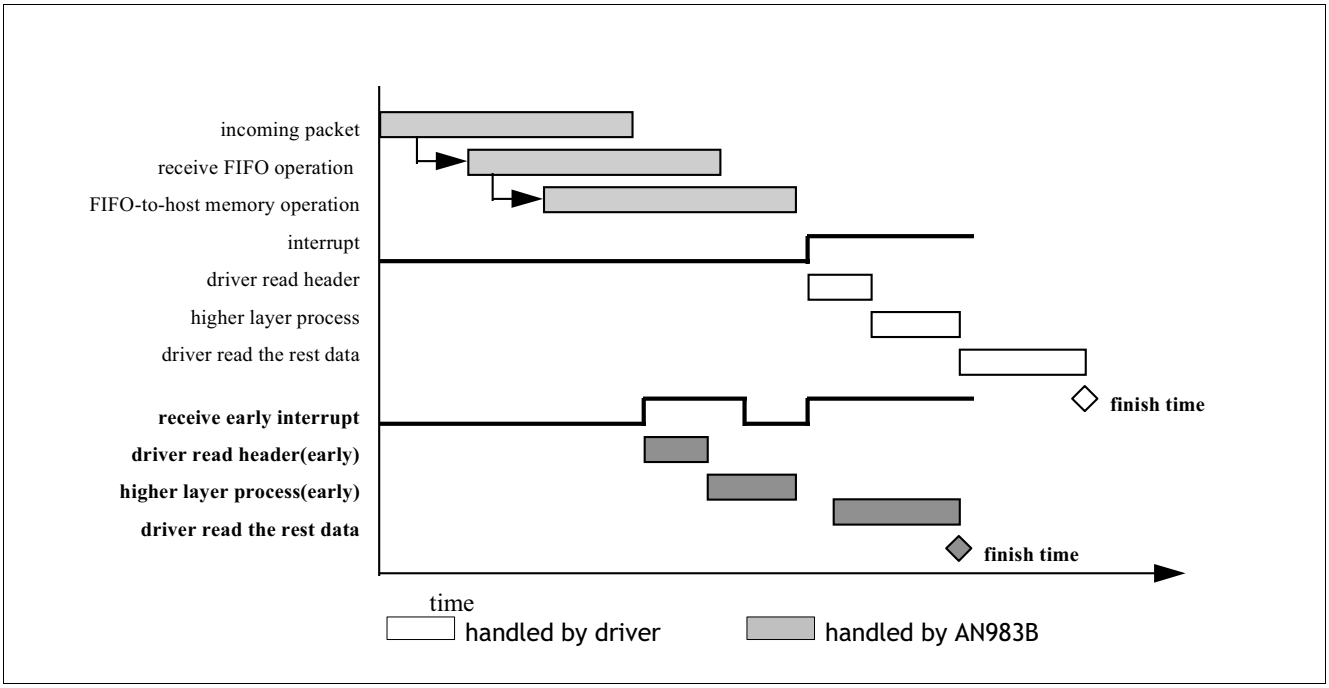


**Figure 12 Receive Data Flow (without early interrupt and with early interrupt)**

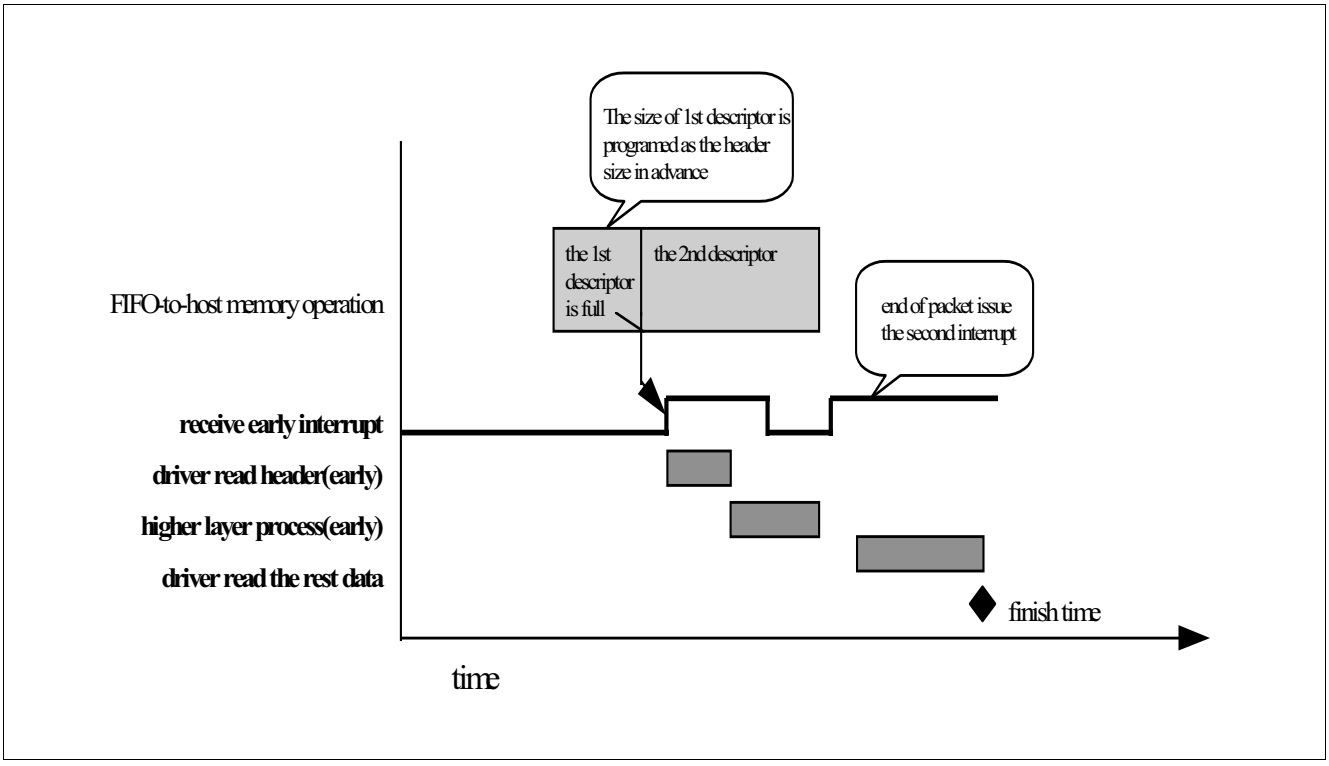


**Figure 13 Detailed Receive Early Interrupt Flow**

## 7.5 Network Operation