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Data Sheet, Rev. 1.51, Nov. 2005

# AN985B/BX

## CardBus-to-Ethernet LAN Controller

Communications

Never stop thinking.

**Edition 2005-11-30**

**Published by Infineon Technologies AG,**
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**81669 München, Germany**



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| Page/Date | Subjects (major changes since last revision) |
|---|---|
| 2005-09-13 | Rev. 1.51: when changed to the new Infineon format |
| 2005-11-30 | Minor change. Included Green package information |
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**Trademarks**

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# 1 General Description

The AN985B/BX is a high performance CARDBUS Fast Ethernet controller with a integrated physical layer interface for 10BASE-T and 100BASE-TX applications. The AN983B/BX is the environmentally friendly “green” package version.

The AN985B/BX was designed with 0.25um CMOS technology to provide glueless 32-bit bus master interface for CARDBUS, boot ROM interface and CSMA/CD protocol for Fast Ethernet, as well as the physical media interface for 100BASE-TX of IEEE802.3u and 10BASE-T of IEEE802.3. The auto-negotiation function is also supported for speed and duplex detections.

The AN985B/BX provides both half-duplex and full-duplex operations, as well as support for full-duplex flow control.

It provides long FIFO buffers for transmission and reception, and an early interrupt mechanism to enhance performance.

The AN985B/BX also supports ACPI and CARDBUS compliant power management functions and Magic Packet wake-up event.

# 2 System Block Diagram

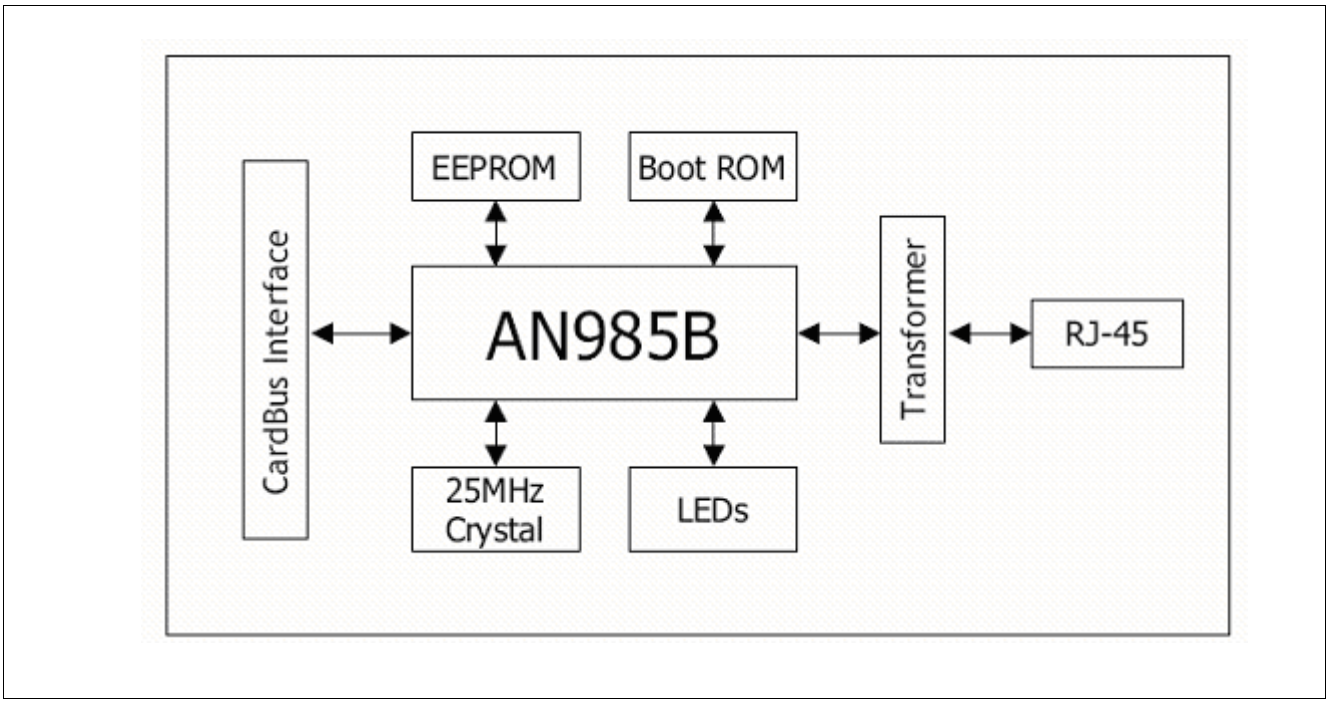


**Figure 1 System Diagram of the AN985B/BX**

# 3 Features

**Industry standard**

- IEEE802.3u 100BASE-TX and IEEE802.3 10BASE-T compliant
- Supports for IEEE802.3x flow control
- IEEE802.3u Auto-Negotiation support for 10BASE-T and 100BASE-TX
- CARDBUS Interface
- ACPI and PCI power management Ver.1.1 compliant

- Supports PC98 wake on LAN

**FIFO**

- Provides two independent long FIFOs with 2k bytes each for transmission and reception
- Pre-fetch up to two transmit packets to minimize inter frame gap (IFG) to 0.96 μs
- Retransmit collided packet without reload from host memory within 64 bytes
- Automatically retransmit FIFO under-run packet with maximum drain threshold until 3 times retry failure and that will not influence the registers and transmit threshold of next packet

**CARDBUS I/F**

- Provides 32-bit PCI bus master data transfer
- Supports CARDBUS clock with frequency from 0 Hz to 33 MHz
- Supports network operation with CARDBUS system clock from 20 MHz to 33 MHz
- Performance meter, CARDBUS bus master latency timer, for tuning the threshold to enhance performance
- Burst transmit packet interrupt and transmit/receive early interrupt to reduce host CPU utilization
- Memory-read, memory-read-line, memory-read-multiple, memory-write, memory-write-and-invalidate command while being bus master
- Supports big or little endian byte ordering

**EEPROM/Boot ROM I/F**

- Write-able Flash ROM and EPROM as boot ROM with size up to 128 KB
- CARDBUS to access boot ROM by byte, word, or double word
- Re-write Flash boot ROM through I/O port by programming register
- Serial interface for read/write 93C46/66 EEPROM
- Automatically loads device ID, vendor ID, subsystem ID, subsystem vendor ID, Maximum-Latency, and Minimum-Grand from the 64 byte contents of 93C46/66 after PCI reset de-asserted in PCI environment
- CIS data is recalled from 93C66 to AN985B/BX PC internal SRAM to speed up CIS access in CARDBUS environment

**MAC/Physical**

- Integrates the whole Physical layer functions of 100BASE-TX and 10BASE-T
- Full -duplex operation on both 100 Mbit/s and 10 Mbit/s modes
- Auto-negotiation (NWAY) function of full/half duplex operation for both 10 and 100 Mbit/s
- Transmits wave-shaper, receive filters, and adaptive equalizer
- MLT-3 transceivers with DC restoration for Base-line wander compensation
- MAC and Transceiver (TXCVR) loop-back modes for diagnostic
- Built in Stream Cipher Scrambler/ De-scrambler and 4B/5B encoder/decoder
- External transmitting transformer with turn ratio 1:1
- External receiving transformer with turn ratio 1:1

**LED Display**

- 3 LEDs display scheme provided:
  - 100 Mbit/s (on) or Speed 10 (off)
  - Link (keeps on when link ok) or Activity (will be blinking with 10 Hz when receiving or transmitting but not collision)
  - FD (keeps on when in Full duplex mode) or Collision (will be blinking with 20 Hz when colliding)
- 4 LEDs displayed scheme provided:
  - 100 Mbit/s and Link (keep on when link and 100 Mbit/s)
  - 10 Mbit/s and Link (keep on when link and 10 Mbit/s)
  - Activity (will be blinking with 10 Hz when receiving or transmitting but not collision)
  - FD (keeps on when in Full duplex mode) or Collision (will be blinking with 20 Hz when colliding)

**Miscellaneous**

- 128-pin QFP package for CARDBUS interface.

# 4 Block Diagram

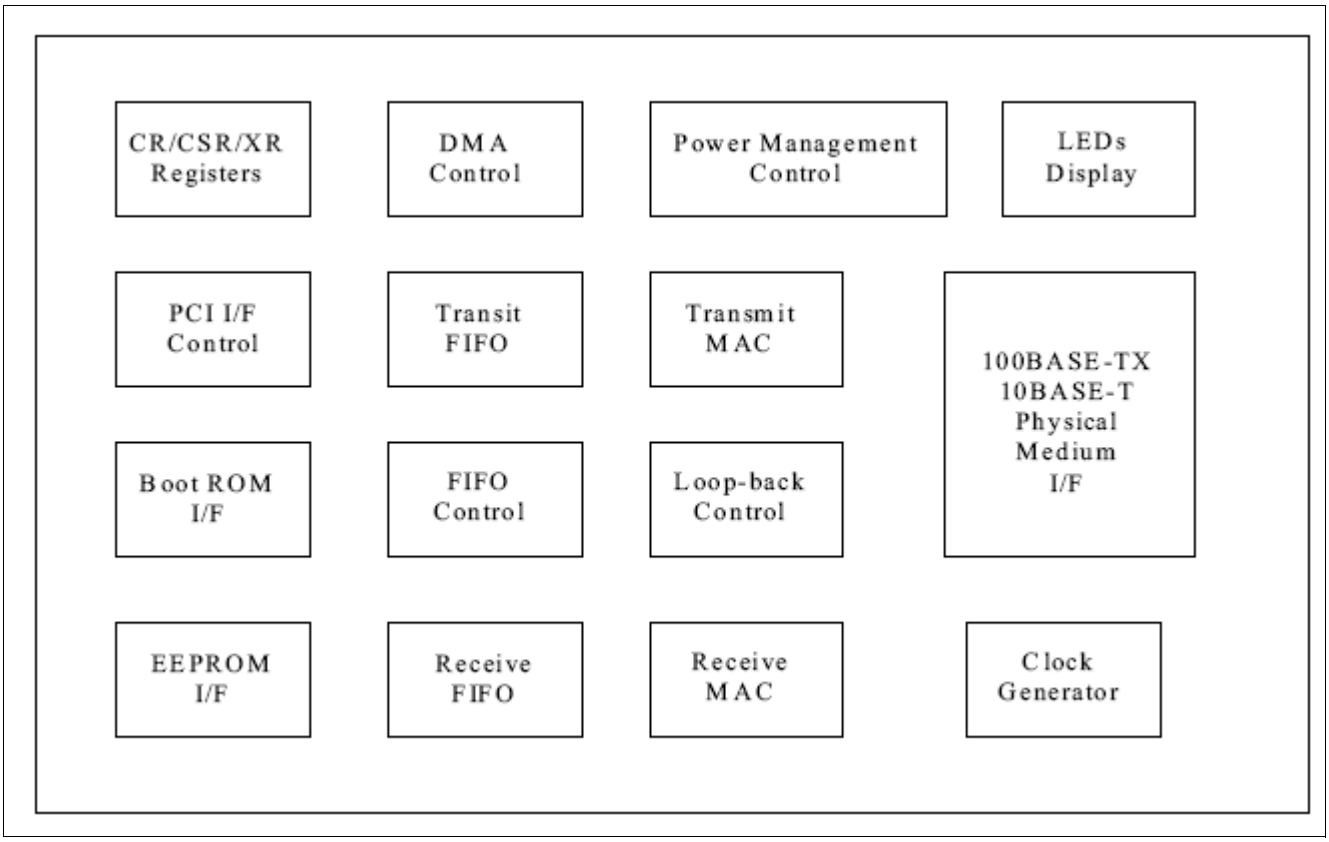


**Figure 2 Block Diagram of the AN985B/BX**

# 5 Pin Assignment Diagram

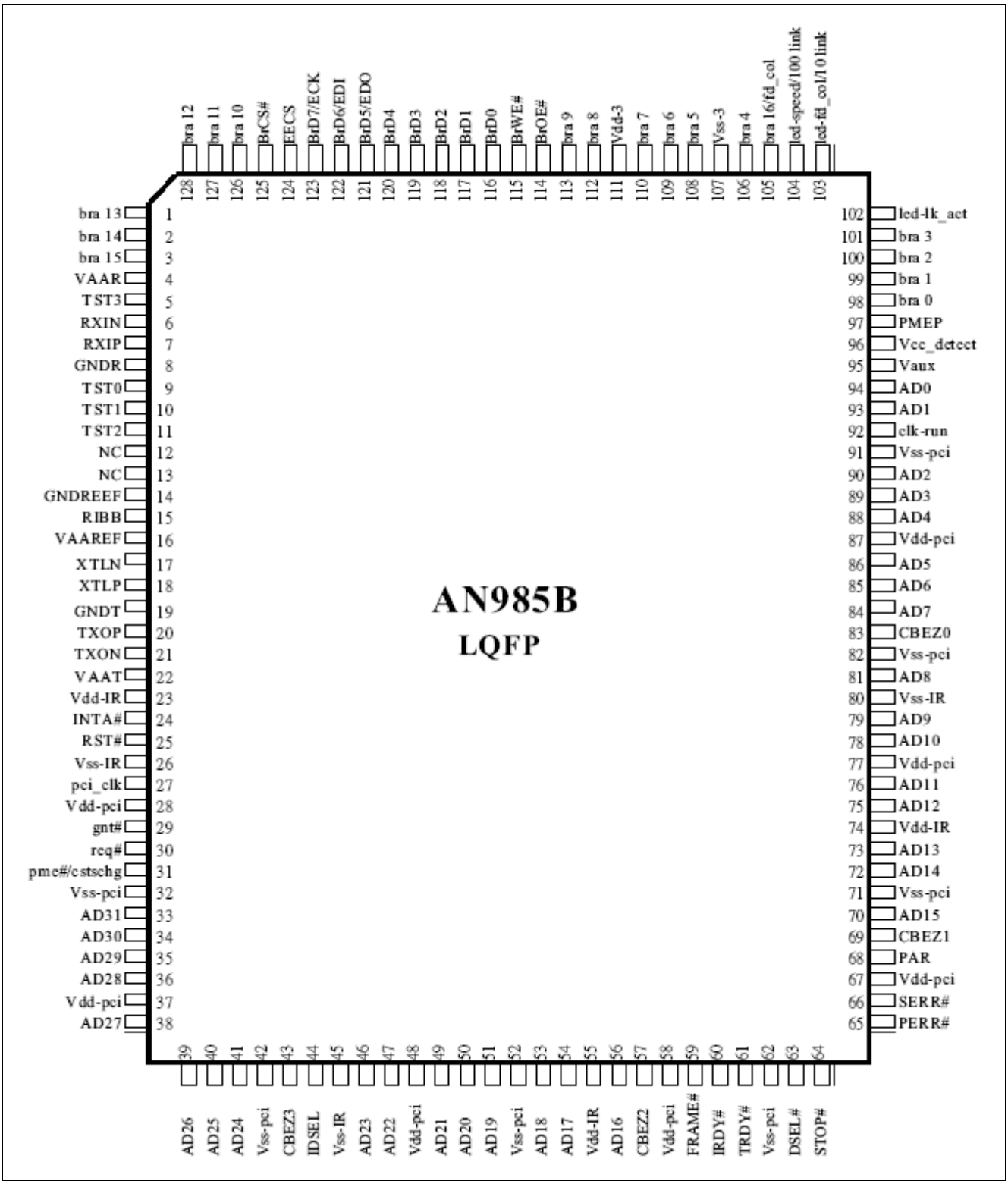


**Figure 3 Pin Assignment (top view)**

## 5.1 Pin Type and Buffer Type Abbreviations

Standardized abbreviations:

**Table 1 Abbreviations for Pin Type**

| Abbreviations | Description |
|---|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| AO | Output. Analog levels. |
| AI/O | Input or Output. Analog levels. |
| PWR | Power |
| GND | Ground |
| MCL | Must be connected to Low (JEDEC Standard) |
| MCH | Must be connected to High (JEDEC Standard) |
| NU | Not Usable (JEDEC Standard) |
| NC | Not Connected (JEDEC Standard) |

**Table 2 Abbreviations for Buffer Type**

| Abbreviations | Description |
|---|---|
| Z | High impedance |
| PU1 | Pull up, 10 kΩ |
| PD1 | Pull down, 10 kΩ |
| PD2 | Pull down, 20 kΩ |
| TS | Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance. |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource. |
| OC | Open Collector |
| PP | Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute). |
| OD/PP | Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute. |
| ST | Schmitt-Trigger characteristics |
| TTL | TTL characteristics |

# 6 Pin Description

**Table 3 Pin Definitions and Functions**

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **PCI Interface** | | | | |
| 24 | INTA# | O/D | | **CARDBUS Interrupt Request**<br>AN985B/BX asserts this signal when one of the interrupt events occurs. |
| 25 | RST# | I | | **CARDBUS Signal to Initialize the AN985B/BX**<br>The active reset signal should be sustained for at least 100μs to guarantee that the AN985B/BX has completed the initializing activity. During the reset period, all the output pins of AN985B/BX will be set to tri-state and all the O/D pins are floated. |
| 27 | CLK | I | | **This CARDBUS Clock Inputs to AN985B/BX for CARDBUS Relative Circuits as the Synchronized Timing Base with CARDBUS**<br>The Bus signals are recognized on the rising edge of CARDBUS-CLK. In order to let the network operate properly, the frequency range of the CARDBUS-CLK is limited to between 20 MHz and 33 MHz when the network is operating. |
| 29 | GNT# | I | | **CARDBUS Bus Granted**<br>This signal indicates that the bus request of AN985B/BX has been accepted. |
| 30 | REQ# | O | | **CARDBUS Bus Request**<br>Bus master device wants to get bus access right |
| 31 | PME#/CSTSCHG | I/O | | **Power Management Event**<br>The Power Management Event signal is an open drain, active low signal for CARDBUS(PME#). When WOL-bit 18 of CSR is set into “1”, this means that the AN985B/BX is set into Wake On LAN mode. In this mode, when the AN985B/BX receives a Magic Packet frame from network then the AN985B/BX will active this signal too. In the Wake On LAN mode, when LWS-bit (bit 17) of CSR18 is set to “1” this means the LAN-WAKE signal is a HP-style signal, otherwise it is an IBM-style signal. |

**Table 3 Pin Definitions and Functions** (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 33 | AD-31 | I/O | | **Multiplexed Address Data Pin of CARDBUS Bus** |
| 34 | AD-30 | | | |
| 35 | AD-29 | | | |
| 36 | AD-28 | | | |
| 38 | AD-27 | | | |
| 39 | AD-26 | | | |
| 40 | AD-25 | | | |
| 41 | AD-24 | | | |
| 46 | AD-23 | | | |
| 47 | AD-22 | | | |
| 49 | AD-21 | | | |
| 50 | AD-20 | | | |
| 51 | AD-19 | | | |
| 53 | AD-18 | | | |
| 54 | AD-17 | | | |
| 56 | AD-16 | | | |
| 70 | AD-15 | | | |
| 72 | AD-14 | | | |
| 73 | AD-13 | | | |
| 75 | AD-12 | | | |
| 76 | AD-11 | | | |
| 78 | AD-10 | | | |
| 79 | AD-9 | | | |
| 81 | AD-8 | | | |
| 84 | AD-7 | | | |
| 85 | AD-6 | | | |
| 86 | AD-5 | | | |
| 88 | AD-4 | | | |
| 89 | AD-3 | | | |
| 90 | AD-2 | | | |
| 93 | AD-1 | | | |
| 94 | AD-0 | | | |
| 43 | C-BEB3 | I/O | | **Bus Command and Byte Enable** |
| 57 | C-BEB2 | | | |
| 69 | C-BEB1 | | | |
| 83 | C-BEB0 | | | |
| 44 | IDSEL | I | | **Initialization Device Select**<br>This signal is asserted when the host issues the configuration cycles to the AN985B/BX. |
| 59 | FRAME# | I/O | | **Begin and Duration of Bus Access**<br>Driven by master device |

**Table 3 Pin Definitions and Functions** (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 60 | IRDY# | I/O | | **Master Device is Ready to Data Transaction** |
| 61 | TRDY# | I/O | | **Slave Device is Ready to Data Transaction** |
| 63 | DEVSEL# | I/O | | **Device Select**<br>Device select, target is driving to indicate the address is decoded |
| 64 | STOP# | I/O | | **Stop the Current Transaction**<br>Target device requests the master device to stop the current transaction |
| 65 | PERR# | I/O | | **Data Parity Error**<br>Data parity error is detected, driven by the agent receiving data |
| 66 | SERR# | O/D | | **Address Parity Error** |
| 68 | PAR | I/O | | **Parity**<br>Parity, even parity (AD [31:0] + C/BE [3:0]); master drives par for address and write data phas; target drives par for read data phase |
| 92 | Clk-run | I/O, O/D | | **Clock Run for CARDBUS System**<br>In the normal operation situation, Host should assert this signal to indicate to AN985B/BX about the normal situation. On the other hand, when Host deasserts this signal the clock is going down to a non-operating frequency. When AN985B/BX recognizes the deasserted status of clk-run, then it will assert clk-run to request Host to maintain the normal clock operation. When the clk-run function is disabled then the AN985B/BX will set clk-run in tri-state. |
| **BOOTROM/EEPROM Interface** | | | | |
| 98 | BrA0 | I/O | | **ROM Data Bus**<br>Provides up to 128kB EPROM or Flash-ROM application space. |
| 99 | BrA1 | | | |
| 100 | BrA2 | | | |
| 101 | BrA3 | | | |
| 106 | BrA4 | | | |
| 108 | BrA5 | | | |
| 109 | BrA6 | | | |
| 110 | BrA7 | | | |
| 112 | BrA8 | | | |
| 113 | BrA9 | | | |
| 126 | BrA10 | | | |
| 127 | BrA11 | | | |
| 128 | BrA12 | | | |
| 1 | BrA13 | | | |
| 2 | BrA14 | | | |
| 3 | BrA15 | | | |
| 105 | BrA16 | | | |

**Table 3 Pin Definitions and Functions** (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 116 | BrD0 | O | | **BootROM Data Bus Bit (0~7)**<br>Inputs/Output data for AN985B/BX<br>EDO: Data Output of serial EEPROM<br>EDI: Data Input of serial EEPROM<br>ECK: Clock input of serial EEPROM<br>The AN985B/BX outputs clock signal to EEPROM. |
| 117 | BrD1 | | | |
| 118 | BrD2 | | | |
| 119 | BrD3 | | | |
| 120 | BrD4 | | | |
| 121 | BrD5/EDO | O/I | | |
| 122 | BrD6/EDI | O/O | | |
| 123 | BrD7/ECK | O/O | | |
| 124 | EECS | O | | **Chip Select of Serial EEPROM** |
| 125 | BrCS# | O | | **BootROM Chip Select** |
| 114 | BrOE# | O | | **BootROM Read Enable for Flash ROM Application** |
| 115 | BrWE# | O | | **BootROM Write Enable for Flash ROM Application** |
| **Physical Interface** | | | | |
| 18 | XTLP | I | | **Crystal Inputs**<br>To be connected to a 25 MHz crystal. |
| 17 | XTLN | | | |
| 6 | RXIN | I | | **Differentials Receive Inputs**<br>The differentials receive inputs of 100BASE-TX or 10BASE-T, these pins are directly inputted from Magnetic. |
| 7 | RXIP | | | |
| 20 | TXOP | O | | **Differential Transmit Outputs**<br>The differential Transmit outputs of 100BASE-TX or 10BASE-T, these pins are directly outputted to Magnetic. |
| 21 | TXON | | | |
| 15 | RIBB | I | | **Reference Bias Resistor**<br>To be tied to an external 10.0K (1%) resistor which should be connected to the analog ground at the other end. |
| 9 | TST0 | I | | **Test Pin** |
| 10 | TST1 | | | |
| 11 | TST2 | | | |
| 5 | TST3 | | | |
| 12 | NC | O | | **Not Connected** |
| 13 | NC | | | |
| **LED Display and Miscellaneous** | | | | |
| 102 | Led-Act | O | | **4 LED Mode: LED Display for Activity Status**<br>This pin will be driven on with 10 Hz blinking frequency when either effective receiving or transmitting is detected. |
| | (Led-lnk/act) | O | | **(3 LED Mode): LED Display for Link and Activity Status**<br>Link and Activity |
| 103 | Led-10Lnk | O | | **4 LED Mode: LED Display for 10 Mbit/s Speed**<br>This pin will be driven on continually when the 10 Mbit/s network operating speed is detected. |
| | (Led-fd/col) | O | | **(3 LED Mode): LED Display for Full Duplex or Collision Status**<br>full duplex/collision |

**Table 3 Pin Definitions and Functions** (cont'd)

| Pin or Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 104 | Led-100Lnk | O | | **4 LED Mode: LED Display for 100 Mbit/s Speed**<br>This pin will be driven on continually when the 100 Mbit/s network operating speed is detected. |
| | (Led-speed) | O | | **(3 LED Mode): LED Display for 100 Mbit/s or 10 Mbit/s speed**<br>speed 100(on)/10(off) |
| 105 | Led-Fd/Col | O | | **4 LED Mode: LED Display for Full Duplex or Collision Status**<br>This pin will be driven on continually when a full duplex configuration is detected. This pin will be driven on with 20 Hz blinking frequency when a collision status is detected in the half duplex configuration. |
| | bra(16) | O | | **(3 LED Mode):bra 16** |
| 95 | Vaux | I | | **When this pin is asserted, it indicates an auxiliary power source is supported.**<br>ACPI purpose, for detecting the auxiliary power source. This pin should be or-wired connected to:<br>1) 3.3 V when 3.3 Vaux support, or<br>2) 5 V when 5 Vaux support from 3-way switch. |
| 96 | Vcc-detect | I | | **When this pin is asserted, it indicates PCI power source is supported.**<br>ACPI purpose, for detecting the main power is remained or not. This pin should be connected to PCI bus power source +5 V. |
| 97 | PMEP | O | | **High pulse/low pulse 50ms** |
| **Digital Power Pins** | | | | |
| 26, 32, 42, 45, 52, 62, 71, 80, 82, 91, 107 | $V_{ss\text{-}pci}$, $V_{ss\text{-}IR}$, $V_{ss\text{-}3}$ | | | |
| 23, 28, 37, 48, 55, 58, 67, 74, 77, 87, 111 | $V_{dd\text{-}pci}$, $V_{dd\text{-}IR}$, $V_{dd\text{-}3}$, Connect to 3.3 V | | | |
| **Analog Power Pins** | | | | |
| 4,16,22 | $V_{AAR}$, $V_{AAREF}$, $V_{AAT}$, 3.3 V | | | |
| 8,14,19 | GNDR, GNDREF, GNDT | | | |

# 7 Functional Descriptions

## 7.1 Network Packet Buffer Management

### 7.1.1 Descriptor Structure Types

For networking operations, the AN985B/BX transmits the data packet from transmitting buffers in host memory to AN985B/BX's transmitting FIFO and receives the data packet from AN985B/BX's receiving FIFO to receive buffers in host memory. The descriptors that the AN985B/BX supports to build in host memory are used as the pointers of these transmitting and receiving buffers.

There are two structure types for the descriptor, **Ring and Chain**, supported by the AN985B/BX and are shown as below. The type selections are controlled by bit 24 of RDES1 and the bit 24 of TDES1.

The transmitting and receiving buffers are physically built in host memory. Any buffer can contain either a whole packet or just part of a packet. But it can't contain more than one packet.

- Ring structure

There are two buffers per descriptor in the ring structure. Support receives early interrupt.

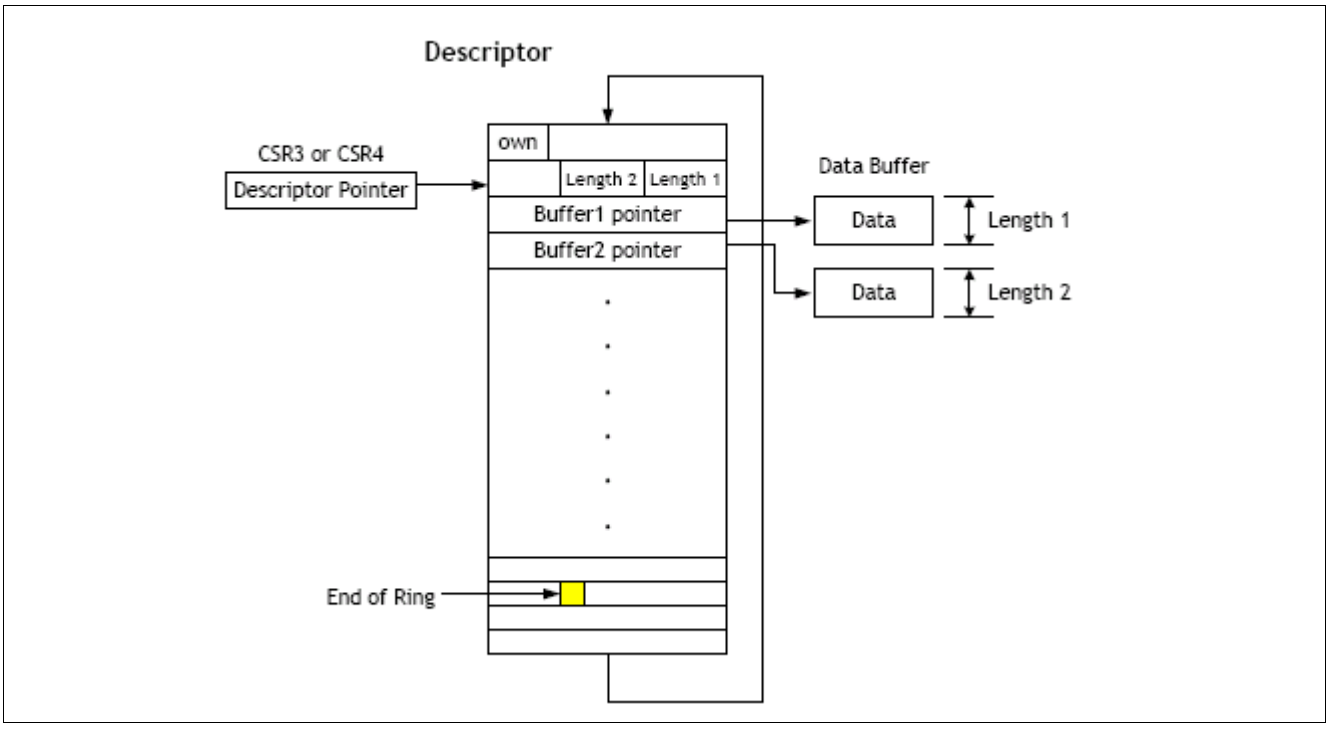


**Figure 4 Ring Structure of Frame Buffer**

- Chain structure

There is only one buffer per descriptor in the chain structure.

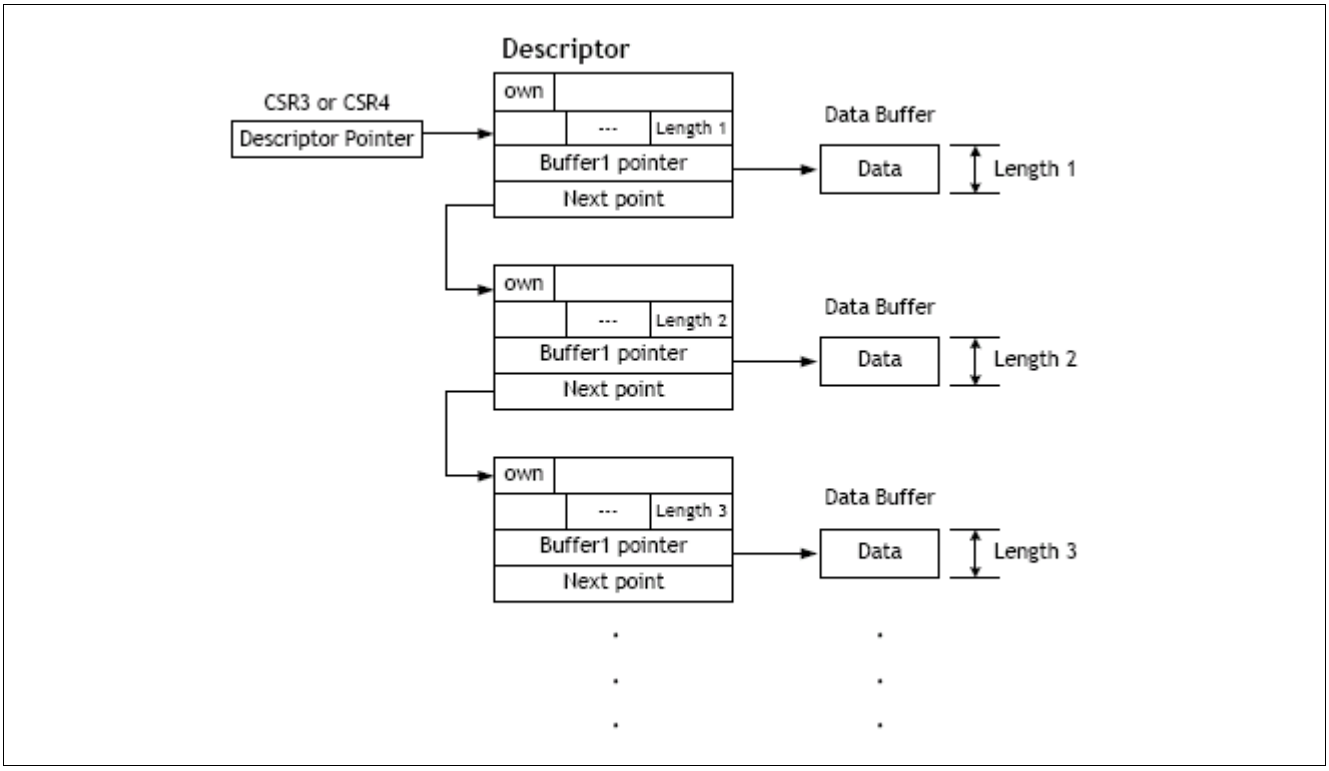


**Figure 5 Chain Structure of Frame Buffer**

### 7.1.2 The Point of Descriptor Management

OWN bit = 1, ready for network side access

OWN bit = 0, ready for host side access

- Transmit Descriptor Pointers

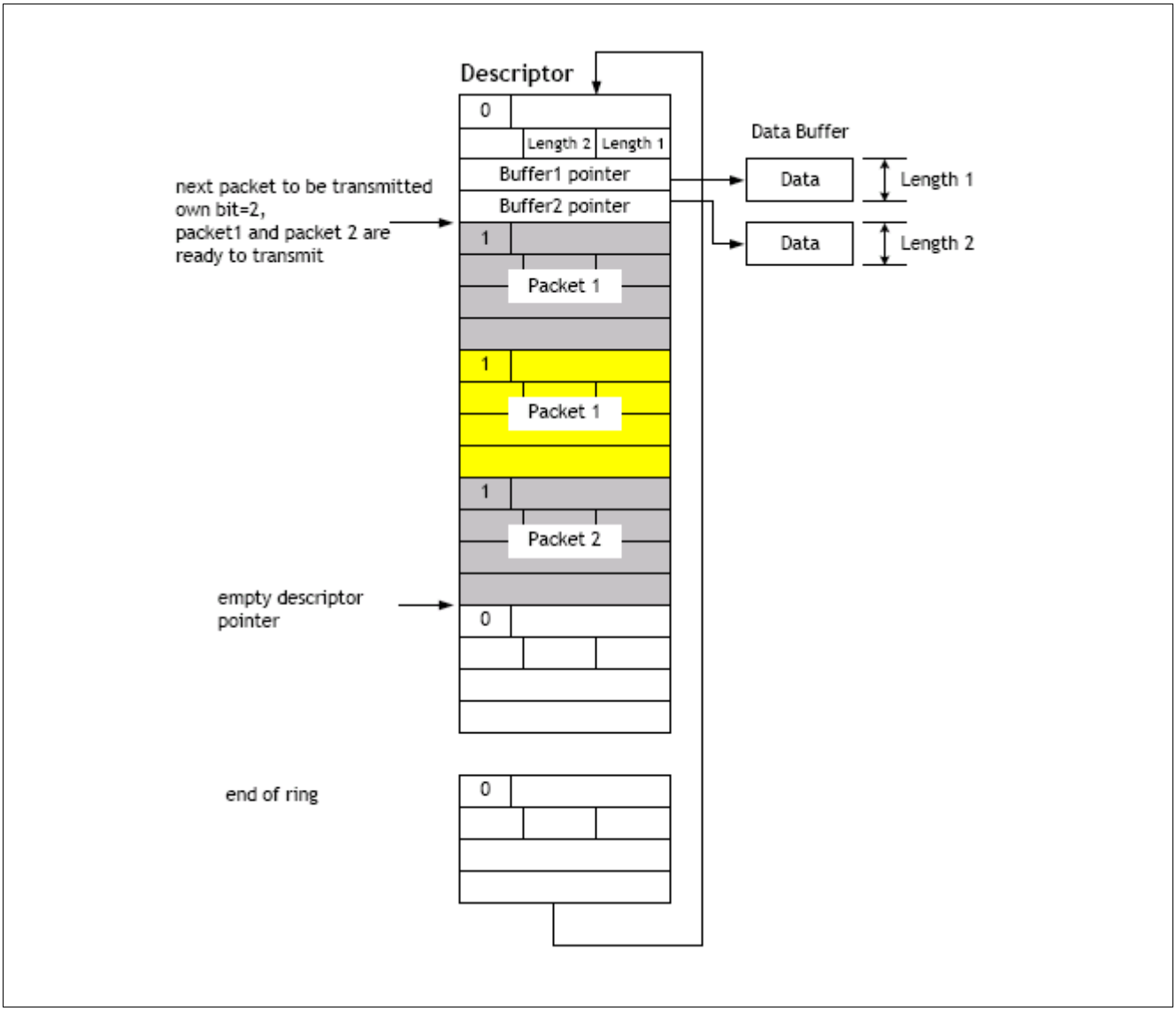


**Figure 6 Transmit Pointers for Descriptor Management**

- Receive Descriptor Pointers

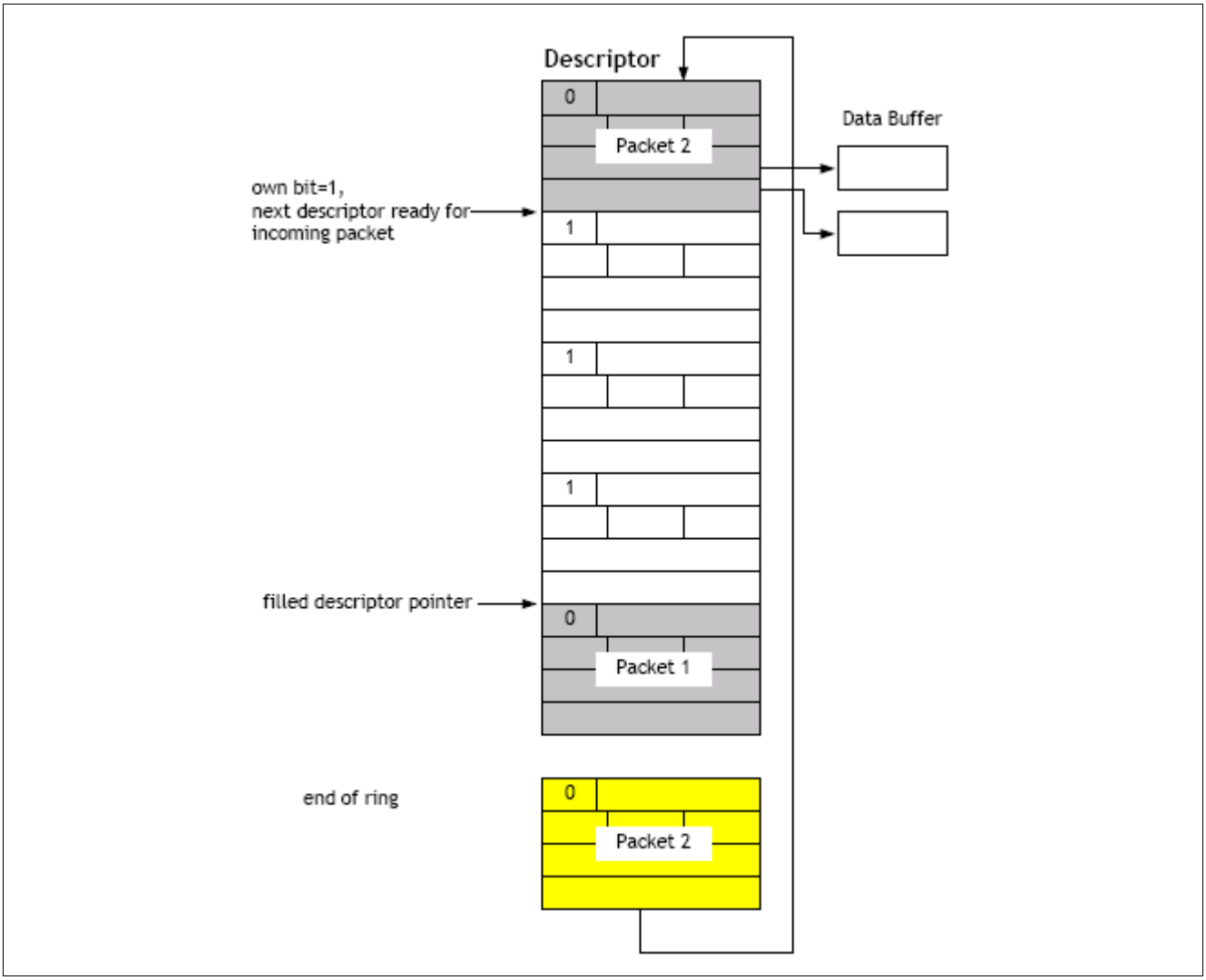


**Figure 7 Receive Pointers for Descriptor Management**

## 7.2 Transmit Scheme and Transmit Early Interrupt

### 7.2.1 Transmit Flow

The flow of packet transmit is shown below.

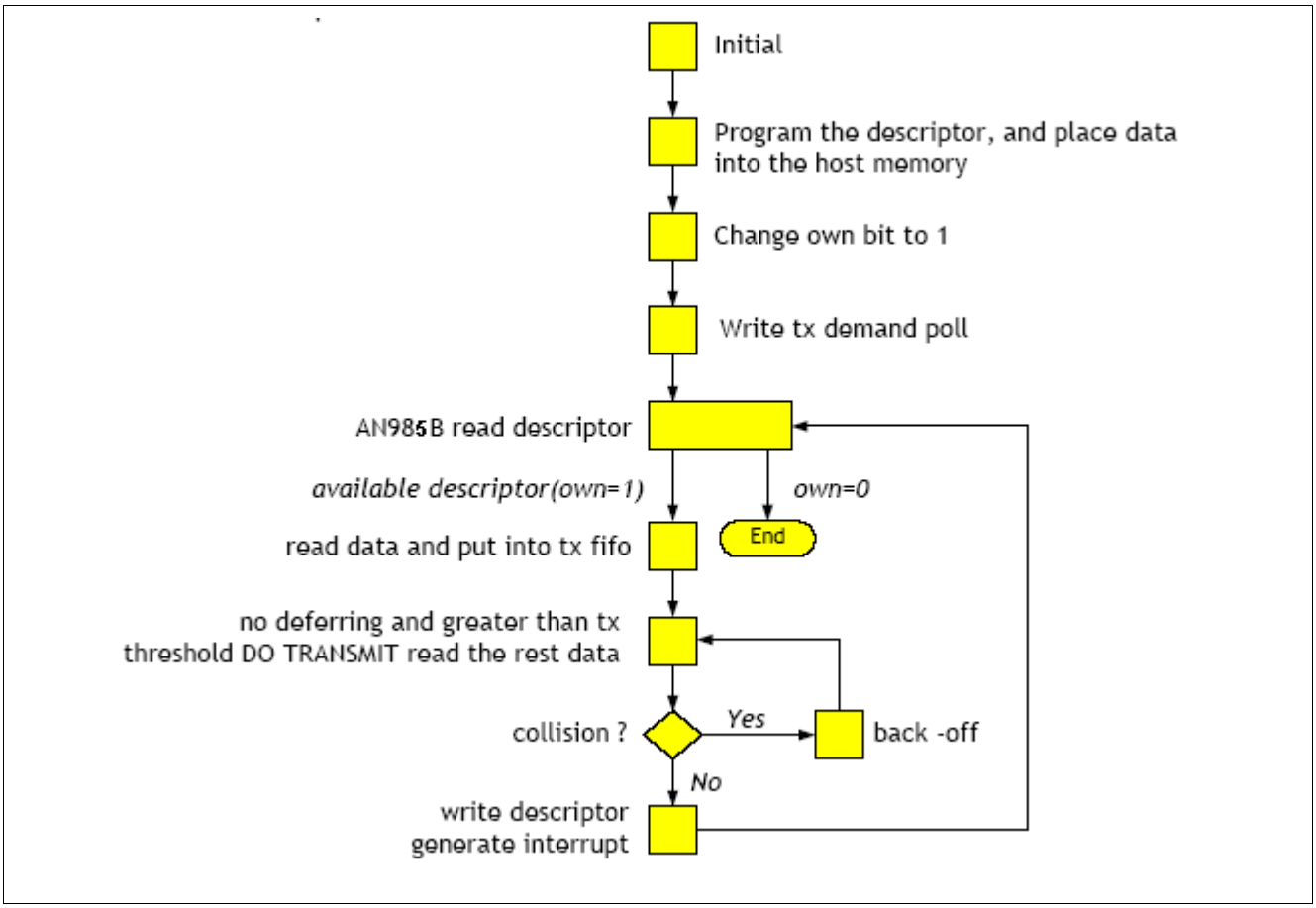


**Figure 8 Transmit Flow**

### 7.2.2 Transmit Pre-fetch Data Flow

- Transmit FIFO size = 2K-byte
- Two packets in the FIFO at the same time
- Meet the transmit min. back-to-back

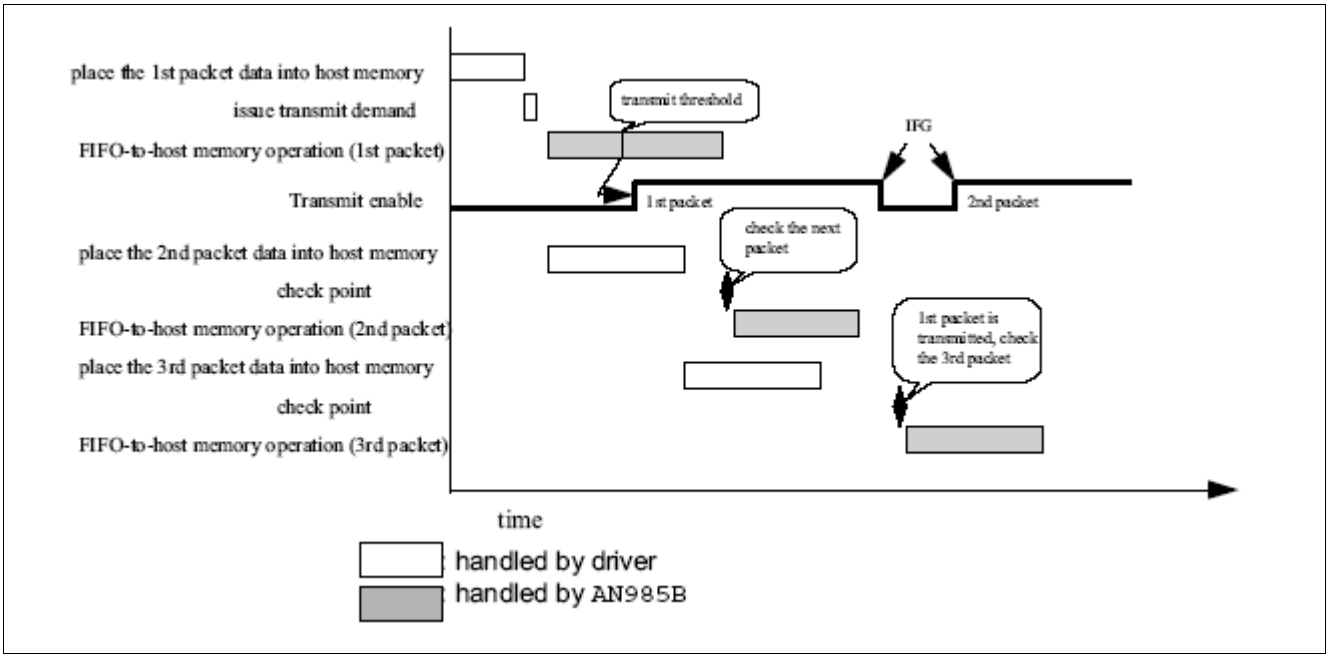


**Figure 9 Transmit Data Flow of Pre-fetch Data**

### 7.2.3 Transmit Early interrupt Scheme

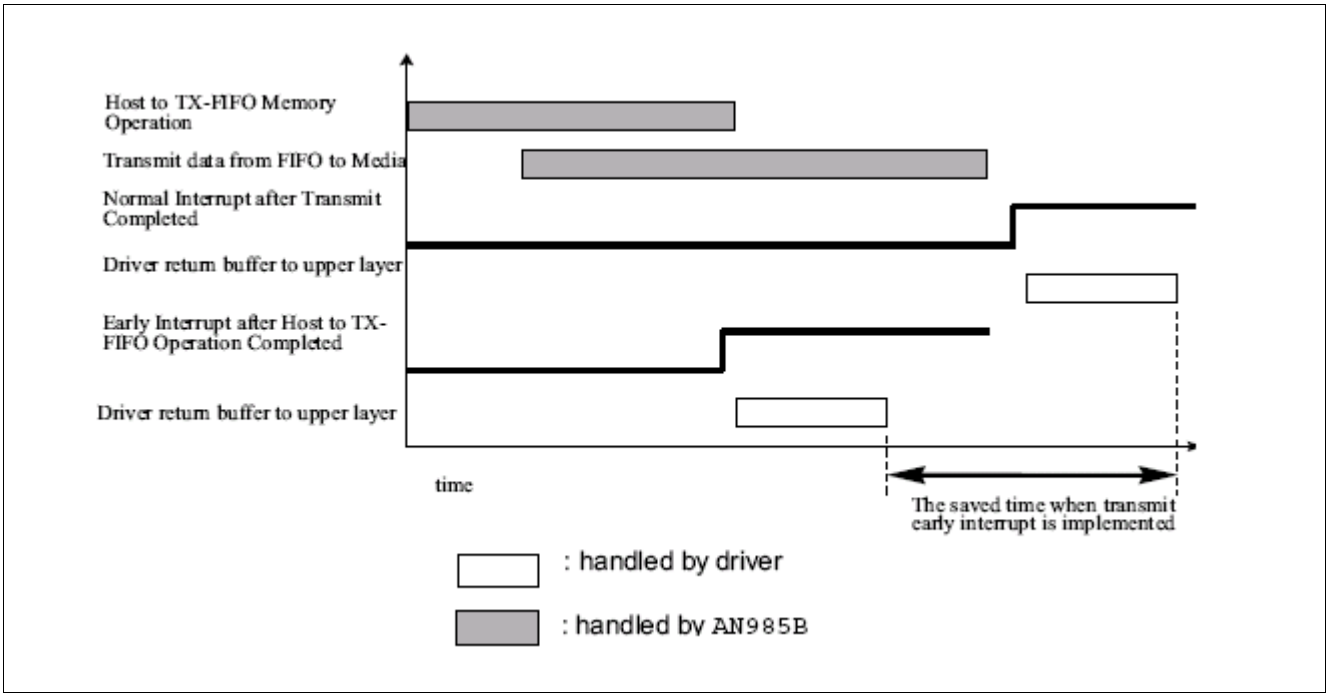


**Figure 10 Transmit Normal Interrupt and Early Interrupt Comparison**

## 7.3 Receive Scheme and Receive Early Interrupt Scheme

The following figure shows the difference of timing without early interrupt and with early interrupt.

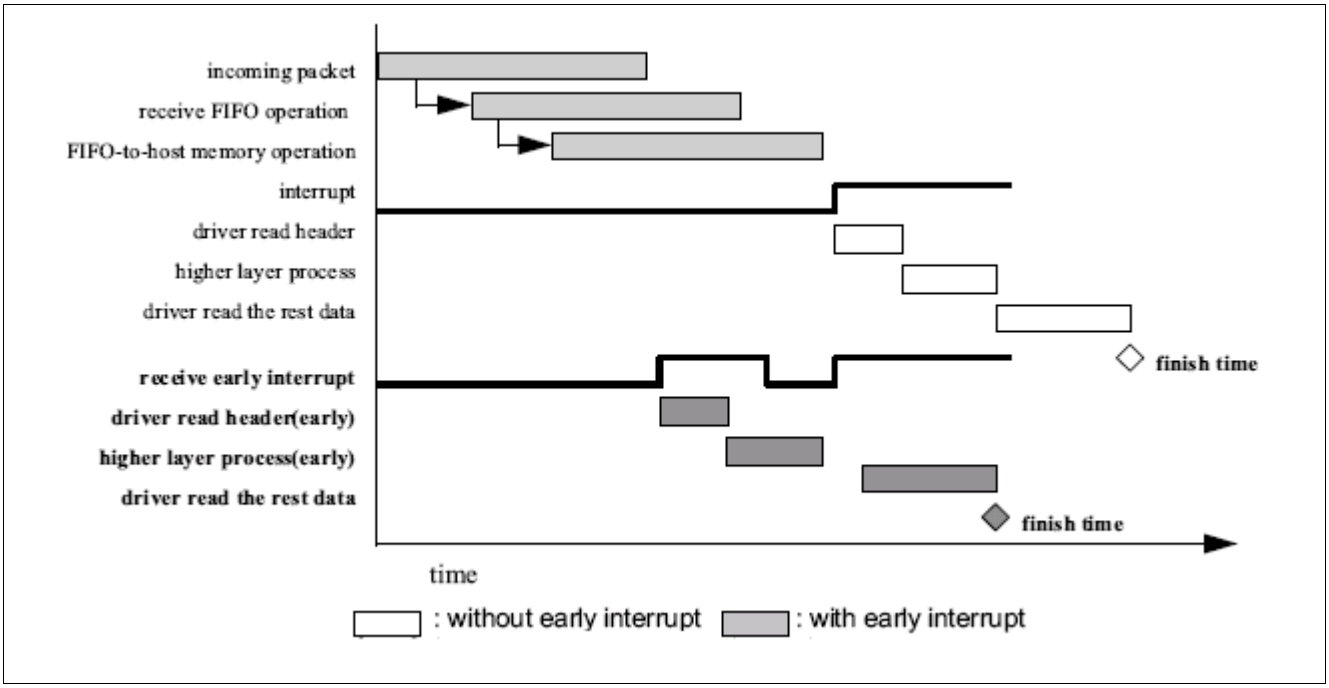


**Figure 11 Receive Data Flow (without early interrupt and with early interrupt)**

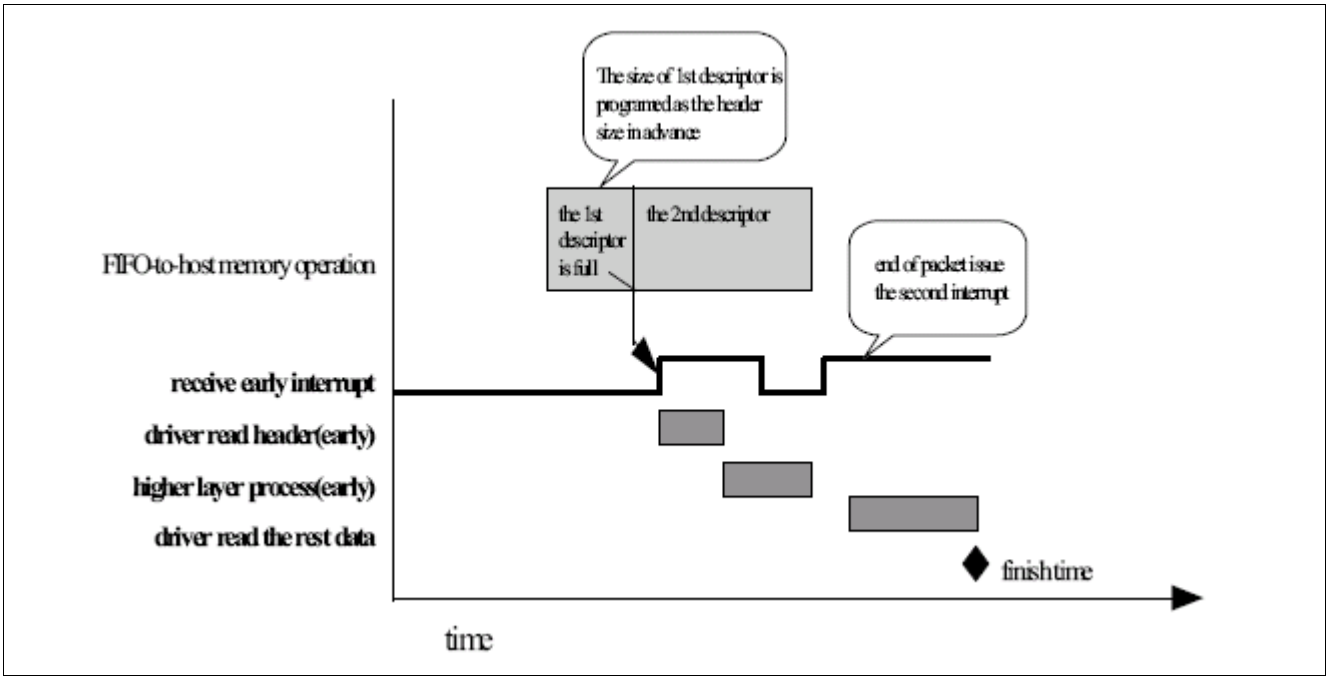


**Figure 12 Detailed Receive Early Interrupt Flow**

## 7.4 Network Operation

### 7.4.1 MAC Operation

The MAC (Media Access Control) portion of AN985B/BX, incorporates the essential protocol requirements for operating as an IEEE802.3 and Ethernet compliant node.

**Table 4 Format**

| Field | Description |
|---|---|
| Preamble | A 7-byte field of (10101010b) |
| Start Frame Delimiter | A 1-byte field of (10101011b) |
| Destination Address | A 6-byte field |
| Source Address | A 6-byte field |
| Length/Type | A 2-byte field indicated the frame is in IEEE802.3 format or Ethernet format.IEEE802.3 format: 0000H ~ 05DCH for Length field Ethernet format: 05DD ~ FFFFH for Type field |
| Data | 46[1] ~ 1500 bytes of data information |
| CRC | A 32-bit cyclic redundant code for error detection |

1) If padding is disabled (TDES1 bit23), the data field may be shorter than 46 bytes.

### Transmit Data Encapsulation

The differences between the encapsulation and a MAC frame while operating in the 100BASE-TX mode are listed as follow:

1. The first byte of the preamble is replaced by the JK code according to the IEE802.3u, clause 24.
2. After the CRC field of the MAC frame, the AN985B/BX inserts the TR code according to the IEE802.3u, clause 24.

### Receive Data Decapsulation

When operating in 100BASE-TX mode the AN985B/BX detects a JK code for a preamble as well as a TR code for the packet end. If a JK code is not detected, the AN985B/BX will abort this frame receiving and wait for a new JK code detection. If a TR code is not detected, the AN985B/BX will report a CRC error.

### Deferring

The Inter-Frame Gap (IFG) time is divided into two parts:

1. IFG1 time (64-bit time): If a carrier is detected on the medium during this time, the AN985B/BX will reset the IFG1 time counter and restart to monitor the channel for an idle again.
2. IFG2 time (32-bit time): After counting the IFG2 time the AN985B/BX will access the channel even though a carrier has been sensed on the network.

### Collision Handling

The scheduling of re-transmissions is determined by a controlled randomization process called “truncated binary exponential back-off”. At the end of enforcing a collision (jamming), the AN985B/BX delays before attempting to re-transmit the packet. The delay is an integer multiple of slot time. The number of slot times to delay before the nth re-transmission attempt is chosen as a uniform distributed integer r in the range:

$0 \leq r < 2^k$, where k = min (n, 10)