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General Description

The AO3400 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is suitable for use as a load switch or in PWM applications.

Product Summary

V_{DS}	30V
I_D (at V_{GS}=10V)	5.8A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 28mΩ
$R_{DS(ON)}$ (at V_{GS} = 4.5V)	< 33mΩ
$R_{DS(ON)}$ (at V_{GS} = 2.5V)	< 52mΩ

Green Product

SOT23
Top View   Bottom View
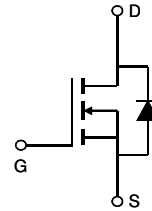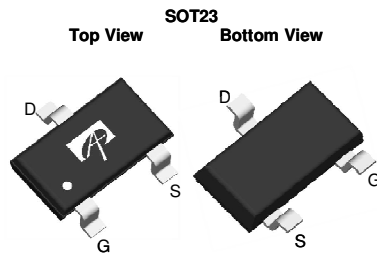
Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A=25℃	I_D	5.8	A
	T_A=70℃		4.9	
Pulsed Drain Current ^{C}		I_{DM}	30	
Power Dissipation ^{B}	T_A=25℃	P_D	1.4	W
	T_A=70℃		0.9	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^{A}	t ≤ 10s	$R_{θJA}$	70	90	℃/W
Maximum Junction-to-Ambient $^{A D}$	Steady-State		100	125	℃/W
Maximum Junction-to-Lead	Steady-State	$R_{θJL}$	63	80	℃/W

Electrical Characteristics (T$_J$=25℃ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=250µA, V$_{GS}$=0V		30			V
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=30V, V$_{GS}$=0V				1	µA
			T$_J$=55℃			5	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$= ±12V				100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=V$_{GS}$ I$_D$=250µA		0.65	1.05	1.45	V
I$_{D(ON)}$	On state drain current	V$_{GS}$=4.5V, V$_{DS}$=5V		30			A
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=5.8A			18	28	mΩ
			T$_J$=125℃		28	39	
		V$_{GS}$=4.5V, I$_D$=5A			19	33	mΩ
		V$_{GS}$=2.5V, I$_D$=4A			24	52	mΩ
g$_{FS}$	Forward Transconductance	V$_{DS}$=5V, I$_D$=5.8A			33		S
V$_{SD}$	Diode Forward Voltage	I$_S$=1A,V$_{GS}$=0V			0.7	1	V
I$_S$	Maximum Body-Diode Continuous Current					2	A
DYNAMIC PARAMETERS							
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=15V, f=1MHz			630		pF
C$_{oss}$	Output Capacitance				75		pF
C$_{rss}$	Reverse Transfer Capacitance				50		pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz		1.5	3	4.5	Ω
SWITCHING PARAMETERS							
Q$_g$	Total Gate Charge	V$_{GS}$=4.5V, V$_{DS}$=15V, I$_D$=5.8A			6	7	nC
Q$_{gs}$	Gate Source Charge				1.3		nC
Q$_{gd}$	Gate Drain Charge				1.8		nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=15V, R$_L$=2.6Ω, R$_{GEN}$=3Ω			3		ns
t$_r$	Turn-On Rise Time				2.5		ns
t$_{D(off)}$	Turn-Off DelayTime				25		ns
t$_f$	Turn-Off Fall Time				4		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=5.8A, dI/dt=100A/µs			8.5		ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=5.8A, dI/dt=100A/µs			2.6		nC

A. The value of R$_{θJA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T$_A$ =25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT$_J$=25° C.

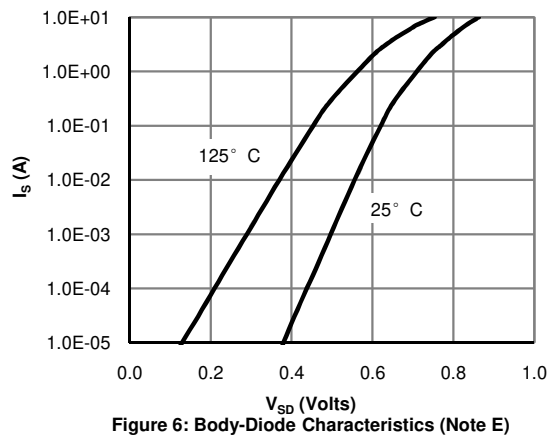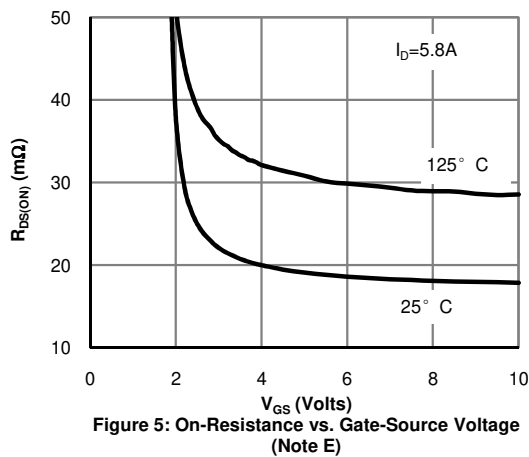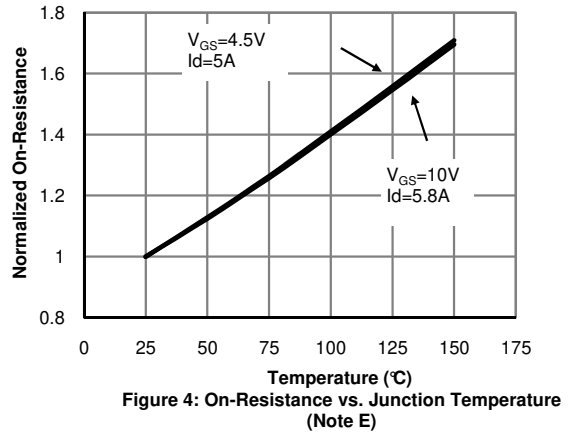D. The R$_{θJA}$ is the sum of the thermal impedence from junction to lead R$_{θJL}$ and lead to ambient.
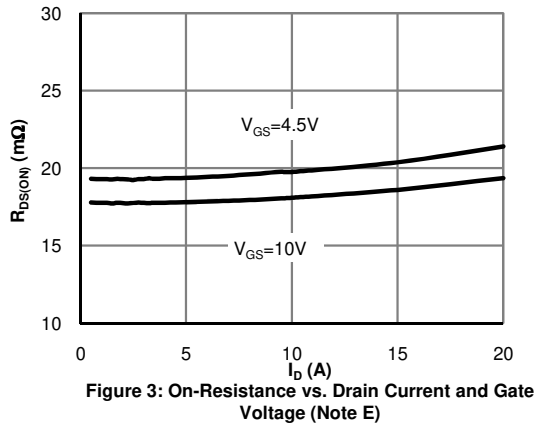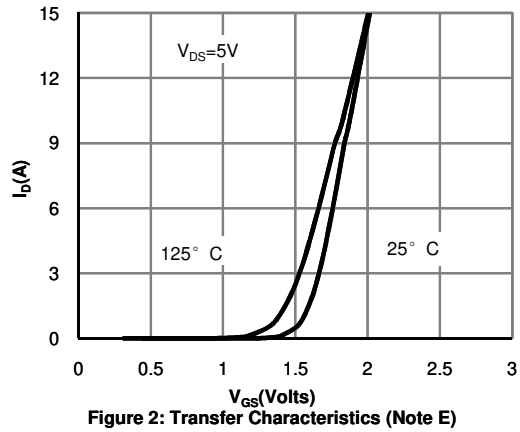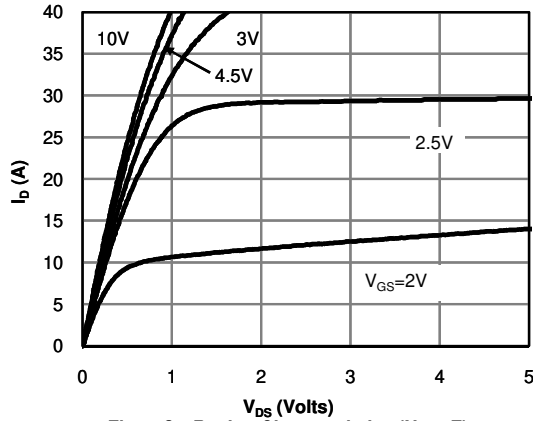
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T$_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Fig 1: On-Region Characteristics (Note E)

Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

Figure 4: On-Resistance vs. Junction Temperature (Note E)

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
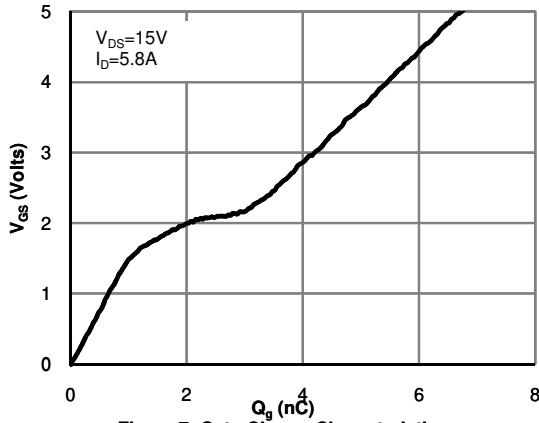
Figure 7: Gate-Charge Characteristics
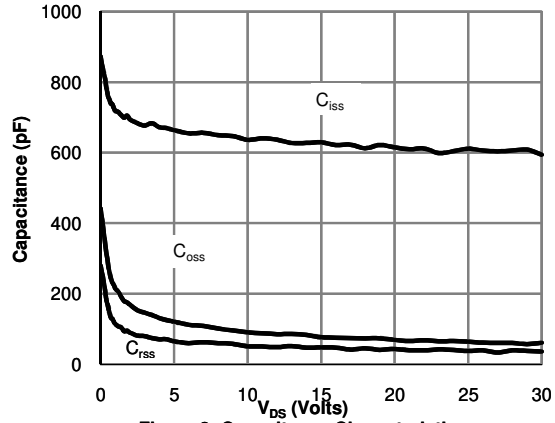
Figure 8: Capacitance Characteristics
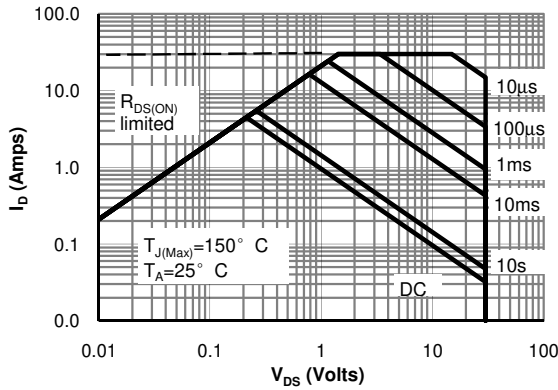
Figure 9: Maximum Forward Biased Safe
Operating Area (Note F)
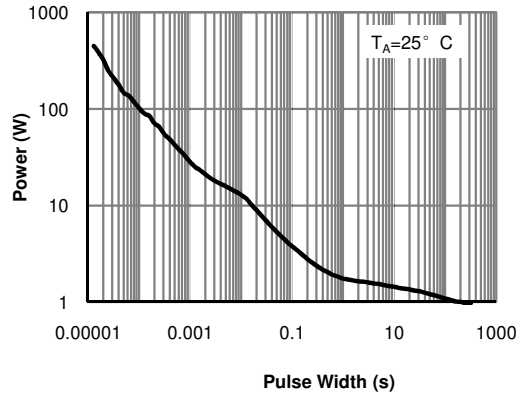
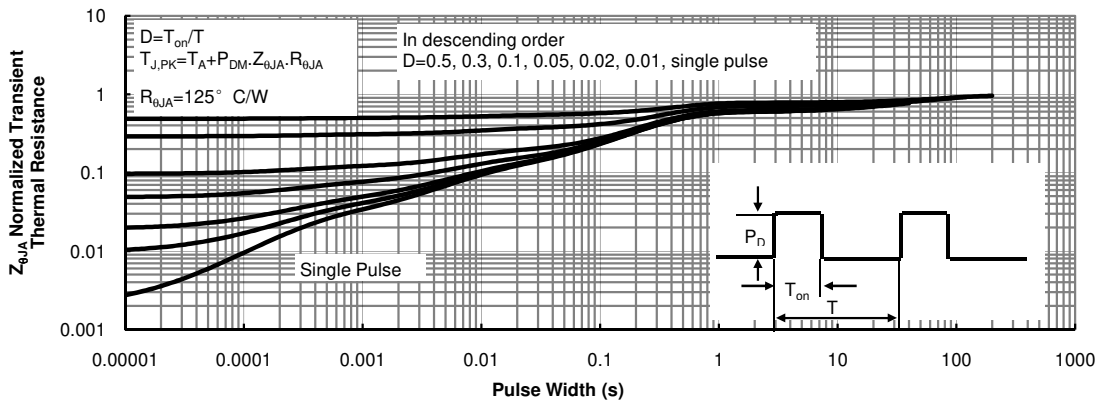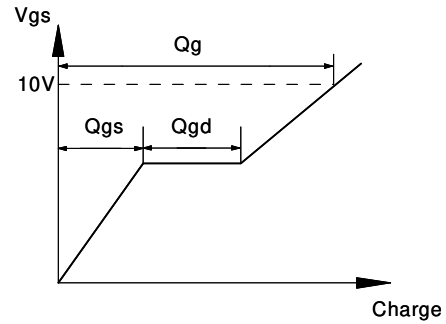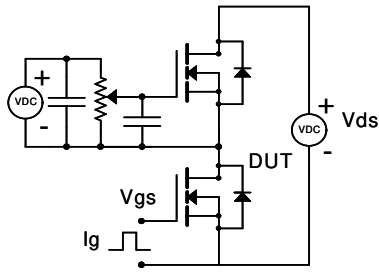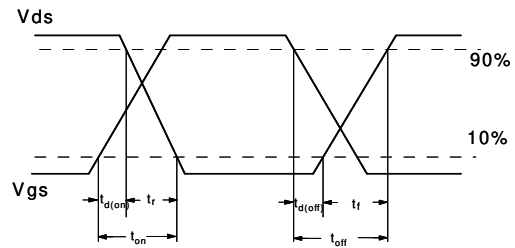Figure 10: Single Pulse Power Rating Junction-to-
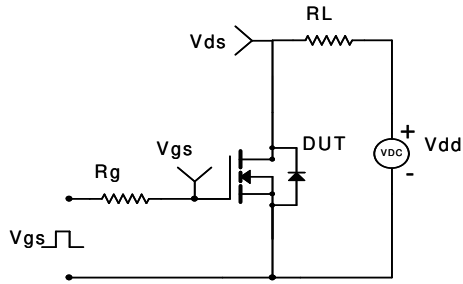Ambient (Note F)

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int I\,dt$$