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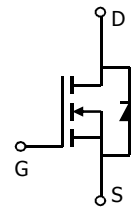
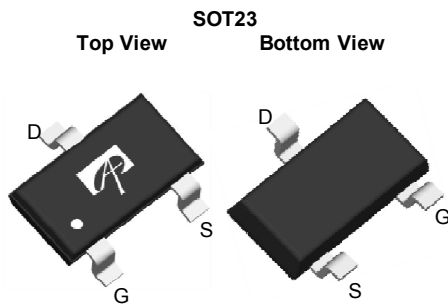
N-Channel Enhancement Mode Field Effect Transistor

General Description

The AO3404A uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications.

Features

V_{DS} (V) = 30V
 I_D = 5.8A ($V_{GS} = 10V$)
 $R_{DS(ON)} < 25m\Omega$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 35m\Omega$ ($V_{GS} = 4.5V$)



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^{A,F}	I_D	$T_A=25^\circ C$	5.8
		$T_A=70^\circ C$	4.9
Pulsed Drain Current ^B	I_{DM}	64	A
Power Dissipation	P_D	$T_A=25^\circ C$	1.4
		$T_A=70^\circ C$	0.9
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	65	90	$^\circ C/W$
$t \leq 10s$				
Maximum Junction-to-Ambient ^A	$R_{\theta JL}$	63	80	$^\circ C/W$
Steady-State				
Maximum Junction-to-Lead ^C				

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1.5	2.1	2.6	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	64			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =5.8A T _J =125°C		18.4 26.2	25 36	mΩ
		V _{GS} =4.5V, I _D =4.8A		24.5	35	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =5.8A		22		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.75	1	V
I _S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		373	448	pF
C _{oss}	Output Capacitance			67		pF
C _{rss}	Reverse Transfer Capacitance			41		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.9	1.8	2.8	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =5.8A		7.1	11	nC
Q _g (4.5V)	Total Gate Charge			3.3		nC
Q _{gs}	Gate Source Charge			1.4		nC
Q _{gd}	Gate Drain Charge			1.7		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =2.6Ω, R _{GEN} =3Ω		4.5	6.5	ns
t _r	Turn-On Rise Time			2.4		ns
t _{D(off)}	Turn-Off DelayTime			14.8		ns
t _f	Turn-Off Fall Time			2.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =5.8A, di/dt=100A/μs		10.5	12.6	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =5.8A, di/dt=100A/μs		4.5		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The SOA curve provides a single pulse rating.

F. The current rating is based on the t ≤ 10s thermal resistance rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

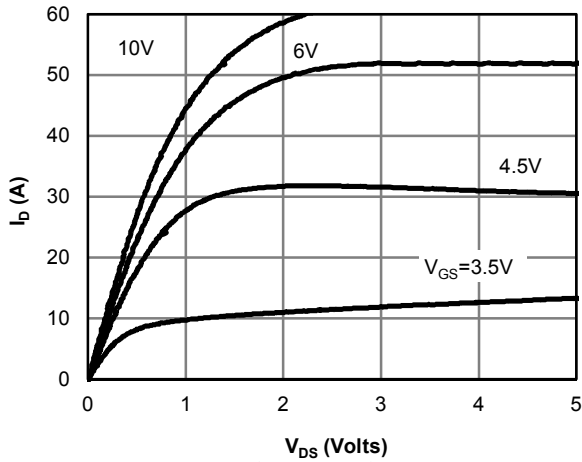


Figure 1: On-Region Characteristics

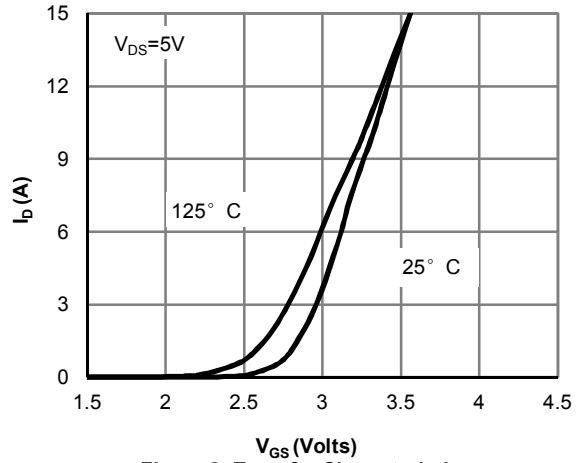


Figure 2: Transfer Characteristics

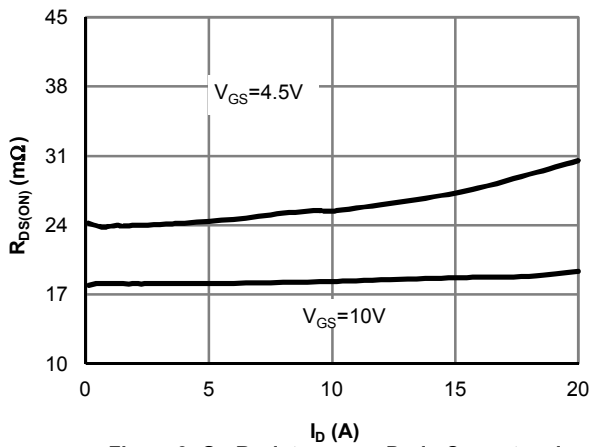


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

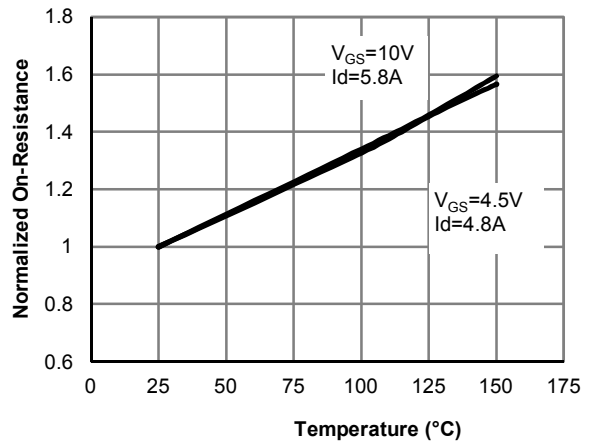


Figure 4: On-Resistance vs. Junction Temperature

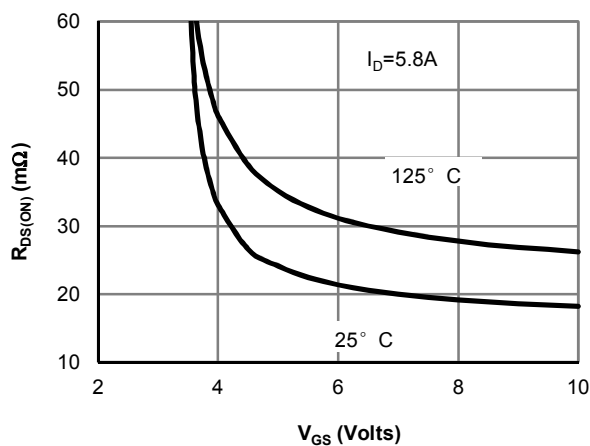


Figure 5: On-Resistance vs. Gate-Source Voltage

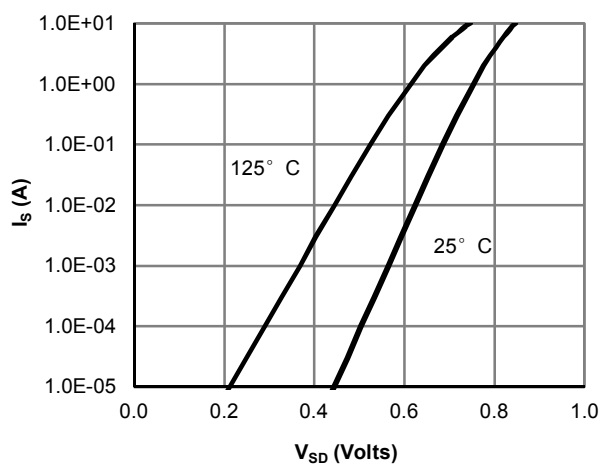


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

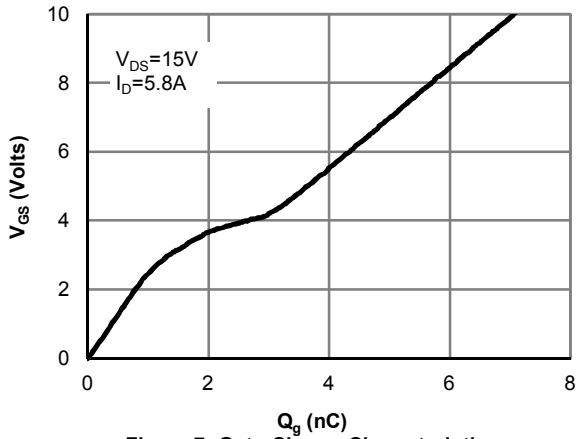


Figure 7: Gate-Charge Characteristics

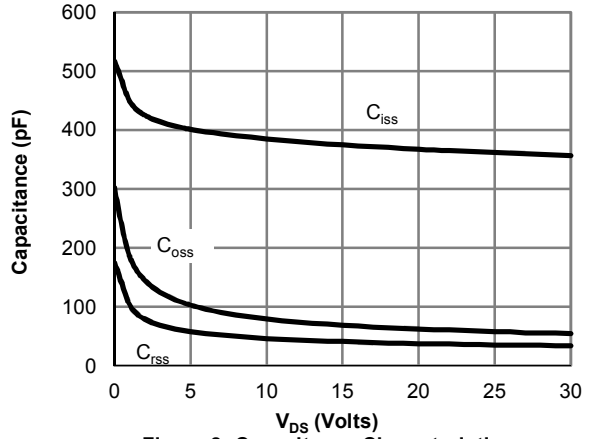


Figure 8: Capacitance Characteristics

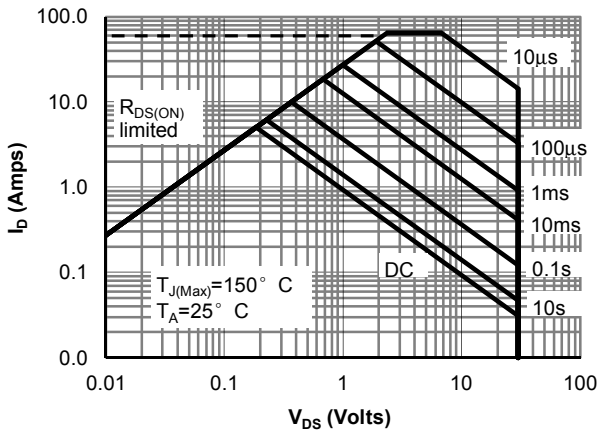


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

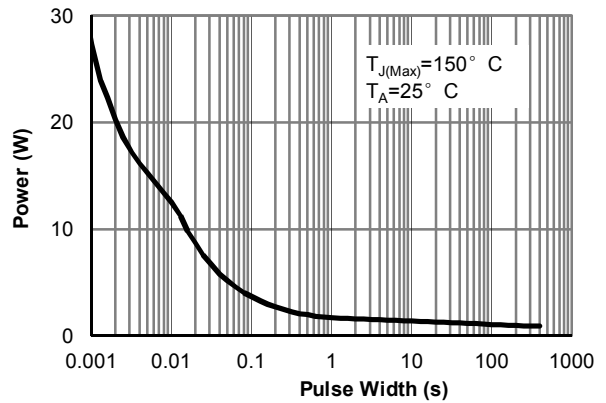


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

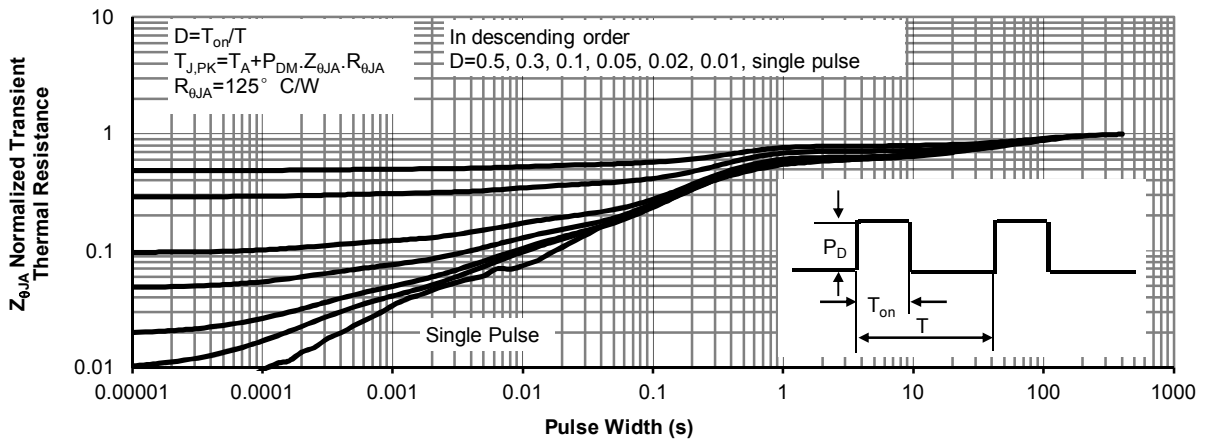


Figure 11: Normalized Maximum Transient Thermal Impedance