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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



General Description

The AO6601 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs form a high-speed power inverter, suitable for a multitude of applications.

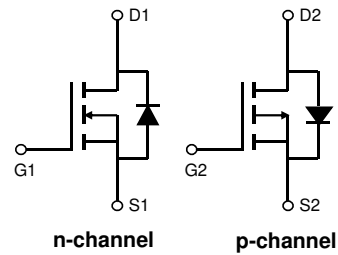
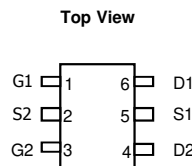
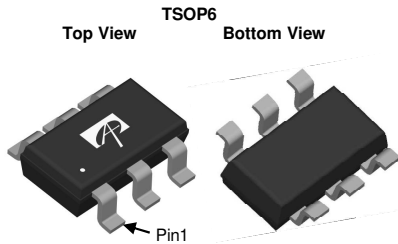
Product Summary

N-Channel

$V_{DS} = 30V$
 $I_D = 3.4A$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 60m\Omega$ ($V_{GS} = 10V$)
 $< 70m\Omega$ ($V_{GS} = 4.5V$)
 $< 90m\Omega$ ($V_{GS} = 2.5V$)

P-Channel

$-30V$
 $-2.3A$ ($V_{GS} = -10V$)
 $R_{DS(ON)} < 115m\Omega$ ($V_{GS} = -10V$)
 $< 150m\Omega$ ($V_{GS} = -4.5V$)
 $< 200m\Omega$ ($V_{GS} = -2.5V$)



Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 12	± 12	V
Continuous Drain Current	I_D	$T_A = 25^\circ C$	-2.3	A
		$T_A = 70^\circ C$	-1.8	
Pulsed Drain Current ^C	I_{DM}	20	-15	
Power Dissipation ^B	P_D	$T_A = 25^\circ C$	1.15	W
		$T_A = 70^\circ C$	0.73	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A $t \leq 10s$	$R_{\theta JA}$	78	110	$^\circ C/W$
Maximum Junction-to-Ambient ^{A,D} Steady-State		106	150	$^\circ C/W$
Maximum Junction-to-Lead Steady-State	$R_{\theta JL}$	64	80	$^\circ C/W$

N-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.5	1	1.5	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	20			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =3.4A T _J =125°C		46 73	60 88	mΩ
		V _{GS} =4.5V, I _D =3A		50	70	mΩ
		V _{GS} =2.5V, I _D =2A		62	90	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =3.4A		14		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.75	1	V
I _S	Maximum Body-Diode Continuous Current				1.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz	185	235	285	pF
C _{oss}	Output Capacitance		25	35	45	pF
C _{riss}	Reverse Transfer Capacitance		10	18	25	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.9	1.8	2.7	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =3.4A		10	12	nC
Q _{g(4.5V)}	Total Gate Charge		4.7	6	nC	
Q _{gs}	Gate Source Charge		0.95		nC	
Q _{gd}	Gate Drain Charge		1.6		nC	
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =4.4Ω, R _{GEN} =3Ω		3.5		ns
t _r	Turn-On Rise Time		1.5		ns	
t _{D(off)}	Turn-Off DelayTime		17.5		ns	
t _f	Turn-Off Fall Time		2.5		ns	
t _{rr}	Body Diode Reverse Recovery Time		I _F =3.4A, di/dt=100A/μs		8.5	12
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =3.4A, di/dt=100A/μs		2.55	4	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

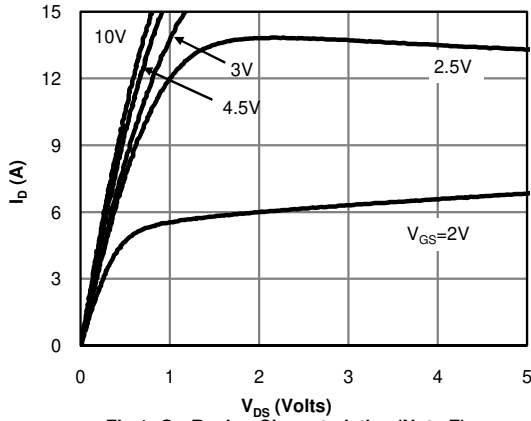


Fig 1: On-Region Characteristics (Note E)

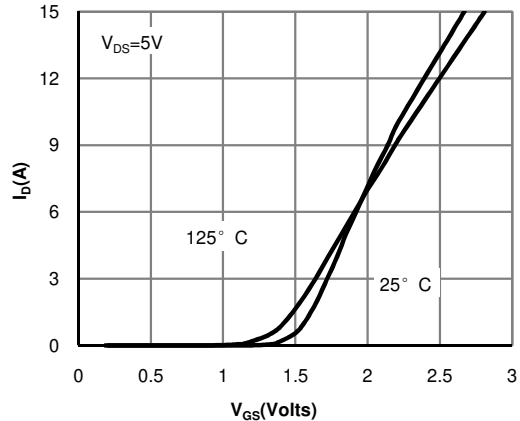


Figure 2: Transfer Characteristics (Note E)

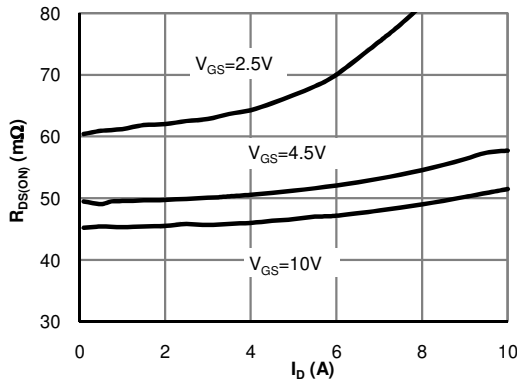


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

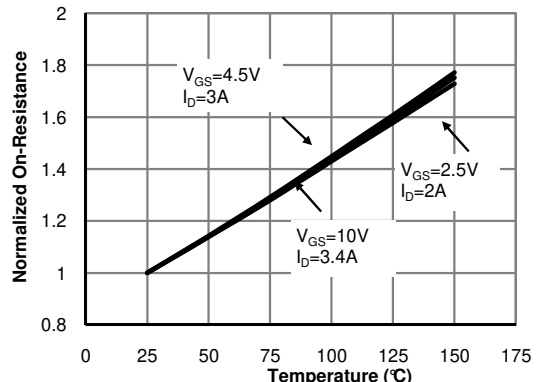


Figure 4: On-Resistance vs. Junction Temperature (Note E)

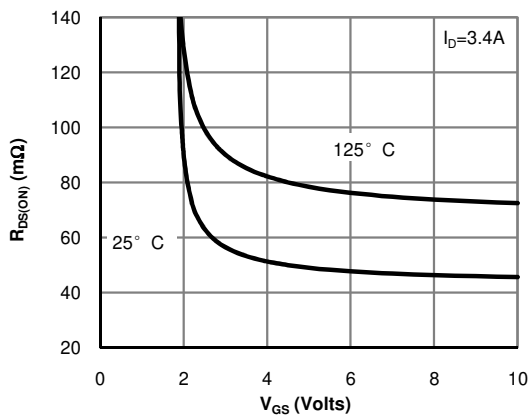


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

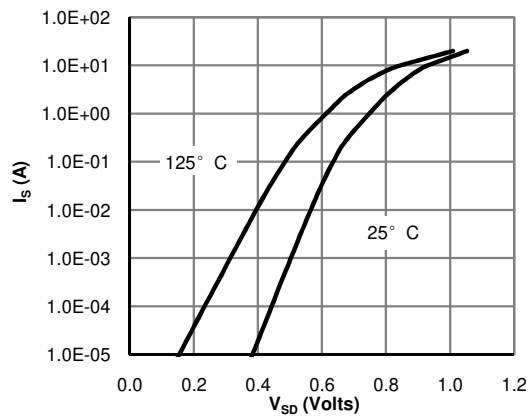


Figure 6: Body-Diode Characteristics (Note E)

N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

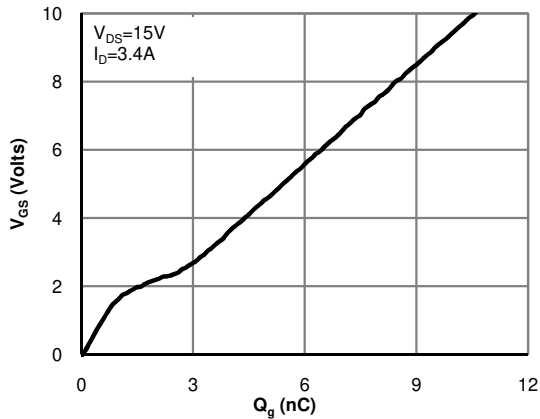


Figure 7: Gate-Charge Characteristics

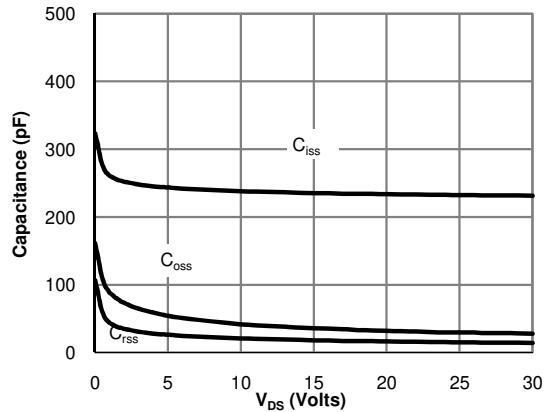


Figure 8: Capacitance Characteristics

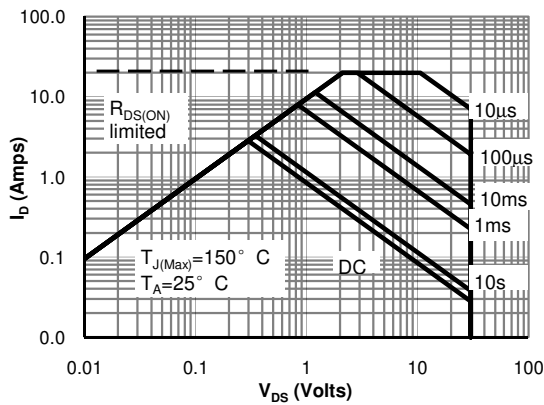


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

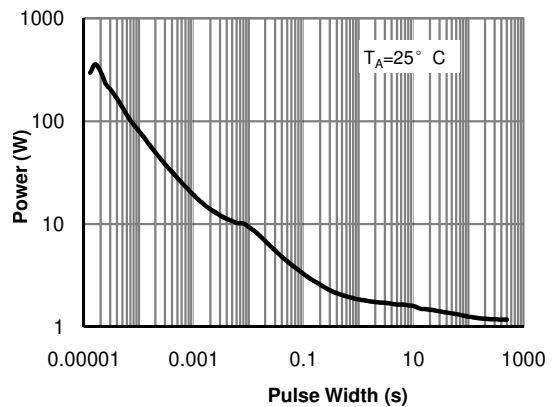


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

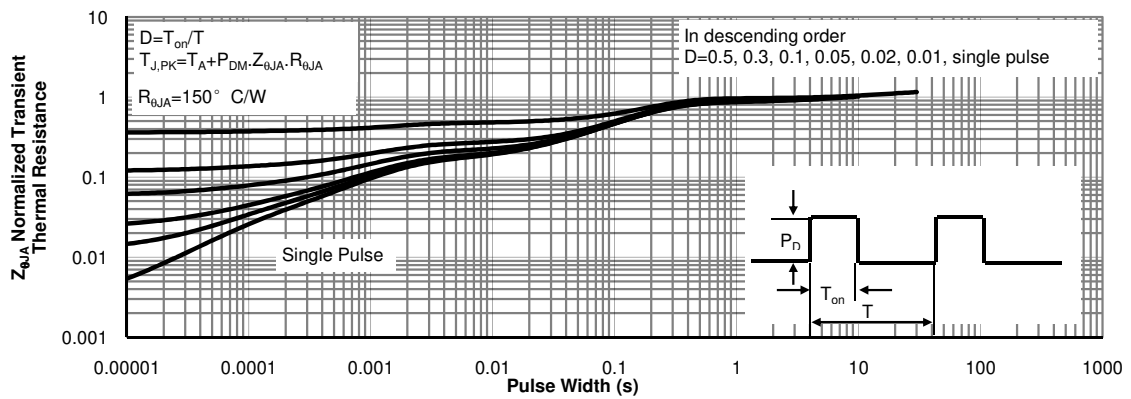
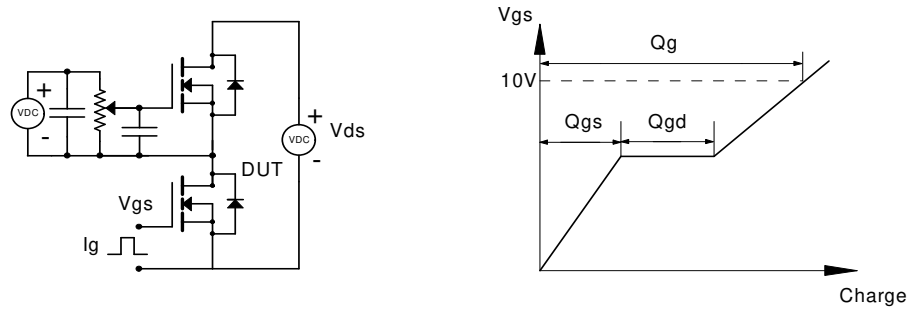
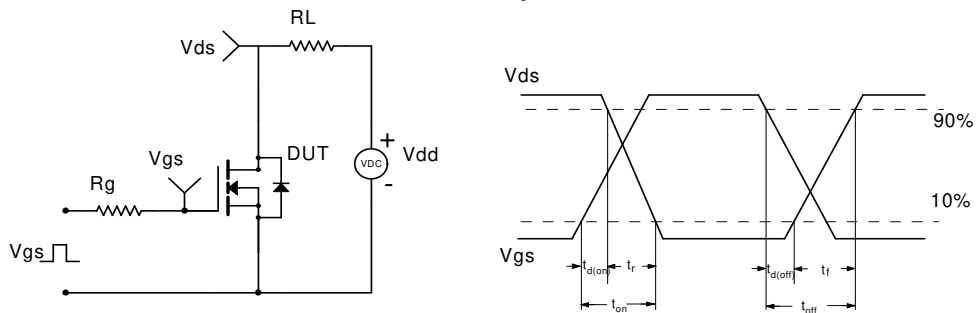


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

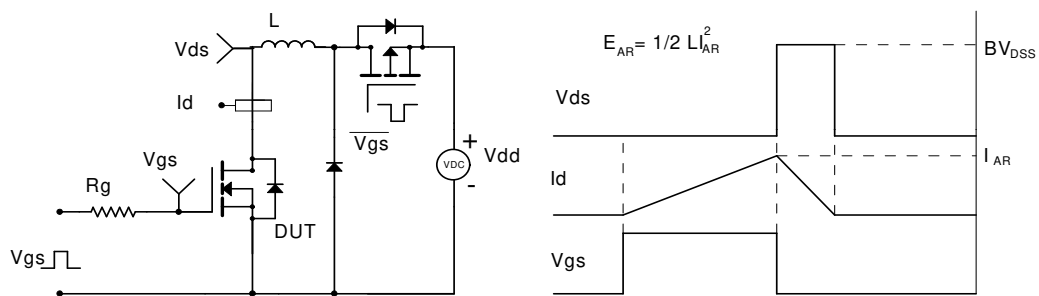
Gate Charge Test Circuit & Waveform



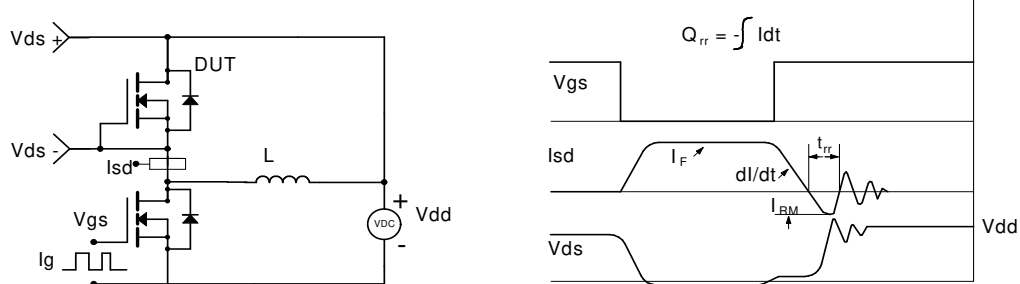
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-0.6	-1	-1.4	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-15			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-2.3A T _J =125°C		88 143	115 200	mΩ
		V _{GS} =-4.5V, I _D =-2A		103	150	mΩ
		V _{GS} =-2.5V, I _D =-1A		139	200	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-2.3A		8		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.78	-1	V
I _S	Maximum Body-Diode Continuous Current				-1.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz	205	260	315	pF
C _{oss}	Output Capacitance		25	37	50	pF
C _{riss}	Reverse Transfer Capacitance		10	20	30	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	4	8	12	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =-15V, I _D =-2.3A	4.5	5.9	7	nC
Q _g (4.5V)	Total Gate Charge		2	2.8	4	nC
Q _{gs}	Gate Source Charge			0.7		nC
Q _{gd}	Gate Drain Charge			1		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =-15V, R _L =6Ω, R _{GEN} =3Ω		6		ns
t _r	Turn-On Rise Time			3.5		ns
t _{D(off)}	Turn-Off DelayTime			20		ns
t _f	Turn-Off Fall Time			5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-2.3A, dI/dt=100A/μs		11.5	15	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-2.3A, dI/dt=100A/μs		4.5	6	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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P-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

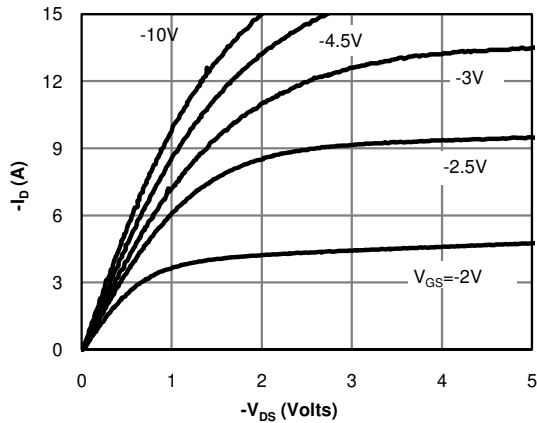


Fig 1: On-Region Characteristics (Note E)

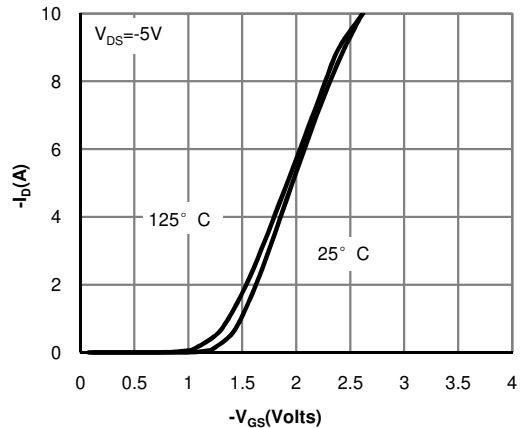


Figure 2: Transfer Characteristics (Note E)

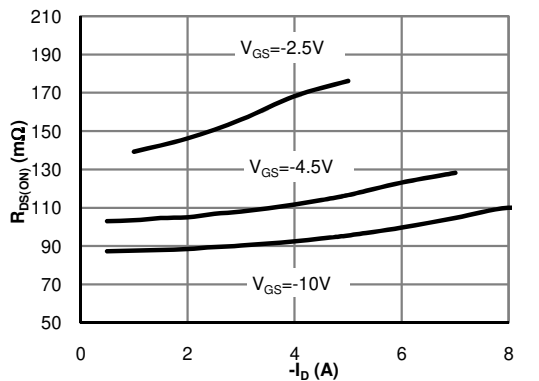


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

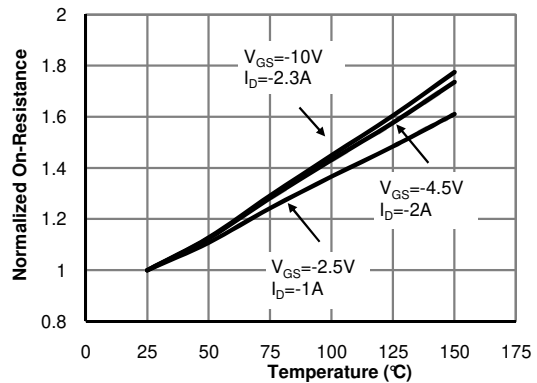


Figure 4: On-Resistance vs. Junction Temperature (Note E)

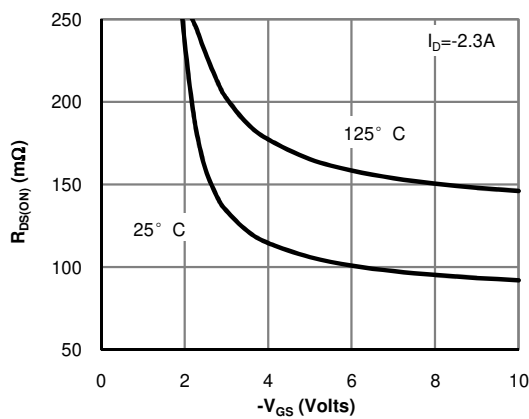


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

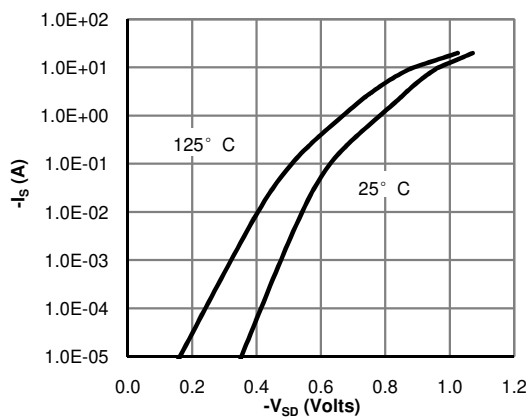


Figure 6: Body-Diode Characteristics (Note E)

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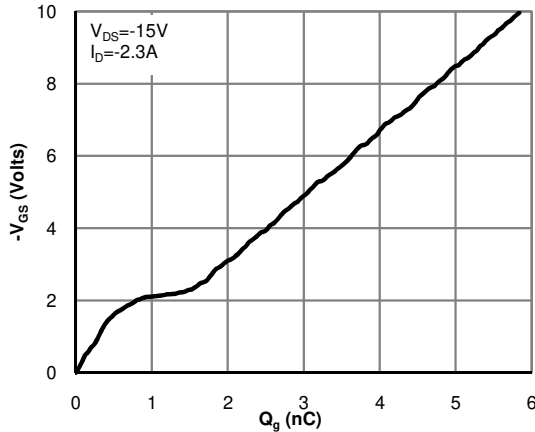


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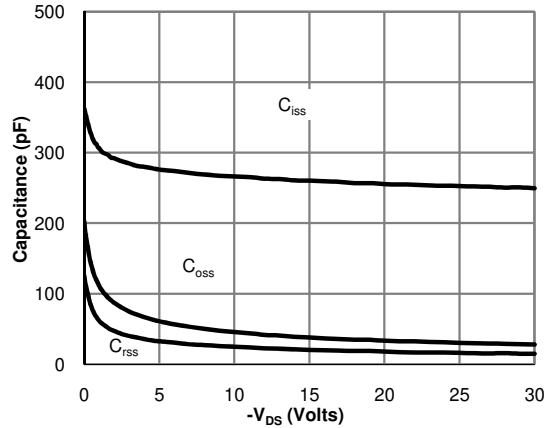


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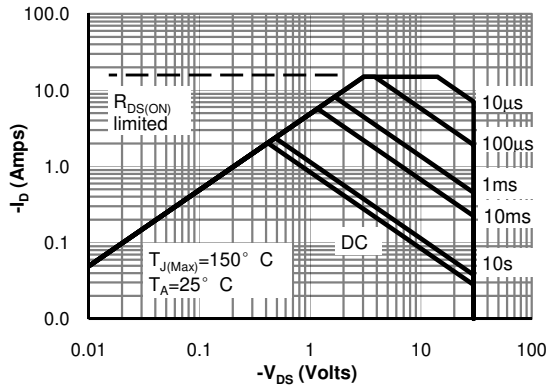


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

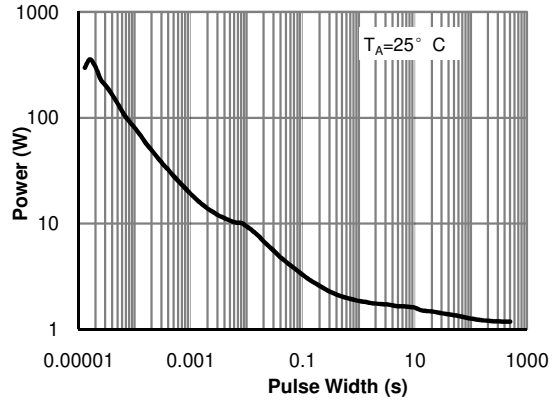


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

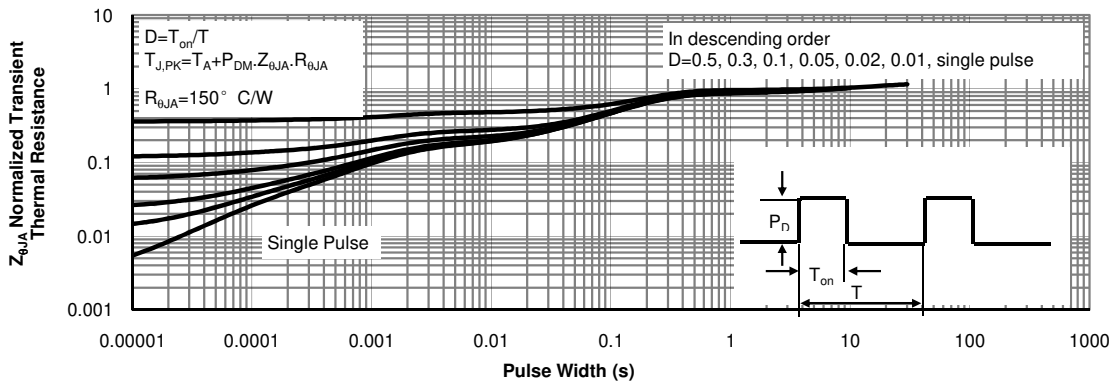
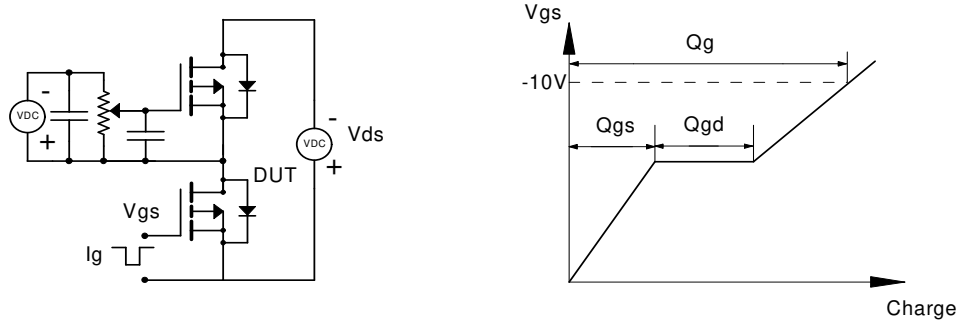
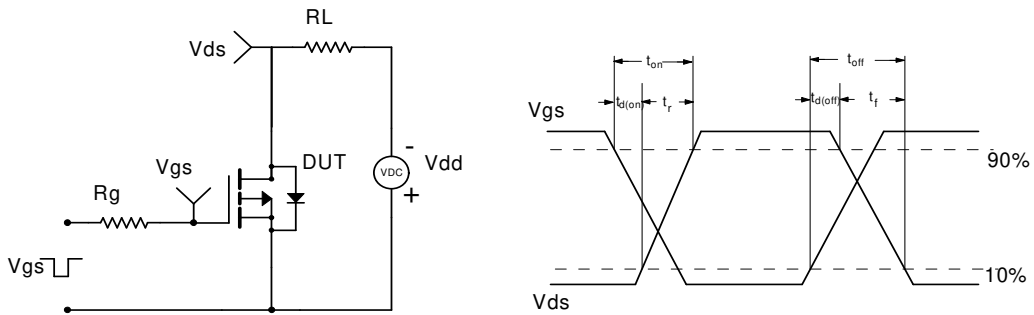


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

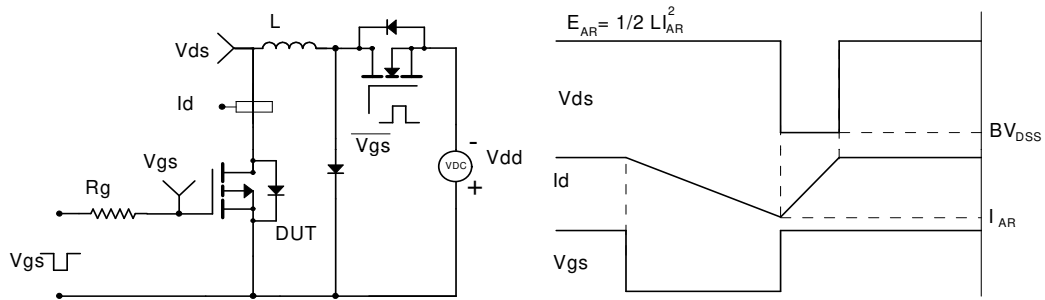
Gate Charge Test Circuit & Waveform



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