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AO8807L

Dual P-Channel Enhancement Mode Field Effect Transistor

General Description

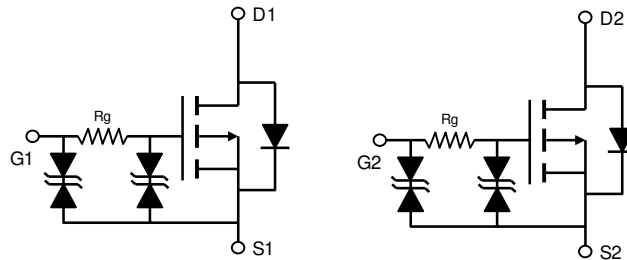
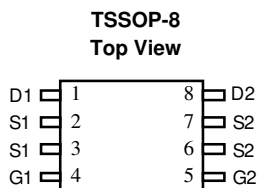
The AO8807L uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch.

- RoHS Compliant
- Halogen Free

Features

- V_{DS} (V) = -12V
- I_D = -6.5 A (V_{GS} = -4.5V)
- $R_{DS(ON)} < 20m\Omega$ (V_{GS} = -4.5V)
- $R_{DS(ON)} < 24m\Omega$ (V_{GS} = -2.5V)
- $R_{DS(ON)} < 30m\Omega$ (V_{GS} = -1.8V)

ESD Protected!



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-12	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current	I_D	$T_A=25^\circ\text{C}$	-6.5
		$T_A=70^\circ\text{C}$	-5
Pulsed Drain Current ^C	I_{DM}	-60	A
Power Dissipation ^B	P_D	$T_A=25^\circ\text{C}$	1.4
		$T_A=70^\circ\text{C}$	0.9
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	73	90	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{AD}		96	125	$^\circ\text{C/W}$
Maximum Junction-to-Lead	$R_{\theta JL}$	63	75	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-12			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-12V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±8V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-0.35	-0.53	-0.85	
I _{D(ON)}	On state drain current	V _{GS} =-4.5V, V _{DS} =-5V	-60			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-4.5V, I _D =-6.5A T _J =125°C		16 23	20 28	mΩ
		V _{GS} =-2.5V, I _D =-6A		19	24	mΩ
		V _{GS} =-1.8V, I _D =-5.5A		23	30	mΩ
		V _{GS} =-1.5V, I _D =-5A		28	36	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-6.5A		45		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.56	-1	V
I _S	Maximum Body-Diode Continuous Current				-1.4	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-6V, f=1MHz		1740	2100	pF
C _{oss}	Output Capacitance		334		pF	
C _{rss}	Reverse Transfer Capacitance		200		pF	
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.3	1.7	kΩ
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =-4.5V, V _{DS} =-6V, I _D =-6.5A		19	23	nC
Q _{gs}	Gate Source Charge		4.5		nC	
Q _{gd}	Gate Drain Charge		5.3		nC	
t _{D(on)}	Turn-On Delay Time	V _{GS} =-4.5V, V _{DS} =-6V, R _L =0.9Ω, R _{GEN} =3Ω		240		ns
t _r	Turn-On Rise Time		580		ns	
t _{D(off)}	Turn-Off Delay Time		7		μs	
t _f	Turn-Off Fall Time		4.2		μs	
t _{rr}	Body Diode Reverse Recovery Time	I _F =-6.5A, dI/dt=100A/μs		22	27	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-6.5A, dI/dt=100A/μs		17		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: The power dissipation P_D is based on T_{J(MAX)}=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

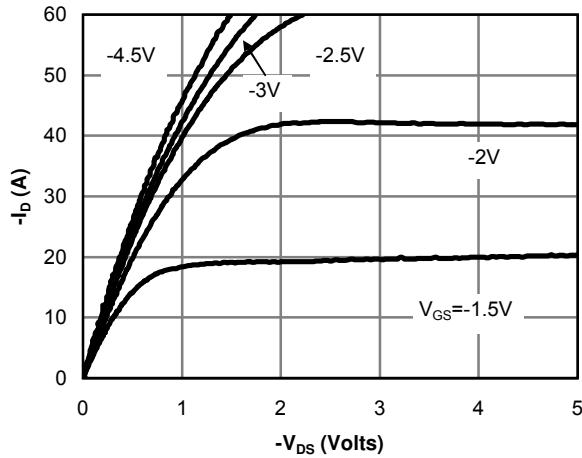


Figure 1: On-Region Characteristics(Note E)

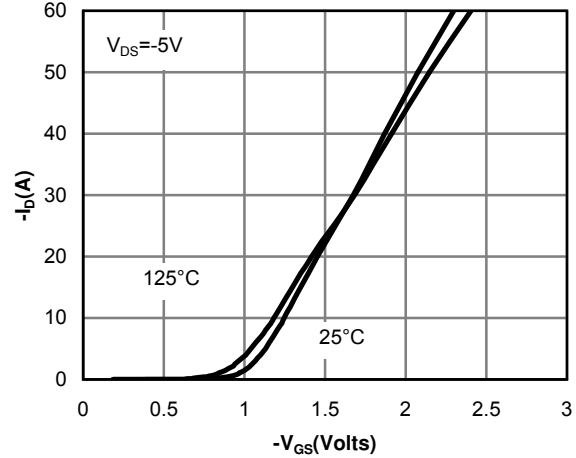


Figure 2: Transfer Characteristics(Note E)

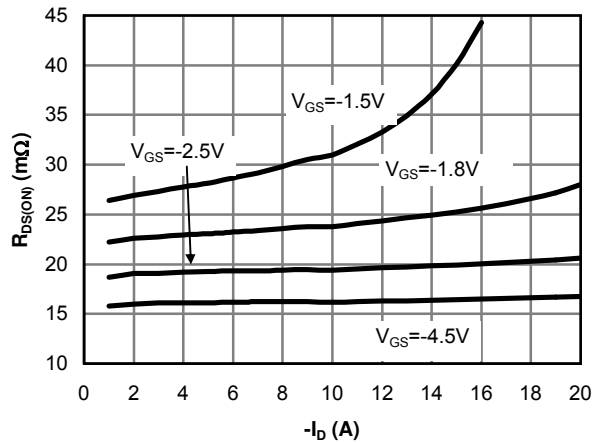


Figure 3: On-Resistance vs. Drain Current and Gate Voltage(Note E)

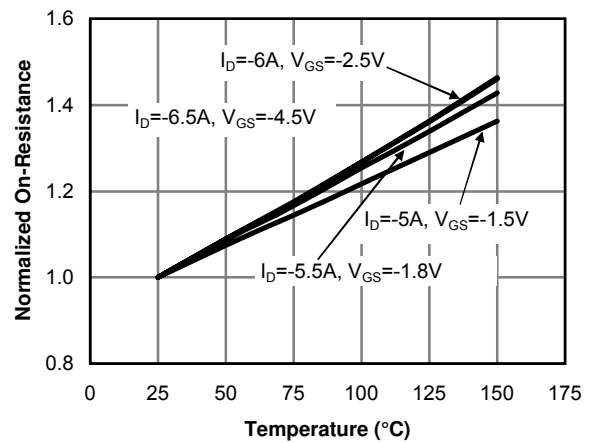


Figure 4: On-Resistance vs. Junction Temperature(Note E)

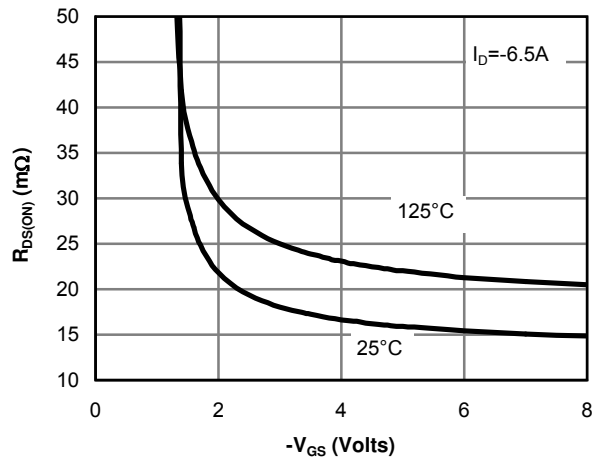


Figure 5: On-Resistance vs. Gate-Source Voltage(Note E)

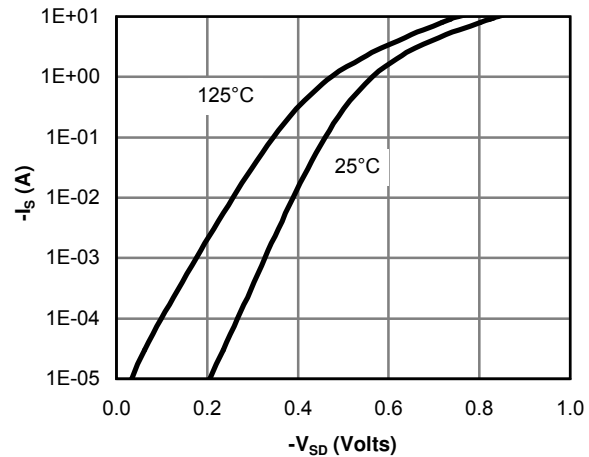


Figure 6: Body-Diode Characteristics(Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

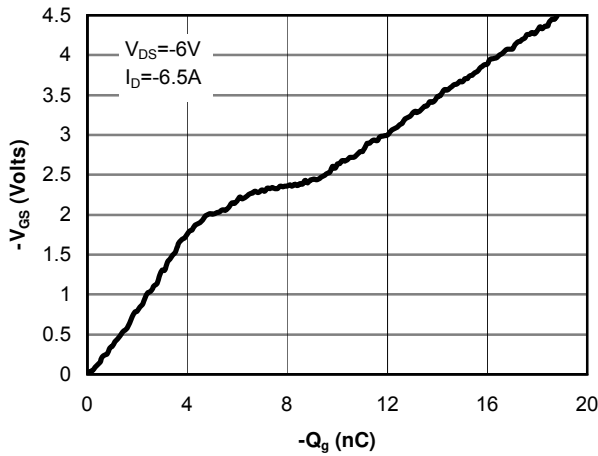


Figure 7: Gate-Charge Characteristics

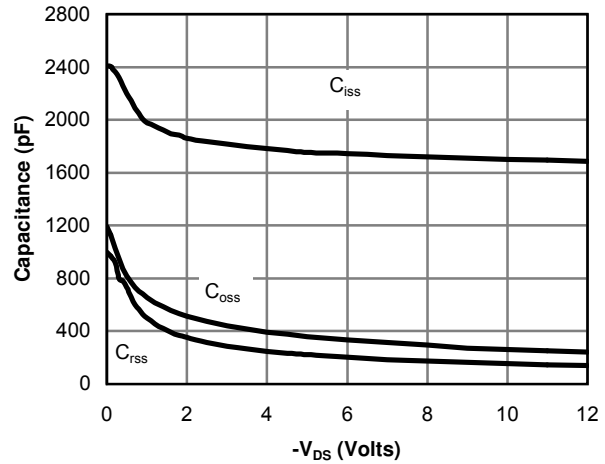


Figure 8: Capacitance Characteristics

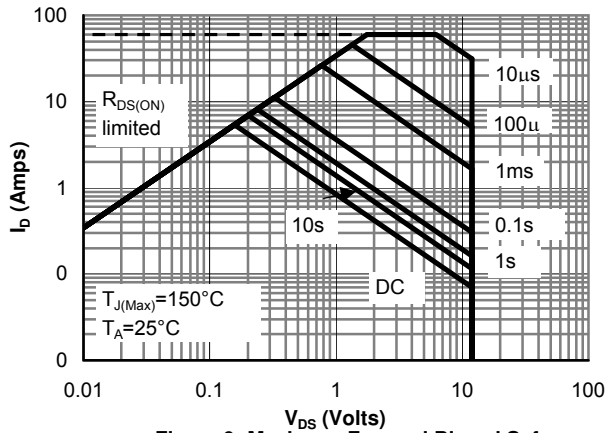


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

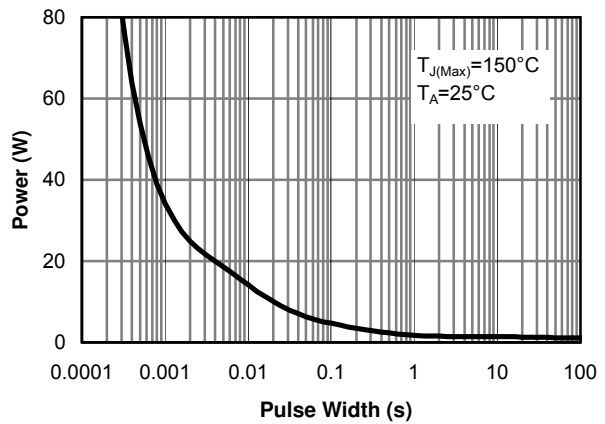


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

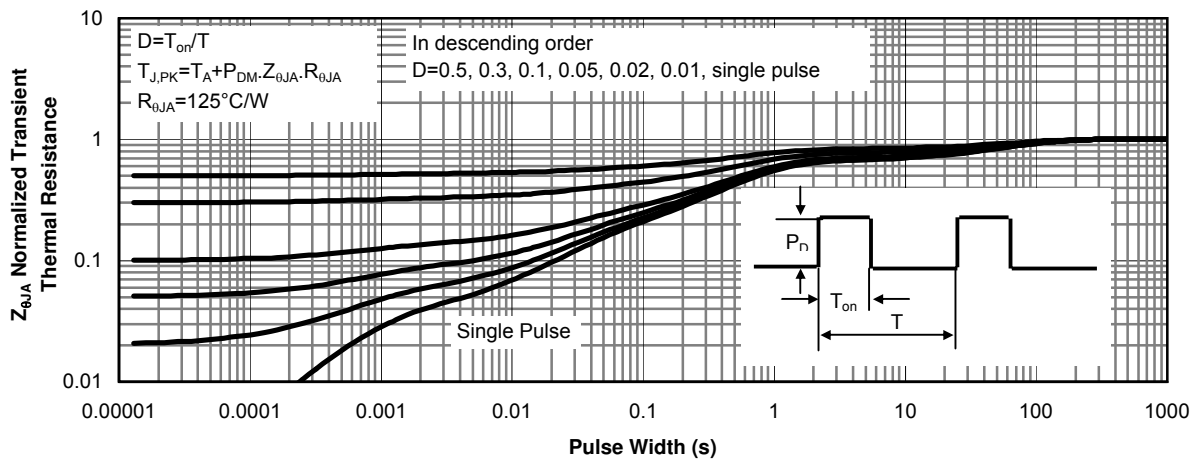
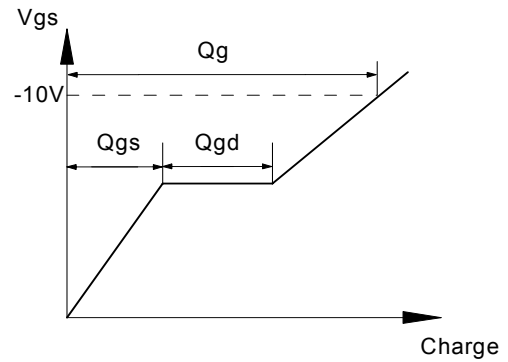
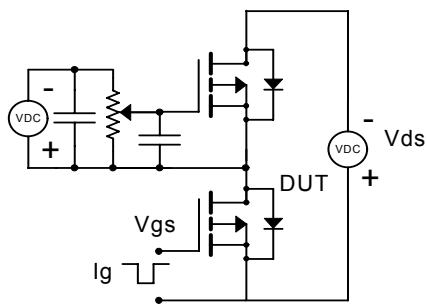
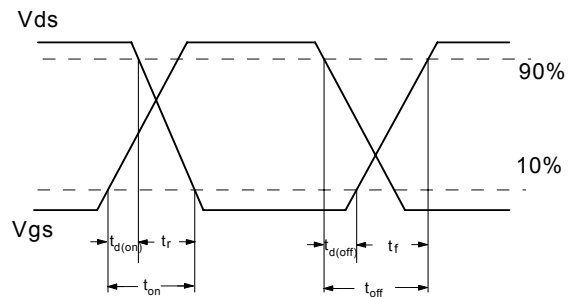
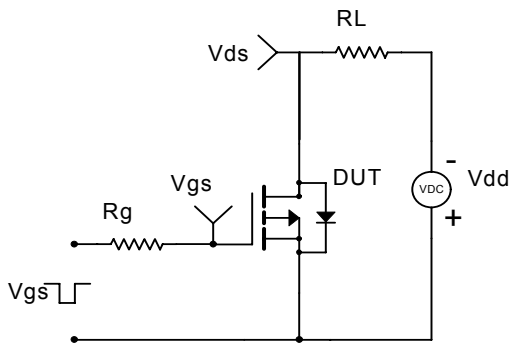


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

