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With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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AOL1702
N-Channel Enhancement Mode Field Effect Transistor
SRFET™
General Description

The AOL1702 uses advanced trench technology with a monolithically integrated Schottky diode to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a low side FET in SMPS, load switching and general purpose applications.

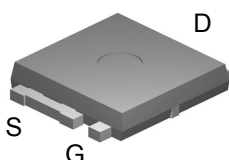
- RoHS Compliant
- Halogen and Antimony Free Green Device*

Features

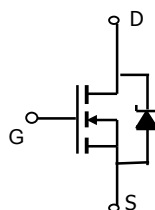
- V_{DS} (V) = 30V
- $I_D = 70A$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 5.8m\Omega$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 7.2m\Omega$ ($V_{GS} = 4.5V$)

- UIS Tested
- $R_g, C_{iss}, C_{oss}, C_{rss}$ Tested

Ultra SO-8™ Top View



Bottom tab connected to drain


SRFET™

Soft Recovery MOSFET:
Integrated Schottky Diode

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^B	$T_C=25^\circ C^G$	70	A
	$T_C=100^\circ C$	52	
Pulsed Drain Current ^C	I_{DM}	100	
Continuous Drain Current ^A	$T_A=25^\circ C$	14	A
	$T_A=70^\circ C$	11	
Avalanche Current ^C	I_{AR}	30	A
Repetitive avalanche energy $L=0.3mH^C$	E_{AR}	135	mJ
Power Dissipation ^B	$T_C=25^\circ C$	58	W
	$T_C=100^\circ C$	29	
Power Dissipation ^A	$T_A=25^\circ C$	2.1	W
	$T_A=70^\circ C$	1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	20	25	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	50	
Maximum Junction-to-Case ^D	$R_{\theta JC}$	2.1	2.6	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
B _V DSS	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V T _J =125°C			0.1 20	mA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±12V			0.1	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1.5	1.85	2.4	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	100			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		4.8 7.2	5.8 9.0	mΩ
		V _{GS} =4.5V, I _D =20A		5.9	7.2	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		110		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.37	0.5	V
I _S	Maximum Body-Diode + Schottky Continuous Current				55	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		4000	5000	pF
C _{oss}	Output Capacitance			520		pF
C _{rss}	Reverse Transfer Capacitance			217		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		0.6	0.9	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		59	77	
Q _{g(4.5V)}	Total Gate Charge			27		nC
Q _{gs}	Gate Source Charge			12		nC
Q _{gd}	Gate Drain Charge			11		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		9		ns
t _r	Turn-On Rise Time			9		ns
t _{D(off)}	Turn-Off DelayTime			37		ns
t _f	Turn-Off Fall Time			8		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=300A/μs		16		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=300A/μs		22		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The power dissipation P_{DSM} and current rating IDSM are based on T_{J(MAX)}=150°C, using t ≤ 10s junction-to-ambient thermal resistance. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

* This device is guaranteed green after date code 8P11 (June 1ST 2008)

Rev1: July 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

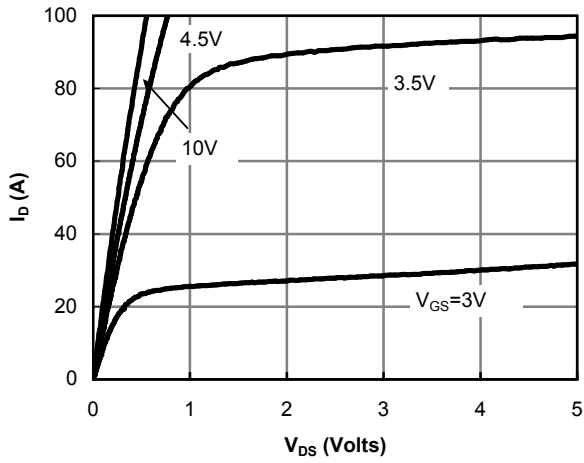


Figure 1: On-Region Characteristics

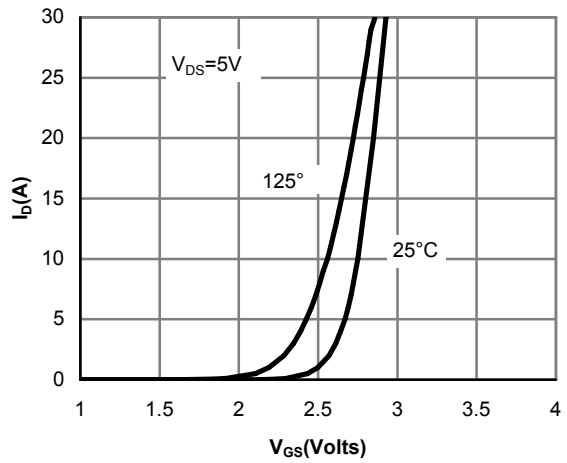


Figure 2: Transfer Characteristics

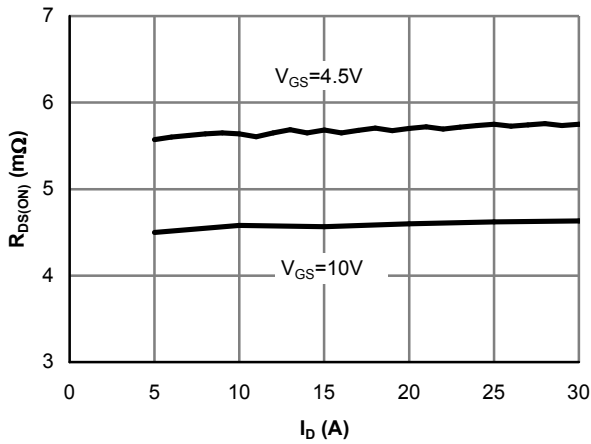


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

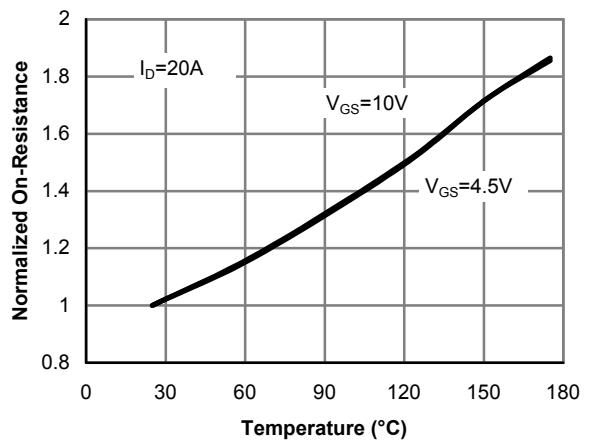


Figure 4: On-Resistance vs. Junction Temperature

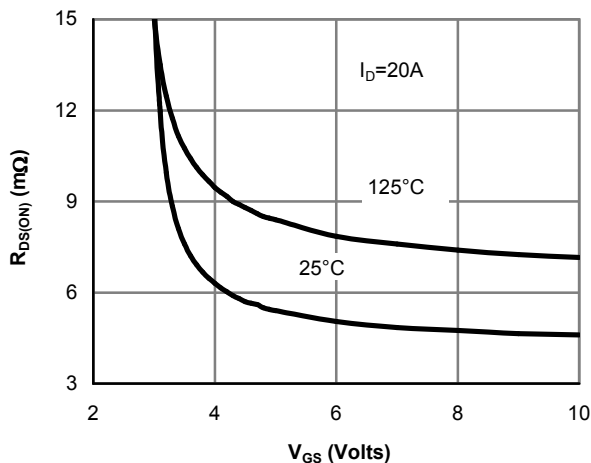


Figure 5: On-Resistance vs. Gate-Source Voltage

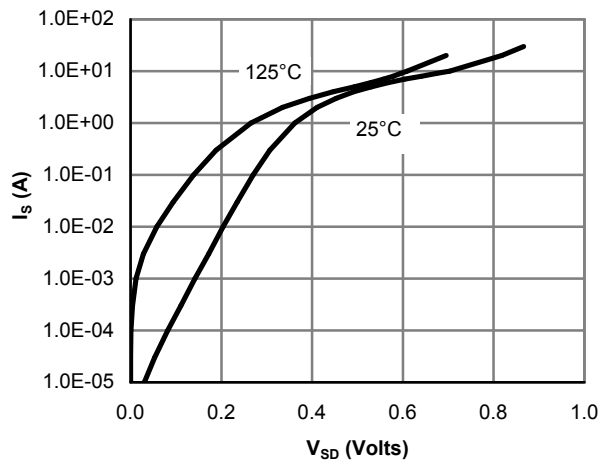


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

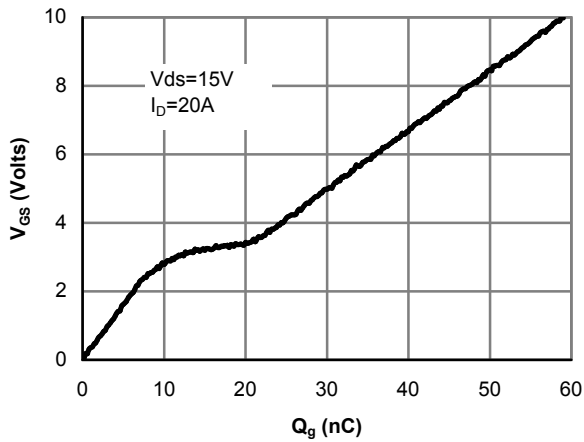


Figure 7: Gate-Charge Characteristics

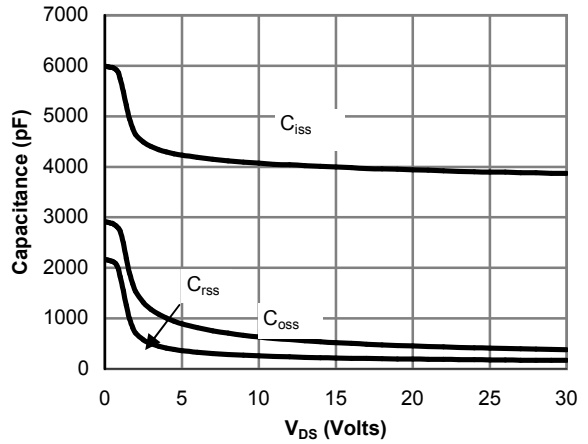


Figure 8: Capacitance Characteristics

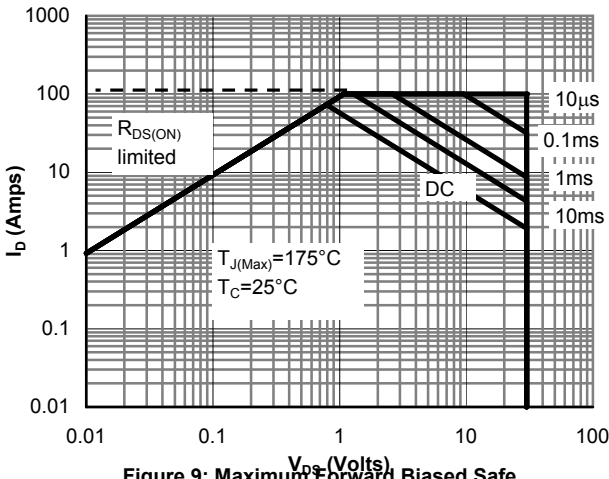


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

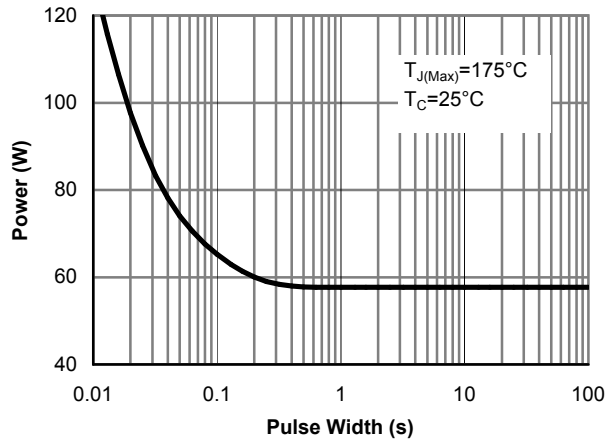


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

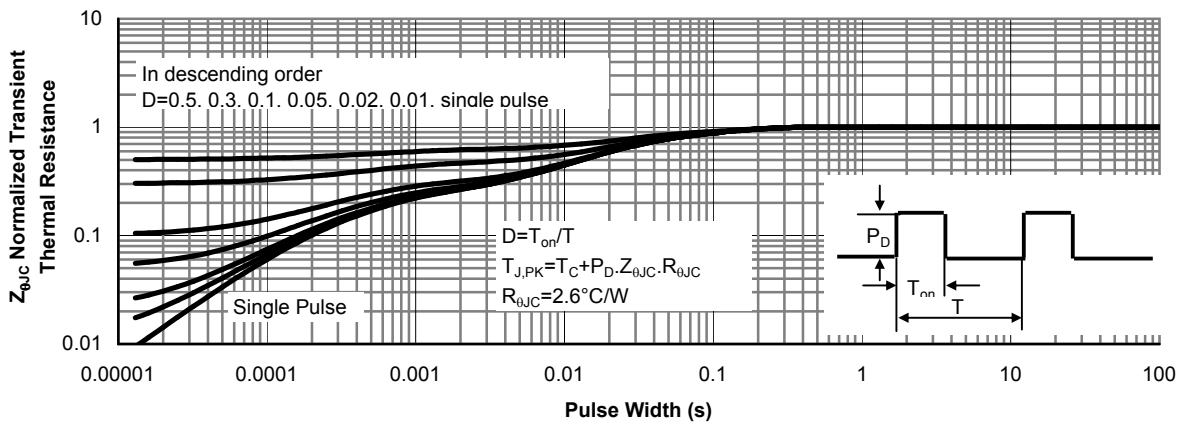


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

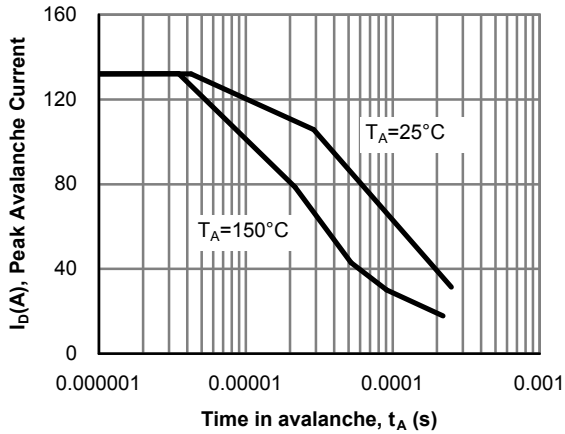


Figure 12: Single Pulse Avalanche capability

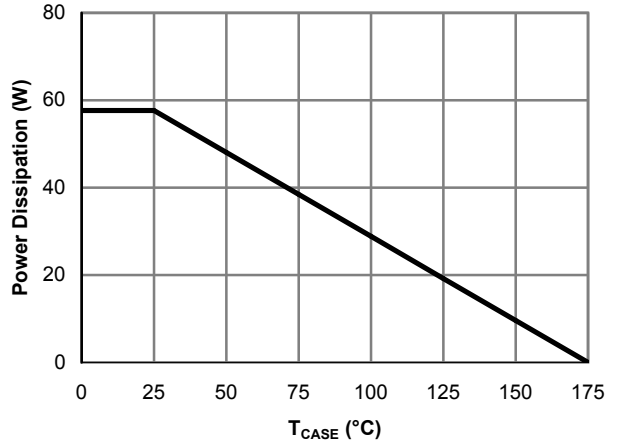


Figure 13: Power De-rating (Note B)

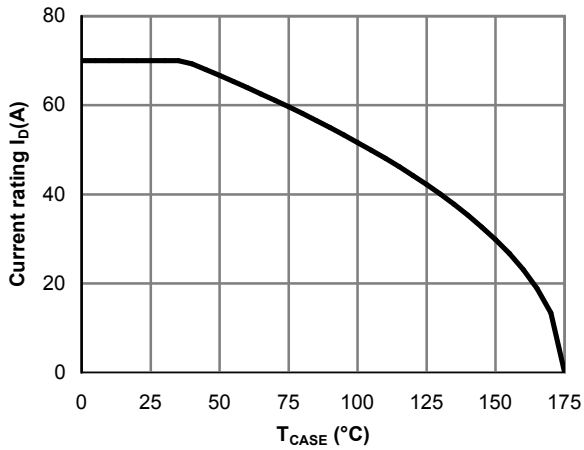


Figure 14: Current De-rating (Note B)

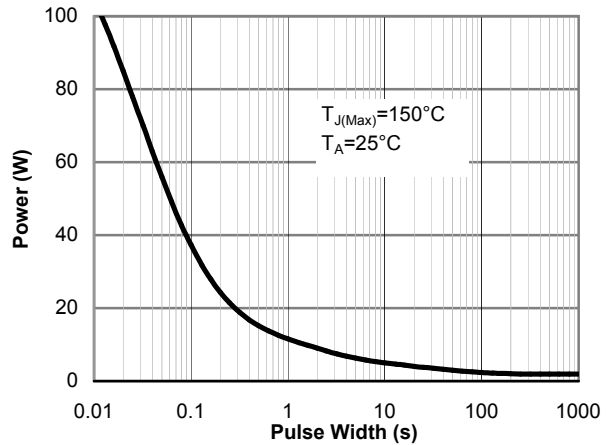


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

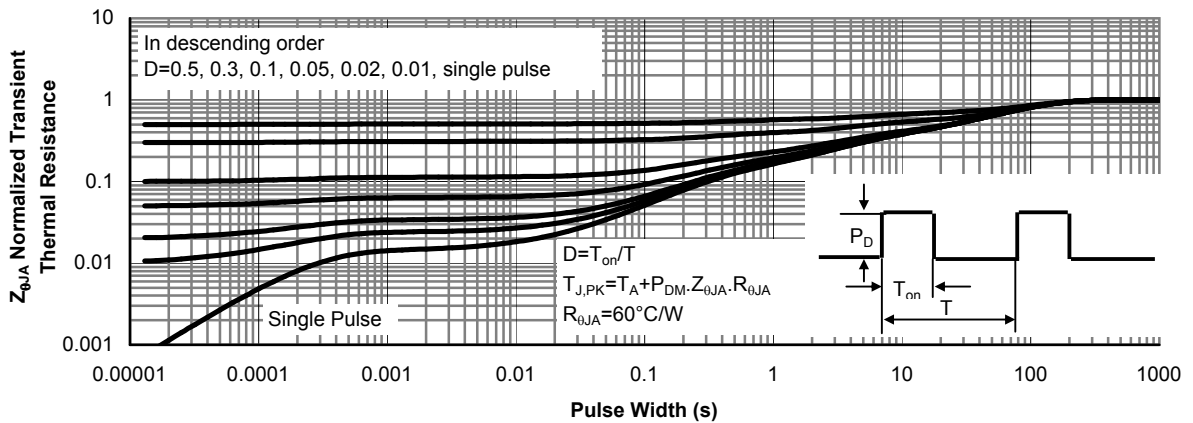


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

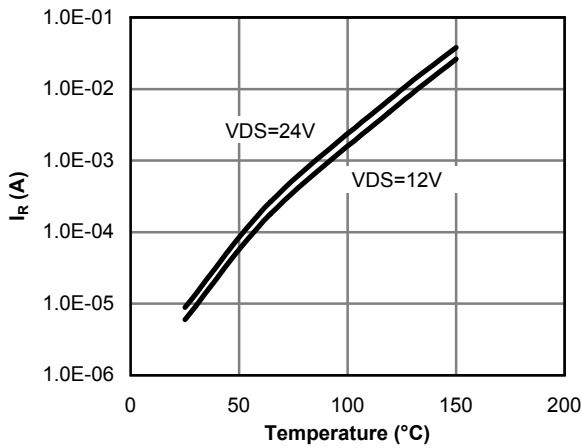


Figure 17: Diode Reverse Leakage Current vs. Junction Temperature

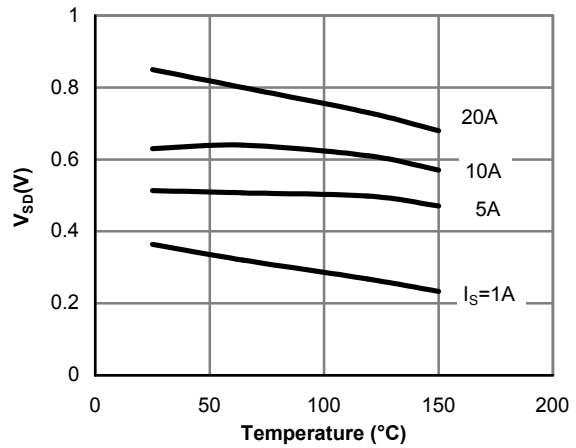


Figure 18: Diode Forward voltage vs. Junction Temperature

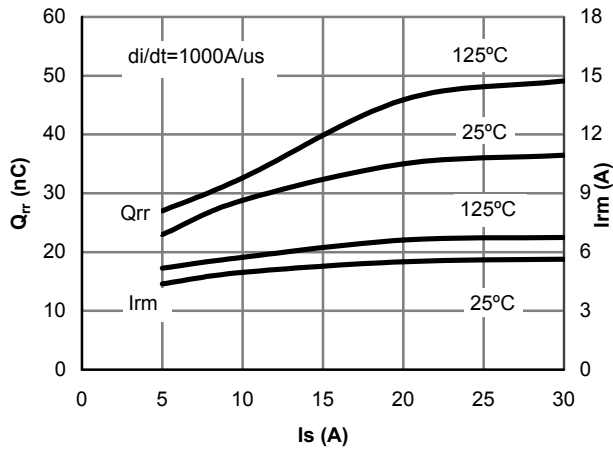


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

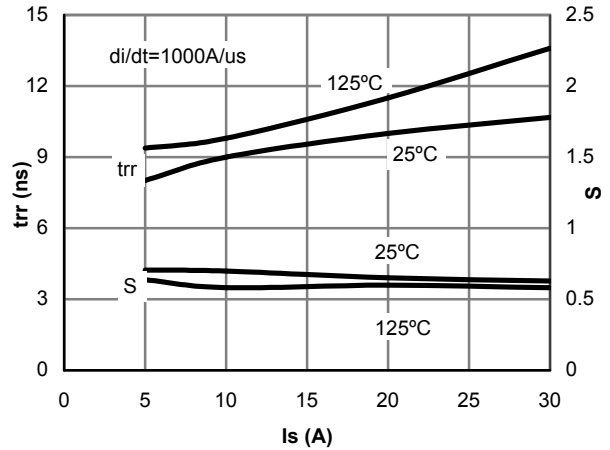


Figure 20: Diode Reverse Recovery Time and Soft Coefficient vs. Conduction Current

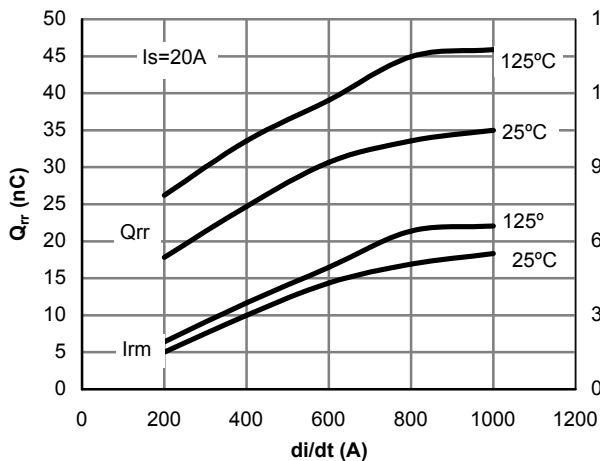


Figure 21: Diode Reverse Recovery Charge and Peak Current vs. di/dt

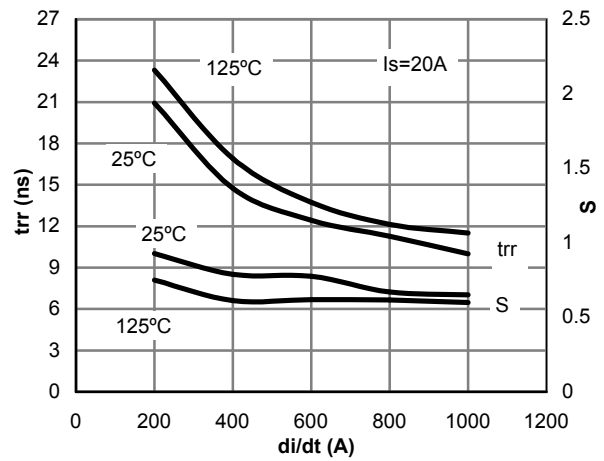
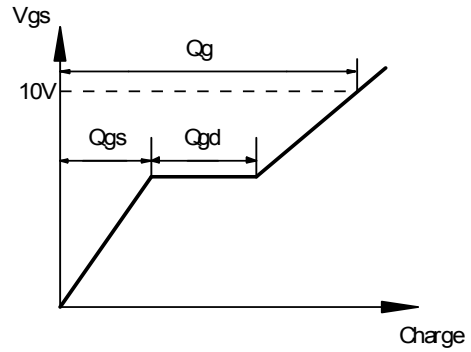
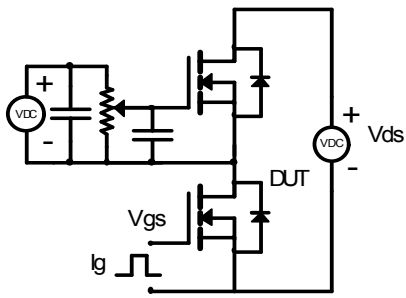
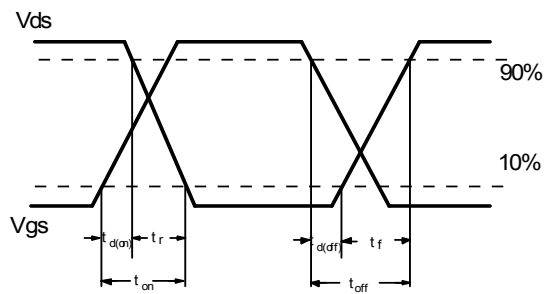
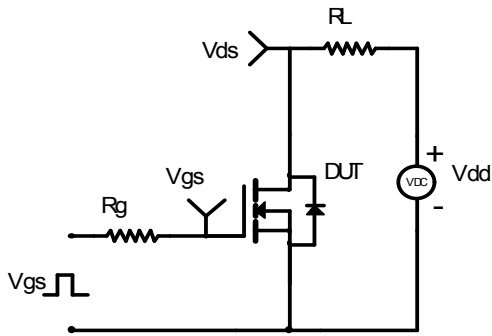


Figure 22: Diode Reverse Recovery Time and Soft Coefficient vs. di/dt

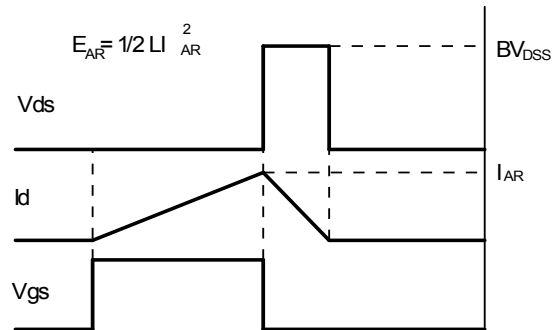
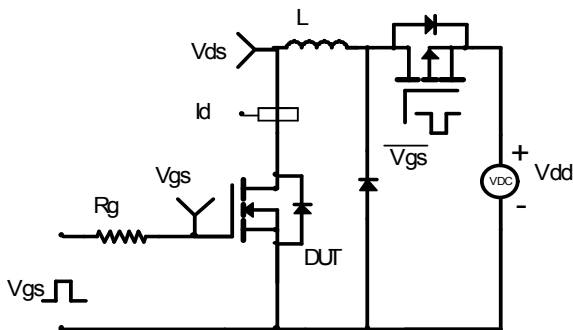
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

