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With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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General Description

- Trench Power AlphaSGT™ technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- ESD protected

Applications

- High efficiency power supply
- Secondary synchronous rectifier

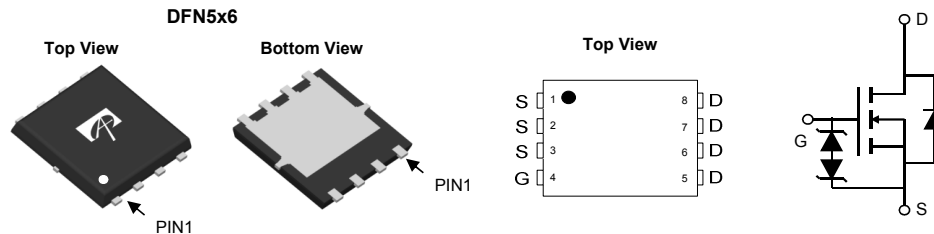
Product Summary

V_{DS}	60V
I_D (at $V_{GS}=10V$)	40A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 6.2m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 8.5m Ω

Typical ESD protection

HBM Class 2

- 100% UIS Tested
- 100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON6262E	DFN 5x6	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	40	A
$T_C=25^\circ\text{C}$		40	
Pulsed Drain Current ^C	I_{DM}	145	
Continuous Drain Current	I_{DSM}	23.5	A
$T_A=25^\circ\text{C}$		18.5	
$T_A=70^\circ\text{C}$			
Avalanche Current ^C	I_{AS}	23	A
Avalanche energy $L=0.3\text{mH}$ ^C	E_{AS}	79	mJ
V_{DS} Spike ^I	V_{SPIKE}	72	V
Power Dissipation ^B	P_D	48	W
$T_C=25^\circ\text{C}$		19	
$T_C=100^\circ\text{C}$			
Power Dissipation ^A	P_{DSM}	6.2	W
$T_A=25^\circ\text{C}$		4.0	
$T_A=70^\circ\text{C}$			
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A $t \leq 10\text{s}$	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A,D} Steady-State		40	50	$^\circ\text{C/W}$
Maximum Junction-to-Case Steady-State	$R_{\theta JC}$	2.1	2.6	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	1.65	2.2	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		4.8	6.2	mΩ
		V _{GS} =4.5V, I _D =20A		7.8	10	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		75		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current ^G				40	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, f=1MHz		1650		pF
C _{oss}	Output Capacitance			520		pF
C _{rss}	Reverse Transfer Capacitance			52		pF
R _g	Gate resistance	f=1MHz	0.6	1.3	2.0	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =30V, I _D =20A		30	45	nC
Q _{g(4.5V)}	Total Gate Charge			15	25	nC
Q _{gs}	Gate Source Charge			3.5		nC
Q _{gd}	Gate Drain Charge			6.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =30V, R _L =1.5Ω, R _{GEN} =3Ω		6		ns
t _r	Turn-On Rise Time			5		ns
t _{D(off)}	Turn-Off DelayTime			29		ns
t _f	Turn-Off Fall Time			7		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=500A/μs		19		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=500A/μs		60		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

I. The spike duty cycle 5% max, limited by junction temperature T_{J(MAX)}=125° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

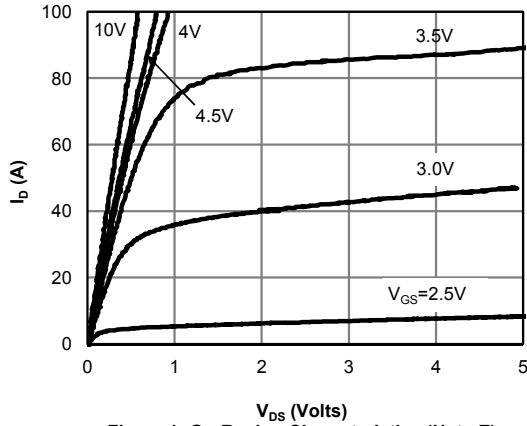


Figure 1: On-Region Characteristics (Note E)

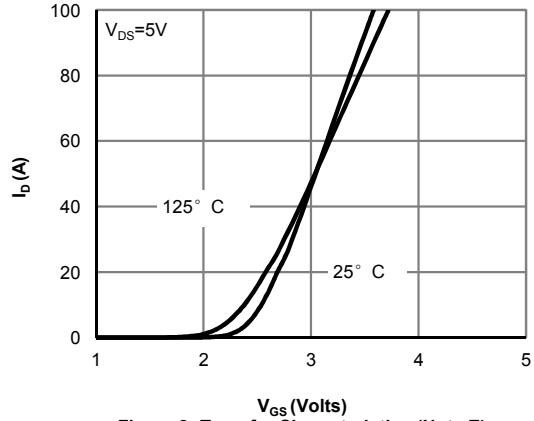


Figure 2: Transfer Characteristics (Note E)

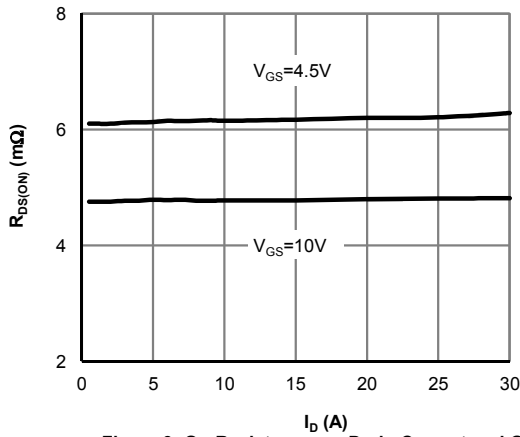


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

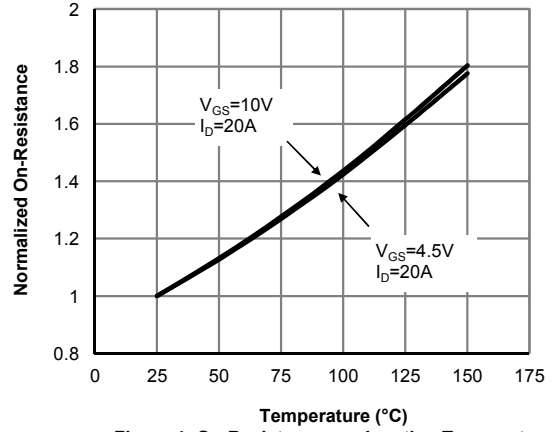


Figure 4: On-Resistance vs. Junction Temperature (Note E)

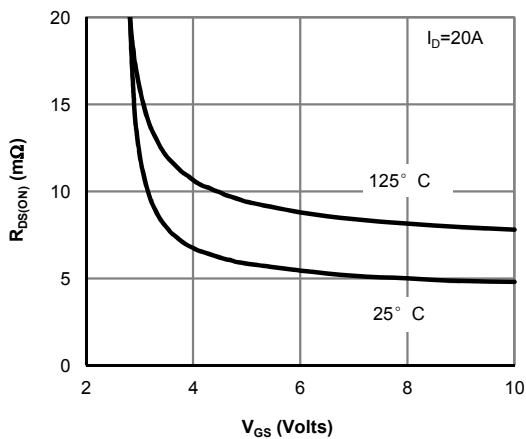


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

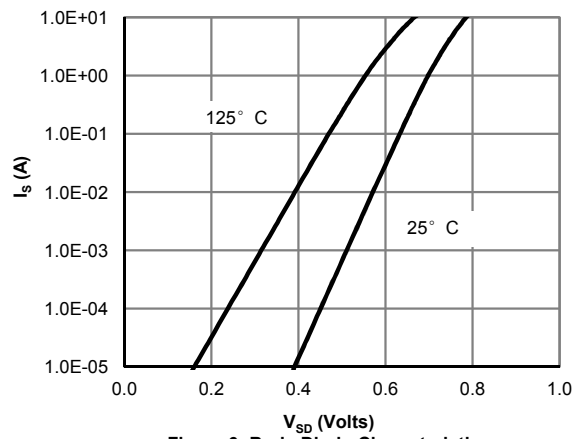


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

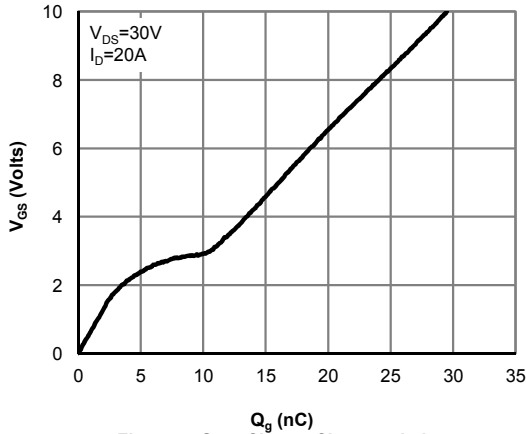


Figure 7: Gate-Charge Characteristics

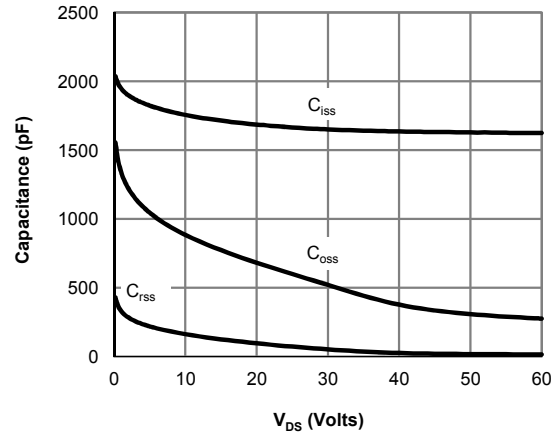


Figure 8: Capacitance Characteristics

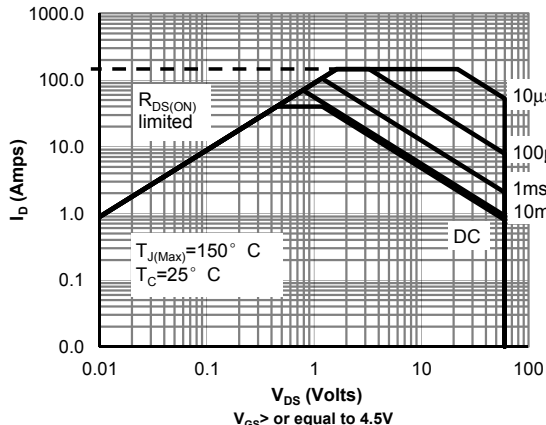


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

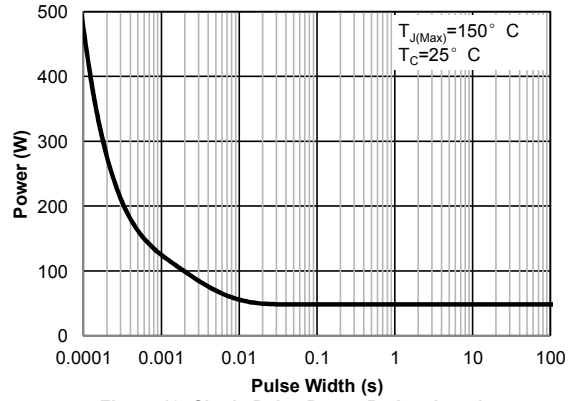


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

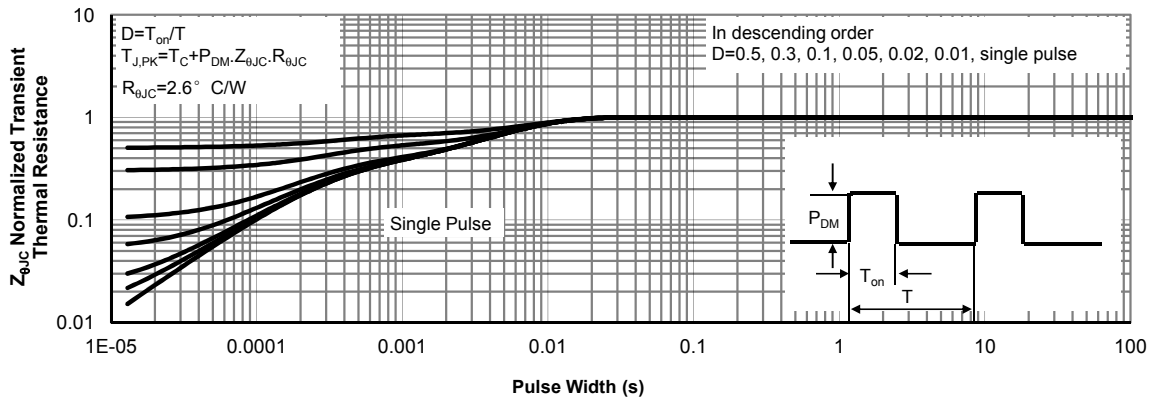


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

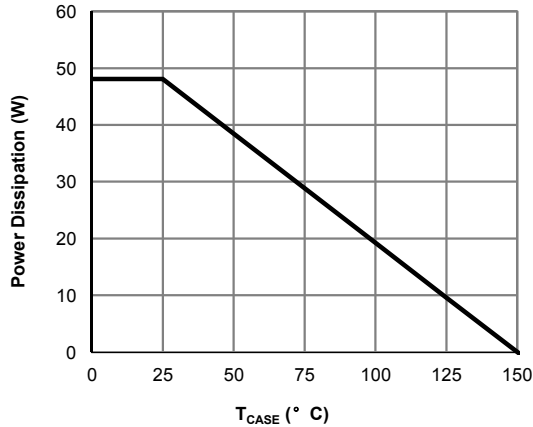


Figure 12: Power De-rating (Note F)

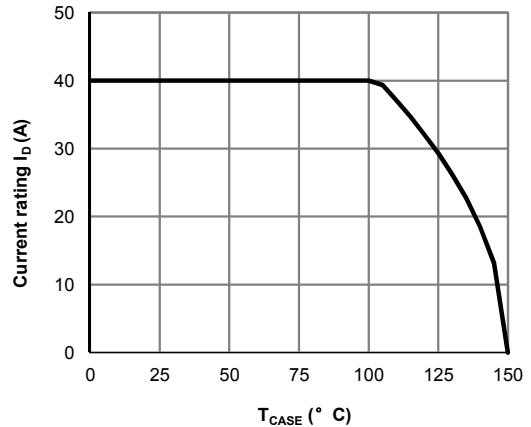


Figure 13: Current De-rating (Note F)

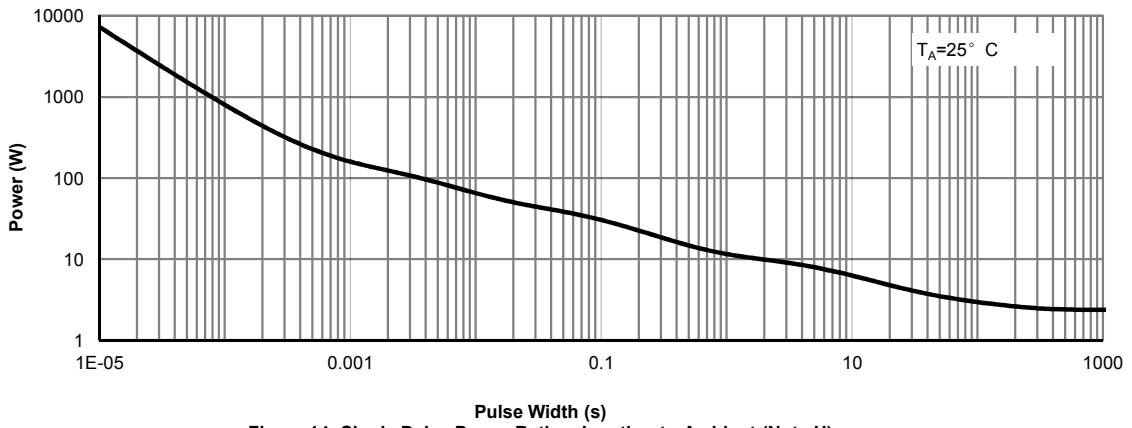


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

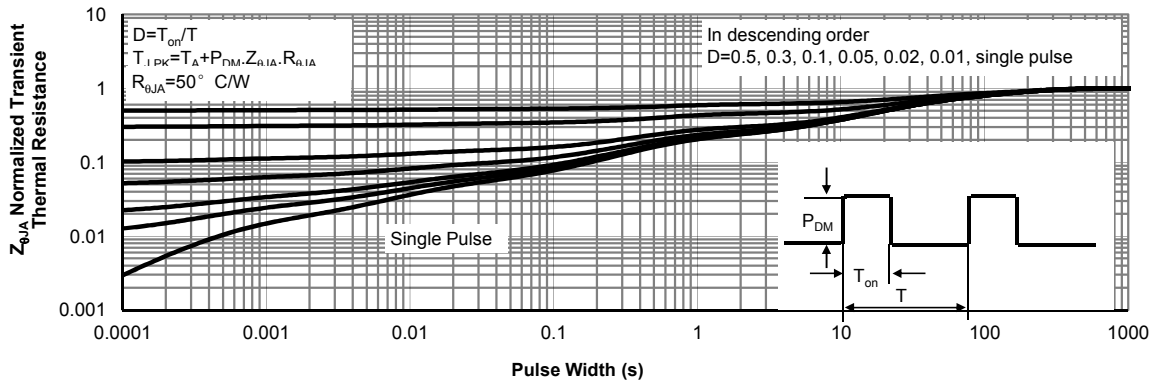


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

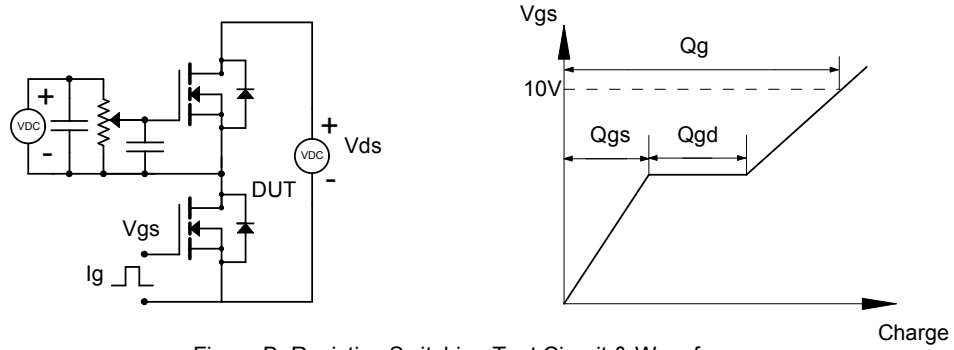


Figure B: Resistive Switching Test Circuit & Waveforms

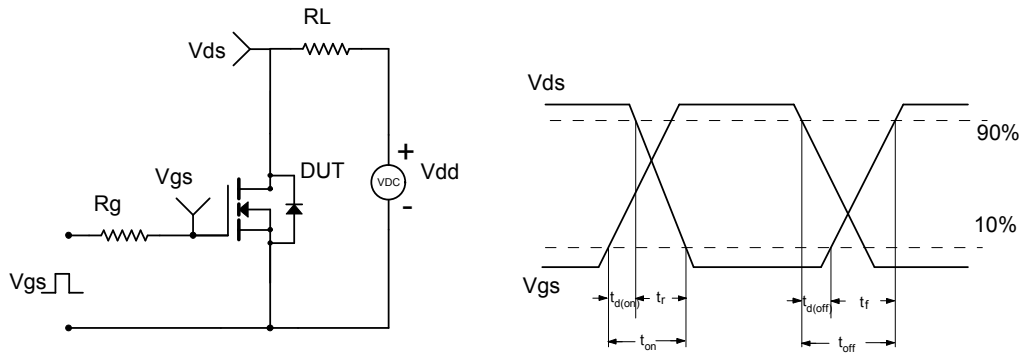


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

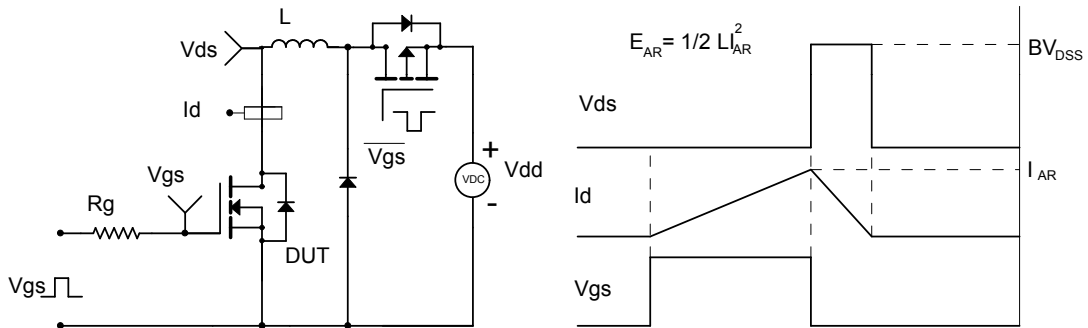


Figure D: Diode Recovery Test Circuit & Waveforms

