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Halogen-free

CompactFlash Series 5

Specifications for Industrial CompactFlash Card

March 14, 2016

Version 1.4



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Features:

- **CompactFlash Association Specification Revision 4.1 Standard Interface**
 - 512 bytes per sector
 - ATA command set compatible
 - ATA transfer mode supports:
 - PIO Mode 6
 - Multiword DMA Mode 4
 - Ultra DMA Mode 5
 - PCMCIA UDMA Mode 5
- **Capacity**
 - 128, 256, 512 MB
 - 1, 2, 4, 8, 16, 32, 64 GB
- **Performance***
 - Sustained read: Up to 55 MB/sec
 - Sustained write: Up to 42 MB/sec
- **Intelligent ATA/IDE Module**
 - Wear-leveling algorithms to substantially increase longevity of flash media
 - Built-in BCH ECC capable of correcting up to 24 bits in 1,024 byte data
 - Flash block management
 - Power failure management
 - Supports S.M.A.R.T commands
- **NAND Flash Type: SLC**
- **Temperature Range**
 - 0°C to 70°C for operation (Standard)
 - -40°C to 85°C for operation (Extended)
 - -40°C to 100°C for storage
- **Operating Voltage**
 - 3.3 V
 - 5.0 V
- **Power Consumption***
 - Active mode: 175 mA
 - Standby mode: 3 mA
- **Connector Type**
 - 50 pins female
- **Physical Dimensions**
 - 36.4mm x 42.8mm x 3.3mm
- **Endurance (TBW: Terabytes Written)**
 - 128 MB: 0.5 TBW
 - 256 MB: 1.1 TBW
 - 512 MB: 2.3 TBW
 - 1 GB: 4.5 TBW
 - 2 GB: 9.1 TBW
 - 4 GB: 18.2 TBW
 - 8 GB: 36.5 TBW
 - 16 GB: 73.0 TBW
 - 32 GB: 146.0 TBW
 - 64 GB: 292.1 TBW
- **Halogen Free**

*Performance and power consumption are typical and may vary depending on host system configurations.

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1. General Description

Apacer's value-added Industrial CompactFlash Card offers high performance, high reliability and power-efficient storage. Regarding standard compliance, this CompactFlash Card complies with CompactFlash specification revision 4.1, supporting transfer modes up to Programmed Input Output (PIO) Mode 6, Multi-word Direct Memory Access (DMA) Mode 4, Ultra DMA Mode 5, and PCMCIA Ultra DMA Mode 5.

Apacer's value-added CFC provides complete PCMCIA – ATA functionality and compatibility. Apacer's CompactFlash technology is designed for applications in Point of Sale (POS) terminals, telecom, IP-STB, medical instruments, surveillance systems, industrial PCs and handheld applications such as the new generation of Digital Single Lens Reflex (DSLR) cameras.

1.1 Intelligent CompactFlash Module

1.1.1 Wear-leveling algorithms

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. On the other hand, NAND flash storage adopts flash as their primary media. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term earlier. Wear leveling is an important mechanism that level out the wearing of blocks so that the wearing-down of blocks can be almost evenly distributed. This will increase the lifespan of SSDs. Commonly used wear leveling types are Static and Dynamic.

1.1.2 S.M.A.R.T. Technology

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure. Apacer SMART feature adopts the standard SMART command B0h to read data from the drive. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before the device is in critical condition.

1.1.3 Built-in Hardware ECC

This CompactFlash card employs BCH Error Correction Code (ECC) algorithms. This on-chip hardware BCH-ECC engines is 13/24 bit programmed that can correct up to 24-bit errors per 1,024 byte data. This built-in hardware ECC performs parity generation and error detection/correction for data integrity.

1.1.4 Flash Block Management

Contemporary process technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a highly minimal number of initial bad block during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. On the other hand, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

1.1.5 Power Failure Management

Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission

2. Functional Block

The CompactFlash Card (CFC) includes a controller and flash media, as well as the CompactFlash standard interface. Figure 2-1 shows the functional block diagram.

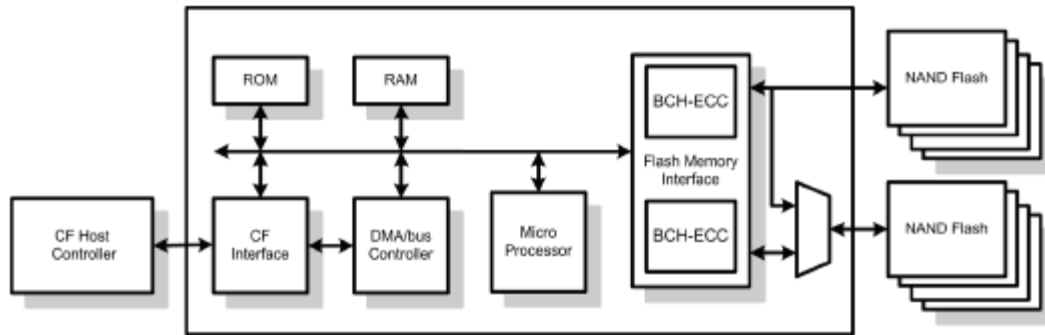


Figure 2-1: Functional Block Diagram

3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 50-pin configuration. A “#” suffix indicates the active low signal. The pin type can be input, output or input/output.

Table 3-1: Pin Assignments (1 of 2)

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
1	GND	-	GND	-	GND	-
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	#CE1	I	#CE1	I	#CS0	I
8	A10	I	A10	I	A10 ¹	I
9	#OE	I	#OE	I	#ATA SEL	I
10	A9	I	A9	I	A9 ¹	I
11	A8	I	A8	I	A8 ¹	I
12	A7	I	A7	I	A7 ¹	I
13	VCC	-	VCC	-	VCC	-
14	A6	I	A6	I	A6 ¹	I
15	A5	I	A5	I	A5 ¹	I
16	A4	I	A4	I	A4 ¹	I
17	A3	I	A3	I	A3 ¹	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	#IOIS16	O	#IOCS16	O
25	#CD2	O	#CD2	O	#CD2	O
26	#CD1	O	#CD1	O	#CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	#CE2	I	#CE2	I	#CS1	I
33	#VS1	O	#VS1	O	#VS1	O
34	#IORD	I	#IORD	I	#IORD	I
35	#IOWR	I	#IOWR	I	#IOWR	I
36	#WE	I	#WE	I	#WE	I
37	RDY/-BSY	O	#IREQ	O	INTRQ	O
38	VCC	-	VCC	-	VCC	-
39	#CSEL	I	#CSEL	I	#CSEL	I
40	#VS2	O	#VS2	O	#VS2	O
41	RESET	I	RESET	I	#RESET	I

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Table 3-1: Pin Assignments (2 of 2)

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
42	#WAIT	O	#WAIT	O	IORDY	O
43	#INPACK	O	#INPACK	O	DMARQ ²	O
44	#REG	I	#REG	I	DMACK ²	I
45	BVD2	O	#SPKR	O	#DASP	I/O
46	BVD1	O	#STSCHG	O	#PDIAG	I/O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	-	GND	-	GND	-

1. The signal should be grounded by the host.
2. Connection required when UDMA is in use.

4. Product Specifications

4.1 Capacity

Capacity specification of the Compact Flash Card series (CFC) is available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1: Capacity Specifications

Capacity	Total bytes ¹	Cylinders	Heads	Sectors	Max LBA
128 MB	128,450,560	980	8	32	250,880
256 MB	256,901,120	980	16	32	501,760
512 MB	512,483,328	993	16	63	1,000,944
1GB	1,024,966,656	1,986	16	63	2,001,888
2GB	2,048,901,120	3,970	16	63	4,001,760
4GB	4,110,188,544	7,964	16	63	8,027,712
8GB	8,195,604,480	15,880	16	63	16,007,040
16GB	16,391,340,032	16,383	16	63	32,014,336
32GB	32,019,316,736	16,383	16	63	62,537,728
64 GB	64,030,244,864	16,383	16	83	125,059,072

Notes:

Display of total bytes varies from operating systems.

Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies

Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performances of the CF cards are listed in Table 4-2.

Table 4-2: Performance Specifications

Capacity Performance	128 MB	256 MB	512 MB	1 GB	2 GB	4 GB	8 GB	16 GB	32 GB	64 GB
Sustained read (MB/s)	21	24	47	45	55	55	55	48	57	50
Sustained write (MB/s)	6	6	22	19	25	35	42	38	27	26

Notes: performance may vary depending on flash configurations or host system settings.

4.3 Environmental Specifications

Environmental specification of the Compact Flash Card series (CFC) follows the MIL-STD-810F standards, as shown in Table 4-3.

Table 4-3: Environmental Specifications

Environment		Specifications
Temperature	Operating	0°C to 70°C (Standard); -40°C to 85°C (Extended)
	Storage	-40°C to 100°C
Vibration (Non-Operation)		Sine wave : 10~2000Hz, 15G (X, Y, Z axes)
Shock (Non-Operation)		Half sine wave 1,500G (X, Y, Z ; All 6 axes)

4.4 Certification & Compliance

The CompactFlash card complies with the following global standards:

- CE
- FCC
- Halogen-free
- CompactFlash Association Specification Revision 4.1
- EMC

4.5 Endurance

The endurance of a storage device is predicted by TeraBytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Capacity	TeraBytes Written
128 MB	0.5
256 MB	1.1
512 MB	2.3
1 GB	4.5
2 GB	9.1
4 GB	18.2
8 GB	36.5
16 GB	73.0
32 GB	146.0
64 GB	292.1

Notes:

- The measurement assumes the data written to the SSD for test is under a typical and constant rate.
- The measurement follows the standard metric: 1 TB (Terabyte) = 1000 GB.
- The estimated values are based on JEDEC Enterprise endurance workload comprised of random data with the payload size distribution with sequential write behavior.

5. Software Interface

5.1 CF-ATA Command Set

Table 5-1: CFC-ATA Command Set

Command	Code	Protocol
Request Sense	03h	Non-data
Write-Sector(s)-Without-Erase	38h	PIO data-out
Erase-Sector(s)	C0h	Non-data
Write-Multiple-Without-Erase	CDh	PIO data-out
Translate-Sector	87h	PIO data-in
Set Features Enable/Disable 8-bit transfer	EFh	Non-data
Execute Drive Diagnostic	90h	Device diagnostic
Flush-Cache	E7h	Non-data
Identify Device	ECh	PIO data-in
Read DMA	C8h	DMA
Read-Multiple	C4h	PIO data-in
Read Sector(s)	20h or 21h	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Set Feature	EFh	Non-data
Set Multiple Mode	C6h	Non-data
Write DMA	CAh	DMA
Write Multiple	C5h	PIO data-out
Write Sectors(s)	30h or 31h	PIO data-out
NOP	00h	Non-data
Read-Buffer	E4h	PIO data-in
Write Buffer	E8h	PIO data-out
Check Power Mode	E5h or 98h	Non-data
Idle	E3h or 97h	Non-data
Idle-Immediate	E1h or 95h	Non-data
Sleep	E6h or 99h	Non-data
Standby	E2h or 96h	Non-data
Standby Immediate	E0h or 94h	Non-data
Security Set Password	F1h	PIO data-out
Security Unlock	F2h	PIO data-out
Security Erase Prepare	F3h	Non-data

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Command	Code	Protocol
Security Erase Unit	F4h	PIO data-out
Security Freeze Lock	F5h	Non-data
Security Disable Password	F6h	PIO data-out
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Return Status	B0h	Non-data
SMART Execute Off-line Immediate	B0h	Non-data
SMART Read Data	B0h	PIO data-in
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
Format Track	50h	PIO data-out
Initialize Drive Parameters	91h	Non-data
Recalibrate	1Xh	Non-data
Seek	7Xh	Non-data
Wear Level	F5h	Non-data
Write Verify	3Ch	PIO data-out

6. Electrical Specifications

Caution: Absolute Maximum Stress Ratings – Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Table 6-1: Operating Range

Standard Operating Temperature	0°C to 70°C
Extended Operating Temperature	-40°C to 85°C
Supply voltage	5V ± 5% (4.75-5.25V)
	3.3V ± 5% (3.135-3.465V)

Table 6-2: Absolute Maximum Power Pin Stress Ratings

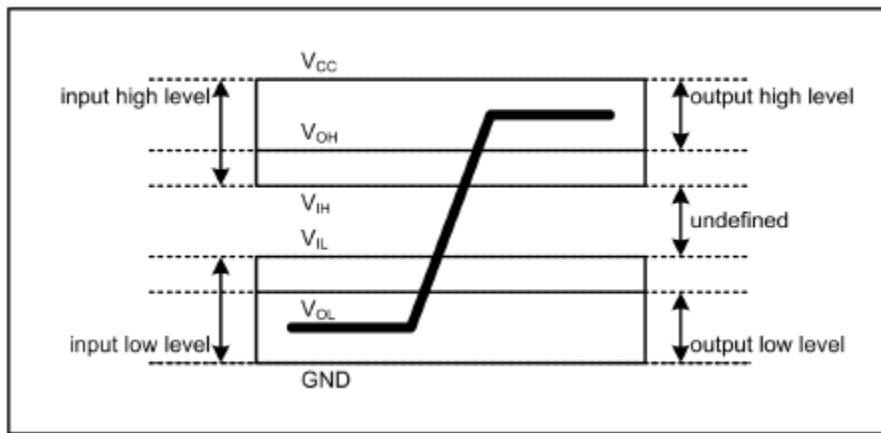
Parameter	Symbol	Conditions
Input Power	V_{DD}	-0.3V min. to 6.5V max.
Voltage on any pin except V_{DD} with respect to GND	V	-0.5V min. to $V_{DD} + 0.5V$ max.

6.1 AC/DC Characteristics

The following section provides general AC/DC characteristics of this CompactFlash card.

6.1.1 General DC Characteristics

Definitions of V_{IH} , V_{CC} , V_{OH} , V_{OL}



● **CompactFlash Interface I/O at 5.0V**

Parameter	Symbol	Minimum	Maximum	Unit	Remark
Supply Voltage	Vcc	4.5	5.5	V	
High Level Output Voltage	VOH	Vcc-0.8		V	
Low Level Output Voltage	VOL		0.8	V	
High Level Input Voltage	VIH	4.0		V	Non-Schmitt trigger
		2.92		V	Schmitt trigger
Low Level Input Voltage	VIL		0.8	V	Non-Schmitt trigger
			1.70	V	Schmitt trigger
Pull-up Resistance	RPU	50	73	kOhm	
Pull-down Resistance	RPD	50	97	kOhm	

● **CompactFlash Interface I/O at 3.3V**

Parameter	Symbol	Minimum	Maximum	Unit	Remark
Supply Voltage	Vcc	2.97	3.63	V	
High Level Output Voltage	VOH	Vcc-0.8		V	
Low Level Output Voltage	VOL		0.8	V	
High Level Input Voltage	VIH	2.4		V	Non-Schmitt trigger
		2.05		V	Schmitt trigger
Low Level Input Voltage	VIL		0.6	V	Non-Schmitt trigger
			1.25	V	Schmitt trigger
Pull-up Resistance	RPU	52.7	141	kOhm	
Pull-down Resistance	RPD	47.5	172	kOhm	

● **Non-CF Interface I/O Pins**

Parameter	Symbol	Minimum	Maximum	Unit	Remark
Supply Voltage	Vcc	2.7	3.6	V	
High Level Output Voltage	VOH	2.4		V	
Low Level Output Voltage	VOL		0.4	V	
High Level Input Voltage	VIH	2.0		V	Non-Schmitt trigger
		1.4	2.0	V	Schmitt trigger
Low Level Input Voltage	VIL		0.8	V	Non-Schmitt trigger
		0.8	1.2	V	Schmitt trigger
Pull-up Resistance	RPU	40		kOhm	
Pull-down Resistance	RPD	40		kOhm	

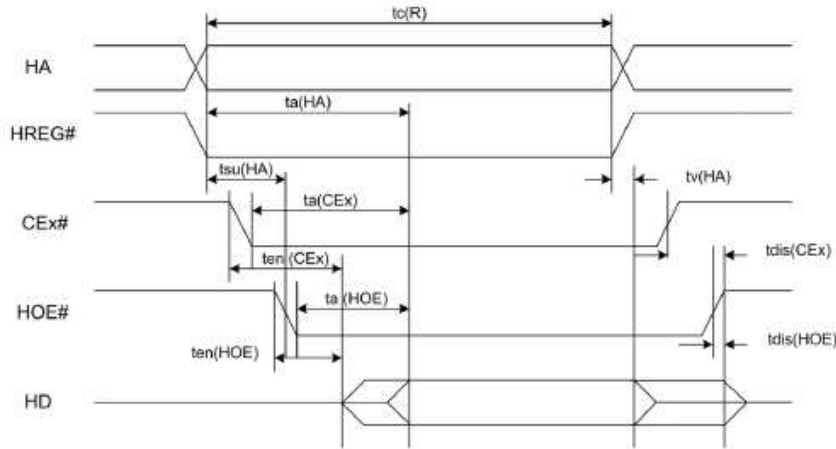
Note: the Schmitt trigger includes CompactFlash I/O pins such as CE1#, CE2#, HREG#, HOE#, HIOE#, HWE# and HIOW#, as well as non CompactFlash I/O pins like RST#, T0, T1, and T2.

6.1.2 General AC Characteristics

- Attribute Memory Read Timing**

Item	Symbol	Min. (ns)	Max. (ns)
Read Cycle Time	tc (R)	300	
Address Access Time	ta (HA)		300
Card Enable Access Time	ta (CEx)		300
Output Enable Access Time	ta (HOE)		150
Output Disable Time from CEx#	tdis (CEx)		100
Output Disable Time from HOE#	tdis (HOE)		100
Address Setup Time	tsu (HA)	30	
Output Enable Time from CEx#	ten (CEx)	5	
Output Enable Time from HOE#	ten (HOE)	5	
Data Valid from Address Change	tv (HA)	0	

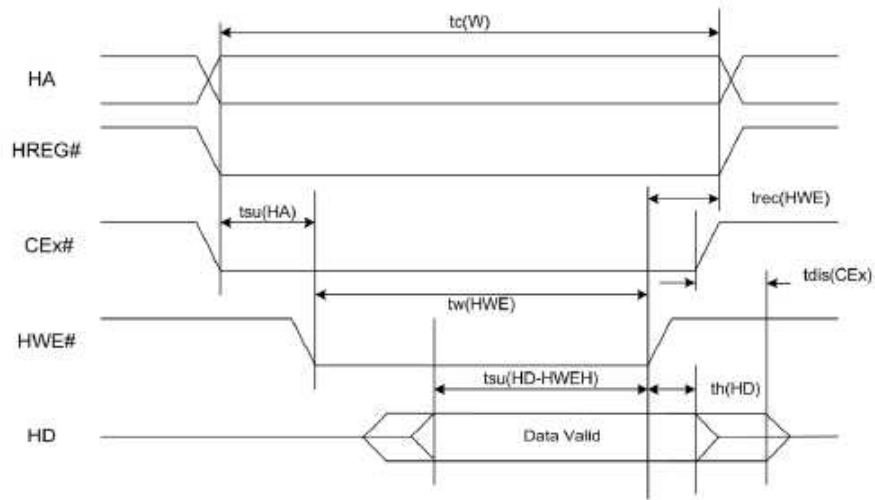
Notes: all time intervals are in nanoseconds. HD refers to the data provided by the CompactFlash card to the system. The CEx# signal or both of the HOE# and the HWE# signal are de-asserted between consecutive cycle operations.



● **Attribute Memory Write Timing**

Item	Symbol	Min. (ns)	Max. (ns)
Write Cycle Time	$t_c(W)$	250	
Write Pulse Width	$t_w(HWE)$	150	
Address setup Time	$t_{su}(HA)$	30	
Write Recovery Time	$t_{rec}(HWE)$	30	
Data Setup Time for HWE#	$t_{su}(HD-HWEH)$	80	
Data Hold Time	$t_h(HD)$	30	

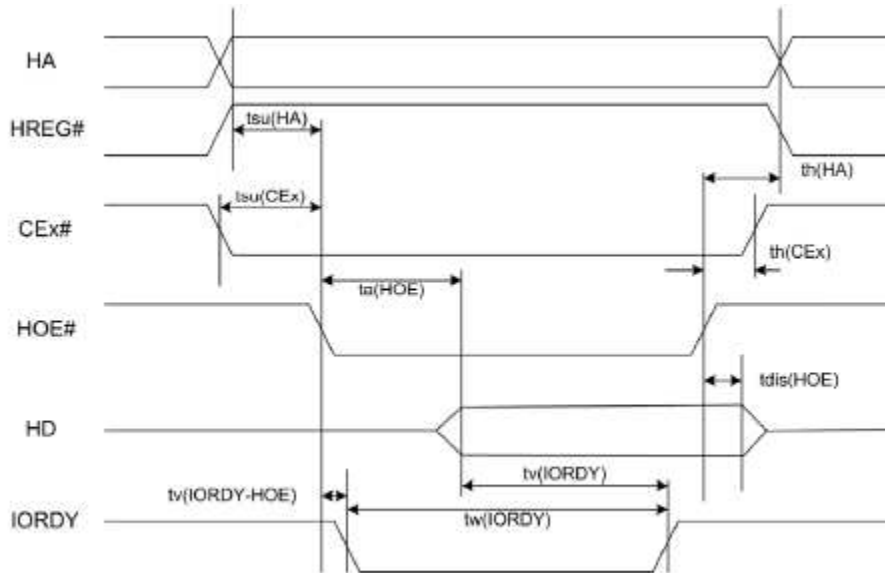
Notes: all time intervals are in nanoseconds. HD refers to the data provided by the CompactFlash card to the system.



● **Common Memory Read Timing**

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Output Enable Access Time	ta (HOE)		125		60		50		45
Output Disable Time from HOE#	tdis (HOE)		100		60		50		45
Address Setup Time	tsu (HA)	30		15		10		10	
Address Hold Time	th (HA)	20		15		15		10	
CEx# Setup before HOE#	tsu (CEx)	5		5		5		5	
CEx# Hold following HOE#	th (CEx)	20		15		15		10	
Wait Delay falling from HOE#	tv (IORDY-HOE)		35		35		35		Na
Data Setup for Wait Release	tv (IORDY)		0		0		0		Na
Wait Width Time	tw (IORDY)		350		350		350		Na

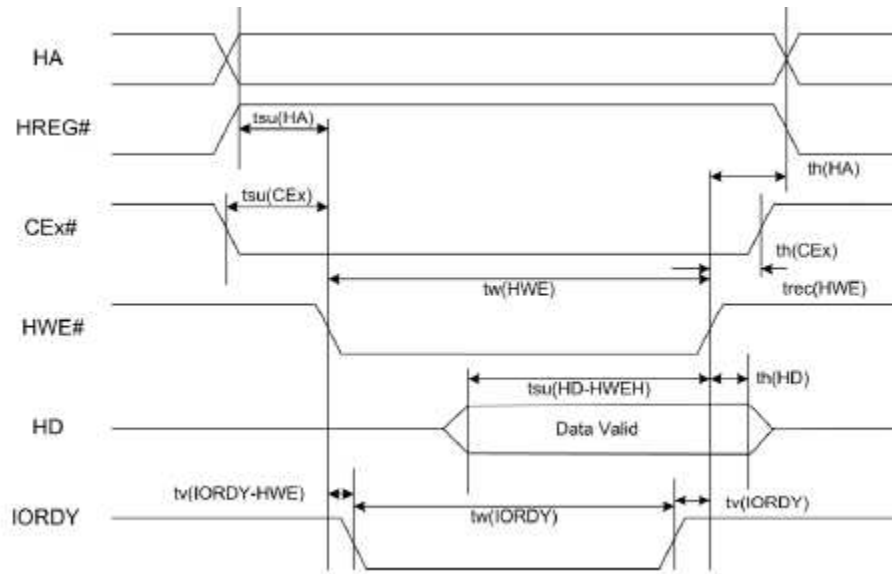
Note: IORDY is not supported in this 80 ns mode. The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. HD refers to the data provided by the CompactFlash card to the system. The IORDY signal can be ignored when the HOE# cycle-to-cycle time is greater than the Wait Width Time. The Max Wait Width Time can be determined from the Card Information Structure (CIS). Although adhering to the PCM-CIA specification, the Wait Width Time is intentionally designed to be lower in this specification.



● **Common Memory Write Timing**

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Setup before HWE#	tsu (HD-HWEH)	80		50		40		30	
Data Hold following HWE#	th (HD)	30		15		10		10	
HWE# Pulse Width	tw (HWE)	150		70		60		55	
Address Setup Time	tsu (HA)	30		15		10		10	
CEx# Setup before HWE#	tsu (CEx)	5		5		5		5	
Write Recovery Time	trec (HWE)	30		15		15		15	
Address Hold Time	th (HA)	20		15		15		15	
CEx# Hold following HWE#	th (CEx)	20		15		15		10	
Wait Delay falling from HWE#	tv (IORDY-HWE)		35		35		35		Na
HWE# High from Wait Release	tv (IORDY)	0		0		0		Na	
Wait Width Time	tw (IORDY)		350		350		350		Na

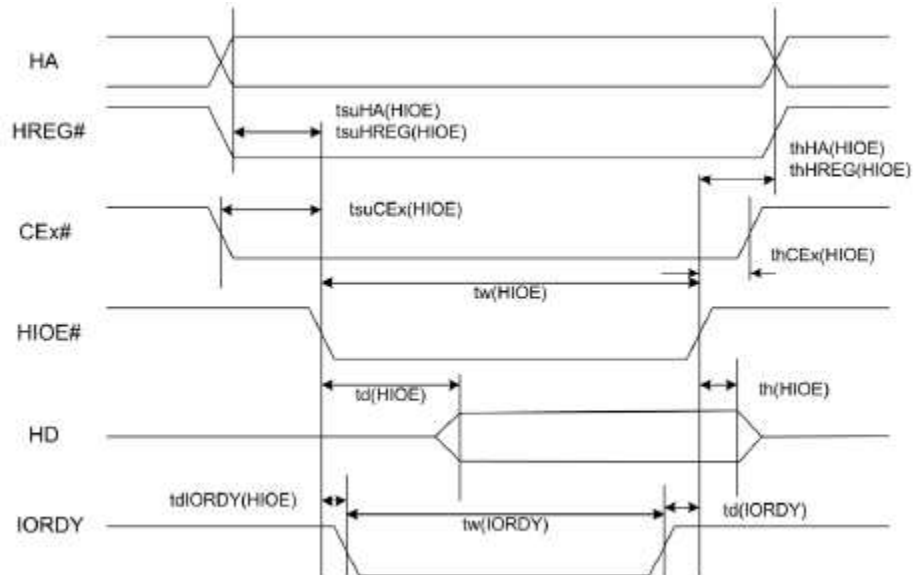
Note: IORDY is not supported in this 80 ns mode. The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. HD refers to the data provided by the CompactFlash card to the system. The IORDY signal can be ignored when the HWE# cycle-to-cycle time is greater than the Wait Width Time. The Max Wait Width Time can be determined from the Card Information Structure (CIS). Although adhering to the PCM-CIA specification, the Wait Width Time is intentionally designed to be lower in this specification.



● **I/O Read Timing**

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Delay after HIOE#	td (HIOE)		100		50		50		45
Data Hold following HIOE#	th (HIOE)	0		5		5		5	
HIOE# Width Time	tw (HIOE)	165		70		65		55	
Address Setup before HIOE#	tsuHA (HIOE)	70		25		25		15	
Address Hold following HIOE#	thHA (HIOE)	20		10		10		10	
CEx# Setup before HIOE#	tsuCEX (HIOE)	5		5		5		5	
CEx# Hold following HIOE#	thCEX (HIOE)	20		10		10		10	
HREG# Setup before HIOE#	tsuHREG (HIOE)	5		5		5		5	
HREG# Hold following HIOE#	thHREG (HIOE)	0		0		0		0	
Wait Delay falling from HIOE#	tdIORDY (HIOE)		35		35		35		Na
Data Delay from Wait Rising	td (IORDY)		0		0		0		na
Wait Width Time	tw (IORDY)		350		350		350		Na

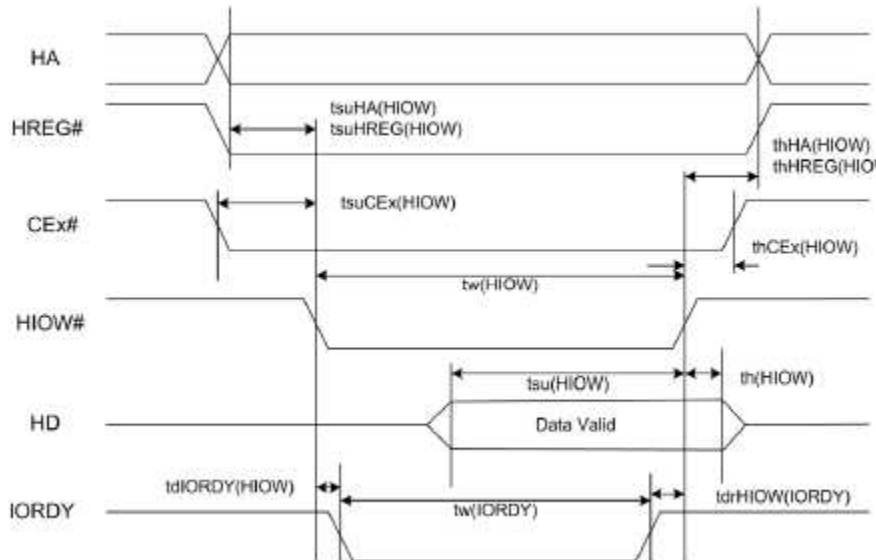
Note: IORDY is not supported in this 80 ns mode. Maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met. HD refers to data provided by the CompactFlash Card to the system. Although following PCMCIA specification, the Wait Width Time is intentionally lower in this specification.



● **I/O Write Timing**

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Setup before HIOW#	tsu (HIOW)	60		20		20		15	
Data Hold following HIOW#	th (HIOW)	30		10		5		5	
HIOW# Width Time	tw (HIOW)	165		70		65		65	
Address Setup before HIOW#	tsuHA (HIOW)	70		25		25		15	
Address Hold following HIOW#	thHA (HIOW)	20		20		10		10	
CEx# Setup before HIOW#	tsuCEx (HIOW)	5		5		5		5	
CEx# Hold following HIOW#	thCEx (HIOW)	20		20		10		10	
HREG# Setup before HIOW#	tsuHREG (HIOW)	5		5		5		5	
HREG# Hold following HIOW#	thHREG (HIOW)	0		0		0		0	
Wait Delay falling from HIOW#	tdIORDY (HIOW)		35		35		35		na
HIOW# high from Wait High	tdHIOW (IORDY)	0		0		0		na	
Wait Width Time	tw (IORDY)		350		350		350		na

Note: IORDY is not supported in this 80 ns mode. The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. Although minimum time from IORDY high to HIOW# high is 0 nsec, the minimum HIOW# width is still met. HD refers to data provided by the CompactFlash Card to the system.



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• True IDE PIO Mode Read/Write Timing

Item	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
Cycle Time (Min.)	t0	600	383	240	180	120	100	80
Address Valid to HIOE# / HIOW# Setup (Min.)	t1	70	50	30	30	25	15	10
HIOE# / HIOW# (Min.)	t2	165	125	100	80	70	65	55
HIOE# / HIOW# (Min.) Register (8-bit)	t2	290	290	290	80	70	65	55
HIOE# / HIOW# Recovery Time (Min.)	t2i	-	-	-	70	25	25	20
HIOW# Data Setup (Min.)	t3	60	45	30	30	20	20	15
HIOW# Data Hold (Min.)	t4	30	20	15	10	10	5	5
HIOE# Data Setup (Min.)	t5	50	35	20	20	20	15	10
HIOE# Data Hold (Min.)	t6	5	5	5	5	5	5	5
HIOE# Data Tristate (Max.)	t6Z	30	30	30	30	30	20	20
Address Valid to IOCS16# Assertion (Max.)	t7	90	50	40	n/a	n/a	n/a	n/a
Address Valid to IOCS16# released (Max.)	t8	60	45	30	n/a	n/a	n/a	n/a
HIOE# / HIOW# to Address Valid Hold	t9	20	15	10	10	10	10	10
Read Data Valid to IORDY Active (Min.), if IORDY initially low after tA	tRD	0	0	0	0	0	0	0
IORDY Setup Time	tA	35	35	35	35	35	Na	Na
IORDY Pulse Width (Max.)	tB	1250	1250	1250	1250	1250	Na	Na
IORDY Assertion to Release (Max.)	tC	5	5	5	5	5	Na	Na

*All timing intervals are measured in nanoseconds. The maximum load on IOCS16# is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met.

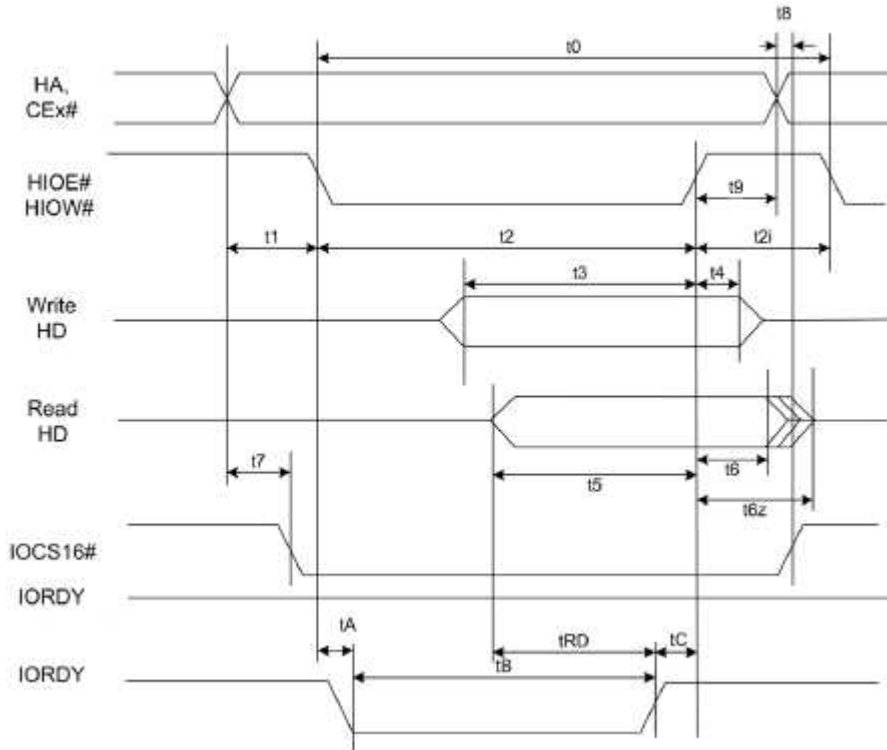
Where t0 denotes the minimum total cycle time; t2 represents the minimum command active time; t2i is the minimum command recovery time or command inactive time. Actual cycle time equals to the sum of actual command active time and actual command inactive time. The three timing requirements for t0, t2, and t2i are met. The minimum total cycle time requirement is greater than the sum of t2 and t2i, implying that a host implementation can extend either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device identity data. A CompactFlash card implementation supports any legal host implementation.

The delay originates from HIOE# or HIOW# activation until the state of IORDY is first sampled. If IORDY is inactive, the host waits until IORDY is active before the PIO cycle is completed. When the CompactFlash Card is not driving IORDY, which is negated at tA after HIOE# or HIOW# activation, then t5 is met and tRD is inapplicable. When the CompactFlash Card is driving IORDY, which is negated at the time tA after HIOE# or HIOW# activation, then tRD is met and t5 is inapplicable.

Both t7 and t8 apply to modes 0, 1, and 2 only. For other modes, the signal is invalid. IORDY is not supported in this mode.

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Device address comprises CE1#, CE2#, and HA[2:0]

Data comprises HD[15:0] (16-bit) or HD[7:0] (8-bit)

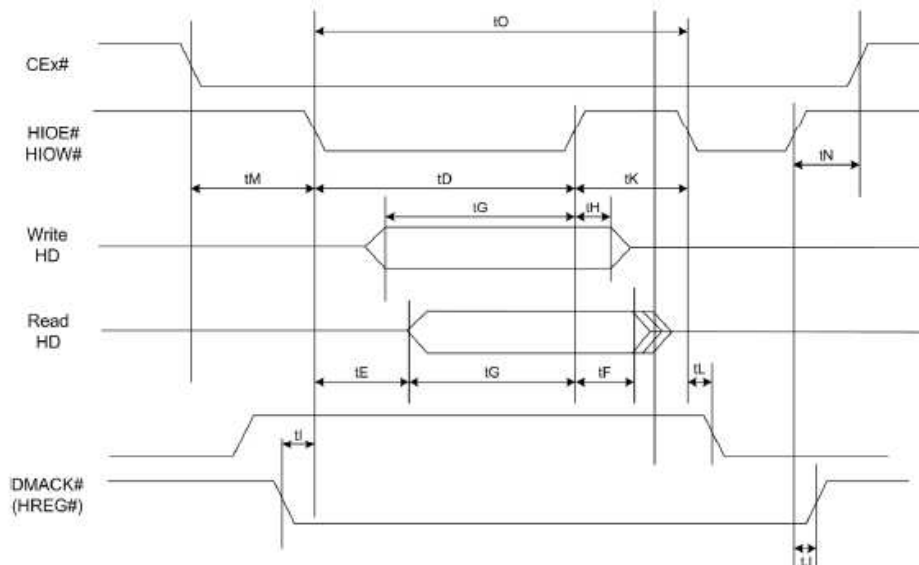
IOCS16# is shown for PIO modes 0, 1, and 2. For other modes, the signal is ignored.

The negation of IORDY by the device is used to lengthen the PIO cycle. Whether the cycle is to be extended is determined by the host after t_A from the assertion of HIOE# or HIOW#. The assertion and negation of IORDY is described in the following cases. First, the device never negates IORDY, so no wait is generated. Secondly, device drives IORDY low before t_A . Thus, wait is generated. The cycle is completed after IORDY is re-asserted. For cycles in which a wait is generated and HIOE# is asserted, the device places read data on D15-D00 for t_{RD} before IORDY is asserted.

• **True IDE Multiword DMA Mode Read/Write Timing**

Item	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
Cycle Time (Min.)	tO	480	150	120	100	80
HIOE#/HIOW# asserted width (Min.)	tD	215	80	70	65	65
HIOE# data access (Max.)	tE	150	60	50	50	45
HIOE# data hold (Min.)	tF	5	5	5	5	5
HIOE# / HIOW# data setup (Min.)	tG	100	30	20	15	10
HIOW# data hold (Min.)	tH	20	15	10	5	5
HREG# to HIOE#/HIOW# setup (Min.)	tI	0	0	0	0	0
HIOE#/HIOW# to HREG# hold (Min.)	tJ	20	5	5	5	5
HIOE# negated width (Min.)	tKR	50	50	25	25	20
HIOW# negated width (Min.)	tKW	215	50	25	25	20
HIOE# to DMARQ delay (Max.)	tLR	120	40	35	35	35
HIOW# to DMARQ delay (Max.)	tLW	40	40	35	35	35
CEx# valid to HIOE#/HIOW#	tM	50	30	25	10	5
CEx# hold	tN	15	10	10	10	10

Note: Where tO is the minimum total cycle time and tD is minimum command active time, whereas tKR and tKW are minimum command recovery time or command inactive time for input and output cycles, respectively. Actual cycle time equals to the sum of actual command active time and actual command inactive time. The three timing requirements of tO, for instance, tD, tKR, and tKW, must be met. The minimum total cycle time requirement exceeds the sum of tD and tKR or tKW for input and output cycles respectively, implying that a host implementation can extend either or both tD and tKR or tKW as deemed necessary to ensure that tO equals or exceeds the value reported in the device identify data. A CompactFlash card implementation supports any legal host, appropriate host implementation.



If a card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ during the time from the start of a DMA transfer cycle (to suspend DMA transfers in progress) and re-assertion of the signal at a relatively later time to continue DMA transfer operations. The host may negate this signal to suspend the DMA transfer in progress.

● **Ultra DMA Signal Usage in Each Interface Mode**

Signal	Type	Non-UDMA Memory Mode	PC Card Memory Mode UDMA	PC Card IO Mode UDMA	True IDE Mode UDMA
DMARQ	Output	(INPACK#)	DMARQ#	DMARQ#	DMARQ
HREG#	Input	(REG#)	DMACK#	DMACK	DMACK#
HIOW#	Input	(IOWR#)	STOP ¹	STOP ¹	STOP ¹
HIOE#	Input	(IORD#)	HDMARDY#(R) ^{1,2} HSTROBE(W) ^{1,3,4}	HDMARDY#(R) ^{1,2} HSTROBE(W) ^{1,3,4}	HDMARDY#(R) ^{1,2} HSTROBE(W) ^{1,3,4}
IORDY	Output	(WAIT#)	DDMARDY#(W) ^{1,3} DSTROBE(R) ^{1,2,4}	DDMARDY#(W) ^{1,3} DSTROBE(R) ^{1,2,4}	DDMARDY#(W) ^{1,3} DSTROBE(R) ^{1,2,4}
HD[15:0]	Bidir	(D[15:00])	D[15:00]	D[15:00]	D[15:00]
HA[10:0]	Input	(A[10:00])	A[10:00]	A[10:00]	A[02:00] ⁵
CSEL#	Input	(CESL#)	CSEL#	CSEL#	CSEL#
HIRQ	Output	(READY)	READY	INTRQ#	INTRQ
CE1#	Input	(CE1#)	CE1#	CE1#	CS0#
CE2#	Input	(CE2#)	CE2#	CE2#	CS1#

1. UDMA interpretation of this signal is valid only during an Ultra DMA data burst.
2. UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Read command.
3. UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.
4. HSTROBE and DSTROBE signals are active on both rising and falling edges.
5. Address lines 03-10 are not used in the True IDE mode.

● **Ultra DMA Data Burst Timing Requirements**

Parameter	UDMA Mode 0	UDMA Mode 1	UDMA Mode 2	UDMA Mode 3	UDMA Mode 4	UDMA Mode 5	Measure Location
t _{2CYCTYP}	240	160	120	90	60	40	Sender
t _{CYC}	112	73	54	39	25	16.8	See note
t _{2CYC}	230	153	115	86	57	38	Sender
t _{DS}	15.0	10.0	7.0	7.0	5.0	4.0	Recipient
t _{DH}	5.0	5.0	5.0	5.0	5.0	4.6	Recipient
t _{DVS}	70.0	48.0	31.0	20.0	6.7	4.8	Sender
t _{DVH}	6.2	6.2	6.2	6.2	6.2	4.8	Sender
t _{CS}	15.0	10.0	7.0	7.0	5.0	5.0	Device
t _{CH}	5.0	5.0	5.0	5.0	5.0	5.0	Device
t _{CVS}	70.0	48.0	31.0	20.0	6.7	10.0	Host
t _{CVH}	6.2	6.2	6.2	6.2	6.2	10.0	Host
t _{ZFS}	0	0	0	0	0	35	Device
t _{DZFS}	70.0	48.0	31.0	20.0	6.7	25	Sender

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t_{FS}	230	200	170	130	120	90	Device
t_{LI}	0 - 150	0 - 150	0 - 150	0 - 100	0 - 100	0 - 75	See note
t_{MLI}	20	20	20	20	20	20	Host
t_{UI}	0	0	0	0	0	0	Host
t_{AZ}	10	10	10	10	10	10	See note
t_{ZAH}	20	20	20	20	20	20	Host
t_{ZAD}	0	0	0	0	0	0	Device
t_{ENV}	20 - 70	20 - 70	20 - 70	20 - 55	20 - 55	20 - 50	Host
t_{RFS}	75	70	60	60	60	50	Sender
t_{RP}	160	125	100	100	100	85	Recipient
t_{IORDYZ}	20	20	20	20	20	20	Device
t_{ZIORDY}	0	0	0	0	0	0	Device
t_{ACK}	20	20	20	20	20	20	Host
t_{SS}	50	50	50	50	50	50	Sender

Notes:

All timing are in nanoseconds and all timing measurement switching points (low to high and high to low) are taken at 1.5V. All signal transitions for a timing parameter are determined at the connector specified in the measurement location column. Parameter t_{CYC} is determined at the connector of the recipient farthest from the sender, while parameter t_{LI} is determined at the connector of a sender or recipient responding to an incoming transition from the recipient or sender, respectively. Both incoming signal and outgoing response are determined at the same connector. Parameter t_{AZ} is determined at the connector of a sender or recipient driving the bus, and must release the bus to allow for a bus turnaround.

• Ultra DMA Data Burst Timing Descriptions

Parameter	Description & Comment	Note
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2,5
t_{DVS}	Data valid setup at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time at device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until DMACK(#) negation)	3
t_{CVH}	CRC word valid hold time at sender (from DMACK(#) negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing	