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AP1154ADLXX

14V Input / 1A Output LDO Regulator

1. Genaral Description

The AP1154ADLXX is a low dropout linear regulator with ON/OFF control, which can supply 1A load current. The IC is an integrated circuit with a silicon monolithic bipolar structure. The output voltage, trimmed with high accuracy, is available from 1.8 to 5.0V in 0.1V steps. The output capacitor is available to use a small 1μF ceramic capacitor. The IC can be used for USB application (500mA), since the output limitation current can be set by external resistor. The over current, thermal and reverse bias protections are integrated, and also the package is high heat radiation type, HSOP-8. The IC is designed for space saving requirements.

2. Feature

- Available to use a small 1μF ceramic capacitor
- Dropout voltage V_{DROP}=160mV at 500mA
- Output current 1A
- High precision output voltage ±1.5% or ±50mV
- High ripple rejection ratio 80dB at 1kHz
- Wide operating voltage range 2.4V to 14.0V
- Very low quiescent current I_Q=320μA at I_{OUT}=0mA
- Programmable output current limitation by an external resistor
- On/Off control (High active)
- Built-in Short circuit protection, thermal shutdown
- Built-in reverse bias over current protection
- Available very low noise application
- Small package HSOP-8

3. Application

- Power supply for low voltage MPU and peripheral equipment
- Digital AV system
- Any electronic equipment

4. Table of Contents

5. Block Diagram

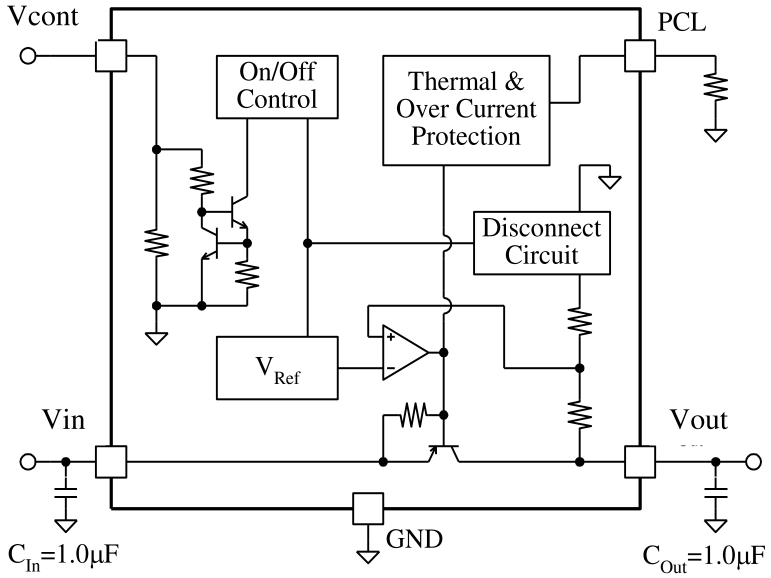


Figure 1. Block Diagram

6. Ordering Information

AP1154ADLXX Ta = -40 to 85°C HSOP-8

・ Output Voltage Code

For product name, please check the below chart. Please contact your authorized ASAHI KASEI MICRODEVICES representative for voltage availability.

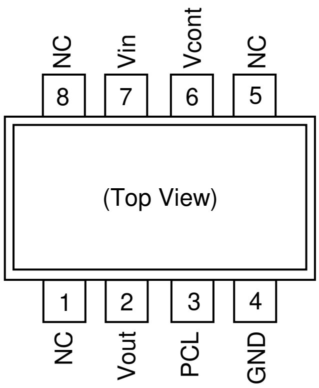
AP1154ADLXX — Output voltage code

Table 1. Standard Voltage Version, Output Voltage & Voltage Code

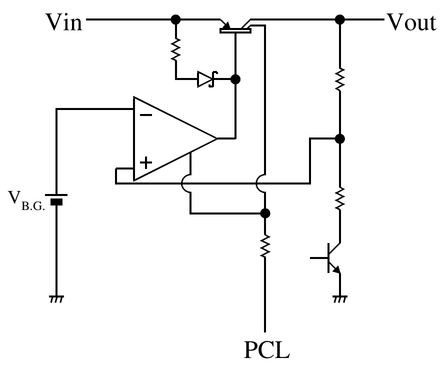
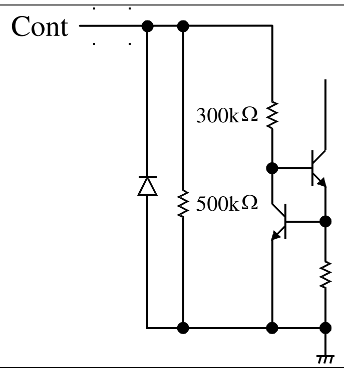
XX	V_{OUT}	XX	V_{OUT}	XX	V_{OUT}
18	1.8	25	2.5	33	3.3
21	2.1	30	3.0	50	5.0

7. Pin Configurations and Functions

■ Pin Configuration



■ Functions

Pin No.	Pin Description	Internal Equivalent Circuit	Description
3	PCL		Programmable Current Limitation The output limitation current can be set by an external resistance (R_{PCL}). The R_{PCL} is connected between the PCL terminal and GND. If there is no need of setting a current limit, connect the PCL terminal to GND.
2	Vout		Output Terminal Connect a capacitor between the Vout terminal and GND as follows. Vout≥2.4V: Capacitance ≥ 1µF Vout<2.4V:Capacitance ≥ 2.2µF
4	GND	-	GND Terminal
6	Vcont		On/Off Control Terminal The On/Off voltages are as follows: V_{Cont}≥1.8V : ON V_{Cont}≤0.35V : OFF Pull-down resistance (500kΩ) is built-in.
7	Vin	-	Input Terminal Connect a capacitor of 1.0µF or higher between the Vin terminal and GND.

8. Absolute Maximum Rating

Parameter	Symbol	min	max	Unit	Condition
Supply Voltage	Vcc_{MAX}	-0.4	16	V	
Reverse Bias	$Vrev_{MAX}$	-0.4	6	V	Vout≦2.0V
		-0.4	10	V	2.1V≦Vout
PCL Terminal Voltage	$Vpcl_{MAX}$	-0.4	5	V	
Vcont Terminal Voltage	$Vcont_{MAX}$	-0.4	16	V	
Junction temperature	Tj	-	150	°C	
Storage Temperature Range	T_{stg}	-55	150	°C	
Power Dissipation	P_D	-	2400	mW	When mounted on PCB (Note 1)

Note 1. Please derate 19.2mW/°C above 25°C or more. Thermal resistance (θ_{JA}) = 52°C/W.

WARNING: The maximum ratings are the absolute limitation values with the possibility of the IC breakage. When the operation exceeds this standard quality cannot be guaranteed.

9. Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Unit	Condition
Operating Temperature Range	Ta	-40	-	85	°C	
Operating Voltage Range	V_{OP}	2.4	-	14	V	

10. Electrical Characteristics

■ Electrical Characteristics of Ta=Tj=25°C

The parameters with min or max values will be guaranteed at Ta=Tj=25°C.

(Vin=Vout(typ)+1V,Vcont=1.8V,Ta=Tj=25°C, unless otherwise specified.)

Parameter	Symbol	Condition	min	typ	max	Unit
Output Voltage	Vout	Iout = 5mA	(Table 2)			V
Line Regulation	LinReg	ΔV=5V, Iout=5mA	-5.0	0.0	5.0	mV
Load Regulation	LoaReg	Iout=5mA ~ 500mA	-25	-	25	mV
		Iout=5mA ~ 1000mA	-45	-	45	mV
Dropout Voltage (Note 2)	Vdrop	Iout=500mA	-	160	300	mV
		Iout=1000mA	-	300	600	mV
Maximum Output Current (Note 3)	Iout,Peak	Vout=Vout(typ) × 0.9	-	1400	-	mA
Short Circuit Current(Note 3)	I_{SHORT}		-	1500	-	mA
Quiescent Current	Iq	Iout = 0mA	-	320	520	µA
Standby Current	Istandby	Vcont = 0V	-	0.0	0.1	µA
GND Terminal Current	Ignd	Iout=30mA	-	0.7	1.4	mA
Reverce Bias Current	Irev	Vrev=Vout(typ), Vin=0V, Vcont=0V	-	0	0.1	µA
Vcont Terminal						
Vcont Terminal Current	Icont	Vcont = 1.8V	-	5	10	µA
Vcont Terminal Voltage	Vcont	Vout ON state	1.8	-	-	V
		Vout OFF state	-	-	0.35	V

Note 2. For Vout ≤ 2.0V , no regulations.
Note 3. The maximum output current is limited by power dissipation.

General Note:
Parameter with only typical value is for reference only.

Table 2. Standard Voltage Version

Part Number	Output Voltage		
	min	typ	max
	V	V	V
AP1154ADL18	1.750	1.800	1.850
AP1154ADL21	2.050	2.100	2.150
AP1154ADL25	2.450	2.500	2.550
AP1154ADL30	2.950	3.000	3.050
AP1154ADL33	3.250	3.300	3.350
AP1154ADL50	4.925	5.000	5.075

■ Electrical Characteristics of Ta=-40°C~85°C

The parameters with min or max values will be guaranteed at Ta=Tj=-40 ~ 85°C.

(Vin=Vout(typ)+1V,Vcont=1.8V,Ta=-40 ~ 85°C, unless otherwise specified.)

Parameter	Symbol	Condition	min	typ	max	Unit
Output Voltage	Vout	Iout = 5mA	(Table 3)			V
Line Regulation	LinReg	ΔV=5V, Iout=5mA	-8.0	0.0	8.0	mV
Load Regulation	LoaReg	Iout=5mA ~ 500mA	-40	-	40	mV
		Iout=5mA ~ 1000mA	-120	-	120	mV
Dropout Voltage (Note 4)	Vdrop	Iout=500mA	-	160	385	mV
		Iout=1000mA	-	300	670	mV
Maximum Output Current (Note 5)	Iout,Peak	Vout=Vout(typ) × 0.9	-	1400	-	mA
Short Circuit Current(Note 5)	I_{SHORT}		-	1500	-	mA
Quiescent Current	Iq	Iout = 0mA	-	320	624	μA
Standby Current	Istandby	Vcont = 0V	-	0.0	1.5	μA
GND Terminal Current	Ignd	Iout=30mA	-	0.7	1.8	mA
Reverce Bias Current	Irev	Vrev=Vout(typ), Vin=0V, Vcont=0V	-	0.0	1.5	μA
Vcont Terminal						
Vcont Terminal Current	Icont	Vcont = 1.8V	-	5	10	μA
Vcont Terminal Voltage	Vcont	Vout ON state	1.8	-	-	V
		Vout OFF state	-	-	0.35	V

Note 4. For Vout ≤ 2.0V , no regulations.
Note 5. The maximum output current is limited by power dissipation.

General Note:
Parameter with only typical value is for reference only.

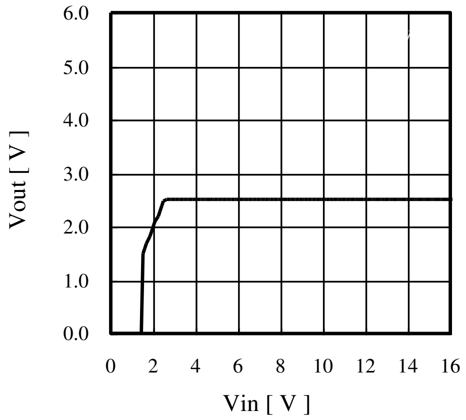
Table 3. Standard Voltage Version

Part Number	Output Voltage		
	min	typ	max
	V	V	V
AP1154ADL18	1.720	1.800	1.880
AP1154ADL21	2.020	2.100	2.180
AP1154ADL25	2.420	2.500	2.580
AP1154ADL30	2.920	3.000	3.080
AP1154ADL33	3.217	3.300	3.383
AP1154ADL50	4.875	5.000	5.125

11. Description

11.1 DC Characteristics

■ Vout vs Vin (AP1154ADL25)



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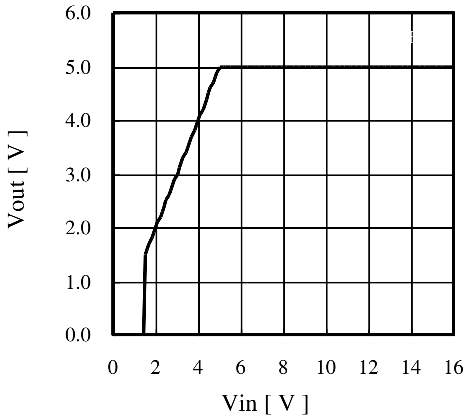
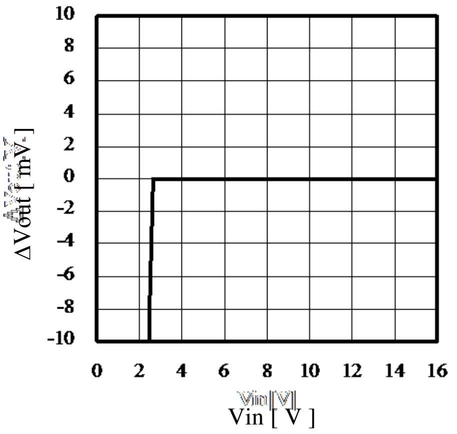
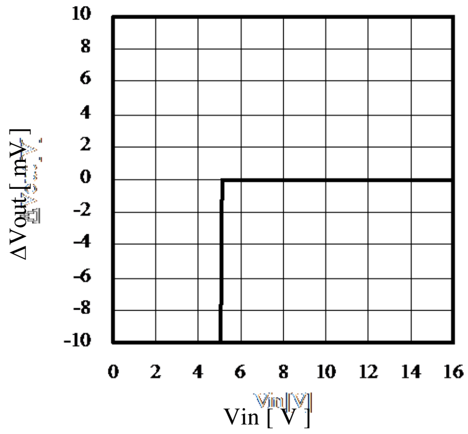


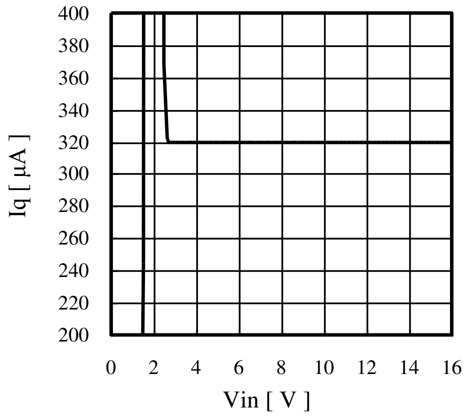
■ Line Regulation (AP1154ADL25)



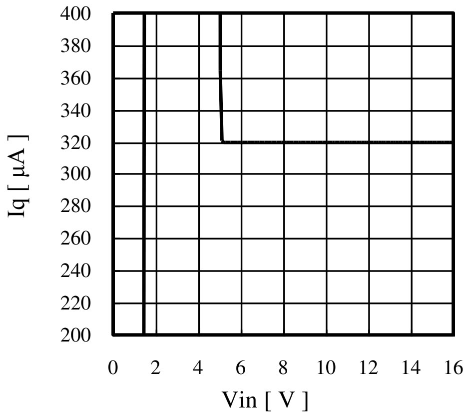
■ Line Regulation (AP1154ADL50)



■ I_Q vs Vin (AP1154ADL25)



■ I_Q vs Vin (AP1154ADL50)



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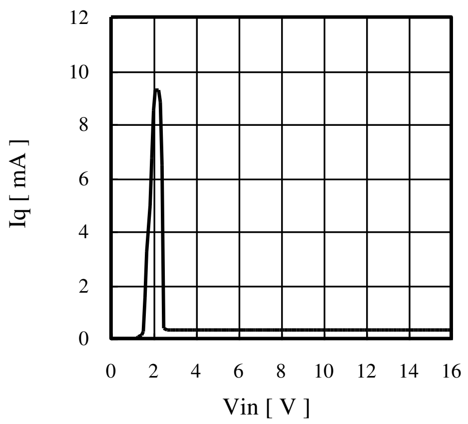

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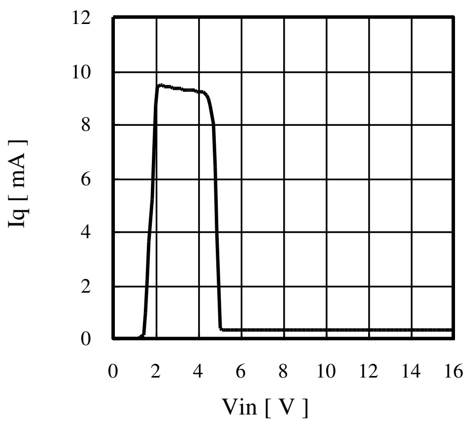
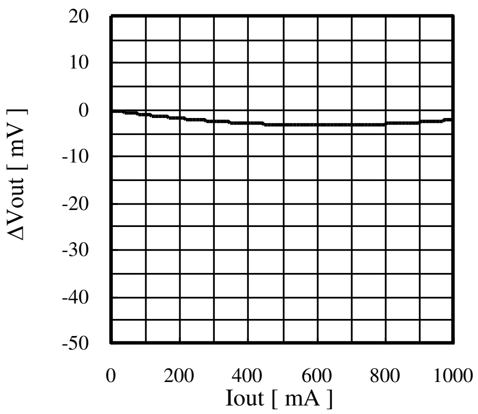


■ Load Regulation (AP1154ADL25)



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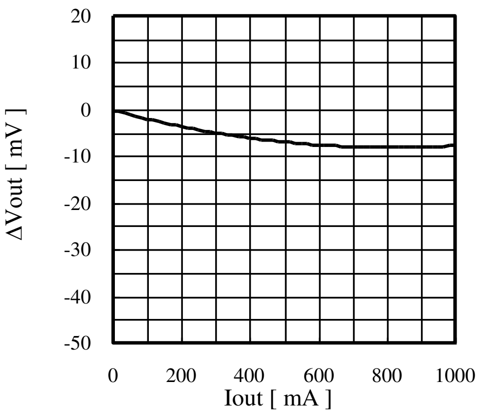
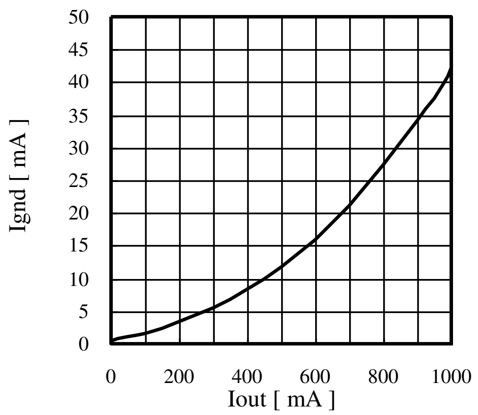


■ I_{GND} vs I_{Out} (AP1154ADL25)



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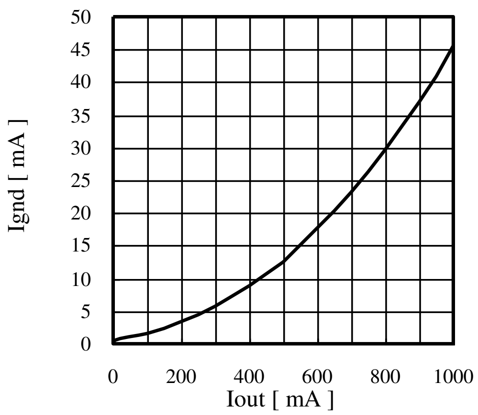
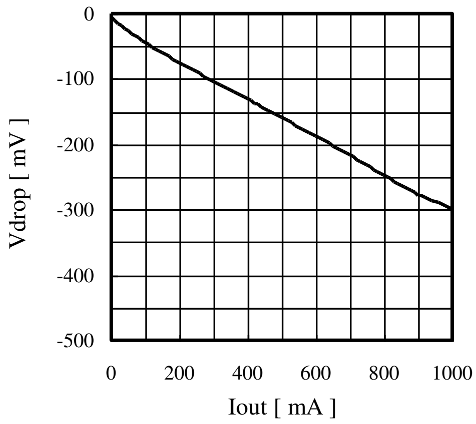


■ V_{Drop} vs I_{Out} (AP1154ADL25)



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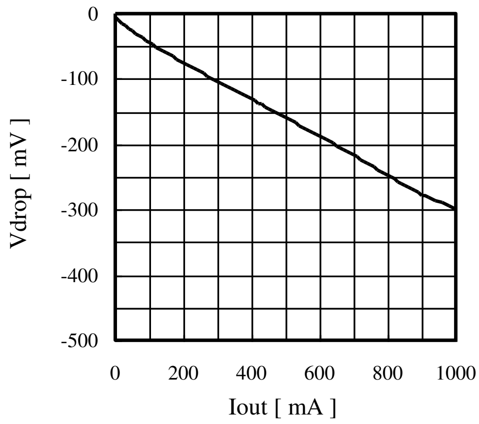
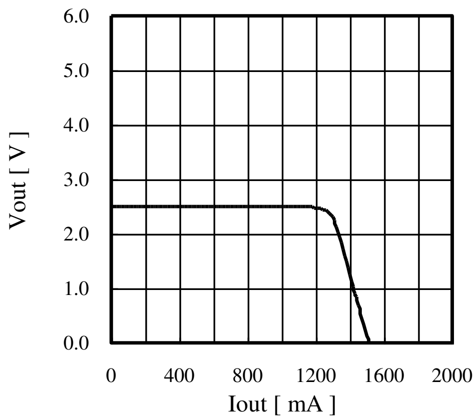
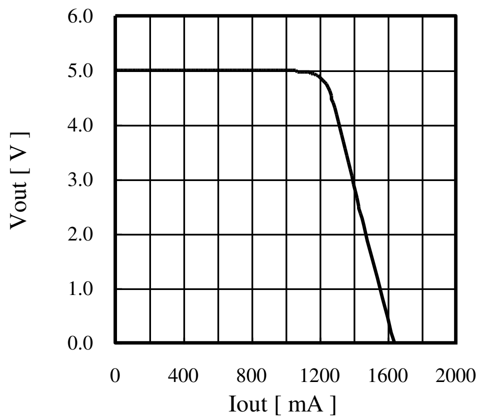


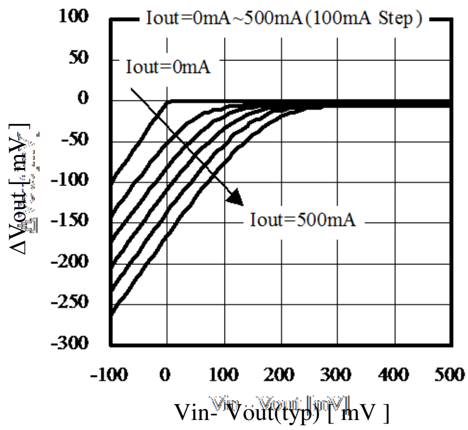
■ Vout vs I_{Out} (AP1154ADL25)



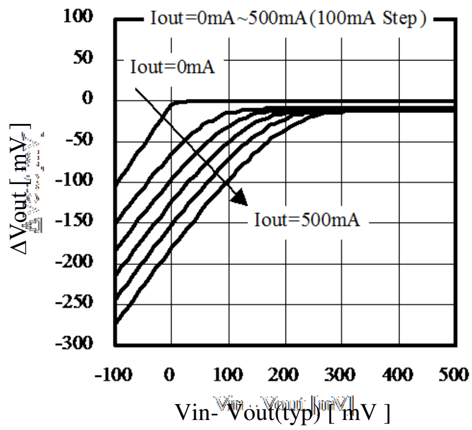
■ Vout vs I_{Out} (AP1154ADL50)



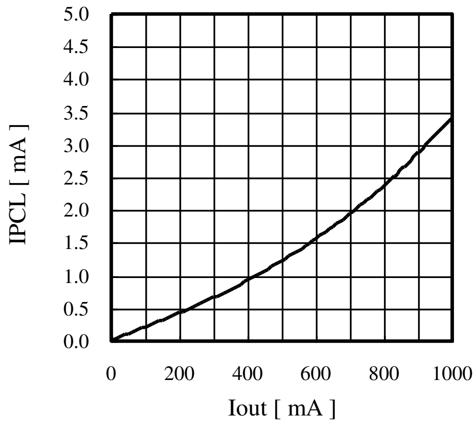
■ ΔVout vs ΔVin (AP1154ADL25)



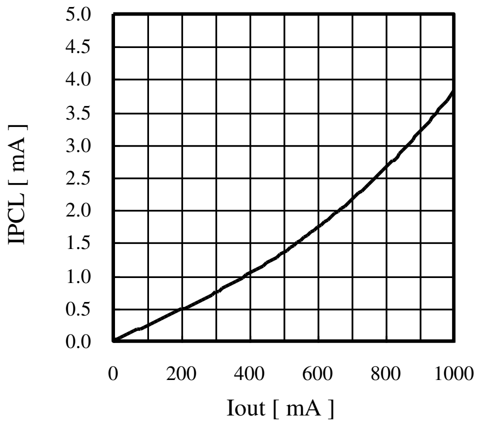
■ ΔVout vs ΔVin (AP1154ADL50)



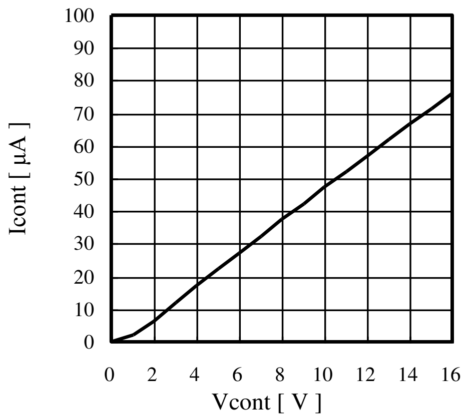
■ PCL terminal current (I_{PCL}) vs I_{Out}
(AP1154ADL25)



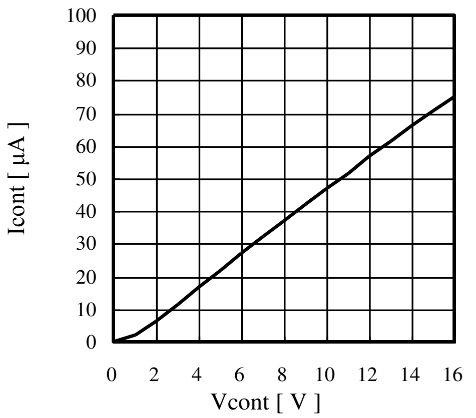
■ PCL terminal current (I_{PCL}) vs I_{Out}
(AP1154ADL50)



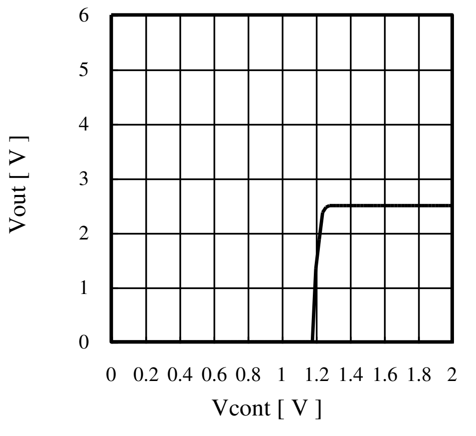
■ I_{Cont} vs V_{Cont} (AP1154ADL25)



■ I_{Cont} vs V_{Cont} (AP1154ADL50)



■ Vout vs V_{Cont} (AP1154ADL25)



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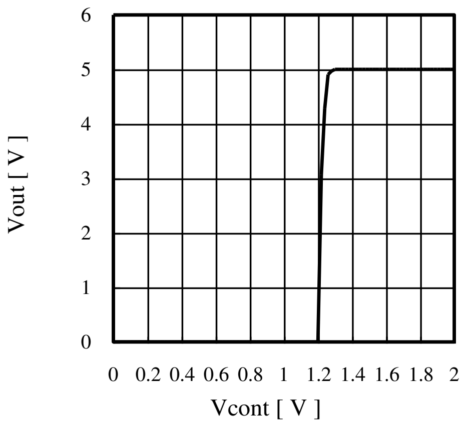
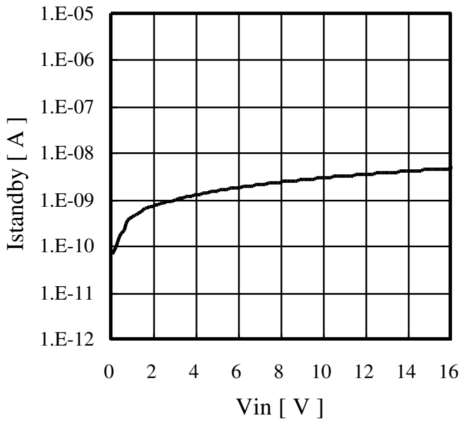
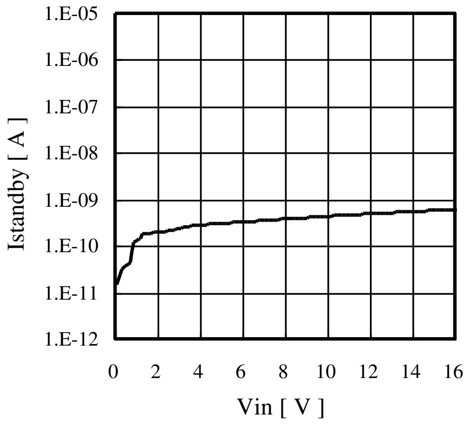


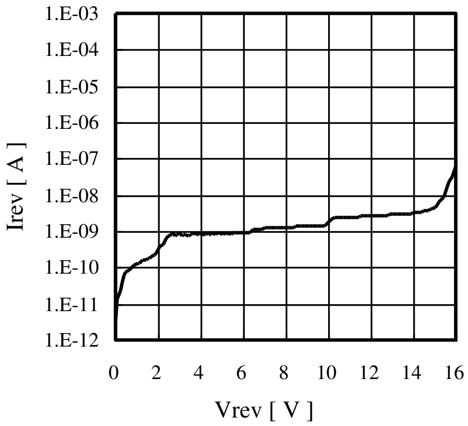
■ $I_{Standby}$ vs Vin (AP1154ADL25)



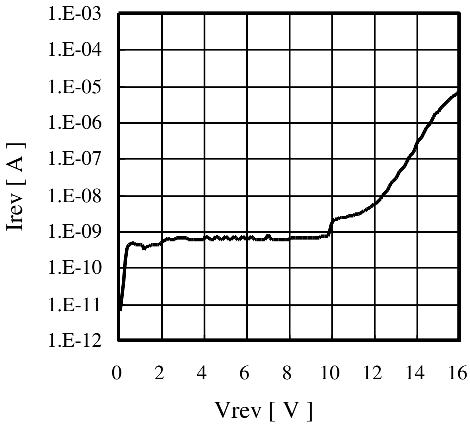
■ $I_{Standby}$ vs Vin (AP1154ADL50)



■ I_{Rev} vs V_{Rev} (AP1154ADL25)

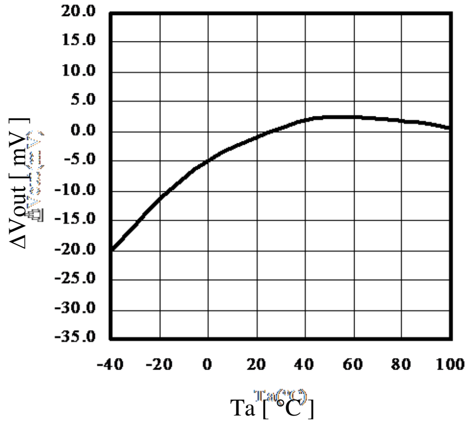


■ I_{Rev} vs V_{Rev} (AP1154ADL50)

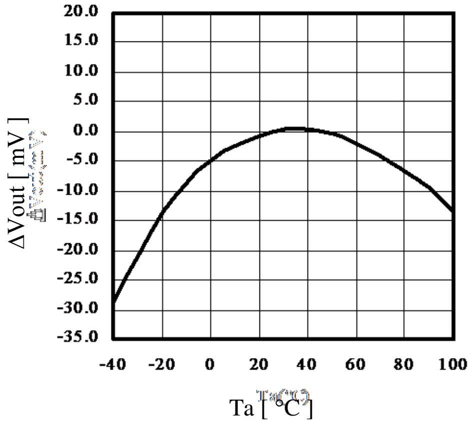


・Temperature Characteristics

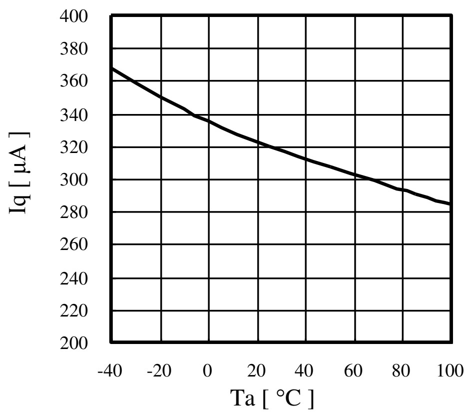
■ ΔVout vs T_a (AP1154ADL25)



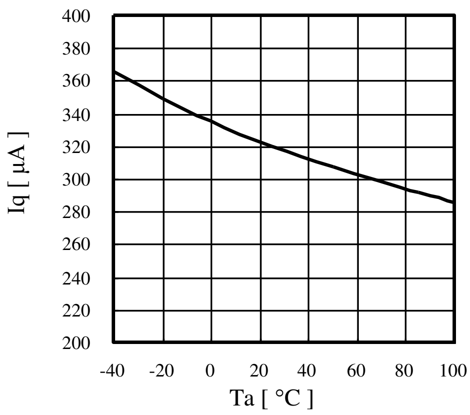
■ ΔVout vs T_a (AP1154ADL50)



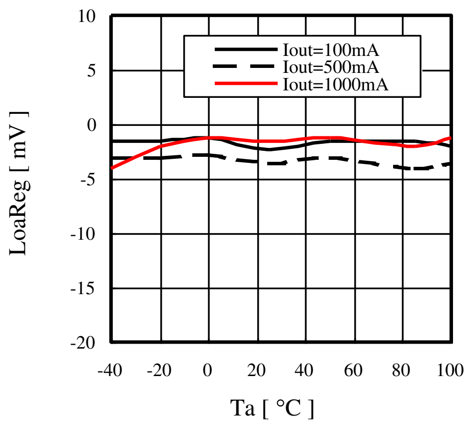
■ I_Q vs T_a (AP1154ADL25)



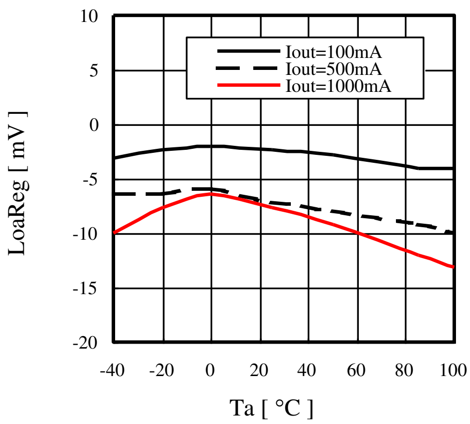
■ I_Q vs T_a (AP1154ADL50)



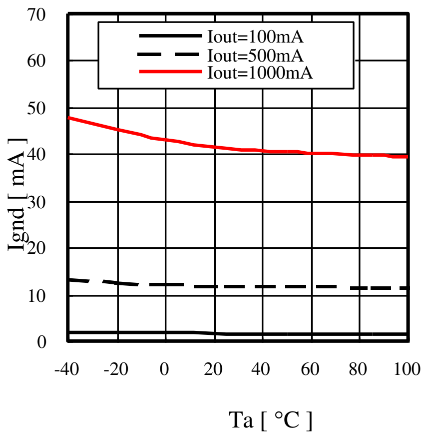
■ LoaReg vs T_a (AP1154ADL25)



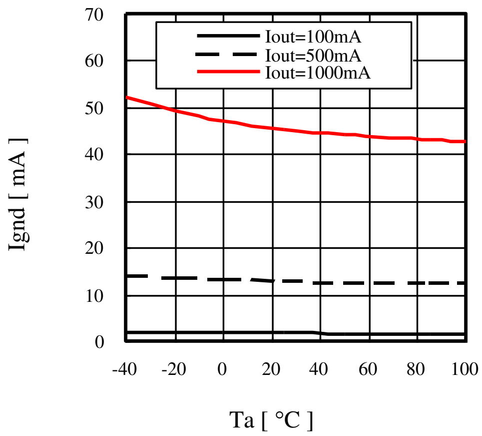
■ LoaReg vs T_a (AP1154ADL50)



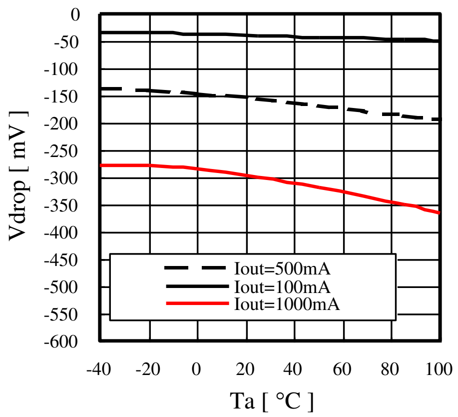
■ I_{GND} vs T_a (AP1154ADL25)



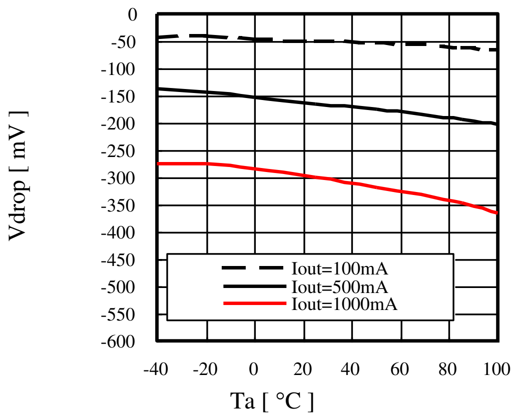
■ I_{GND} vs T_a (AP1154ADL50)



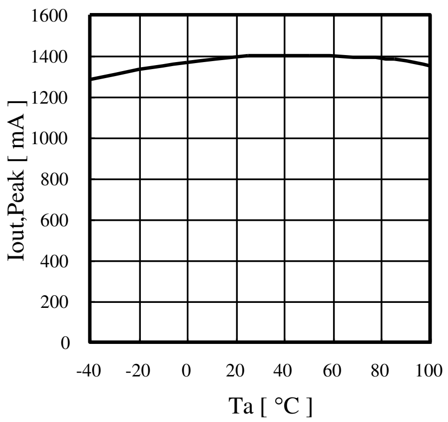
■ V_{Drop} vs T_a (AP1154ADL25)



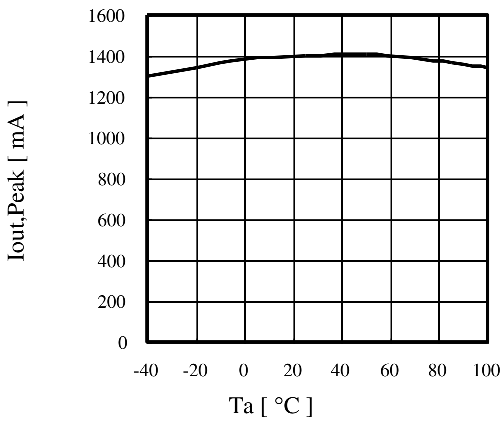
■ V_{Drop} vs T_a (AP1154ADL50)



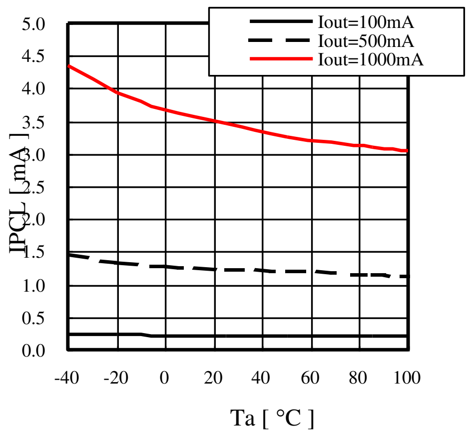
■ $I_{Out,MAX}$ vs T_a (AP1154ADL25)



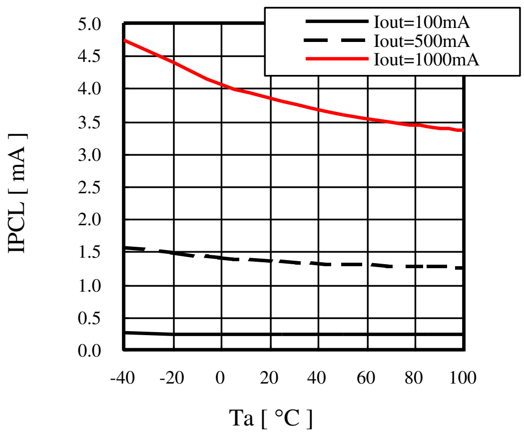
■ $I_{Out,MAX}$ vs T_a (AP1154ADL50)



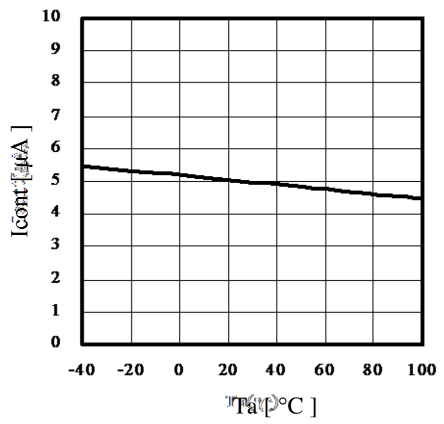
■ I_{PCL} vs T_a (AP1154ADL25)



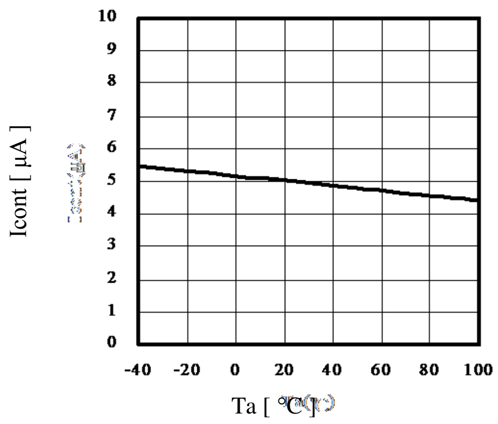
■ I_{PCL} vs T_a (AP1154ADL50)



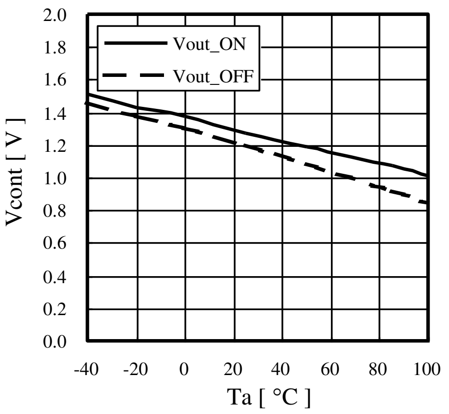
■ I_{Cont} vs T_a (AP1154ADL25) (Vcont=1.8V)



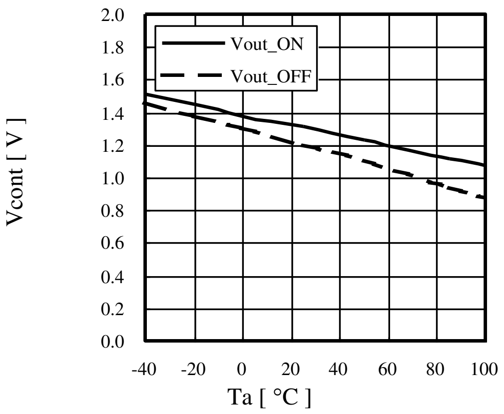
■ I_{Cont} vs T_a (AP1154ADL50) (Vcont=1.8V)



■ Vout On/Off Point vs T_a (AP1154ADL25)

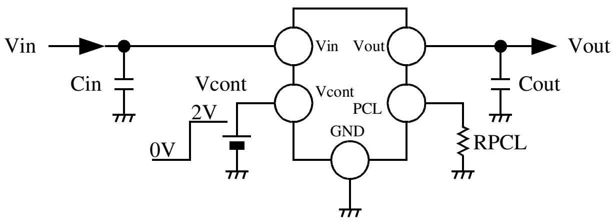


■ Vout On/Off Point vs T_a (AP1154ADL50)



11.2 ON/OFF Transient

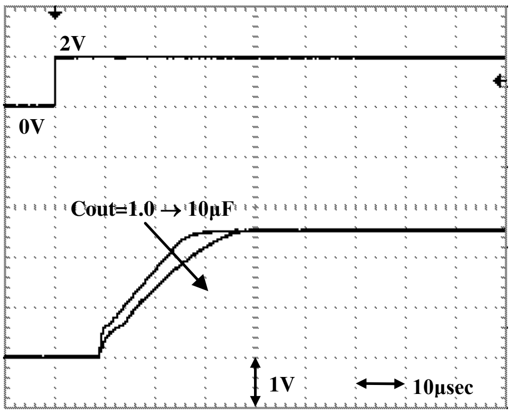
Measurement circuit



Measurement Condition

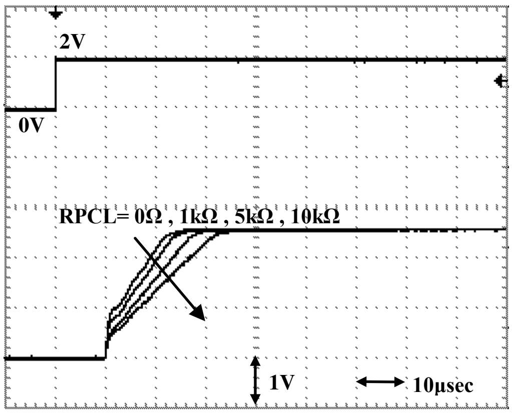
Vin = Vout(typ) + 1V
Vcont = 0V → 2V (f = 10Hz)
Iout = 1000mA
Cin = 1μF
Cout = 1μF
RPCL = 0Ω

■AP1154ADL25 Cout : 1μF , 10μF



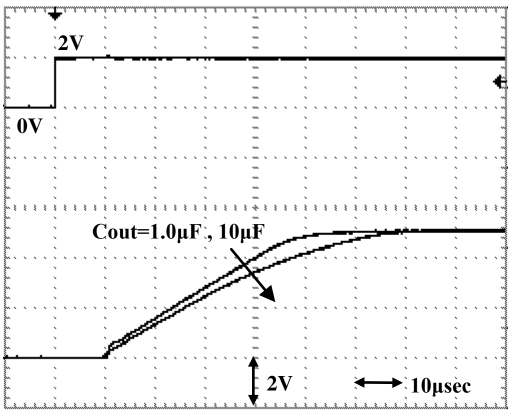
Vertical axis:1V/Div, Horizontal axis:10μsec/Div

■AP1154ADL25
RPCL : 0Ω ~ 10kΩ , Iout=50mA



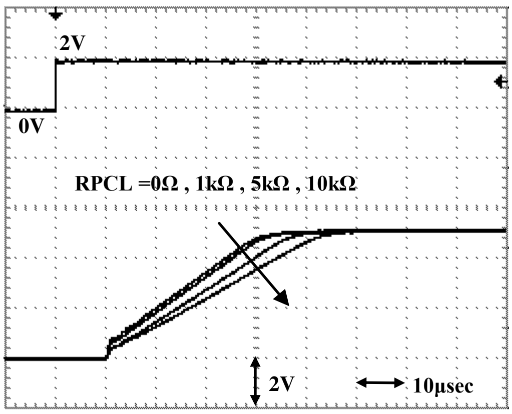
Vertical axis:1V/Div, Horizontal axis:10μsec/Div

■AP1154ADL50 Cout : 1μF , 10μF



Vertical axis:1V/Div, Horizontal axis:10μsec/Div

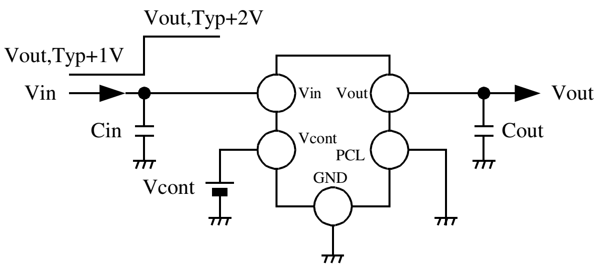
■AP1154ADL50
RPCL : 0Ω ~ 10kΩ , Iout=50mA



Vertical axis:1V/Div, Horizontal axis:10μsec/Div

11.3 Line transient

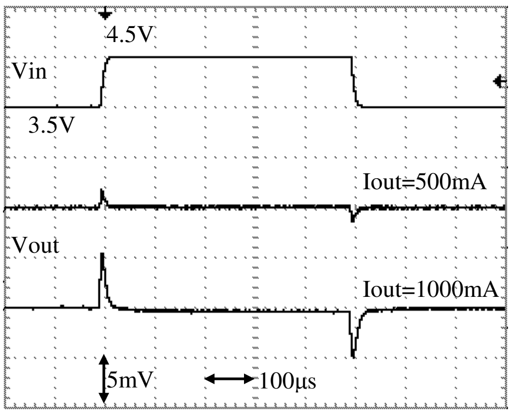
Measurement circuit



Measurement condition

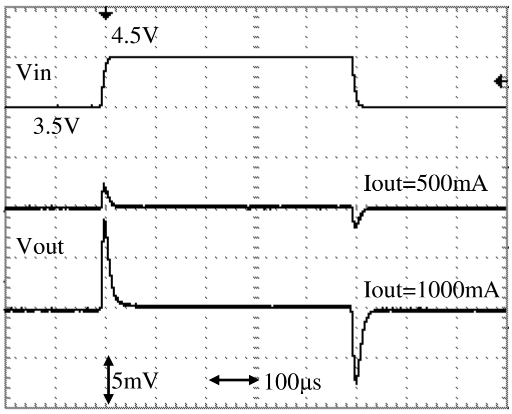
Vin = Vout(typ) + 1V → Vout(typ) + 2V (f = 1kHz)
Vcont = 2V
Cin = 1μF
Cout = 1μF
RPCL = 0Ω

■AP1154ADL25



Vertical axis: 5mV/Div, Horizontal axis:100μsec/Div

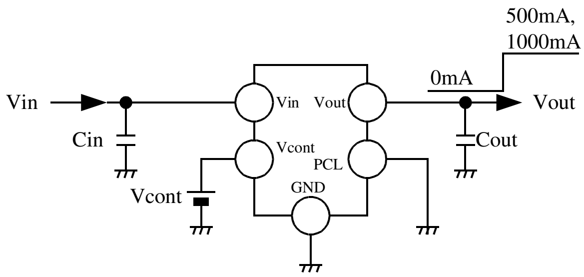
■AP1154ADL50



Vertical axis: 5mV/Div, Horizontal axis:100μsec/Div

11.4 Load transient

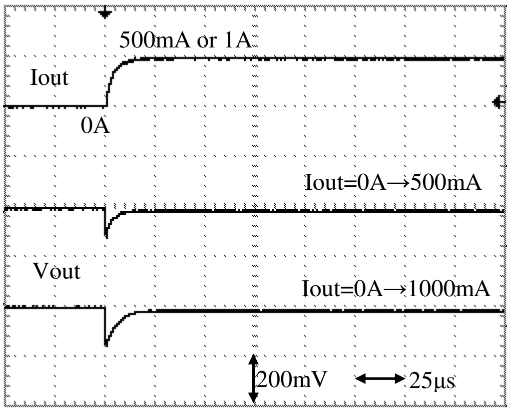
Measurement circuit



Measurement condition

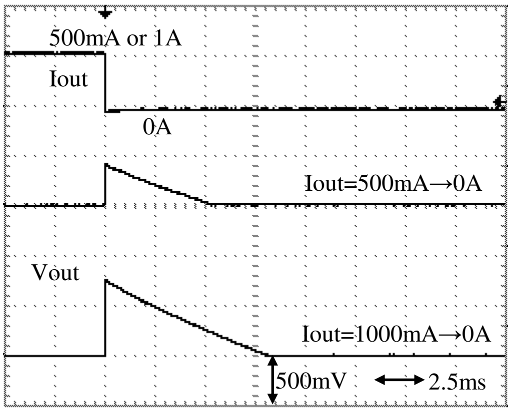
Vin = Vout(typ) + 1V
Vcont = 2V
Cin = 1µF
Cout = 1µF
RPCL = 0Ω

■AP1154ADL25
Iout:0A→500mA, 1000mA (Freq=10Hz)



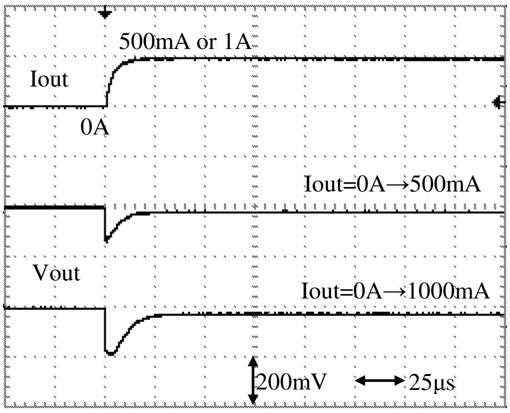
Vertical axis: 200mV/Div, Horizontal axis:25µsec/Div

■AP1154ADL25
Iout:500mA, 1000mA→0A (Freq=10Hz)



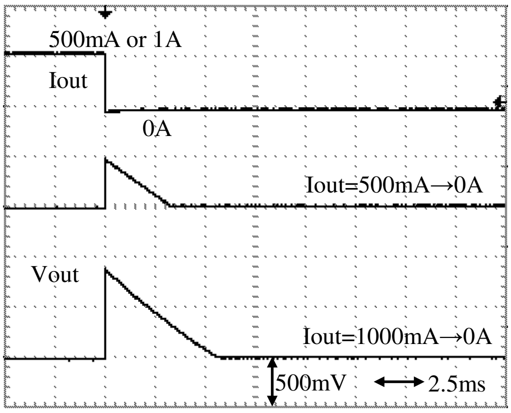
Vertical axis: 500mV/Div, Horizontal axis:2.5msec/Div

■AP1154ADL50
Iout:0A→500mA, 1000mA (Freq=10Hz)



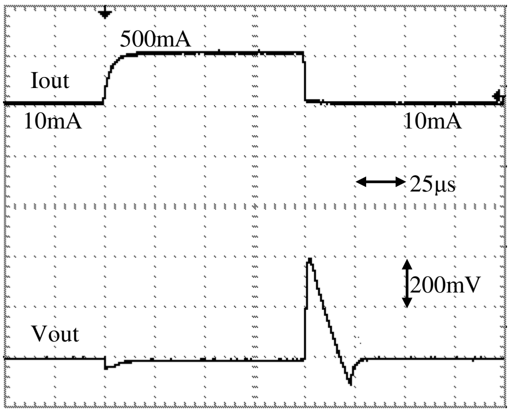
Vertical axis: 200mV/Div, Horizontal axis:25µsec/Div

■AP1154ADL50
Iout:500mA, 1000mA→0A (Freq=10Hz)



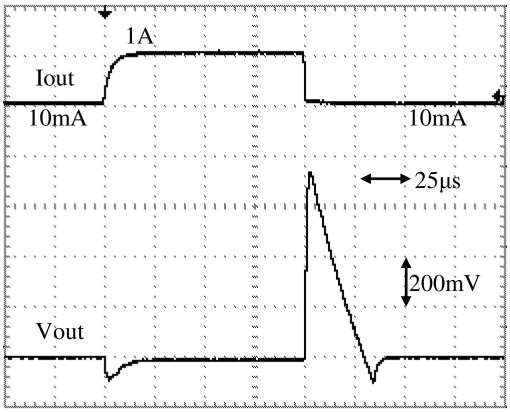
Vertical axis: 500mV/Div, Horizontal axis:2.5msec/Div

■AP1154ADL25
Iout:10mA→500mA→10mA(Freq=5kHz)



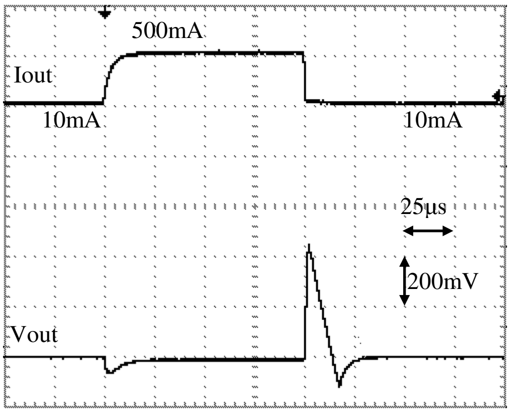
Vertical axis: 200mV/Div, Horizontal axis:25μsec/Div

■AP1154ADL25
Iout:10mA→1000mA→10mA(Freq=5kHz)



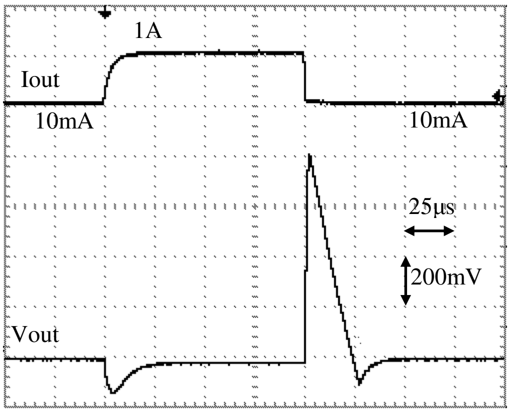
Vertical axis: 200mV/Div, Horizontal axis:25μsec/Div

■AP1154ADL50
Iout:10mA→500mA→10mA(Freq=5kHz)



Vertical axis:200mV/Div, Horizantal axis:25μsec/Div

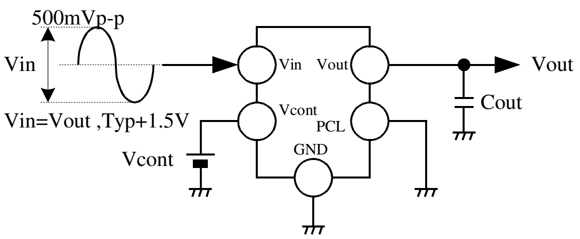
■AP1154ADL50
Iout:10mA→1000mA→10mA(Freq=5kHz)



Vertical axis:200mV/Div, Horizantal axis:25μsec/Div

11.5 Ripple Rejection

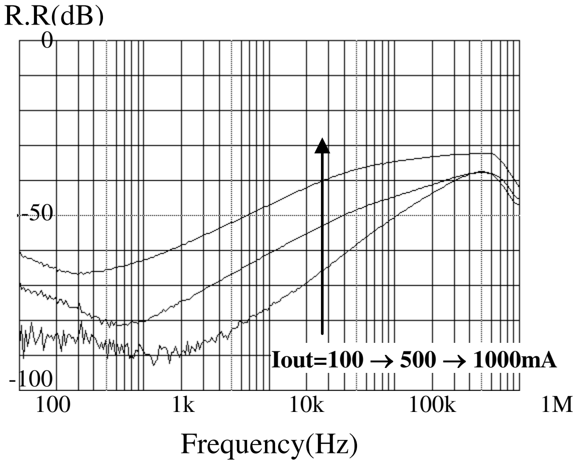
Measurement circuit



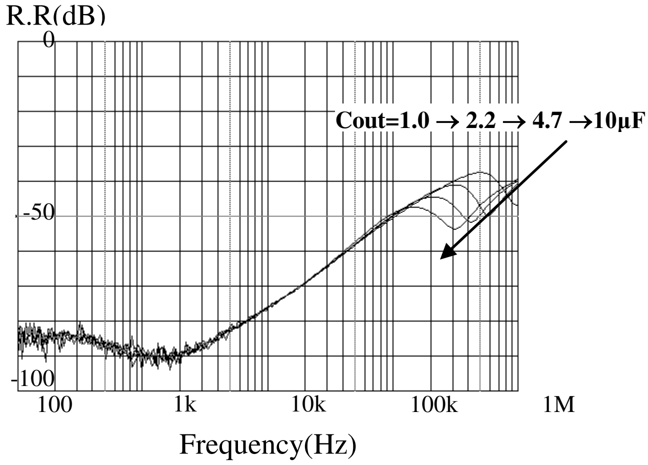
Measurement condition

Vin = Vout(typ) + 1.5V
Ripple Noise = 500mVp-p (f = 1kHz , Sine wave)
Vcont = 2V
Iout=100mA
Cin : None
Cout = 1µF
RPCL = 0Ω

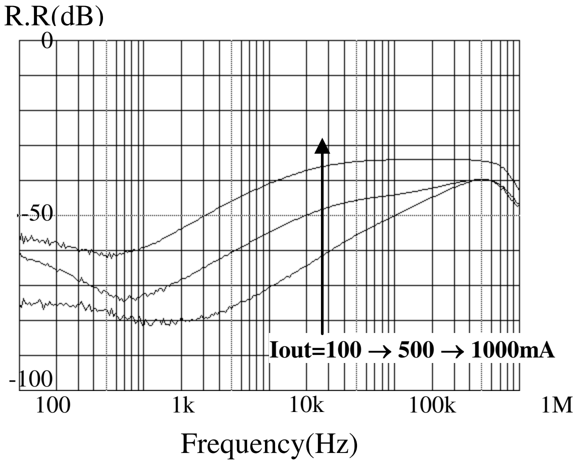
■AP1154ADL25 Iout=100mA ~ 1A



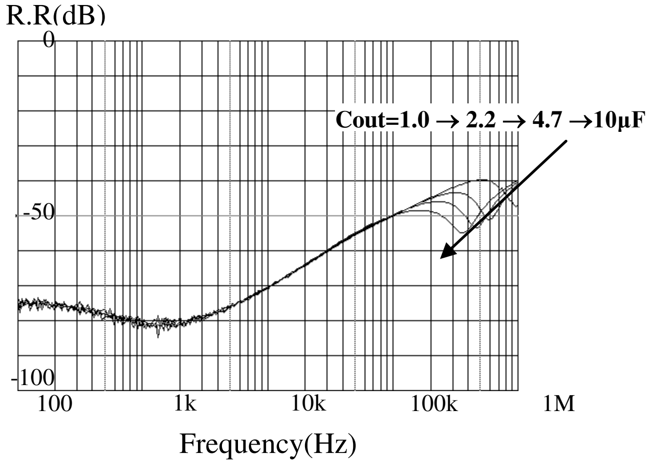
■AP1154ADL25 Cout=1.0µF ~ 10µF



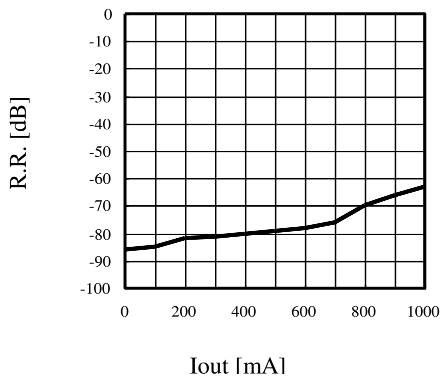
■AP1154ADL50 Iout=100mA ~ 1A



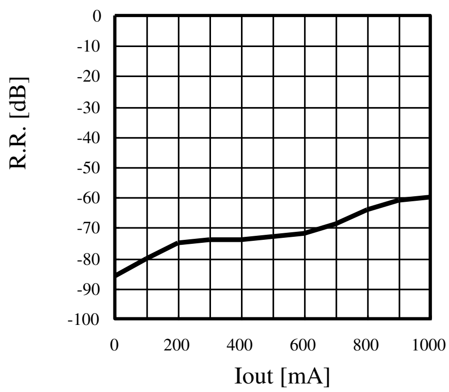
■AP1154ADL50 Cout=1.0µF ~ 10µF



■AP1154ADL25 Iout=1mA~1A , f=1kHz

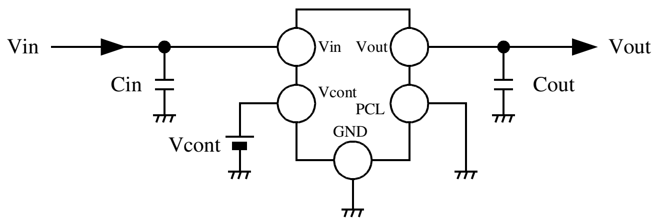


■AP1154ADL50 Iout=1mA~1A , f=1kHz



11.6 Output Noise

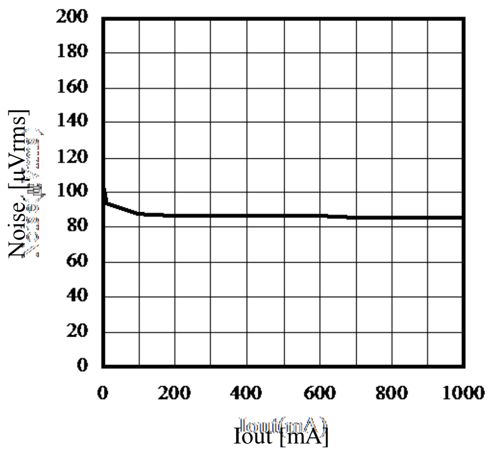
Measurement circuit



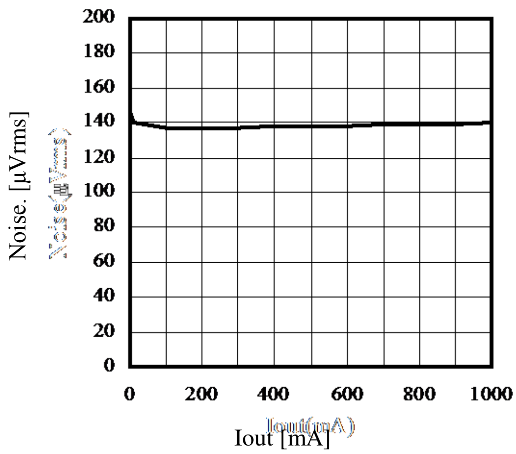
Measurement condition

Vin = Vout(typ) + 1V
Vcont = 2V
Cin = 1µF
Cout = 1µF
RPCL = 0Ω

■AP1154ADL25 (f = 10 ~ 100kHz)

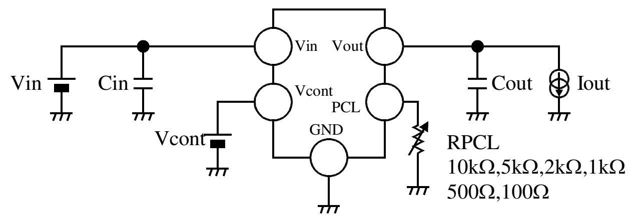


■AP1154ADL50 (f = 10 ~ 100kHz)

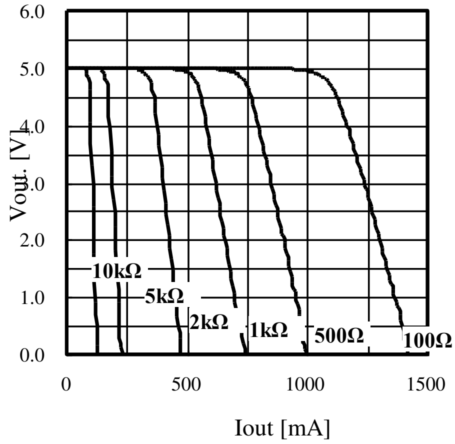


11.7 Setting of output current limitation

The output current limit can be set by connecting an external resistance (R_{PCL}) between the PCL terminal and GND. If there is no need of setting a current limit, connect the PCL terminal to GND

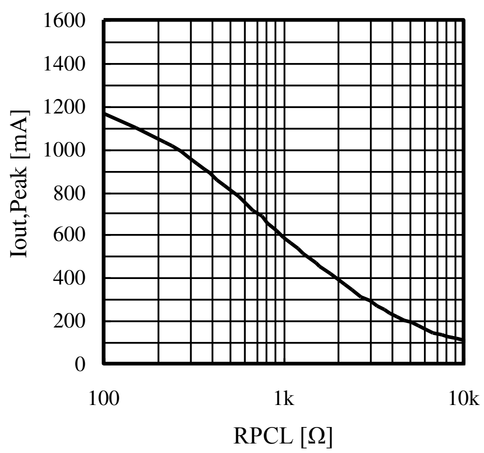


■AP1154ADL50 Iout,Peak vs Iout with R_{PCL}

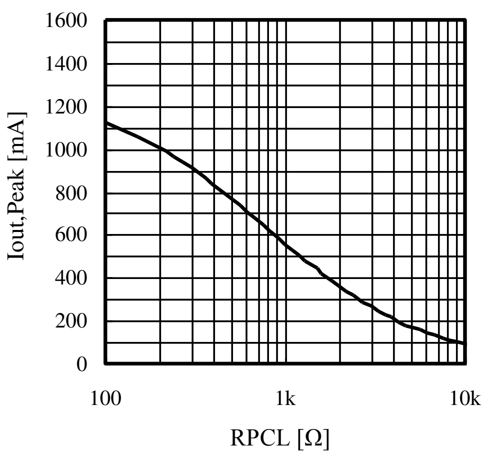


The below figures show relation between R_{PCL} value and Iout,Peak at Vin=Vout(typ)+1V , Ta=25°C

■AP1154ADL25 Iout,Peak vs R_{PCL}



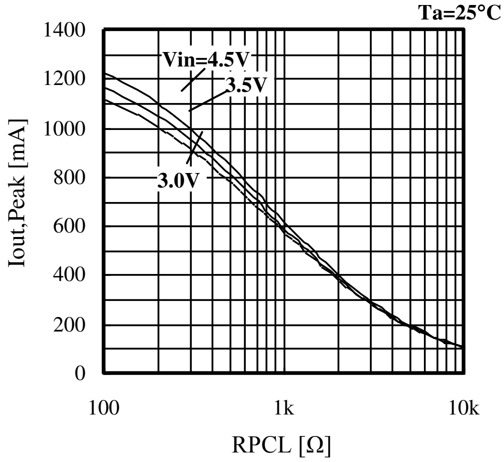
■AP1154ADL50 Iout,Peak vs R_{PCL}



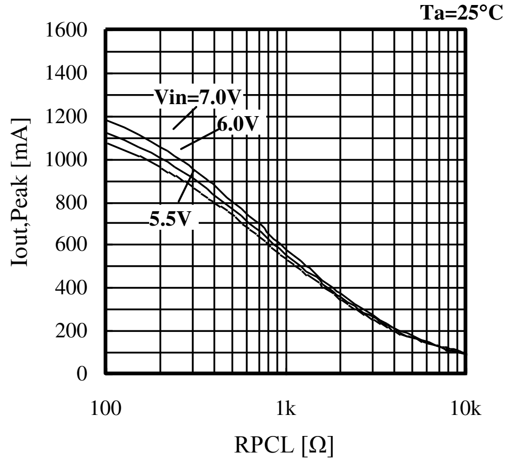
* Iout,Peak : Output current at 10% drop from typical output voltage.

Relation between RPCL and IoutPeak has variation based on the supply voltage and the ambient temperature. Please ensure the suitable value on the environment.

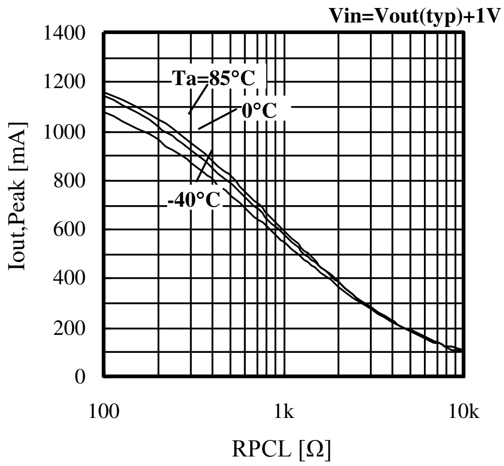
■AP1154ADL25 Iout,Peak vs R_{PCL} with Vin



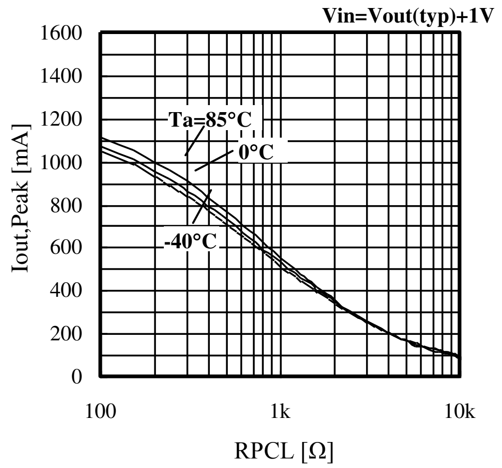
■AP1154ADL50 Iout,Peak vs R_{PCL} with Vin



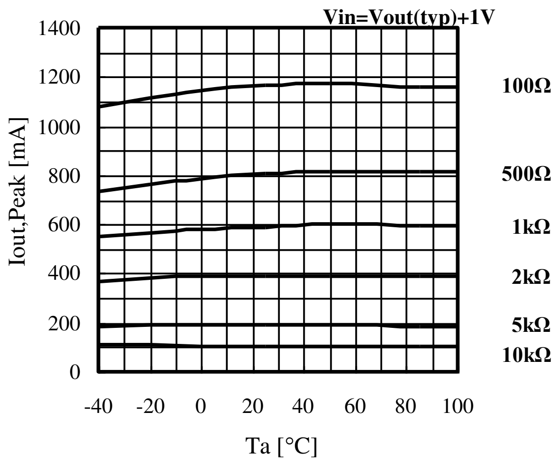
■AP1154ADL25 Iout,Peak vs R_{PCL} with Ta



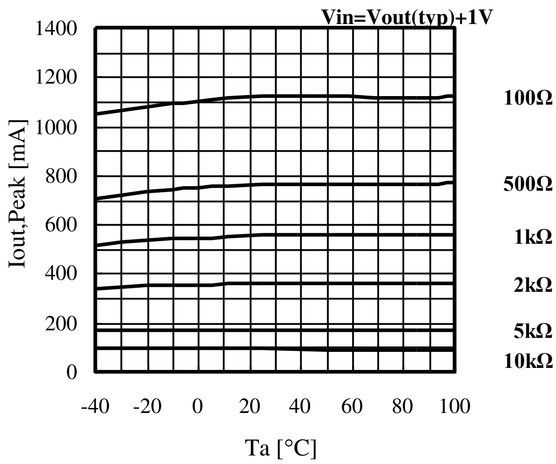
■AP1154ADL50 Iout,Peak vs R_{PCL} with Ta



■AP1154ADL25 Iout,Peak vs Ta with R_{PCL}



■AP1154ADL50 Iout,Peak vs Ta with R_{PCL}



11.8 Stability

The standard capacitor recommended for use on the output side is a ceramic capacitor equal to or greater than 1.0μF. For operations at 2.4V or less, use at least a 2.2μF capacitor.

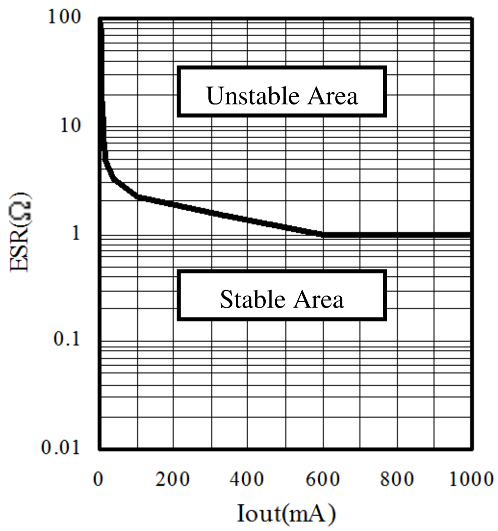


Figure 2. Stable operation area (C_{Out}≥0.47μF)

Figure 2 indicates that operation is stable in the entire current range with a resistance of 1Ω or less (equivalent series resistance or 'ESR') connected in series to the output capacitor. Generally, the ESR of a ceramic capacitor is very low (several tens of mΩ), and no problems should arise in actual use. If an application requires use of a large ESR capacitor, connecting a ceramic capacitor with low ESR in parallel will enable operations at this level. When parallel output capacitors are used, be sure to position the ceramic capacitor as close to the IC as possible. The other capacitor connected in parallel may be located away from the IC. The IC will not be damaged by the increased capacitance.
Input capacitors are necessary when the power supply impedance increases due to battery depletion or when the line to the power supply is particularly long. There is no general rule that can be used to determine the required number of capacitors used for such purposes. In some cases, only one capacitor is necessary for several regulator ICs. In some cases, one capacitor is required for each IC. To determine the required number of capacitors in a specific application, be sure to verify operation with all parts in the installed configuration.
Ceramic capacitors normally have specific temperature and voltage characteristics. Be sure to take the operating voltage and temperature into consideration when selecting parts for use. We recommend parts featuring B characteristics.

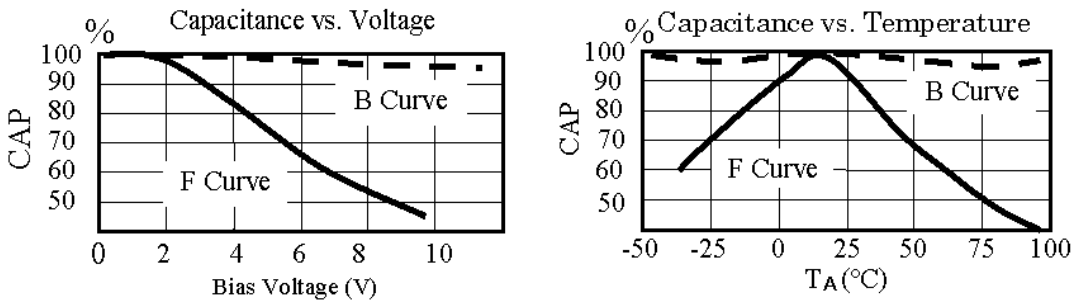


Figure 3. Example Ceramic Capacitance vs. Bias Voltage, Temperature

For evaluation
Kyocera : CM05B104K10AB , CM05B224K10AB , CM105B104K16A , CM105B224K16A , CM21B225K10A
Murata : GRM36B104K10 , GRM42B104K10 , GRM39B104K25 , GRM39B224K10 , GRM39B105K6.3

11.9 Operating Region and Power Dissipation

Power dissipation capability is limited by the junction temperature that triggers the built-in overheat protection circuit. Therefore, power dissipation capability is regarded as an internal limitation. The package itself does not offer high heat dissipation because of its small size. The package is, however, designed to release heat effectively when mounted on the PCB. Therefore, the heat-dissipation value will vary depending on the material, copper pattern, etc. of the PCB on which the package is mounted.
When the regulator loss is large (high ambient temperature, poor heat radiation), the overheat protection circuit is activated. When this occurs, output current cannot be obtained, and an output voltage drop is observed. When the junction temperature reaches the set value, the IC stops operating. However, after the IC has stopped operation and the junction temperature lowers sufficiently, the IC restarts operation immediately.

The thermal resistance when mounted on PCB

The chip junction temperature during operation is expressed by

$$T_j = \theta_{ja} \times P_D + T_a$$

The junction temperature of the AP1154ADLxx is limited to approximately 145°C by the overheat protection circuit. P_D is the value observed when the overheat protection circuit is activated. The following example is based on an ambient temperature of 25°C.

$$145 = \theta_{ja} \times P_D + 25$$

$$\theta_{ja} \times P_D = 120$$

$$\theta_{ja} = \frac{120}{P_D} \ (°C/W)$$

Glass epoxy substrate with double-layer wiring
(x=30mm, y=30mm, t=1.0mm, copper pattern thickness: 35μm)

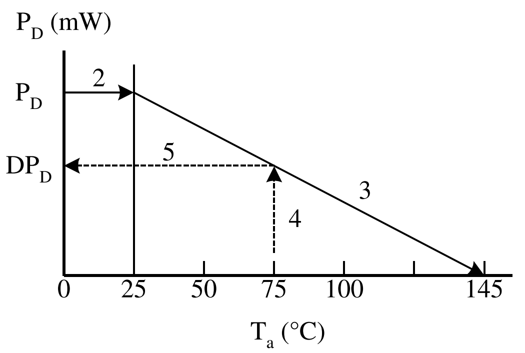
AP1154ADLXX (HSOP-8)

P_D is 2400mW. If the temperature exceeds 25°C, be sure to derate at -20mW/°C.

Method of obtaining Pd easily

With the output terminal shorted-circuited to GND, gradually increase the input voltage and measure the input current. Slowly increase the input voltage to about 10V. The initial input current value becomes the maximum instantaneous output current value, but gradually lowers as the chip temperature rises, and ultimately reaches a state of thermal equilibrium (through natural air cooling).
P_D is calculated using the input value for input current and the input voltage value in the equilibrium state.

$$P_D \cong V_{In} \times I_{In}$$



Procedure (conducted at the time of installation on PCB)
1: Obtain P_D ($V_{In} \times I_{In}$ when output is short-circuited).
2: Plot P_D on the 25°C line.
3: Draw a straight line between P_D and the 145°C line.
4: Extend a straight-line perpendicular from the point of the designed maximum operating temperature (for example, 75°C).
5: Extend a line to the left from the intersection of the derating curve and the line drawn in 4, and read the P_D value (this value is DP_D).
6: $DP_D \div (V_{In,MAX} \times V_{Out}) = I_{Out}$ at 75°C

The maximum operating current at the maximum temperature is as follows:

$$I_{Out} \cong \{DP_D \div (V_{In,MAX} - V_{Out})\}$$

Try to achieve maximum heat dissipation in your design in order to minimize the part's temperature during operation. Generally, lower part temperatures result in higher reliability in operation.