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Description

The AP3302 is a Peak-Current control, Quasi-Resonant (QR) PWM controller which is optimized for high performance, low standby power and cost effective offline flyback converters.

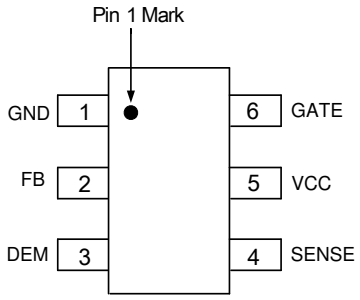
At no load or light load, the IC will enter the burst mode to minimize standby power consumption. The minimum switching frequency (about 22kHz) is set to avoid the audible noise. When the load increases, the IC will enter valley lock QR mode with frequency foldback to improve system efficiency and EMI performance. The maximum switching frequency (about 120kHz) is set to clamp the QR frequency to reduce switching power loss. Furthermore, the frequency dithering function is built in to reduce EMI emission.

Internal piecewise linear line compensation ensures constant output power limit over entire universal line voltage range.

Comprehensive protection features are included, such as brown out protection, cycle-by-cycle current limit (OCP), V_{CC} Over Voltage Protection (VOVP), Secondary-side Output OVP (SOVP) and UVP (SUVP), internal OTP, Over Load Protection (OLP) and pins' fault protection.

Pin Assignments

(Top View)



SOT26

Features

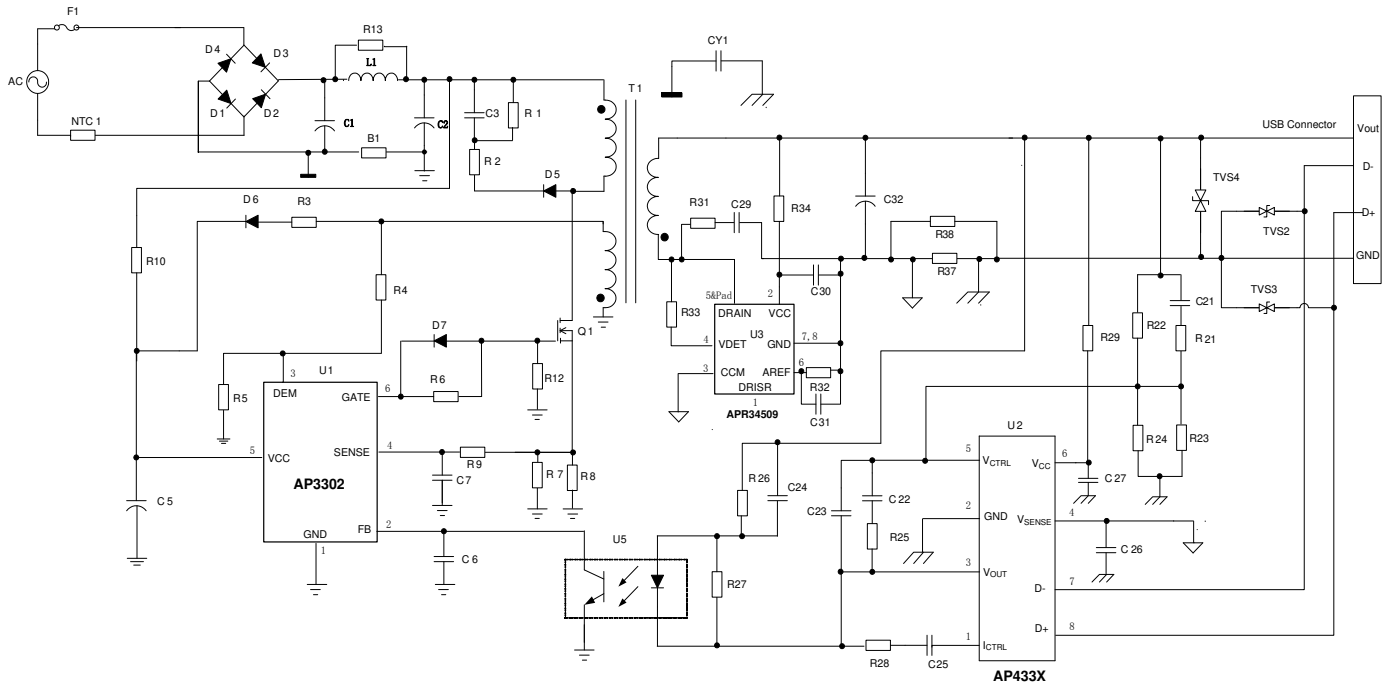
- Very Low Start-Up Current
- Quasi-Resonant Operation with Valley Lock under All Line and Load Condition
- Non-Audible-Noise Quasi-Resonant Control
- Soft Start During Startup Process
- Frequency Fold Back for High Average Efficiency
- Constant Over Current Protection
- Secondary Winding Short Protection with FOCP
- Frequency Dithering for Reducing EMI
- V_{CC} Maintain Mode
- Useful Pin Fault Protection:
  SENSE Pin Floating
  FB/Opto-Coupler Open/Short
- Comprehensive System Protection Feature:
  V_{CC} Over Voltage Protection (VOVP)
  Over Load Protection (OLP)
- Brown Out Protection (BNO)
- Secondary Side OVP (SOVP) and UVP (SUVP)
- Mini Size Package of SOT26
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- Switching AC-DC Adapter/Charger
- ATX/BTX Auxiliary Power
- Set -Top Box (STB) Power Supply
- Open Frame Switching Power Supply

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

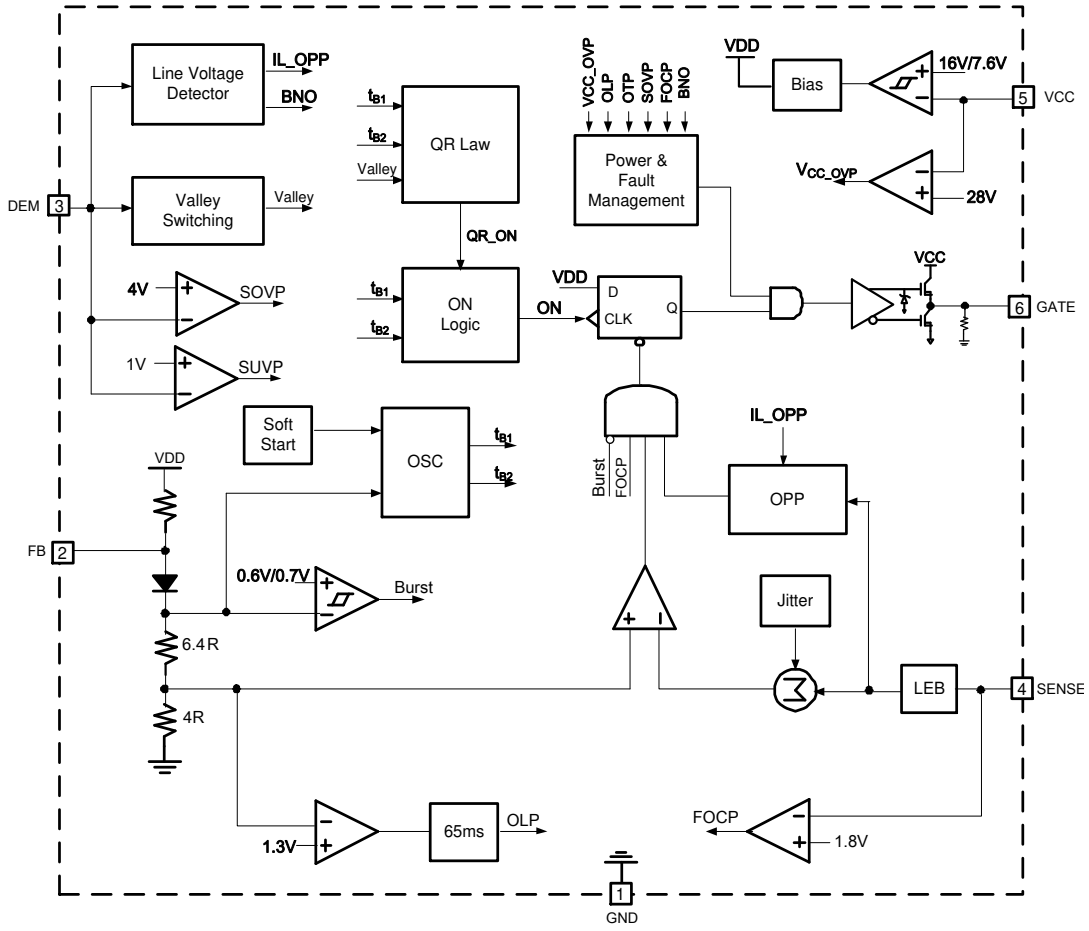
Typical Applications Circuit



Pin Descriptions

Pin Number	Pin Name	Function
1	GND	Signal ground. Current return for driver and control circuits
2	FB	Feedback. Directly connected to the opto-coupler
3	DEM	Valley detection for QR control, AC line voltage detection for Brown-in/Brown-out, Sample output voltage for SOVP and SUVP, Set OCP line compensation current.
4	SENSE	Current Sense
5	VCC	Supply voltage of driver and control circuits
6	GATE	Gate driver output

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{CC}	Power Supply Voltage	35	V
I_O	Gate Output Current	350	mA
V_{FB}, V_{SENSE}, V_{DEM}	Input Voltage to FB, SENSE,DEM	-0.3 to 7	V
θ_{JA}	Thermal Resistance (Junction to Ambient)	250	°C/W
P_D	Power Dissipation at T_A < +25°C	500	mW
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature Range	+150	°C
–	ESD (Human Body Model)	3000	V
–	ESD (Machine Model)	200	V

Note: 4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	10	28	V
T_A	Ambient Temperature	-40	+85	°C

Electrical Characteristics (@T_A = -40 to +85°C, V_{CC} = 18V, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage (VCC Pin)						
I_{ST}	Startup Current	–	–	1	5	μA
I_{CC}	Operating Supply Current	V_{FB} = 4V, C_L = 1nF (Note 5)	1.2	1.8	2	mA
$I_{CC-FAULT}$	Operating Current If Fault Occurs	V_{FB} = 4V, V_{CS} = 0V (Note 5)	0.25	0.4	0.55	
V_{ST}	Startup Voltage	–	14.5	15.8	16.5	V
V_M	V_{CC} Maintain	–	8.4	8.9	9.4	V
V_{UVLO}	Shutdown Voltage	–	7.1	7.6	8.1	V
V_{CC-OVP}	V_{CC} OVP	–	31	32	33	V
PWM Section/Oscillator Section						
$f_{OSC-MAX}$	Maximum Clamp Frequency	–	105	120	135	kHz
$f_{OSC-MIN}$	Minimum Clamp Frequency	–	18	22	25	kHz
Current Sense Section (SENSE Pin)						
V_{CS-MAX}	Maximum SENSE Voltage For Valley One	I_{DEM_SOURCE} = 150μA	0.89	0.96	1.04	V
$V_{TH-FOCP}$	FOCP Voltage	–	1.6	1.8	2.0	V
$t_{DELAY-FOCP}$	FOCP Debounce Time (Note 6)	–	–	6	–	Cycles
t_{LEB}	LEB Time of SENSE	–	150	250	350	ns
$t_{DELAY-CS}$	Delay to Output (Note 6)	–	–	150	–	ns
Feedback Input Section (FB Pin)						
K_{FB-CS}	The Ratio of Input Voltage to Current Sense Voltage	–	–	3	–	V/V
R_{FB}	Input Impedance	–	15	20	25	kΩ
$I_{FB-SOURCE}$	Source Current	V_{FB} = 0V	0.15	0.25	0.35	mA
G_{QR}	QR Mode Frequency Modulation Slope Versus V_{FB}	–	–	94	–	kHz/V
V_{BURST}	Threshold for Entering Burst Mode	–	1.35	1.55	1.75	V
V_{FB-OLP}	Over Load Protection	–	–	4.5	–	V
t_{ON-MAX}	Maximum on Time	–	17	20	24	μs
$t_{SOFT-ST}$	Soft-Start Time (Note 6)	–	–	5	–	ms
$t_{DELAY-OLP}$	Delay of Over Load Protection	–	–	70	–	ms

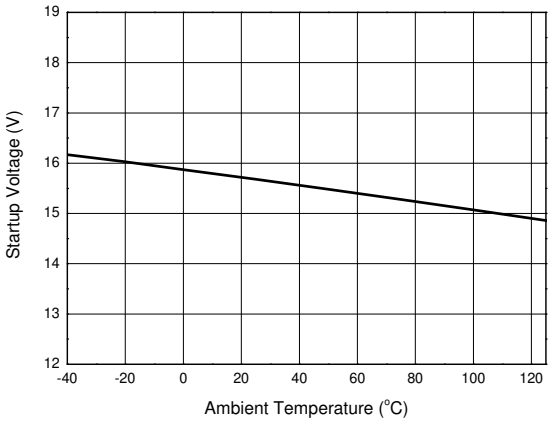
Electrical Characteristics (Cont.) (@T_A = -40 to +85°C, V_{CC} = 18V, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Output Section (GATE Pin)						
V_{GATE-L}	Output Low Level	I_O = 20mA, V_{CC} = 12V	–	–	1	V
V_{GATE-H}	Output High Level	I_O = 20mA, V_{CC} = 12V	8	–	–	V
$V_{GATE-CLP}$	Output Clamping Voltage	–	11	13	15	V
$t_{GATE-RISE}$	Rising Time (Note 6)	C_L = 1nF, V_{CC} = 13V	–	140	230	ns
$t_{GATE-FALL}$	Falling Time (Note 6)	C_L = 1nF, V_{CC} = 13V	–	50	120	ns
Demagnetization Section (DEM Pin)						
V_{TH-DEM}	De-Magnetization Voltage(Note 6)	–	–	75	–	mV
I_{BNI}	Brown In Reference	–	70	78	86	μA
I_{BNO}	Brown Out Reference	–	72	79	84	μA
$V_{TH-SOVP}$	SOVP Threshold	–	4.05	4.2	4.35	V
$V_{TH-SUVP}$	SUVP Threshold (Note 6)	–	–	1	–	V
t_{SAMPLE}	Sample Delay Time (Note 6)	–	–	1.85	–	μs
Delay Time Section						
$t_{DELAY-BNO}$	Brown Out Debounce Time	–	–	50	–	ms
$t_{DELAY-HICCUP}$	Delay of Hiccup Protection (Note 6)	SOVP, SUVP, Vcc OVP	–	6	–	Cycles
$t_{BLANK-SUVP}$	SUVP Blank Time After Startup	–	–	30	–	ms
Internal OTP Section						
OTP	OTP Threshold (Note 6)	–	–	+150	–	°C
T_{HYS}	OTP Recovery Hysteresis (Note 6)	–	–	+125	–	°C

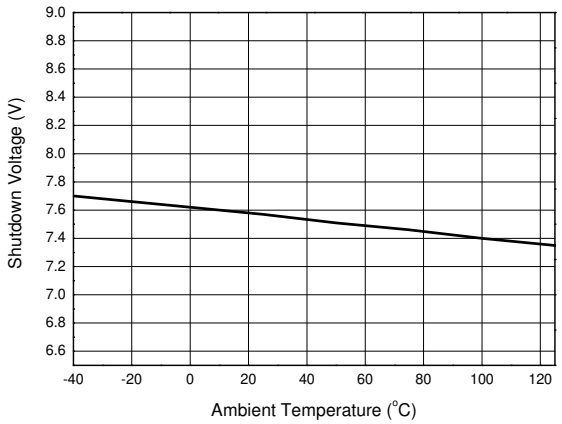
Notes: 5. Data measured in IC test mode.
6. Guaranteed by design.

Performance Characteristics

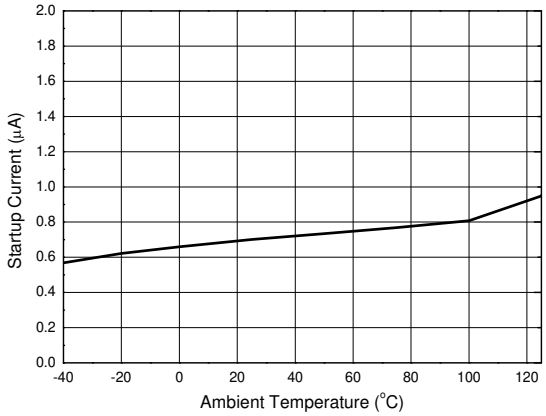
Startup Voltage vs. Ambient Temperature



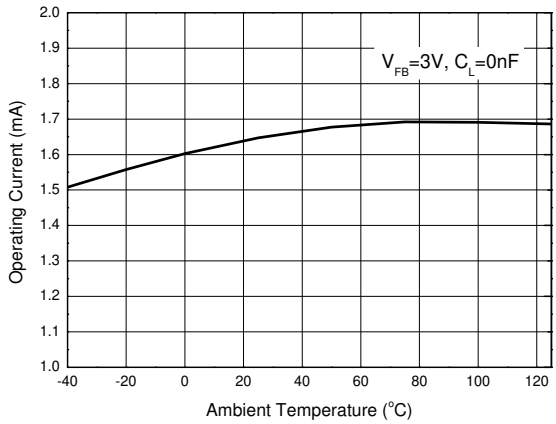
Shutdown Voltage vs. Ambient Temperature



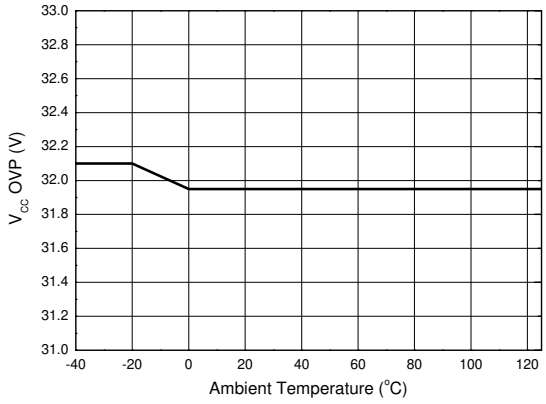
Startup Current vs. Ambient Temperature



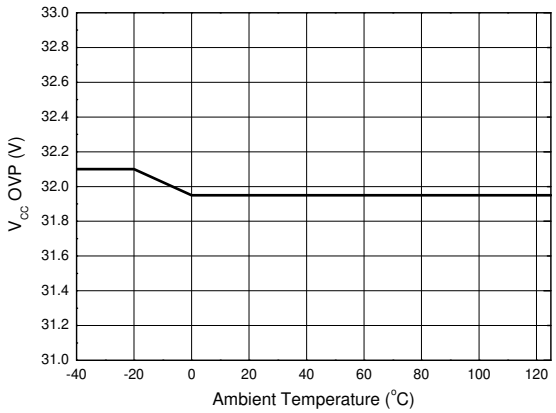
Operating Current vs. Ambient Temperature



V_{CC} OVP vs. Ambient Temperature

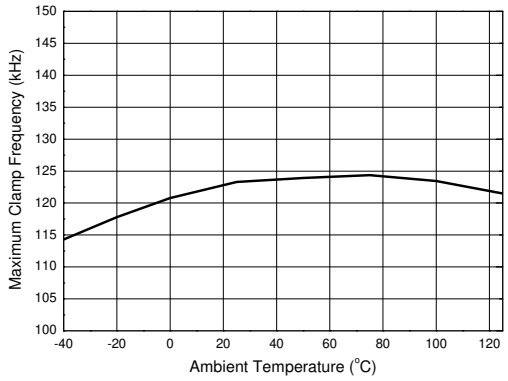


Green Mode Frequency vs. Ambient Temperature

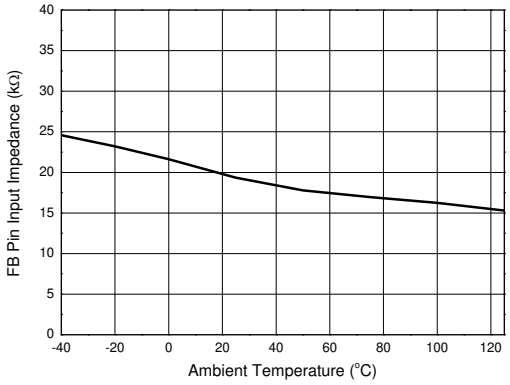


Performance Characteristics (Cont.)

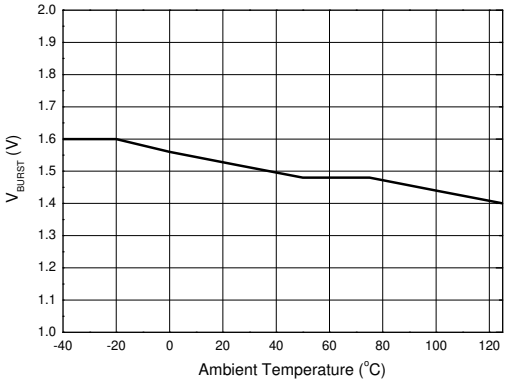
Maximum Clamp Frequency vs. Ambient Temperature



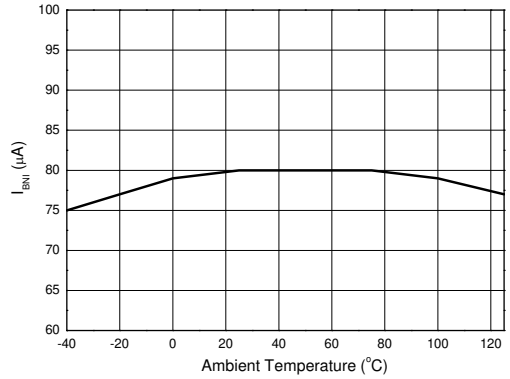
FB Pin Input Impedance vs. Ambient Temperature



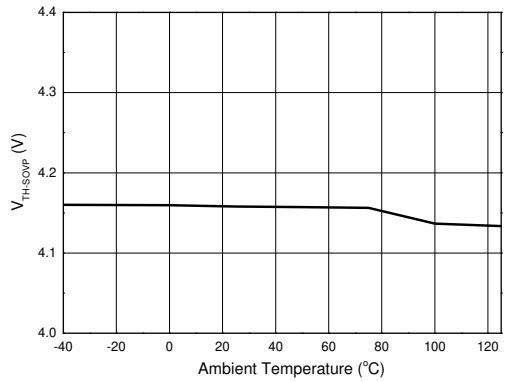
V_{BURST} vs. Ambient Temperature



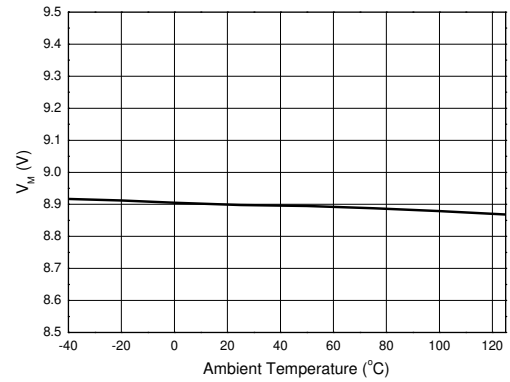
I_{BNI} vs. Ambient Temperature



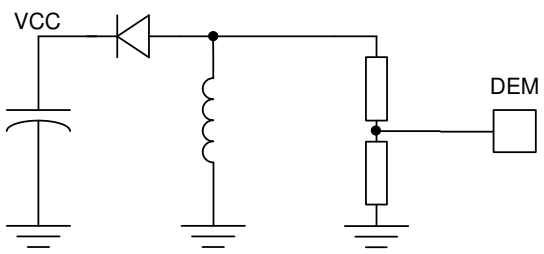
SOVP Threshold vs. Ambient Temperature



V_M vs. Ambient Temperature



PIN3 Utilization for BNO/SOVP/SUVP/OCP COMP



Operation Description

Quasi-Resonant (QR) Mode

Quasi-Resonant operation is regarded as a soft switching technology which always turns on the primary MOSFET at the valley status of Drain-to-Source voltage (V_{DS}). Compared to traditional hard switching, QR switching-on can reduce the switching power loss of MOSFET and achieve good EMI behavior without any additional BOM cost.

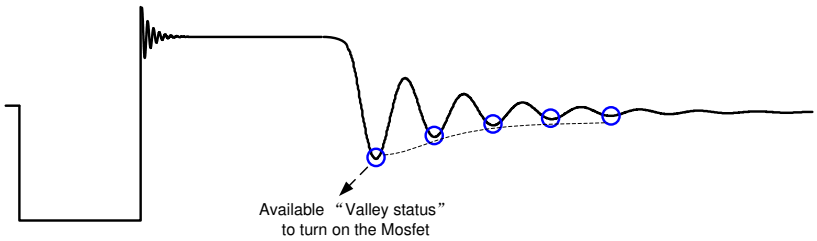


Figure 1

Figure 1 shows the primary MOSFET V_{DS} waveform. When the secondary-side current flows to zero, the primary inductance L_M and the effective MOSFET output capacitor Coss begin to resonant. The valley is detected by DEM Pin through a pair of voltage divider. At primary MOSFET turning off time, once the voltage on DEM Pin is detected below 75mV, one "valley status" is counted. To prevent the false trigger of the V_{DS} ring caused by leakage inductance, the valley detection function is blanked within the t_{SAMPLE} (2μs,refer to figure 6) when primary MOSFET turns off.

Each "valley status" of MOSFET V_{DS} will be detected and counted by DEM Pin, according to the frequency control strategy of AP3302; one proper "valley status" will be selected to turn on the MOSFET.

Frequency Modulation Strategy

The AP3302 operates with QR mode, green mode and burst mode to achieve the high efficiency performance.

In general, the AP3302 power system operates with first "valley status" under low line & full load condition, in which the maximum primary peak current and transformer flux density occur. The power system designer is required to choose transformer size and switching frequency according to this worst case condition.

With output load decreasing from full load, the switching frequency of AP3302 increases correspondingly in first "valley status" operation. In order to avoid performance degrading at very high switching frequency operation, there is a fixed 120kHz maximum frequency limitation in AP3302. Since too high switching frequency will lead to the worse performance, the 120kHz frequency limitation is not preferred to reach in system design. Actually AP3302 has built-in reference in FB pin voltage to adjust "valley status" for green mode operation, as shown in Figure 2. When FB pin voltage decreases to a modulating reference, the first "valley status" is forced to shift the secondary "valley status", and the switching frequency decrease accordingly. When output load continues decreasing, the secondary "valley status" will change to the third "valley status", the fourth "valley status until the fifteenth "valley status". When the "valley status" number is higher than 15, the valley turn on function will be disabled since the benefit of valley turn on is weak enough to ignore. AP3302 uses an advanced "valley lock" technology to avoid system oscillation and audible noise issue under the "valley status" shift condition, in which there is loading value hysteresis when two "valley status" increasing and decreasing occurs with loading changing.

The AP3302 has the minimum switching frequency limit of 22kHz to avoid audible noise issue. When the switching frequency decrease below 22kHz with output load decreasing, the switching frequency will keep at 22kHz. When FB pin voltage is lower than V_{BURST}, the power system enters burst mode to reduce the power dissipation under very light load condition.

Operation Description (Cont.)

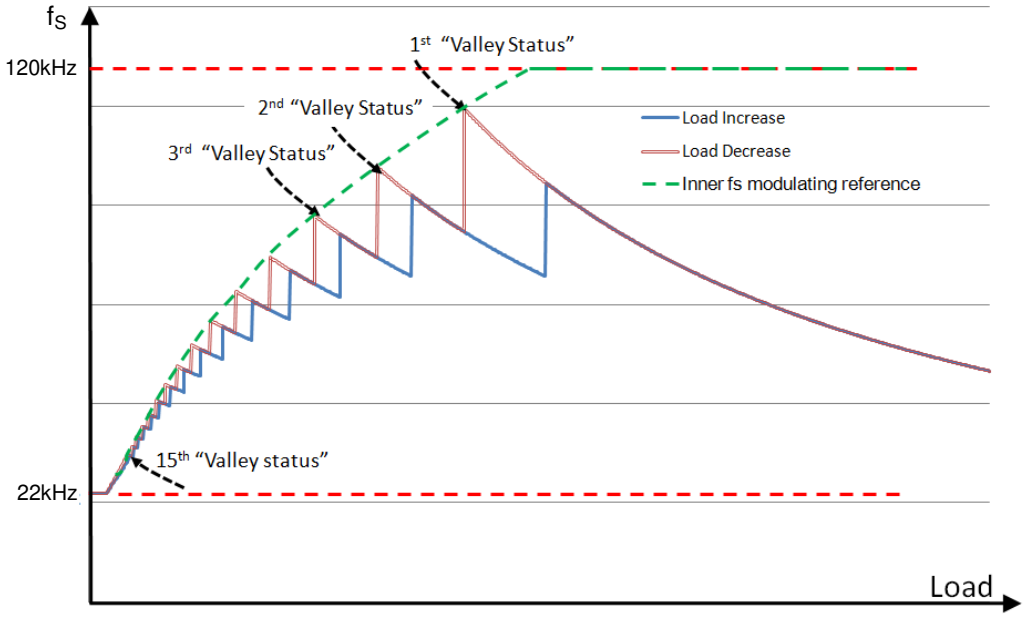


Figure 2

Active Frequency Dithering

To improve the EMI performance, the AP3302 integrates an active frequency dithering function. A consecutive frequency-dithering signal is injected to the SENSE pin after LEB time. As shown in figure 3, the frequency-dithering signal is repeating over and over again with a period of 500μs and amplitude of +/-V_{S_Jitter}. With the injection of frequency-dithering signal on SENSE pin, the switching frequency will has a periodical excursion to improve the EMI performance.

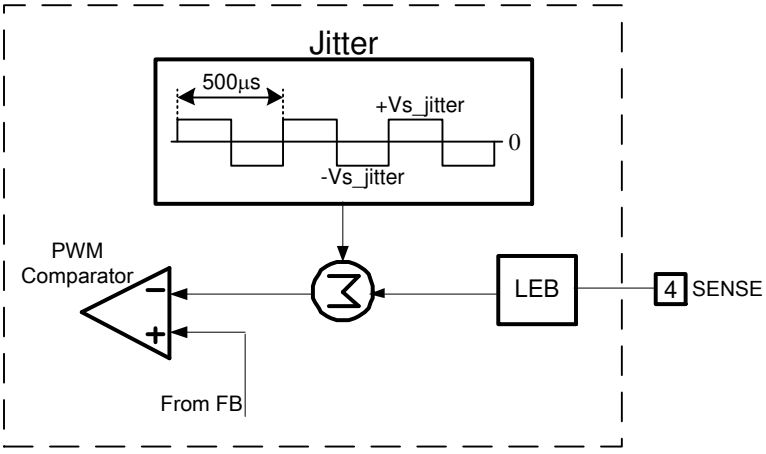


Figure 3

Current Mode PWM Control

The AP3302 operates as a current mode controller; the output switch is turned on by every oscillator cycle and turned off when the primary peak current reaches the threshold level established by the FB pin. The primary current signal is converted to a voltage signal on current sense resistor R_S. The relation between primary peak current (I_{PK}) and V_{FB} is:

$$I_{PK} = (V_{FB} - 1.0) / 3R_S$$

Operation Description (Cont.)

Start-Up Current and UVLO

The start-up current of the AP3302 is optimized to realize ultra low current (1μA typical) so that V_{CC} capacitor can be charged more quickly. The direct benefit of low start-up current is the availability of using large start-up resistor, which minimizes the resistor power loss for high voltage AC input.

An UVLO comparator is included in AP3302 to detect the voltage on VCC pin. It ensures that AP3302 can draw adequate energy from V_{CC} capacitor during power-on.

V_{CC} Maintain Mode

During some transient load condition, V_{FB} will drop below 1.55V, thus the PWM drive signal will be stopped, and there is no more energy transferring to the output side and auxiliary winding V_{CC} supply. Therefore, the IC V_{CC} voltage may reduce to the UVLO threshold voltage which will results in unexpected system restart. To avoid this failure condition, the AP3302 has a so-called V_{CC} maintain mode to maintain VCC voltage above UVLO. Whenever V_{CC} decreases to a setting threshold as V_M, the V_{CC} maintain mode will be awaked and AP3302 will output a driving pulse to turn on primary switch for providing enough energy to V_{CC} capacitor.

Leading-Edge Blanking Time

A narrow spike on the leading edge of the current waveform can usually be observed when the power MOSFET is turning on. A 250ns leading-edge blank is built-in to prevent the false-trigger caused by the turn-on spike. During this period, the current limit comparator and the PWM comparator are disabled and the gate driver cannot be switched off.

At the time of turning-off the MOSFET, a negative undershoot (maybe larger than -0.3V) can occur on the SENSE pin. So it is strongly recommended to add a small RC filter or at least connect a resistor "R" on this pin to protect the IC (Shown as Figure 4).

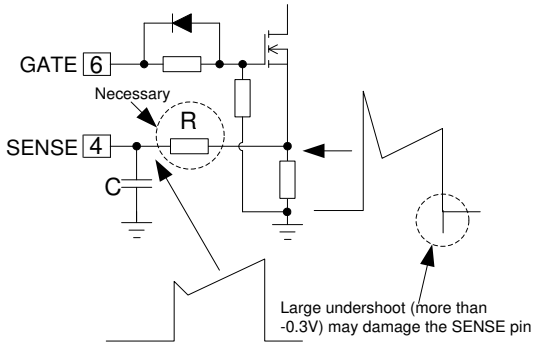


Figure 4

Protections

Brown In and Brown Out

The AP3302 can easily achieve brown in and brown out protection with the help of an external setting resistor. To determine the brown in voltage, according to the formula:

$$R_{DEM} = \frac{Vindc * Naux}{Np * I_{DEM}}$$

R_{DEM} mainly determines the brown in voltage, it's the upper resistor connected to the DEM Pin as shown in figure 5. Vindc is the peak value of targeted brown-in AC voltage, Np is the primary winding turns and the Naux is the auxiliary winding turns. When the system is plugged in, the AP3302 will output 4 switching pulses to identify the AC voltage value, when the primary MOSFET turns on, the DEM Pin is clamped to GND and a current I_{DEM} will flow out of the DEM pin, passing through R_{DEM} and the auxiliary winding. The smaller R_{DEM}, the larger I_{DEM}. If the IC controller detects that I_{DEM} is larger than I_{BNI} for the continuous 4 cycles, the IC will start outputting driving signal normally. Otherwise, whenever the I_{DEM} is lower than I_{BNO} for a period of $t_{DELAY-BNO}$, it will trigger the brown out protection and the IC will stop outputting driving signal.

Operation Description (Cont.)

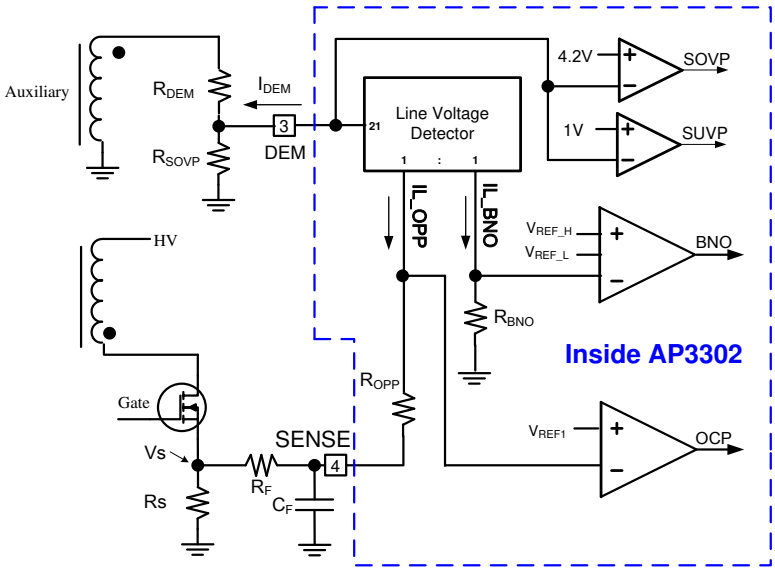


Figure 5

Constant Over Current Protection

Cycle-by-cycle current limit is a popular method to achieve output over current protection. Actually, the turn-off delay of the MOSFET and the higher switching frequency always result in the higher OCP current at high line voltage. To obtain a constant OCP current value with universal input voltage, AP3302 adopts an effective line compensation circuitry. The function block is illustrated in figure 5. The current I_{DEM} which reflects line voltage is scaled down and inversed to $IL_{\_OPP}$ within AP3302, this $IL_{\_OPP}$ flows through the inner compensation resistor R_{OPP} and an external compensation resistor R_F , and then the final line compensation voltage is formed as

$$V_S + \frac{Vindc * Naux}{Np * R_{DEM} * 21} * (R_{OPP} + R_F) = V_{REF1}$$

As above formula indicates, changing the compensation voltage at different line voltage is a good way to balance the OCP current. In a real system, usually keep the R_{DEM} value fixed when the BNO voltage is set up, to change the line compensation voltage, a good solution is to change R_F. Whenever the R_F is changed, adjust the C_F at the same time to offer an enough RC time to filter the spike on SENSE pin.

Secondary OVP and UVP

The AP3302 provides output OVP and UVP protection function. The auxiliary winding voltage during secondary rectifier conducting period reflects the output voltage. Refer to figure 5,a voltage divider network containing R_{DEM} and R_{SOVP} is connected to the auxiliary winding and DEM Pin, the DEM Pin will detect the equivalent output voltage with a delay of t_{SAMPLE} from the falling edge of GATE driver signal, as shown in figure 6. The detected voltage will be compared to the SOVP and SUVP threshold voltage $V_{TH-SOVP}$ and $V_{TH-SUVP}$. If the SOVP or SUVP threshold is reached continuously by 6 switching cycles, the SOVP or SUVP protection will be triggered, the AP3302 will shut down and the system will restart when the VCC voltage falls below the UVLO voltage.

To prevent from false-trigger of SUVP during start up consequence, a blank time of $t_{BLANK-SUVP}$ is set during which the SUVP protection function is ignored.

Operation Description (Cont.)

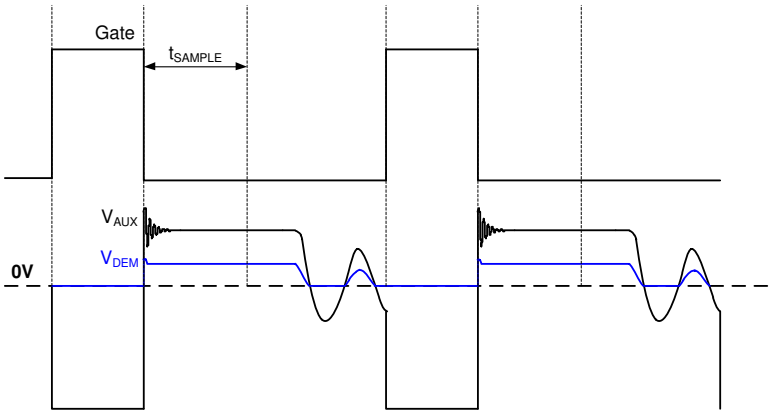


Figure 6

Internal OTP Protection Function

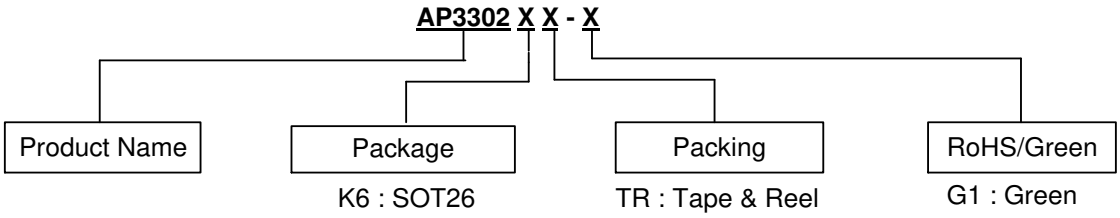
The AP3302 integrates an internal temperature sensor. It has a trigger window of +150°C enter and +125°C exit. The internal OTP protection mode is auto-recovery mode.

Other Protections: FOCP, SSCP, VCC OVP and Pin Fault

The AP3302 provides versatile protection to ensure the reliability of the power system. FOCP protection is an ultra fast short-current protection which is helpful to avoid catastrophic damage of the system when the secondary rectifier is short. The primary peak current will be monitored by SENSE pin through a primary sense resistor, whenever the sampled voltage reaches the threshold of $V_{TH-FOCP}$ for 6 switching cycles continuously, the FOCP protection will be active to shut down the switching pulse. SSCP might be triggered at ultra low line voltage condition or other failure condition that short the SENSE pin to ground. The SSCP module senses the voltage across the primary sense resistor with a delay of 3 s after the rising edge of primary GATE signal, this sensed signal is compared with $V_{TH-SSCP}$, if it is lower than $V_{TH-SSCP}$ for 6 switching cycles, the SSCP protection will be triggered and the drive signal will be disabled. All these protections described above will restart the system when the VCC voltage falls below UVLO.

The AP3302 also has pin fault connection protection including floating and short connection. The floating pin protection includes the SENSE, FB, etc. The short pin protection includes the DEM pin short protection. When these pins are floated or DEM pin is shorted to ground, PWM switching will be disabled, thus protecting the power system.

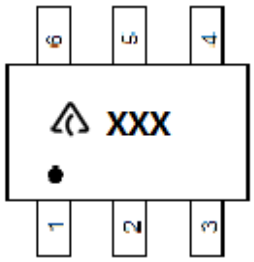
Ordering Information



Package	Part Number	Marking ID	Packing
SOT26	AP3302K6TR-G1	GTE	3000 / Tape & Reel

Marking Information

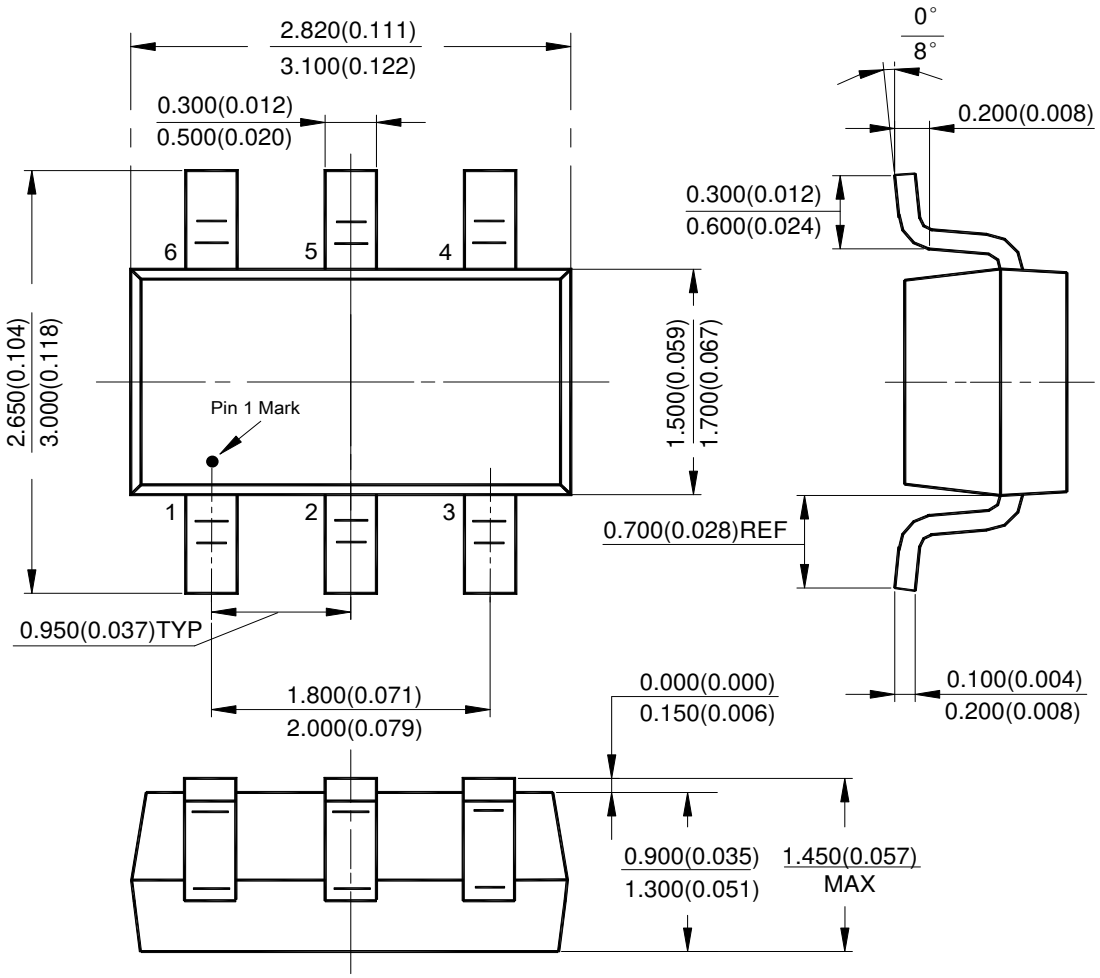
(Top View)



: Logo
XXX: Marking ID (See Ordering Information)

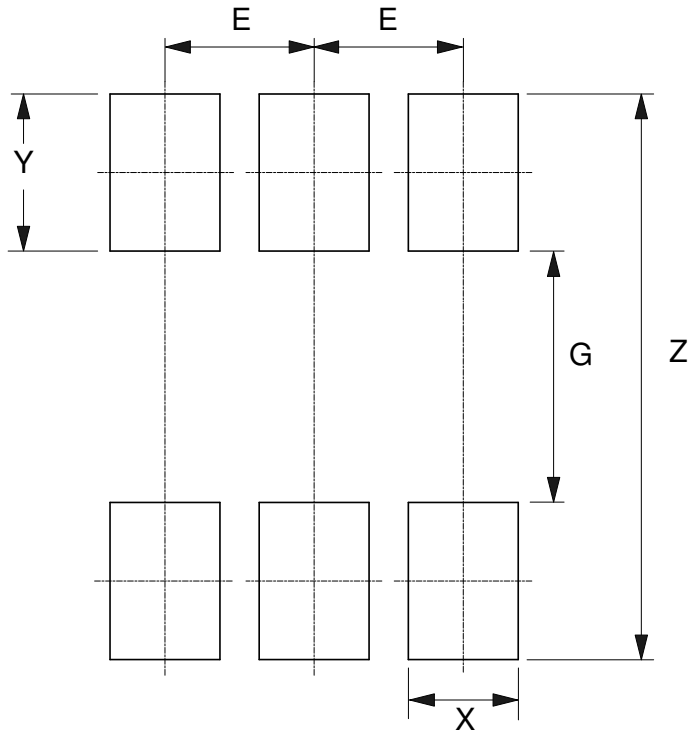
Package Outline Dimensions (All dimensions in mm(inch).)

(1) Package Type: SOT26



Suggested Pad Layout

(1) Package Type: SOT26



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	E (mm)/(inch)
Value	3.600/0.142	1.600/0.063	0.700/0.028	1.000/0.039	0.950/0.037

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