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AP3790

PUMP EXPRESS™ COMPATIBLE AC/DC PSR CONTROLLER

Description

The AP3790 is a high accuracy and low cost switching mode power supply controller to drive power bipolar transistor for battery charger/adapter applications. The controller regulates the output voltage and current in the primary side by piece-wise Pulse Frequency Modulation (p-PFM) in discontinuous conduction mode (DCM). The controller uses adaptive source current to optimize driving current to reduce driving loss. The system operating frequency reduces linearly from heavy load to light load in each interval of the p-PFM, and enters constant current mode when the load current is equal to the maximum system output current.

The output voltage of AP3790 can be adjusted based on the patterns of load current aligned to MTK Pump Express protocol.

The AP3790 provides operating frequency Jitter function from light to full load range to improve the power supply EMI performance. The AP3790 also has built-in fixed cable voltage drop compensation (6% of nominal system output voltage) and adjustable line voltage compensation.

The AP3790 can work individually to achieve Ultra-Low standby power under 5V output.

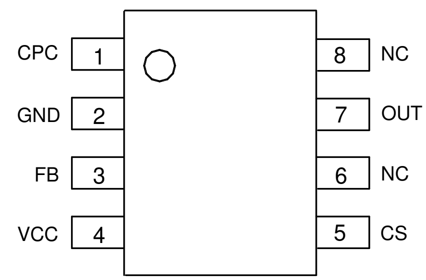
The AP3790 is packaged in SO-8.

Applications

- Adapters/Chargers

Pin Assignments

(Top View)



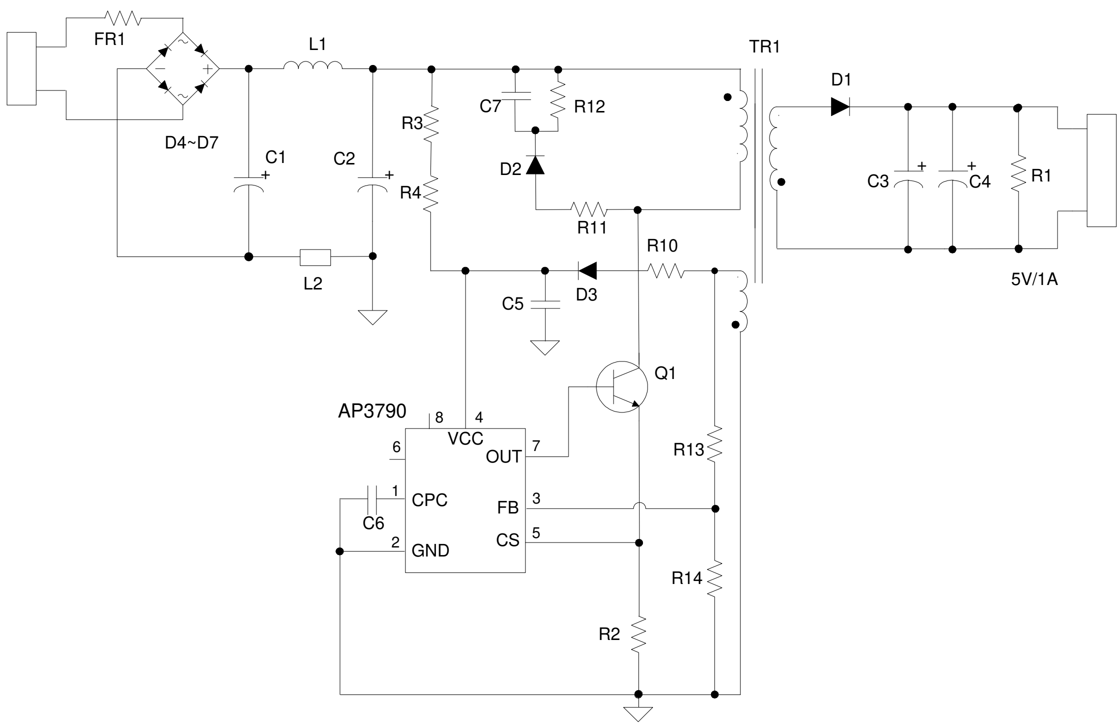
SO-8

Features

- Compatible to MediaTek Pump Express™ Protocol
- Ultra-Low Standby Power Consumption
- Valley-turn On to Reduce Switching Loss and Benefit for EMI
- Piece-wise Frequency Reduction to Enhance Conversion Efficiency and Suppress Audio Noise
- ±5% Constant Voltage Accuracy for 5V Output
- Audio Noise Suppression
- Open Circuit Protection (OCkP)
- Current Sense Resistor Short Protection
- Over Voltage Protection (OVP)
- Over Temperature Protection (OTP)
- Short Circuit Protection (SCP) with Hiccup
- **Totally Lead-free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

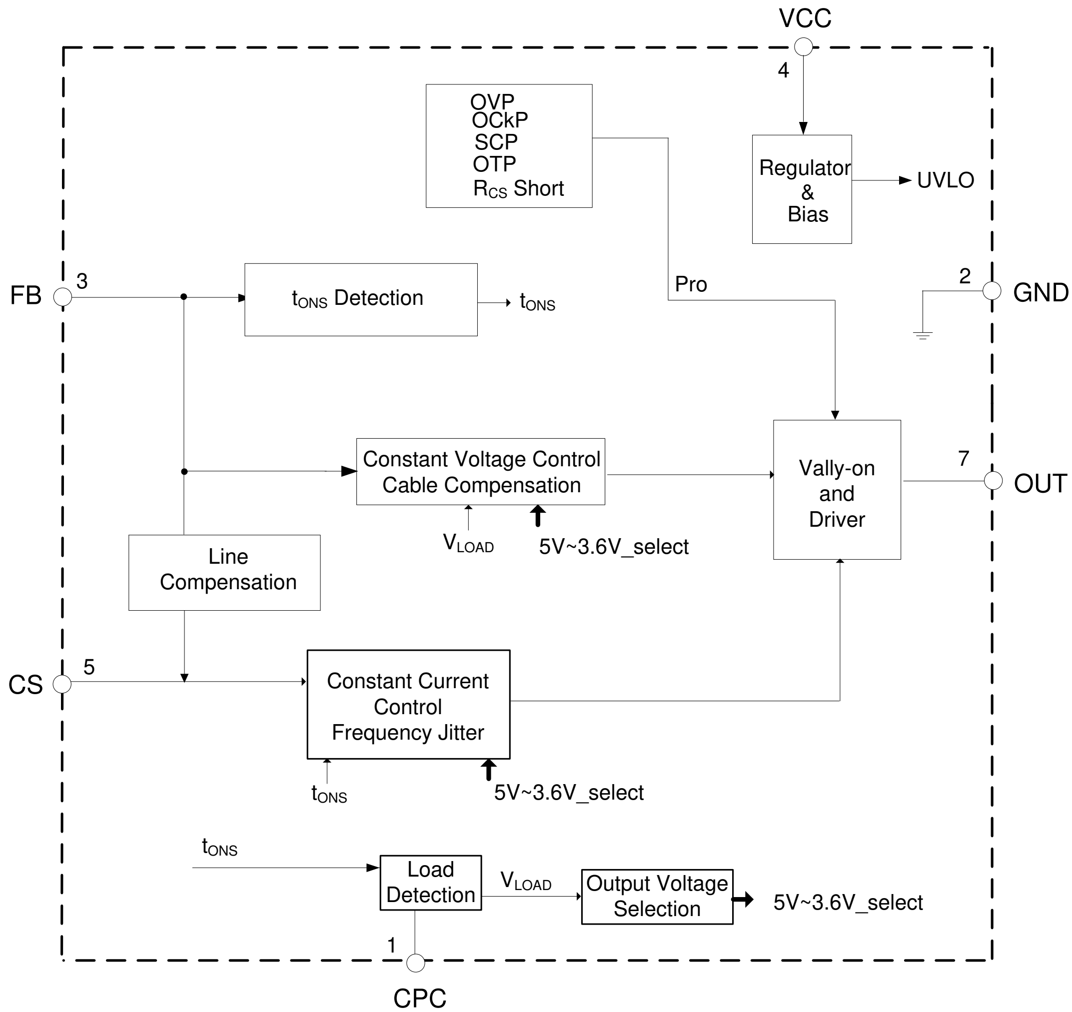
Typical Applications Circuit



Pin Descriptions

Pin Number	Pin Name	Function
1	CPC	A capacitor is connected to this pin to form a low pass filter for cable voltage drop compensation, audio noise suppression and detecting the patterns of load current to change the output voltage and current
2	GND	The ground of the controller
3	FB	The CV and CC regulation are realized base on the voltage sampling of this pin
4	VCC	VCC supply pin for the controller. A capacitor with low ESR should be placed as close as possible to this pin
5	CS	Current senses pin of IC. The CS pin will turn off the power transistor when the CS pin voltage reaches turn off threshold.
7	OUT	The OUT pin is used to drive the external power transistor
6, 8	NC	Not connected

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	-0.3 to 35	V
V_{CS}, V_{CPC}	Voltage on CS, CPC Pin	-0.3 to 7	V
V_{FB}	FB Input Voltage	-0.3 to 8	V
I_{SOURCE}	Source Current from OUT Pin	Internally Limited	A
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10 sec)	+300	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	165	°C/W
ESD	ESD (Human Body Model)	4000	V
	ESD (Machine Model)	300	V

Note 4: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Electrical Characteristics (@V_{CC} = 12V, T_A = +25°C, unless otherwise specified.)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
STARTUP AND UVLO SECTION						
V_{TH_ST}	Startup Threshold	–	13	15.5	18	V
$V_{OPR(MIN)}$	Minimal Operating Voltage	–	5.2	5.8	6.4	V
STANDBY CURRENT SECTION						
I_{ST}	Startup Current	$V_{CC} = V_{TH\_ST}$-1V before startup	0	0.2	0.6	μA
I_{CC_QST}	Quiescent Current	Static current @ OUT pin no load	435	500	565	
DRIVING OUTPUT SECTION						
$R_{DS(ON)}$	Sink Resistance	1V @ OUT pin	2	2.4	2.8	Ω
$I_{OUT(MAX)}$	The Maximum Source Current	–	25	32	39	mA
OPERATING FREQUENCY SECTION (5% Load to Full Load)						
$t_{OFF(MAX)}$	Maximum Off Time	–	691	768	845	μs
t_{SAMPLE}	Sampling Time	37% to 100% full load	5.4	6	6.6	μs
		4% to 37% full load	3.2	3.6	4.0	μs
		0% to 4% full load (Note 5)	2.25	2.5	2.75	μs
FREQUENCY JITTER						
$\Delta V_{CS}/V_{CS}$	V_{CS} Modulation	7% to 100% full load	2	3	4	%
t_{MOD}	V_{CS} Modulation Period	–	230	256	282	μs
CURRENT SENSE SECTION						
V_{CS_H}	Current Sense Threshold	37% to 100% full load	830	900	970	mV
V_{CS_M}		4% to 37% full load	550	600	650	
V_{CS_L}		0% to 4% full load (Note 5)	320	350	380	
R_{LINE}	Built-in Line Compensation Resistor	–	160	200	240	Ω
t_{LEB}	Leading Edge Blanking	V_{CS_H} and V_{CS_M}	425	500	575	ns
		V_{CS_L} (Note 5)	170	200	230	
CONSTANT VOLTAGE SECTION						
V_{FB}@5V	Feedback Threshold Voltage	–	3.94	4.0	4.06	V
V_{FB}@4.8V			3.75	3.85	3.95	
V_{FB}@4.6V			3.61	3.7	3.79	
V_{FB}@4.4V			3.47	3.56	3.65	
V_{FB}@4.2V			3.32	3.41	3.5	
V_{FB}@4V			3.18	3.26	3.34	

Electrical Characteristics (@V_{CC} = 12V, T_A = +25°C, unless otherwise specified.) (Cont.)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{FB}@3.8V	Feedback Threshold Voltage	–	3.03	3.11	3.19	V
V_{FB}@3.6V			2.89	2.96	3.03	
R_{FB}	FB Pin Input Resistance	V_{FB}=4V	560	700	840	kΩ
V_{CABLE}/V_{OUT}%	Cable Compensation Ratio@5V	–	5	6	7	%
CONSTANT CURRENT SECTION						
t_{ONS}/t_{SW}	Maximum Secondary Duty Cycle	V_{FB}=2V (Note 5)	0.47	0.5	0.53	–
DYNAMIC SECTION						
V_{UV_H}	Under Voltage of Feedback Pin for V_{CS_H}	(Note 5)	3.61	3.68	3.75	V
OUTPUT VOLTAGE SELECTION SECTION						
V_{CPC_L}	Current Control Threshold	V_{CPC} control_L	–	59	–	mV
V_{CPC_H}		V_{CPC} control_H	–	100	–	
t_{ON_A}	Current Control Pattern Time	(Note 5)	400	500	600	ms
t_{ON_B}			220	300	380	
t_{ON_C}			50	100	150	
t_{OFF_D}			50	100	150	
t_{WDT}	Watch Dog Time	–	180	210	240	ms
PROTECTION FUNCTION SECTION						
$V_{FB(OVP)}$	Over Voltage Protection	–	7.1	7.5	7.9	V
$V_{CC(OVP)}$	Over Voltage Protection at VCC Pin	–	27	30	33	V
$V_{OUT(OVP)}$	Over Voltage Protection at OUT Pin	–	3.4	3.65	3.9	V
$V_{FB(SCP)}$	Short Circuit Protection	V_{FB} @ Hiccup	1.61	1.7	1.79	V
t_{SCP}	Maximum Time under $V_{FB(SCP)}$	–	116	128	140	ms
T_{OTP}	Shutdown Temperature	–	+128	+140	+152	°C
T_{HYS}	Temperature Hysteresis	–	+36	+40	+44	°C

Note 5: Guaranteed by design.

Operation Principle Description

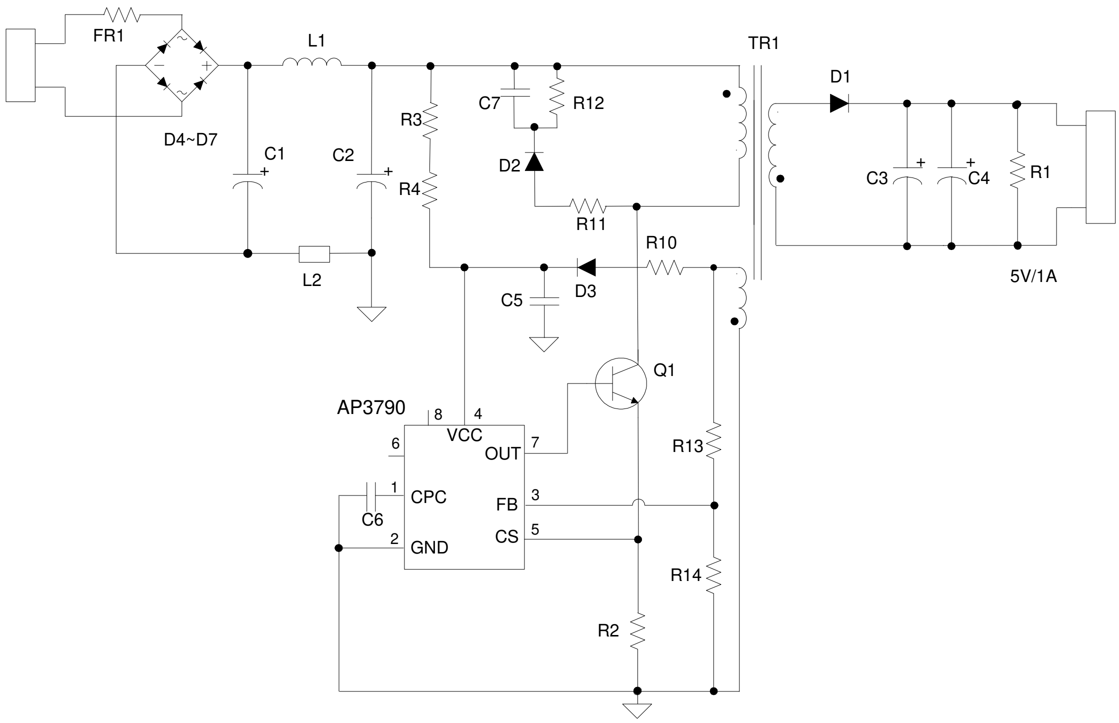


Figure 1. 7.5W Battery Charger

Figure 1 is the typical application circuit of AP3790, which is a conventional Flyback converter with a 3-winding transformer---primary winding (N_P), secondary winding (N_S) and auxiliary winding (N_{AUX}). The auxiliary winding is used for providing VCC supply voltage for IC and sensing the output voltage feedback signal to FB pin.

Figure 2 shows the typical waveforms which demonstrate the basic operating principle of AP3790 application. And the parameters are defined as following.

I_P---The primary side current

I_S ---The secondary side current

I_{PK}---Peak value of primary side current

I_{PKS}---Peak value of secondary side current

V_{SEC}---The transient voltage at secondary winding

V_S---The stable voltage at secondary winding when rectification diode is in conducting status, which equals the sum of output voltage V_{OUT} and the forward voltage drop of diode

V_{AUX}---The transient voltage at auxiliary winding

V_A--- The stable voltage at auxiliary winding when rectification diode is in conducting status, which equals the sum of voltage VCC and the forward voltage drop of auxiliary diode

t_{SW} ---The period of switching frequency

t_{ONP} ---The conduction time when primary side switch is “ON”

t_{ONS} ---The conduction time when secondary side diode is “ON”

t_{OFF} ---The dead time when neither primary side switch nor secondary side diode is “ON”

t_{OFFS} --- The time when secondary side diode is “OFF”

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Operation Principle Description (Cont.)

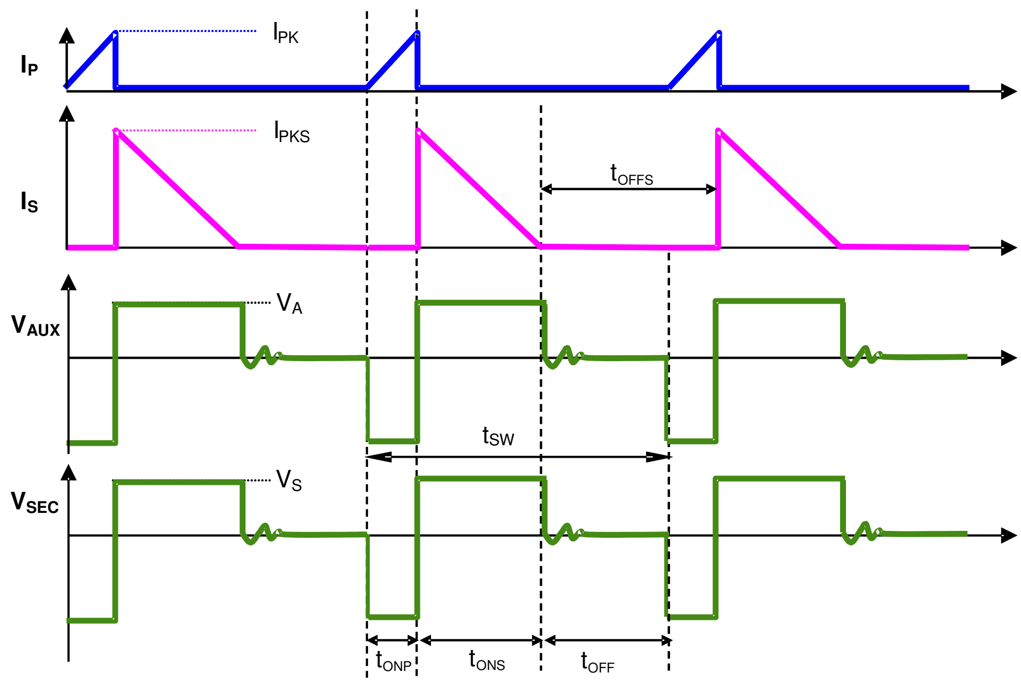

Figure 2. The Operation Waveform of Flyback PSR System

For primary-side regulation, the primary current ip(t) is sensed by a current sense resistor R_{CS} (R2 as shown in Figure 1). The current rises up linearly at a rate of:

$$\frac{dip(t)}{dt} = \frac{V_{IN}(t)}{L_M} \quad (1)$$

As illustrated in Figure 2, when the current ip(t) rises up to I_{PK}, the switch Q1 turns off. The constant peak current is given by:

$$I_{PK} = \frac{V_{CS}}{R_{CS}} \quad (2)$$

The energy stored in the magnetizing inductance L_M each cycle is therefore:

$$Eg = \frac{1}{2} \times L_M \cdot I_{PK}{}^2 \quad (3)$$

So the power transferring from the input to the output is given by:

$$P = \frac{1}{2} \times L_M \times I_{PK}{}^2 \times f_{SW} \quad (4)$$

Where, the f_{SW} is the switching frequency. When the peak current I_{PK} is constant, the output power depends on the switching frequency f_{SW}.

Constant Voltage Operation

As to constant-voltage (CV) operation mode, the AP3790 detects the auxiliary winding voltage at FB pin to regulate the output voltage. The auxiliary winding voltage is coupled with secondary side winding voltage, so the auxiliary winding voltage at D1 conduction time is:

$$V_{AUX} = \frac{N_{AUX}}{N_S} \times (Vo + Vd) \quad (5)$$

Where the Vd is the diode forward voltage drop.

Operation Principle Description (Cont.)

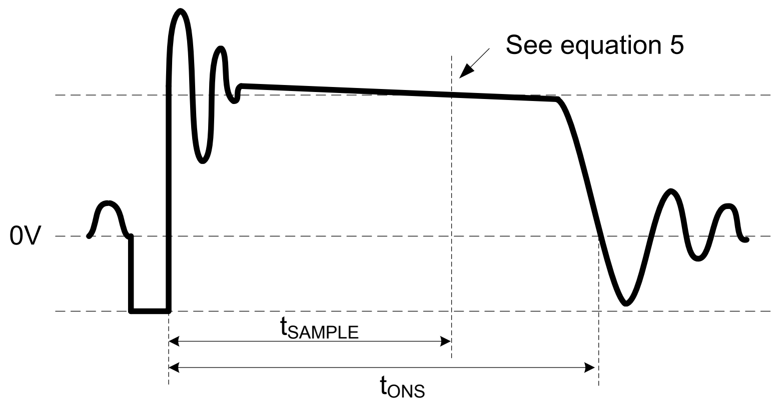

Figure 3. Auxiliary Voltage Waveform

The voltage detection point is at a constant delay time of the D1 on-time. The constant delay time is changed with the different primary peak current. The CV loop control function of AP3790 then generates a D1 off-time to regulate the output voltage.

Constant Current Operation

The AP3790 can work in constant-current (CC) mode. Figure 2 shows the secondary current waveforms.

In CC operation mode, the CC control loop of AP3790 will keep a fixed proportion between D1 on-time t_{ONS} and D1 off-time t_{OFFS}. The fixed proportion is

$$\frac{t_{ONS}}{t_{OFFS}} = \frac{4}{4} \qquad (6)$$

The relationship between the output current and secondary peak current I_{PKS} is given by:

$$I_{OUT} = \frac{1}{2} \times I_{PKS} \times \frac{t_{ONS}}{t_{ONS} + t_{OFFS}} \qquad (7)$$

As to tight coupled primary and secondary winding, the secondary peak current is

$$I_{PKS} = \frac{N_P}{N_S} \times I_{PK} \qquad (8)$$

Thus the output constant-current is given by:

$$I_{OUT} = \frac{1}{2} \times \frac{N_P}{N_S} \times I_{PK} \times \frac{t_{ONS}}{t_{ONS} + t_{OFFS}} = \frac{2}{8} \times \frac{N_P}{N_S} \times I_{PK} \qquad (9)$$

Therefore, AP3790 can realize CC mode operation by constant primary peak current and fixed diode conduction duty cycle.

Multiple Segment Constant Peak Current

As to the original PFM PSR system, the switching frequency decreases with output current decreasing, which will encounter audible noise issue since switching frequency decreases to audio frequency range, about less than 20kHz.

In order to avoid audible noise issue, AP3790 uses 3-segment constant primary peak current control method. At constant voltage mode, the current sense threshold voltage is multiple segment with different loading, as shown in Figure 4, which are V_{CS_H} for high load, V_{CS_M} for medium load and V_{CS_L} for light load. At constant current mode, the peak current is still V_{CS_H}.

Operation Principle Description (Cont.)

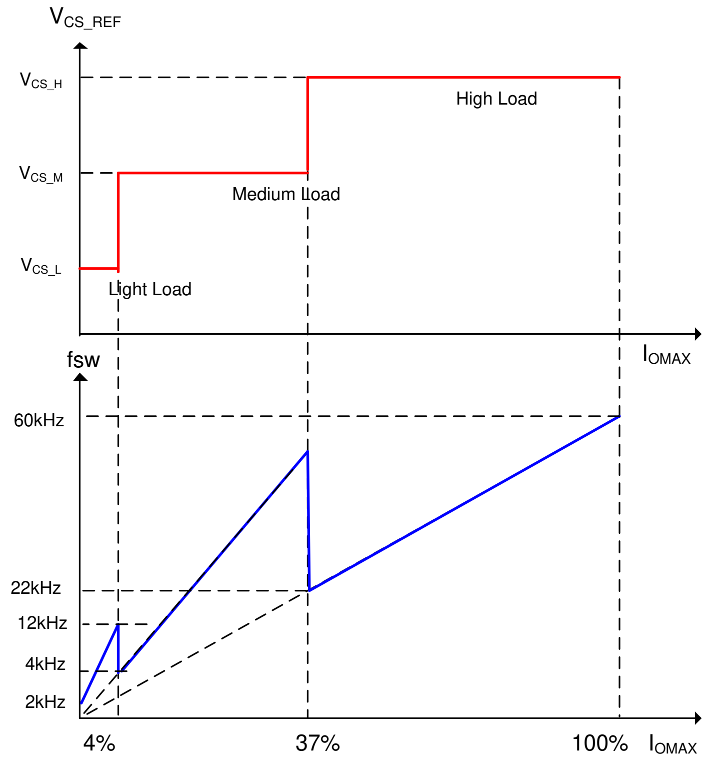

Figure 4. Multiple Segment Peak Current at CV Mode

It can be seen from Figure 4, with multiple segment peak current control, AP3790 power system can get the good audible noise performance.

Leading Edge Blanking (LEB) Time

When the power switch is turned on, a turn-on spike will occur on the sense-resistor. To avoid false turn off switch, a 500ns leading-edge blanking is built in. During this blanking time, the current sense comparator is disabled and the external power switch cannot be turned off. Furthermore, because of multiple segment peak current design, the required maximum on time t_{ONP} changes with different load condition. Therefore the LEB time parameter also changes with different load condition.

Adjustable Line Compensation and Fixed Cable Compensation

The AP3790 power system can adjust line compensation by changing the upper resistor at FB pin. The line compensation capability is increased by decreasing the resistance of the upper FB resistor.

Cable compensation is fixed in AP3790.

Valley Turn-on

When the off time (t_{OFF}) is lower than 32µs, AP3790 power system can work with valley turn on. It can reduce BJT switching on power losses which is result from the equivalent output capacitance. At the same time, because of valley turn on the switching frequency has the random jitter feature, which will be benefit for conductive EMI performance. And valley turn on can also reduce the power switch turn on spike current and then result in the better radiative EMI performance.

Frequency Jitter

Even though the valley turn on function can lead the random frequency jitter feature, an active frequency jitter function is added to AP3790 to ensure the frequency jitter performance in the whole loading condition. By adjusting the V_{CS_REF} with deviation of 3.0% in a random pulse sequence, the active frequency jitter can be realized with 256µs repetitive cycles.

Operation Principle Description (Cont.)

Output Voltage Selection Section

The output voltage of AP3790 can be adjusted based on the patterns of load current aligned to MTK Pump Express protocol.

The voltage of CPC pin of AP3790 is changed with the load current. AP3790 can detect the load current patterns through CPC pin. The pattern of decrease output voltage is shown in Figure 5 and the pattern of increase output voltage is shown in Figure 6.

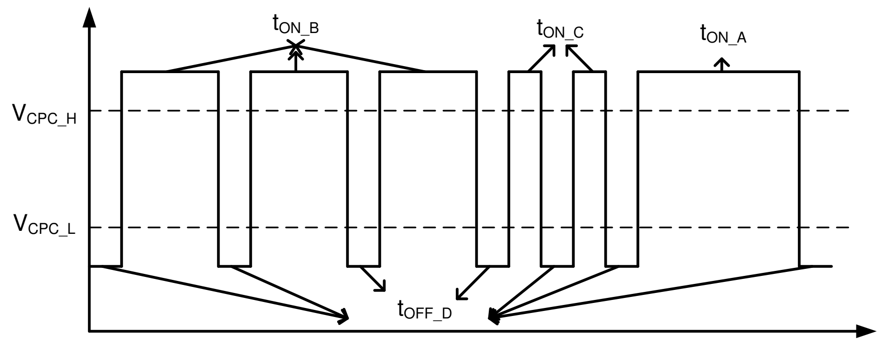

Figure 5 The Pattern of Decrease Output Voltage

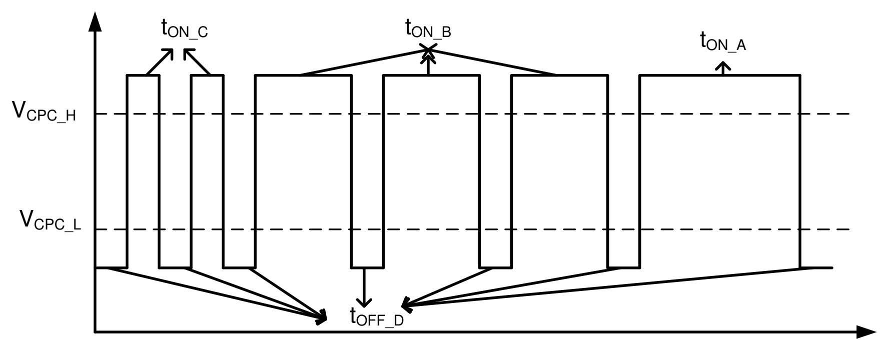

Figure 6 The Pattern of Increase Output Voltage

Just shown as Figure 7, the voltage is changed step by step among 4.8V and 3.6V. When the AP3790 detects one full pattern of decrease output voltage, the output voltage will decrease 0.2V from the current voltage level. When the output voltage is 3.6V, the pattern of decrease output voltage is invalid. When the AP3790 detects one full pattern of increase output voltage, the output voltage will increase 0.2V from the current voltage level. When the output voltage is 5V, the pattern of decrease output voltage is invalid. At any voltage level among 4.8V to 3.6V, once the WDT function (V_{CPC}<V_{CPC_L} and the time of duration is more than t_{WDT}.) is triggered, the output voltage will return to 5V directly. And At any voltage level among 4.8V to 3.6V, once any protect function is triggered, the output voltage will return to 5V directly.

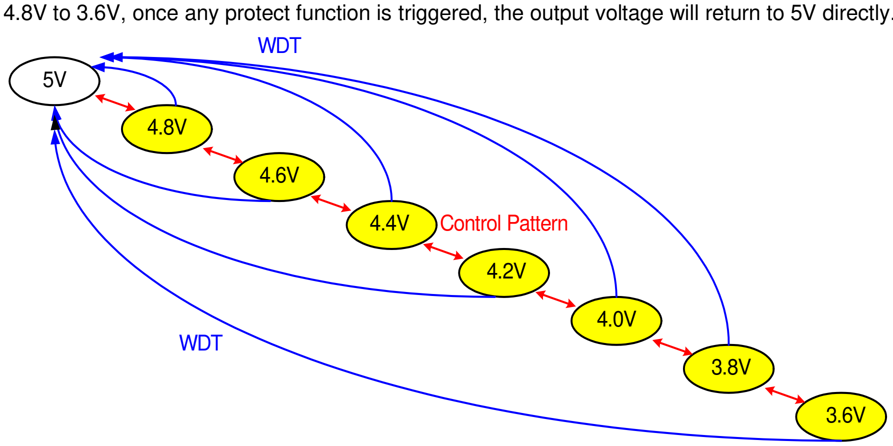

Figure 7. Voltage State Flow

Operation Principle Description (Cont.)

CCM Protection

The AP3790 is designed to operate in discontinuous conduction mode (DCM) in both CV and CC modes. To avoid operating in continuous conduction mode (CCM), the AP3790 detects the falling edge of the FB input voltage on each cycle. If a 0V falling edge of FB is not detected, the AP3790 stops working.

OVP & OCkP

The AP3790 includes output over-voltage protection (OVP) and open circuit protection (OCkP) circuitry. If the voltage at FB pin exceeds 7.5V, 90% above the normal detection voltage, or the 0V falling edge of the FB input can't be monitored, the AP3790 immediately shuts down and keeps the internal circuitry enabled to discharge the VCC capacitor to the UVLO turn-off threshold. After that, the device returns to the start state and a start-up sequence ensues.

Short Circuit Protection (SCP)

Short Circuit Protection (SCP) detection principle is similar to the normal output voltage feedback detection by sensing FB pin voltage. When the detected FB pin voltage is below V_{FB}(SCP) for a duration of about t_{SCP}, the SCP is triggered. Then the AP3790 enters hiccup mode that the IC immediately shuts down and then restarts, so that the VCC voltage changes between V_{TH_ST} and UVLO threshold until V_{FB}(SCP) condition is removed.

As to the normal system startup, the time duration of FB pin voltage below V_{FB}(SCP) should be less than t_{SCP} to avoid entering SCP mode. But for the output short condition or the output voltage below a certain level, the SCP mode should happen.

Figure 8 is the AP3790 normal start-up waveform that the voltage of FB pin is above V_{FB}(SCP) during t_{SCP} after V_{CC} gets to the V_{TH_ST}, which doesn't enter the SCP mode. As shown in Figure 9, V_{OUT} is short and the voltage of FB pin is lower than V_{FB}(SCP) over than t_{SCP}, the AP3790 triggers the SCP and enters the hiccup mode.

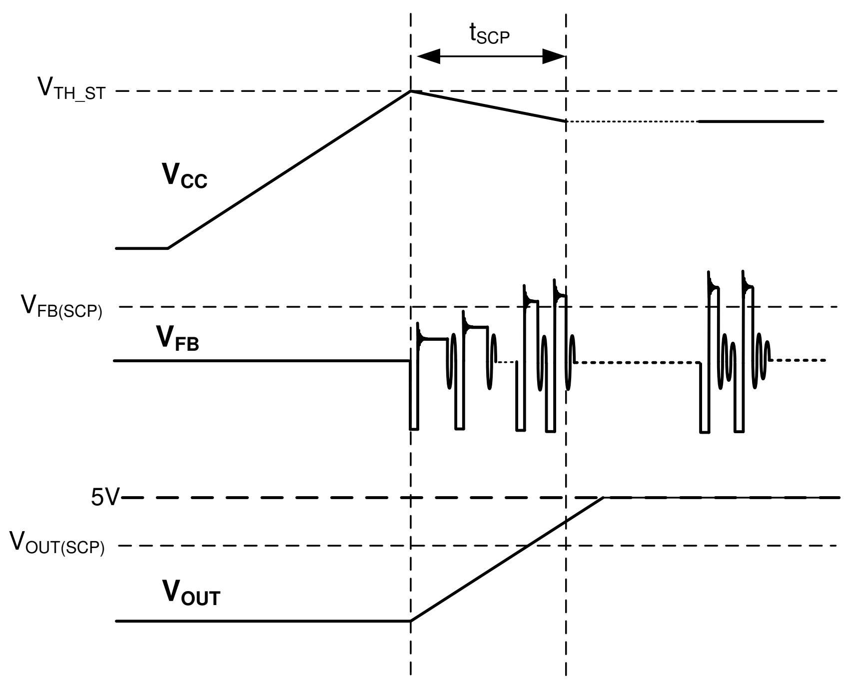

Figure 8. Normal Start-up

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Operation Principle Description (Cont.)

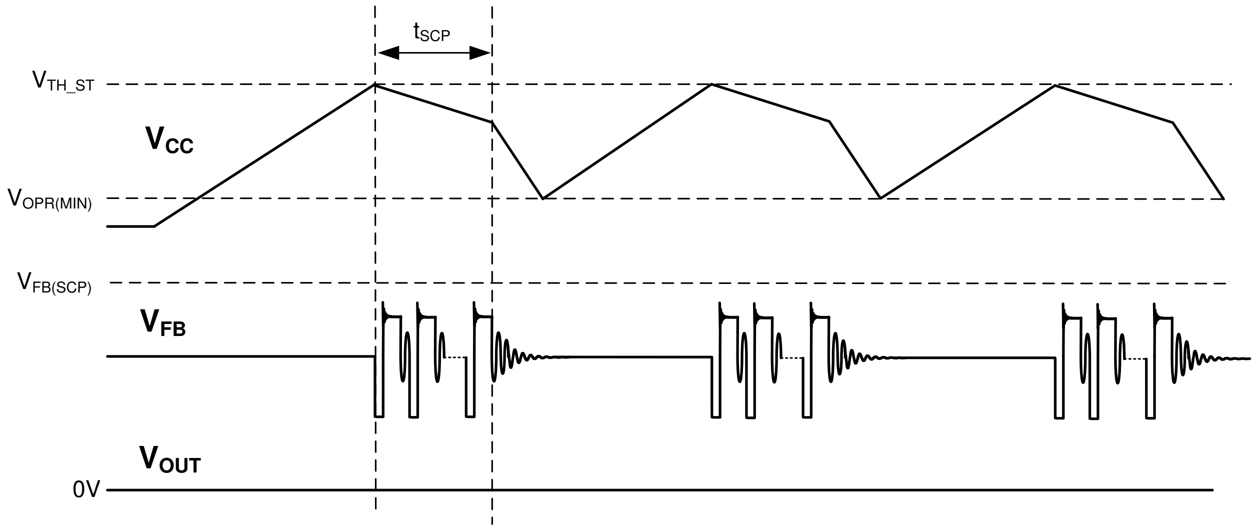


Figure 9. Short Circuit Protection (SCP) and Hiccup Mode

OTP

If the junction temperature reaches the threshold of +140ºC, AP3790 shuts down immediately. Before VCC voltage decreases to UVLO, if the junction temperature decreases to +100ºC, AP3790 can recover to normal operation. If not, the power system enters restart Hiccup mode until the junction temperature decreases below +100ºC.

Performance Characteristics

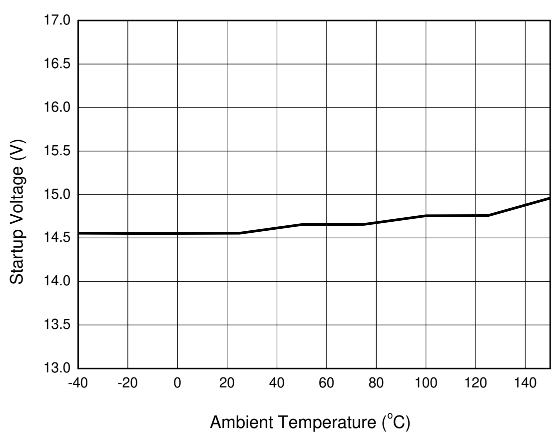


Figure 10. Startup Voltage vs. Ambient Temperature

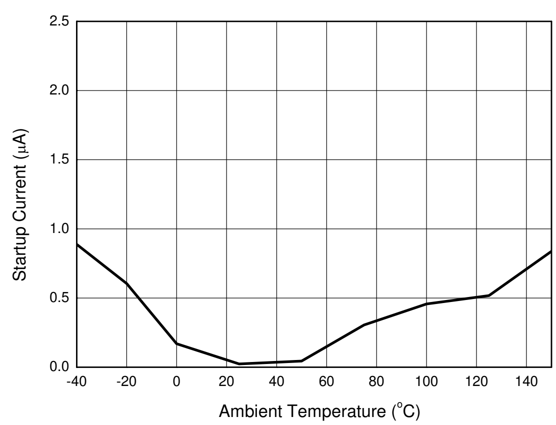


Figure 11. Startup Current vs. Ambient Temperature

Performance Characteristics (Cont.)

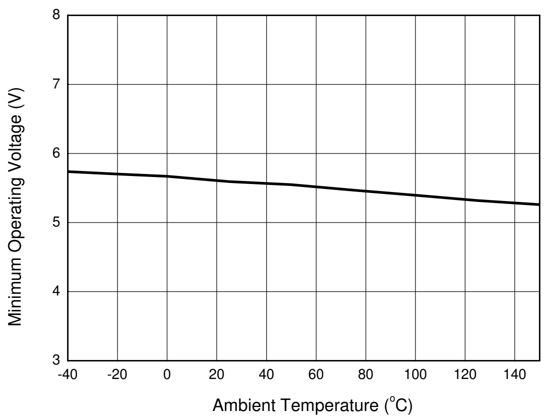


Figure 12. Minimum Operating Voltage vs. Ambient Temperature

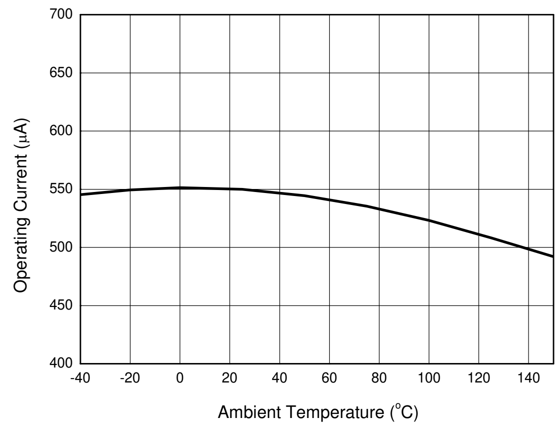


Figure 13. Operating Current vs. Ambient Temperature

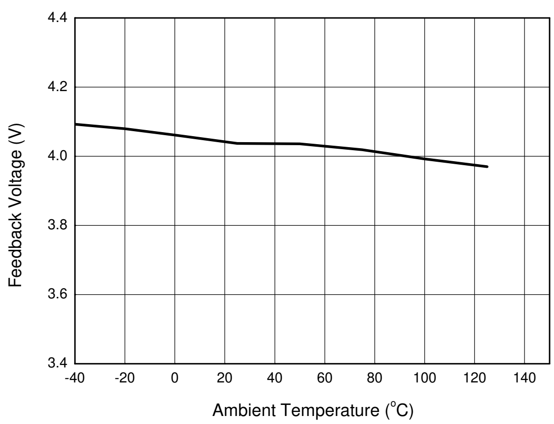


Figure 14. Feedback Voltage vs. Ambient Temperature

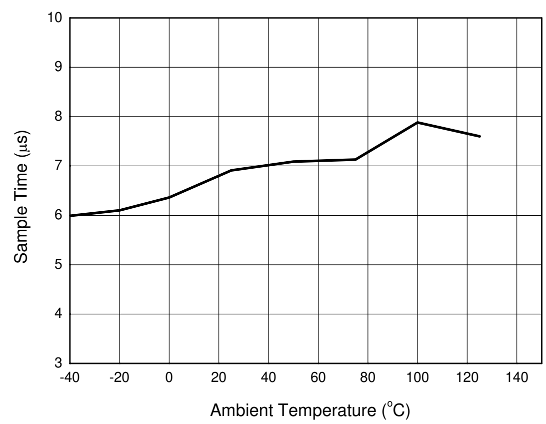


Figure 15. Sample Time vs. Ambient Temperature

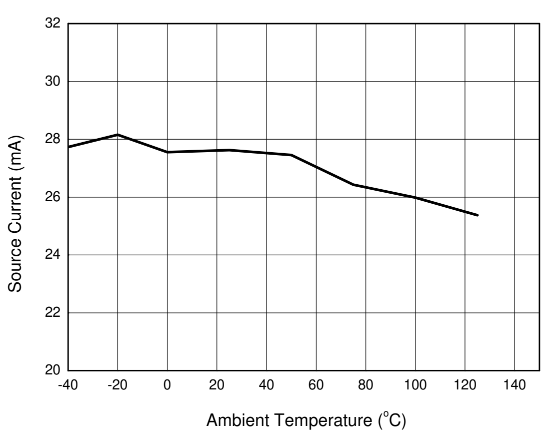


Figure 16. Source Current vs. Ambient Temperature

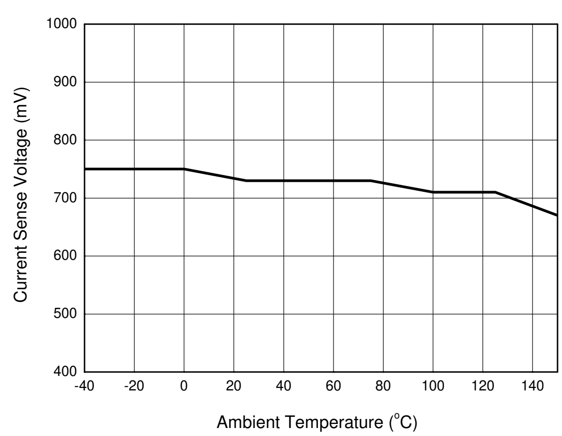


Figure 17. Current Sense Voltage vs. Ambient Temperature

Performance Characteristics (Cont.)

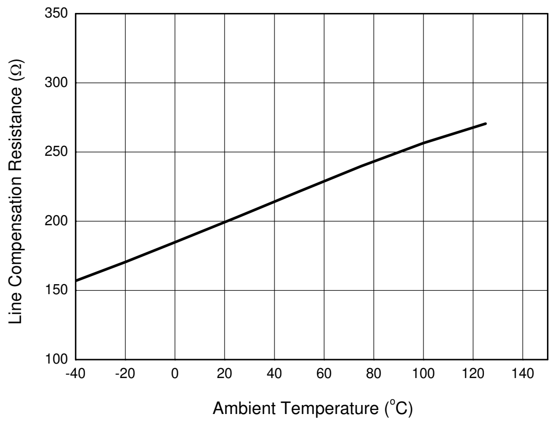


Figure 18. Line Compensation Resistance vs. Ambient Temperature

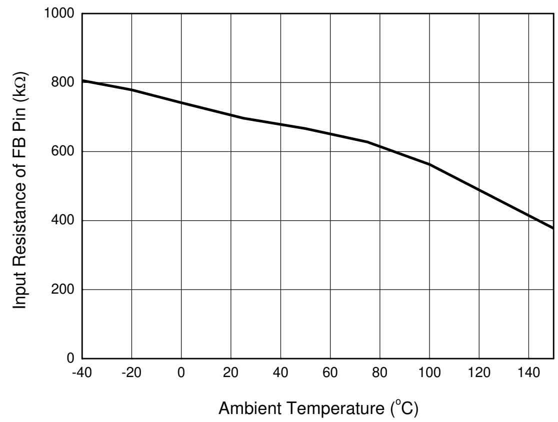
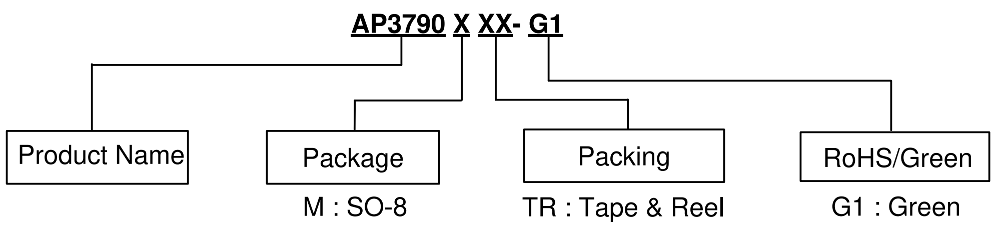


Figure 19. Input Resistance of FB Pin vs. Ambient Temperature

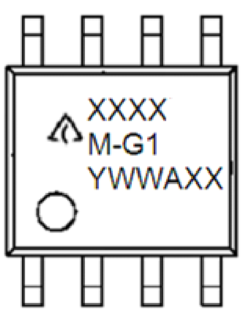
Ordering Information



Package	Temperature Range	Cable Compensation Voltage	Part Number	Marking ID	Packing
SO-8	-40 to +150°C	6%	AP3790MTR-G1	3790M-G1	4000/Tape & Reel

Marking Information

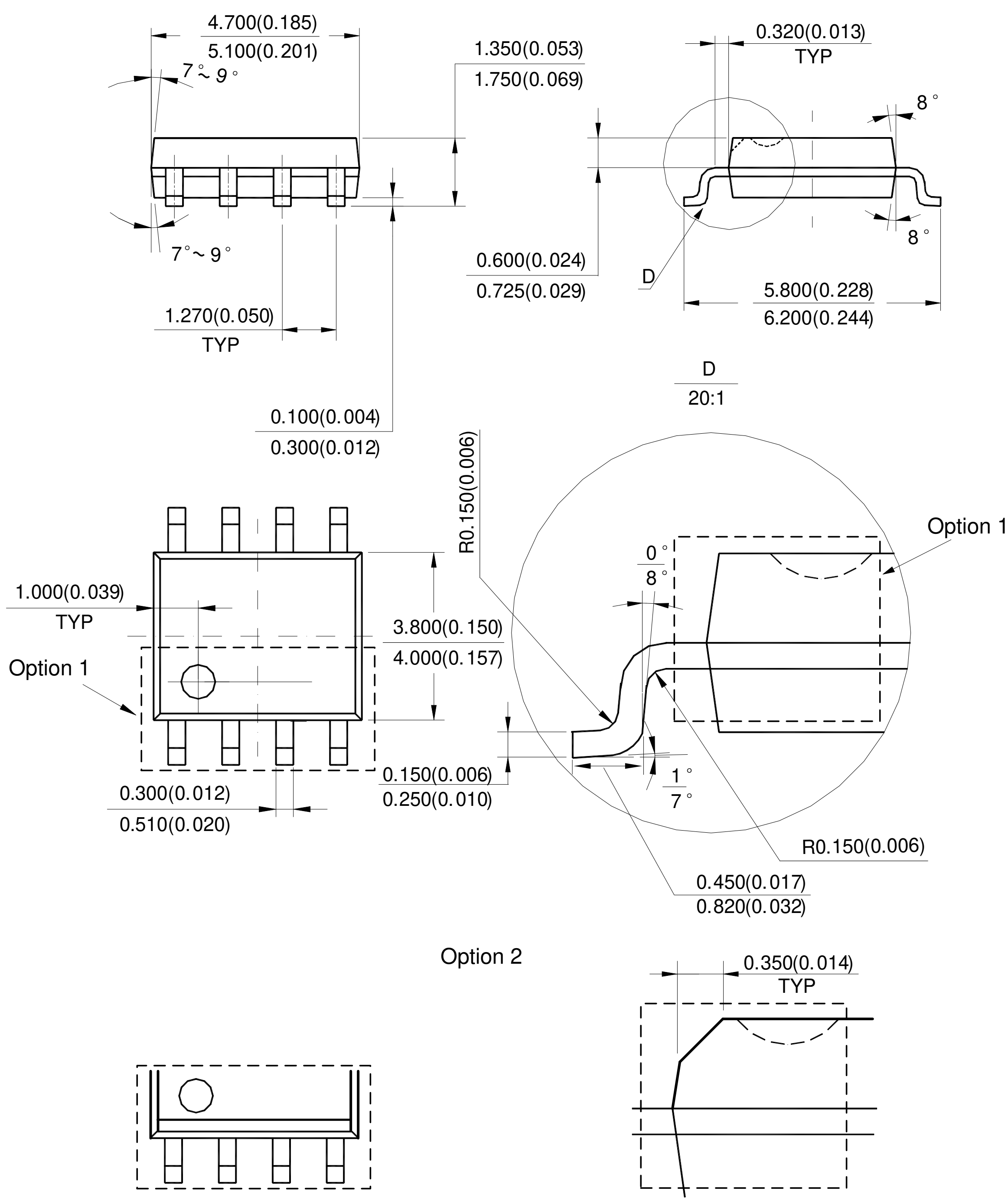
(Top View)



: Logo
XXXXM-G1: Marking ID
Third Line: Date Code
Y: Year
WW: Work Week of Molding
A: Assembly House Code
XX: 7th and 8th Digits of Batch No.

Package Outline Dimensions (All dimensions in mm(inch).)

(1) Package Type: SO-8

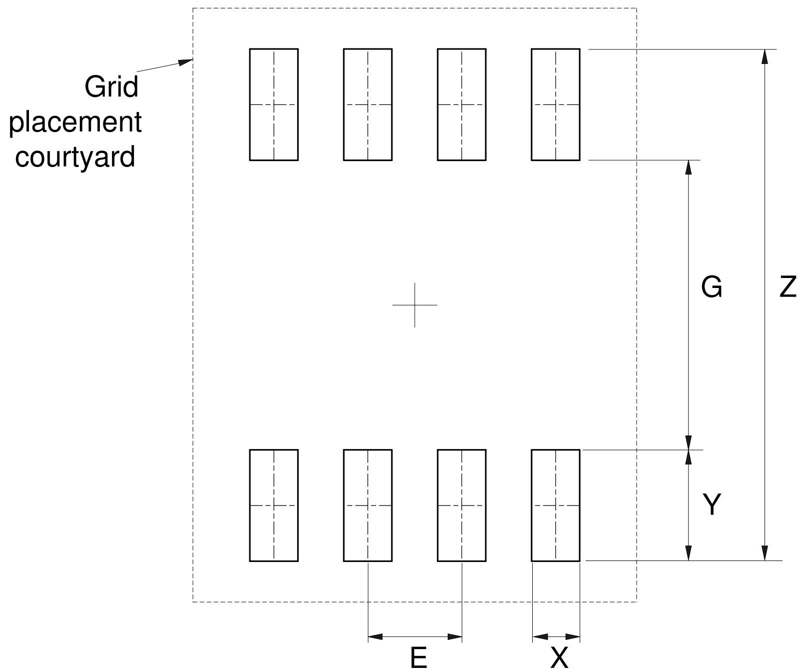


Note: Eject hole, oriented hole and mold mark is optional.

NEW PRODUCT

Suggested Pad Layout

(1) Package Type: SO-8



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	E (mm)/(inch)
Value	6.900/0.272	3.900/0.154	0.650/0.026	1.500/0.059	1.270/0.050

NEW PRODUCT