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AP4460

Step-up DC-DC Converter with Power Path for Single Solar Cell

1. General Description

The AP4460 is a synchronous step-up DC-DC converter that can be operated by a single solar cell. It has a power management function which supplies power to an external system, charges super capacitors, or supplies power from the super capacitor to the system. The DC-DC converter is a hysteric comparator type and composed of an ultra-low power start-up circuit which starts from only 0.35 V. Because the power consumption is extremely low, the AP4460 can operate with low input power generated by a solar panel under indoor lighting. The input voltage of the DC-DC converter, i.e. output voltage of the solar cell is controlled by external resistors for the reference voltage of the IC. The best power efficiency can be obtained by adjusting this input level setting according to the characteristics of a connected solar cell. The AP4460 has a Power-Path Control switches for supplying power to the external system and charging a super capacitor. When the output voltage of DC-DC converter reaches a target voltage, the IC starts to charge a compact capacitor. After charging up to the target voltage of a compact capacitor, then the IC starts to supply power to the external system. Supplying power to the external system via capacitor makes it possible to operate high load external system even with a low input power. If the input power is surplus, the extra power is stored gradually in a super capacitor. The super capacitor automatically supplies power to the external system, if the power supply input is low. The AP4460 is suitable for sensor nodes of energy harvesting equipment.

2. Features

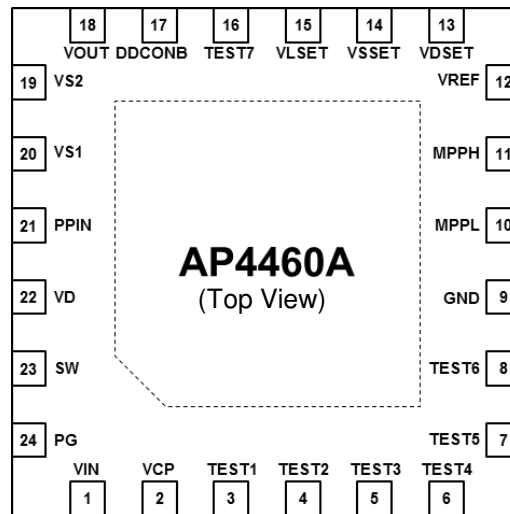
- Start-up with Ultra-low Input Voltage 0.35V(typ)
- Ultra-low Current Consumption (internal current consumption from storage element) 10nA
- Operating Temperature Range -30 ~ 85°C
- Input Voltage from 0.14V
- DC-DC Output Voltage 2.5 ~ 4.0V
- Step up DC-DC Converter with Hysteric Comparator Control
- Synchronous Rectification by High-side Zero-cross Detection
- Built-in Output Control MOSFET
- Power Path Function that Automatically Supplies Power to External System from Storage Element (when input power is insufficient)
- DC-DC Operation Monitoring Function
- Supply power to External System Quickly without depending on Storage Element
- Efficiency 80% (When 0.5V and 1mA Input, 3V output)
- Package 24-pin QFN
- Applications
 - Power Supply Systems by Single Solar Cell
 - Portable Electronics
 - Sensor Nodes
 - Wearable Devices

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6. Pin Configurations and Functions

■ Pin Configurations



Please connect exposed pad to GND or leave it OPEN.

■ Functions

No.	Pin Name	I/O	Function	Condition
1	VIN	PWR	Power input pin	
2	VCP	O	Charge pump output pin	
3	TEST1	-	Test pin	Connect to GND.
4	TEST2	-	Test pin	Connect to GND.
5	TEST3	-	Test pin	Connect to GND.
6	TEST4	-	Test pin	Connect to GND.
7	TEST5	-	Test pin	Connect to GND.
8	TEST6	I	Test pin	Connect to GND.
9	GND	PWR	Ground pin	
10	MPPL	I	MPPL reference voltage input pin	
11	MPPH	I	MPPH reference voltage input pin	
12	VREF	O	Reference voltage output pin	
13	VDSET	I	VDSET reference voltage input pin	
14	VSSET	I	VSSET reference voltage input pin	
15	VLSET	I	VLSET reference voltage input pin	
16	TEST7	I	Test pin	Connect to GND.
17	DDCONB	O	DC-DC activation signal pin	Open Drain Outputs "L" if the voltage is over MPPH voltage during V_{IN} is increasing. Outputs "H" if the voltage is less than MPPL voltage during V_{IN} is decreasing.
18	VOUT	PWR	Power supply for external system pin	
19	VS2	PWR	Storage element connect pin 2	
20	VS1	PWR	Storage element connect pin 1	
21	PPIN	PWR	Power path input pin	
22	VD	PWR	DC-DC output pin	
23	SW	PWR	Coil connect pin	
24	PG	PWR	DC-DC Ground pin	

7. Absolute Maximum Ratings

Parameter	Symbol	min	max	Unit	Condition
Pin Voltage	V_{IN}	-0.3	6.5	V	
Operation Temperature	T_a	-30	85	°C	
Storage Temperature	T_{STG}	-40	150	°C	
Junction Temperature	T_j	-40	150	°C	
Power Dissipation	P_D	-	2.9	W	(Note 2)

Note 1. All voltages are with respect to GND, unless otherwise specified.

Note 2. 2-layer board is used. This is calculated as $\theta_{JA}=42^{\circ}\text{C}/\text{W}$. (Metal area of each layer should be more than 70%, Exposed Pad should be connected to GND)

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

8. Recommended Operating Conditions

Parameter	Symbol	Condition	min	typ	max	Unit
Input Voltage (V_{IN} pin)	V_{VIN}	$V_{VD} > V_{PORL}$ (after start-up)	0.14	-	V_{VDTGT}	V
MPPH Voltage	V_{MPPH}		0.16	-	0.8	V
MPPL Voltage	V_{MPPL}	$V_{MPPH} > V_{MPPL}$	0.14	-	0.7	V
Output Voltage	V_{VDTGT}		2.5	-	4.0	V
Power supplying threshold	V_{VOUTEN}		2.2	-	$0.94 \times V_{VDTGT}$	V
Stop power supply threshold	$V_{VOUTDIS}$		2.0	-	$0.90 \times V_{VSSET}$	V
Operation Temperature	T_a		-30	-	85	°C
Junction Temperature	T_j		-30	-	95	°C
Reference resistor 1	-	$R_{OUT} + R_{VDSET} + R_{VSSET} + R_{VLSET}$	3.6	4	4.4	$M\Omega$
Reference resistor 2	-	$R_{IN} + R_{MPPH} + R_{MPPL}$	4.6	4	4.4	$M\Omega$

9. Electrical Characteristics

(Ta=25°C, The external Circuit is as [Figure 13](#), unless otherwise specified.)

Parameter	Symbol	Condition	min	typ	max	Unit
Start-up Circuit						
Minimum input voltage to start-up operation	V _{INSTUP}	T _j ≥ 25°C	-	0.35	0.40	V
Stop start-up operation (When VD is increasing)	V _{PORH}		1.8	1.9	2.0	V
Restart start-up operation (When VD is decreasing)	V _{PORL}		1.7	1.8	1.9	V
DC-DC Converter						
V _{VDTGT} voltage	V _{VDTGT}		-	4 × V _{VDSET}	-	V
V _{VDTGT} voltage accuracy	-		-5	-	+5	%
V _{VDTGT} hysteresis	V _{VDTGTHYS}		0.01 × V _{VDTGT}	0.03 × V _{VDTGT}	0.05 × V _{VDTGT}	V
High-side on resistance	R _{ONTOP}		-	1.5	-	Ω
Low-side on resistance	R _{ONBOT}		-	0.6	-	Ω
Low-side on Time	T _{ON}	V _{VD} =3.3V	2.3	4.5	6.8	μs
VD pin internal consumption current	I _{QVD}	V _{VD} =3.3V (When DC-DC converter is in skip state)	-	4.5	15	μA
MPPT Circuit						
Accuracy of V _{VIN} to activate DC-DC (Include V _{OSMPP})	V _{MPPH}	0.55V < set value < 0.8V	-5	0	+5	%
	V _{MPPH1}	0.25V < set value	-7	0	+7	%
Accuracy of V _{VIN} to be skip state (Include V _{OSMPP})	V _{MPPPL}	0.40V < set value < 0.7V	-5	0	+5	%
	V _{MPPPL1}	0.25V < set value	-7	0	+7	%
Power Path Switch						
F1 switch ON resistance	R _{F1}	VD > 2.5V, 20mA	-	2.5	5	Ω
F2 charge switch ON resistance	R _{F2C}	VS1 > 2.5V, 2mA	-	200	300	Ω
F2 discharge switch ON resistance	R _{F2D}	VS2 > 2.5V, 20mA	-	2	5	Ω
F3 switch ON resistance	R _{F3}	VS1 > 2.5V, 20mA	-	2	5	Ω
F1 switch ON voltage	V _{F1ON}	VD pin	-	V _{VDTGTH}	-	V
F1 switch OFF voltage	V _{F1OFF}	VD pin	-	V _{VDTGTH} -V _{VDTGTHYS}	-	V
F2 charge switch ON voltage (when charging)	V _{VS2CHG}	VS1 pin	-	4 × V _{VSSET} × 1.03	-	V
F2 charge switch OFF voltage (when charging)	V _{VS2HLD}	VS1 pin	-	4 × V _{VSSET} × 0.97	-	V
F2 discharge switch ON voltage (when discharging)	V _{VS2DCH}	VS1 pin	-	4 × V _{VSSET} × 0.94	-	V
F2 discharge switch OFF voltage (when discharging)	V _{VS2DIS}	VS1 pin	-	4 × V _{VLSET}	-	V
F3 switch ON voltage	V _{VOUTEN}	VS1 pin	-	4 × V _{VSSET}	-	V
F3 switch OFF voltage	V _{VOUTDIS}	VS1 pin	-	4 × V _{VLSET} × 0.97	-	V
F1, F2, F3 Control Voltage Accuracy	-	Include V _{VRFEF} accuracy	-5	0	+5	%
Reference Voltage						
Reference Voltage Output	V _{VREF}		1.187	1.236	1.285	V
Current Consumption						

Parameter	Symbol	Condition	min	typ	max	Unit
VS1, VS2, VOUT pin total current (Note 3)	-	$V_{VD} < V_{PORL}$	-	10	20	nA
Protect Function						
F2 discharge switch over current protection	I_{F2CLIM}	VS1 pin grounding	50	250	700	mA
F3 switch over current protection	I_{F3CLIM}	VOUT pin grounding	50	250	700	mA
VD over voltage protection	V_{OV}		4.2	4.45	4.7	V
VD over voltage protection hysteresis	V_{OVHYS}		0.35	0.45	0.55	V
Logic I/O						
DDCONB Output Voltage	$V_{OLDDCON}$	I load < 10 μ A	0	-	0.3	V
DDCONB Leakage Current	$I_{OHDDCON}$	$V_{DDCON} < 4V$	-	1	10	nA

Note 3. If there is no input power and $V_{VD} < V_{PORL}$, F1 becomes off and F2 and F3 become on. The internal current consumption of the IC is 10nA(typ) at this time.

10. Functional Descriptions

10.1 Operation

The AP4460 is a synchronous step-up DC-DC converter that can be activated by a single solar cell. The IC has a power management function which supplies power to an external system, charges super capacitors, or controls the power path to supply power from the super capacitor to the external system. The AP4460 can be operated from 0.35V (typ) at the VIN pin. The start-up circuit is operated when V_{VIN} voltage reaches V_{INSTUP}. Then, the internal charge pump circuit boosts V_{VIN} voltage and charges the capacitor connected to the VCP pin (C_{VCP}). When the VCP voltage reaches enough level, the internal start-up circuit switches the N-channel MOSFET transistor (S1) and charges the external capacitor connected to the VD pin (C_{VD}). The start-up circuit is stopped when the VD voltage reaches V_{PORH} level, then the DC-DC converter starts the operation. When the VD voltage drops to the level less than V_{PORL}, the DC-DC converter stops and the start-up circuits is operated again.

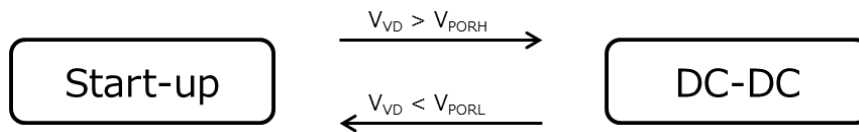


Figure 2. State transition of Start-up and DC-DC operation

The DC-DC converter activates the N-channel MOSFET transistor (N1) during T_{ON} period to charge the coil. After T_{ON} period, the energy stored in the coil is charged to the C_{VD} capacitor by a power switching of N1 transistor (becomes OFF) and the P1 transistor (becomes ON). The control circuits of the DC-DC sets the P1 transistor off when the SW voltage becomes less than the VD voltage, and then the N1 transistor turns on. The operation of DC-DC converter is controlled by three reference voltages such as VDSET, MPPL and MPPH voltages. The VDSET voltage controls the output voltage level (V_{VDTGT}) of DC-DC converter. When the VD voltage reaches V_{VDTGT} level, the DC-DC converter stops the switching operation and enters 'Skip' state to save current consumption. When the VD voltage becomes less than V_{VDTGT} - V_{VDTGT_HYS}, the DC-DC converter goes to 'Switching' state and boosts the VD voltage. The inputs of the MPPH pin and the MPPL pin (V_{MPPH} and V_{MPPL}) control the input voltage of the DC-DC converter (V_{VIN}) for effective voltage level of a solar cell. When the V_{VIN} voltage becomes less than V_{MPPTL} voltage, the DC-DC converter stops switching operation and goes to Skip state until V_{VIN} voltage reaches V_{MPPTH} voltage. By adjusting input levels of the MPPH pin and the MPPL pin (V_{MPPH} and V_{MPPL}), the maximum output solar power can be efficiently generated.

The DDCONB (N-channel MOSFET open drain) pin outputs "L" when V_{VIN} voltage is in between V_{MPPL} and V_{MPPH}. The DC-DC converter has the over voltage protection function for the VD pin. When the VD voltage exceeds V_{OV} level, the DC-DC converter transitions to Skip state to prevent further voltage increase. When the VD voltage becomes lower than V_{OV}-V_{OVHYS}, the converter restarts switching operation.

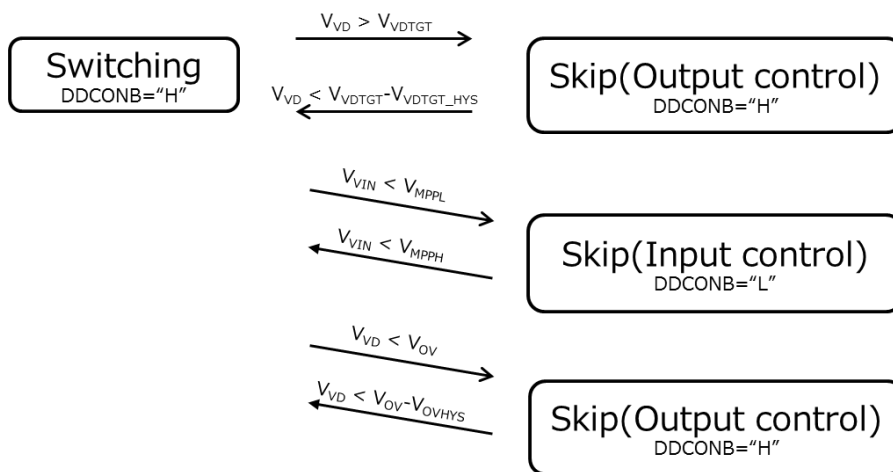


Figure 3. State Transition of DC-DC Operation

F1, F2 and F3 switches compose the Power Path function. The F1 switch is placed between the PPIN pin and the VS1 pin, F2 switch is placed between the VS1 pin and the VS2 pin and F3 switch is placed between the VS1 pin and the VOUT pin. The F1 switch is synchronized with DC-DC converter statement that is controlled by the VD condition. When the VD voltage reaches V_{VDTGT} by DC-DC converter, the F1 switch becomes ON state and the VD charge is transferred to VS1 to charge the external capacitor until VD voltage becomes less than $V_{VDTGT} - V_{VDTGT_HYS}$. In other situations, the F1 switch is in OFF state to prevent reverse current flowing from the VS1 pin to the VD pin. When the VS1 voltage reaches V_{VOUTEN} , the F3 switch becomes ON state and the VOUT output is available for system loads. The F3 switch is turned OFF when the VS1 voltage becomes less than $V_{VOUTDIS}$. When the VS1 voltage reaches V_{VS2CHG} , the F2 switch changes to ON state and the VS1 charge is transferred to the capacitor connected to the VS2 pin until the VS1 voltage becomes V_{VS2HLD} . When VS1 voltage drops less than V_{VS2DCH} , the F2 switch also becomes ON state and the VS2 charge is transferred to the capacitor connected to the VS1 pin. If the VS1 voltage is below $V_{VOUTDIS}$, the F2 switch is turned OFF. Unnecessary power dissipation of the external system can be reduced by setting $V_{VOUTDIS}$ higher than the lowest operation voltage of the external system connected to the VOUT pin. When the VD voltage becomes less than V_{VPORL} , the F2 and F3 switches become ON state. At this time, if the capacitor connected to the VS2 pin (C_{VS2}) is charged enough, the power supply operation to the external system is continued. In case the VD voltage again reaches V_{VDTGT} , the F2 and F3 switches remain in ON state if the VS1 voltage is over $V_{VOUTDIS} \times 1.03$. If VS1 voltage is below $V_{VOUTDIS}$, the F2 and F3 switches change to OFF state.

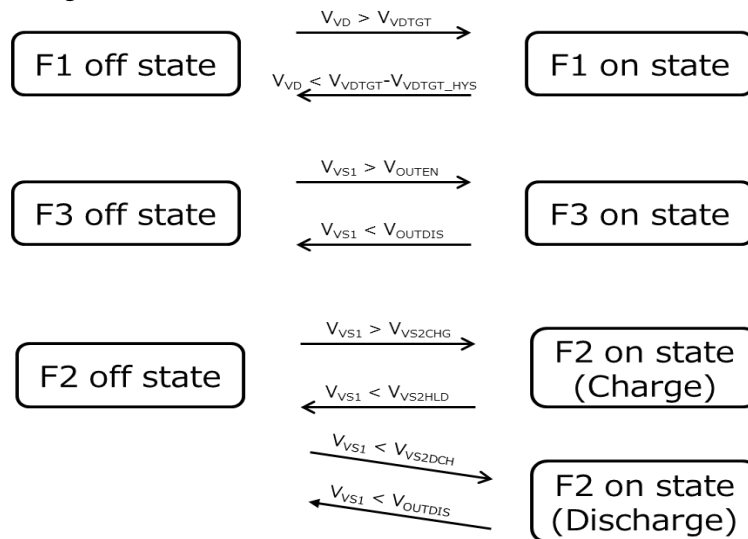


Figure 4. State Transition of the Power Path Switches

10.2 Determine the control threshold of the DC-DC converter and power path

Four resistors are needed to connect in series between the VREF pin and GND to determine the output target of the DC-DC converter (V_{VDTGT}), the output start voltage of the VOUT pin and charge/discharge threshold of the super capacitor. The voltages between each resistor should be input to the VDSET pin, the VSSET pin and the VLSET pin. The control threshold of the DC-DC converter input voltage can be determined by connecting three resistors in series between the VREF pin and GND, and the voltages between each resistor should be input to the MPPH pin and the MPPL pin. The connection of resistors is shown in Figure 5.

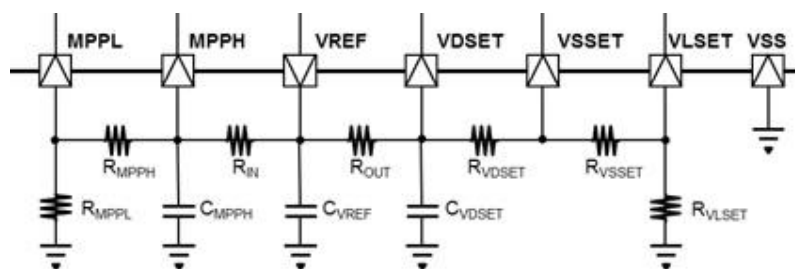


Figure 5. Resistor connection circuit

■ Determination of the control threshold voltage and external resistors

Table 1. Calculation of the control threshold voltage

Symbol	Calculation Formula
V_{MPPL}	$V_{REF} \times R_{MPPL} / (R_{MPPL} + R_{MPPH} + R_{IN})$
V_{MPPH}	$V_{REF} \times (R_{MPPL} + R_{MPPH}) / (R_{MPPL} + R_{MPPH} + R_{IN})$
V_{VDSET}	$V_{REF} \times (R_{VDSET} + R_{VSSET} + R_{VLSET}) / (R_{OUT} + R_{VDSET} + R_{VSSET} + R_{VLSET})$
V_{VSSET}	$V_{REF} \times (R_{VSSET} + R_{VLSET}) / (R_{OUT} + R_{VDSET} + R_{VSSET} + R_{VLSET})$
V_{VLSET}	$V_{REF} \times R_{VLSET} / (R_{OUT} + R_{VDSET} + R_{VSSET} + R_{VLSET})$

Note 4. Refer to 9. Electrical Characteristics as for V_{VDTGT} , F2 charge/discharge switch ON/OFF voltage and F3 switch ON voltage.

Table 2. Example settings of the external resistors, V_{MPPL} and V_{MPPH} (typ)

V_{REF}	R_{MPPL}	R_{MPPH}	R_{IN}	V_{MPPL}	V_{MPPH}
1.236V	1.6MΩ	0.2MΩ	2.4MΩ	0.471V	0.530V

Note 5. $R_{MPPL} + R_{MPPH} + R_{IN}$ should be more than 3.6MΩ. Above setting is just an example, please choose appropriate numbers according to the input conditions.

Table 3. Example settings of V_{DSET} , V_{SSET} and V_{LSET} (typ)

V_{REF}	R_{OUT}	R_{VDSET}	R_{VSSET}	R_{VLSET}	V_{VDSET}	V_{VSSET}	V_{VLSET}
1.236V	1.3MΩ	0.24MΩ	0.56MΩ	1.8MΩ	3.296 / 4 = 0.824V	2.992 / 4 = 0.748V	2.282 / 4 = 0.571 V

Note 6. $R_{OUT} + R_{VDSET} + R_{VSSET} + R_{VLSET}$ should be more than 3.6MΩ. Above setting is just an example, please choose appropriate numbers according to the input conditions.

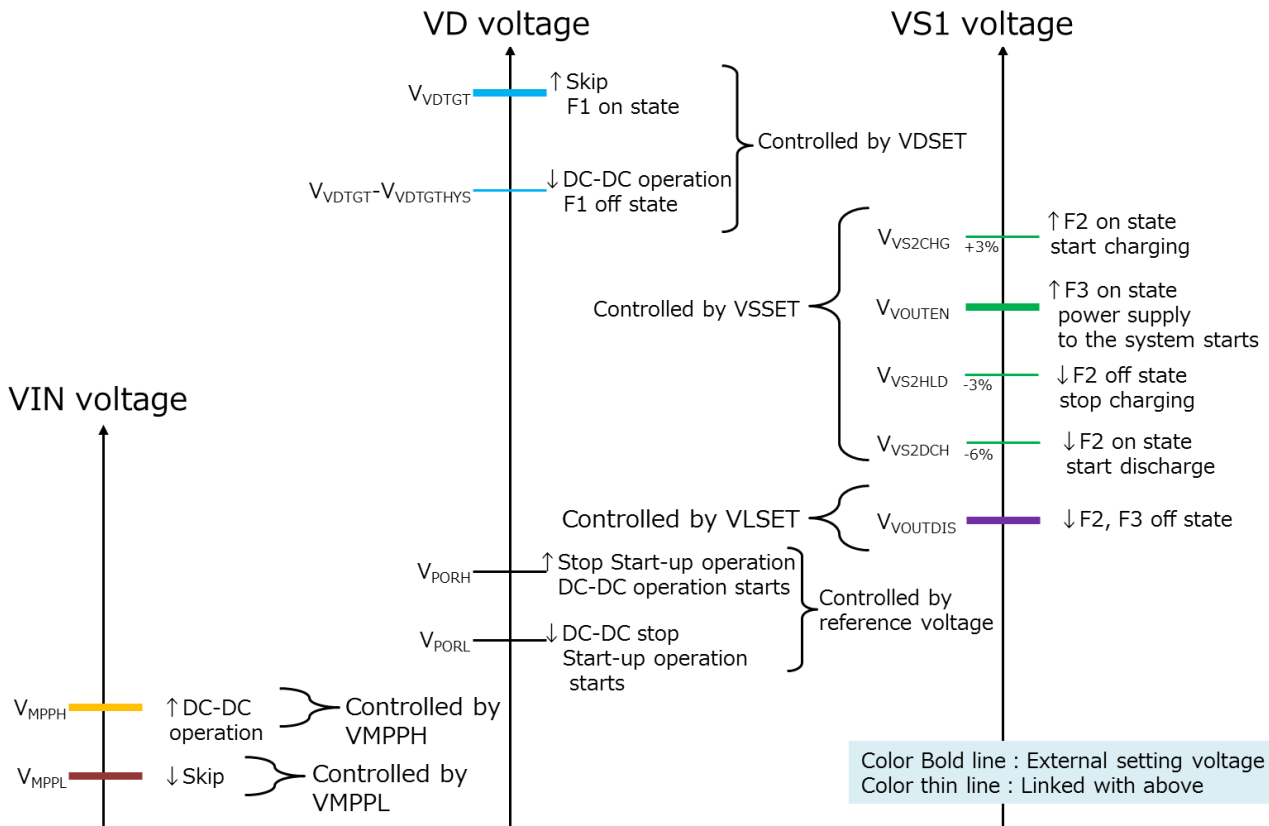


Figure 6. Control Threshold Voltages

10.3 Timing Chart

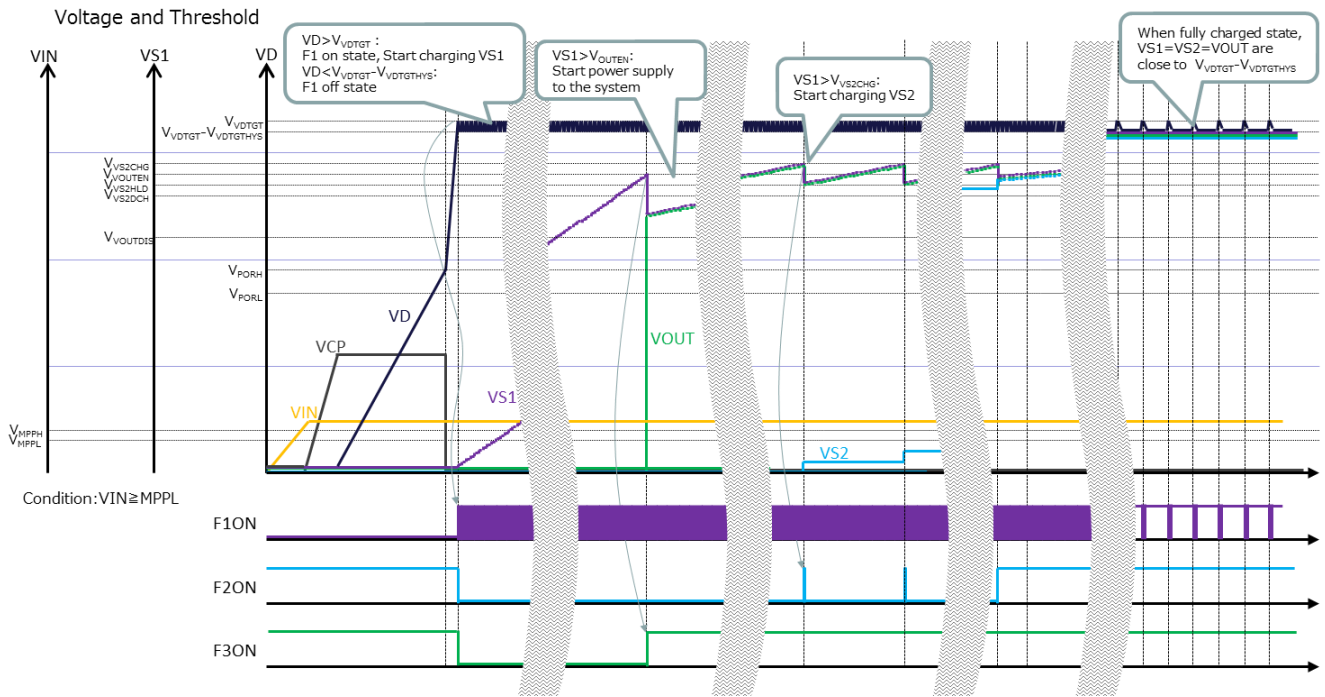


Figure 7. Timing Chart 1: from Start-up to Charge (No Initial Charging)

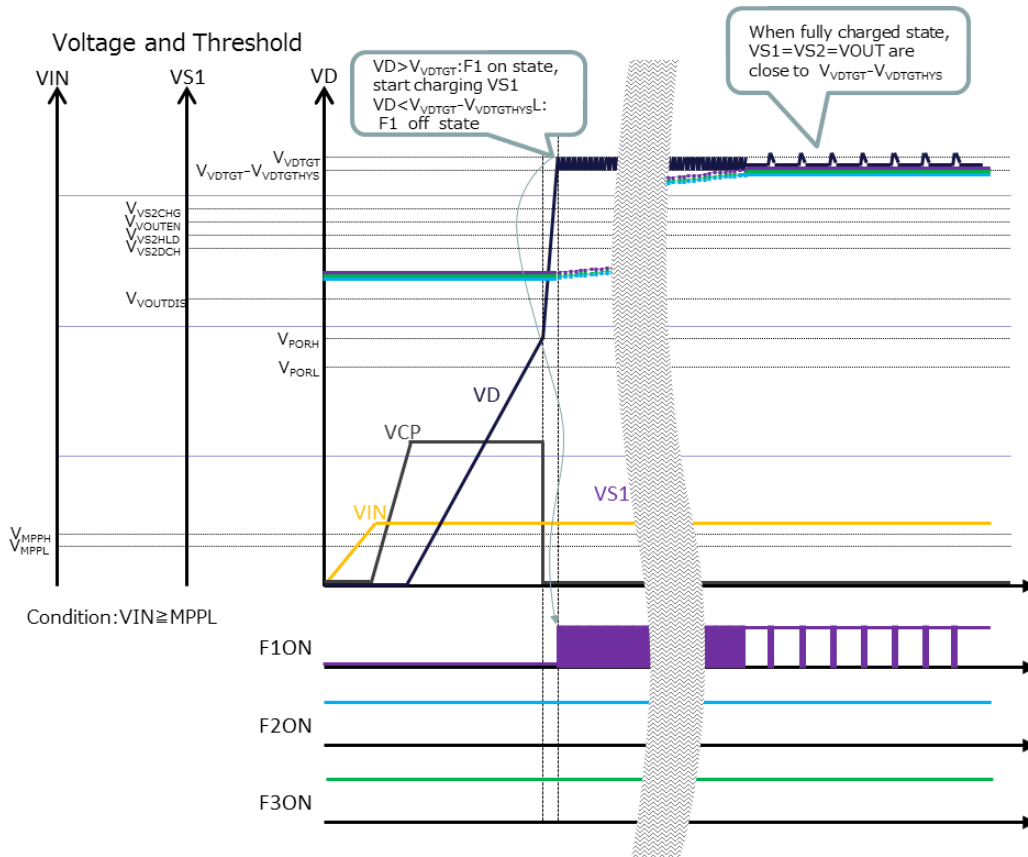


Figure 8. Timing Chart 2: from Start-up to Charge (With Initial Charging)

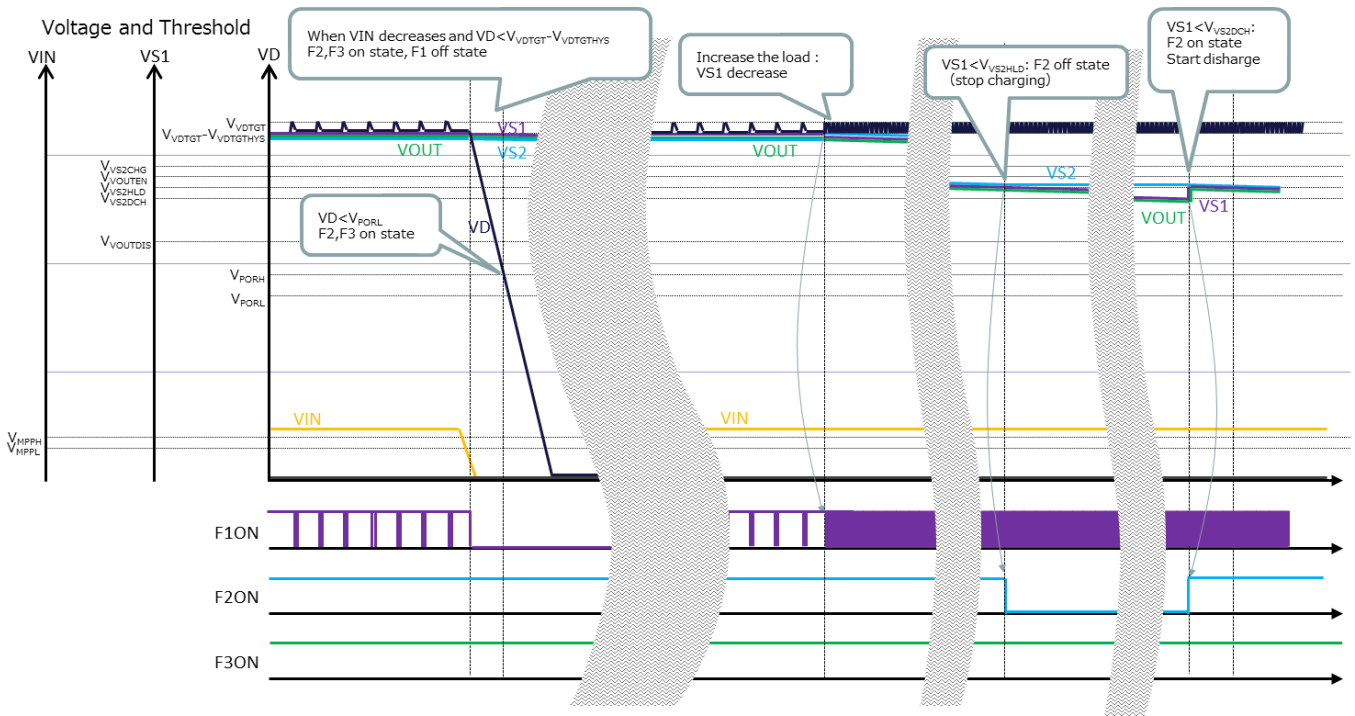


Figure 9. Timing Chart 3: (Left) VIN decrease, (Right) Load increase

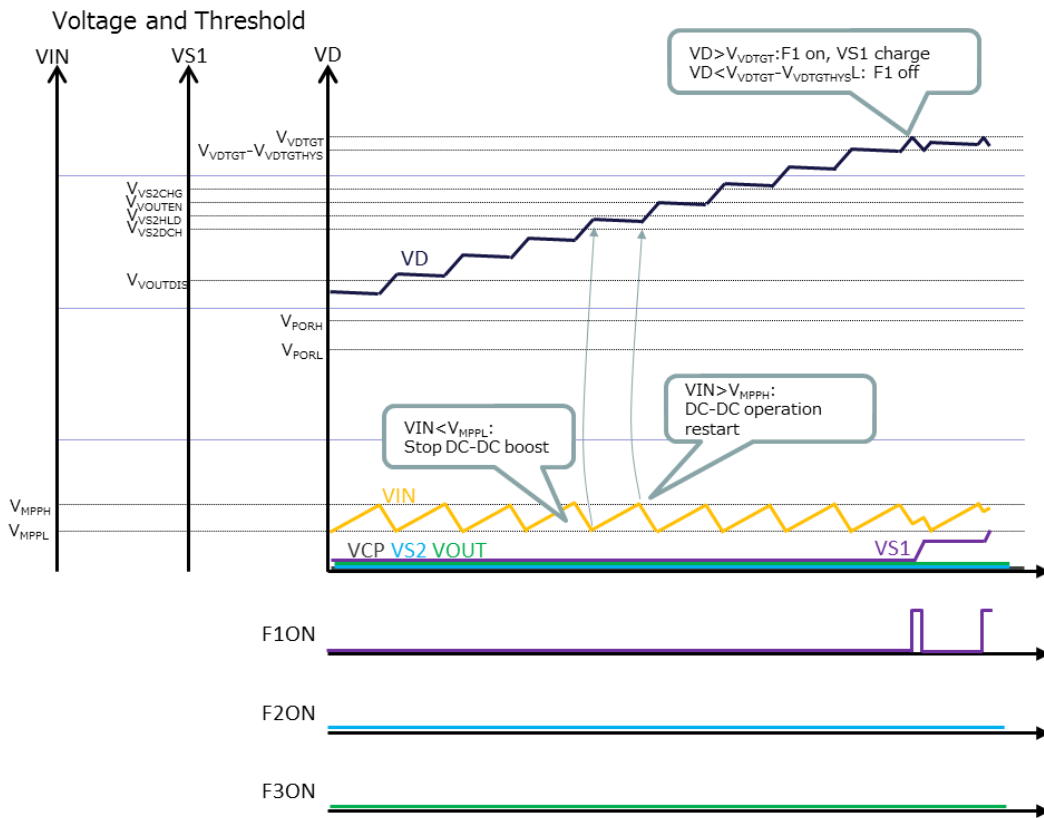


Figure 10. Timing Chart 4: Control VIN voltage

10.4 Input/output Current Characteristic

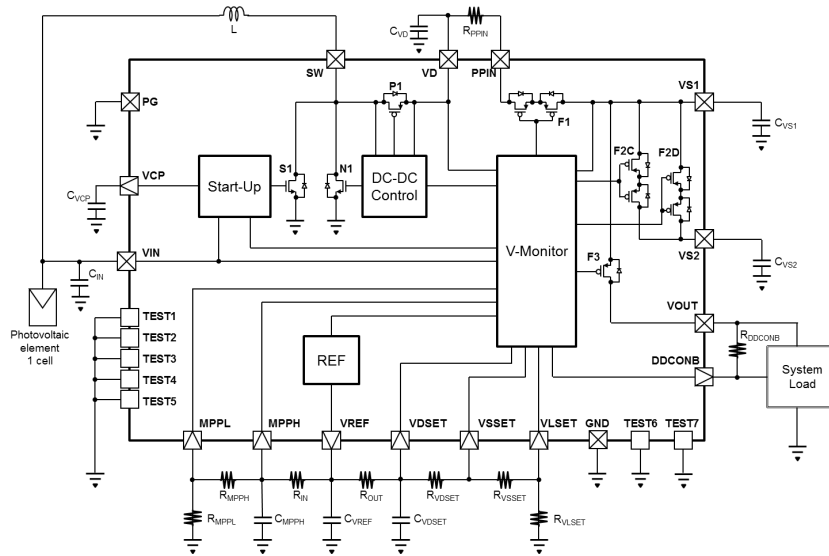


Figure 11. Circuit Example

Internal current consumption of each pin is shown in Figure 12.

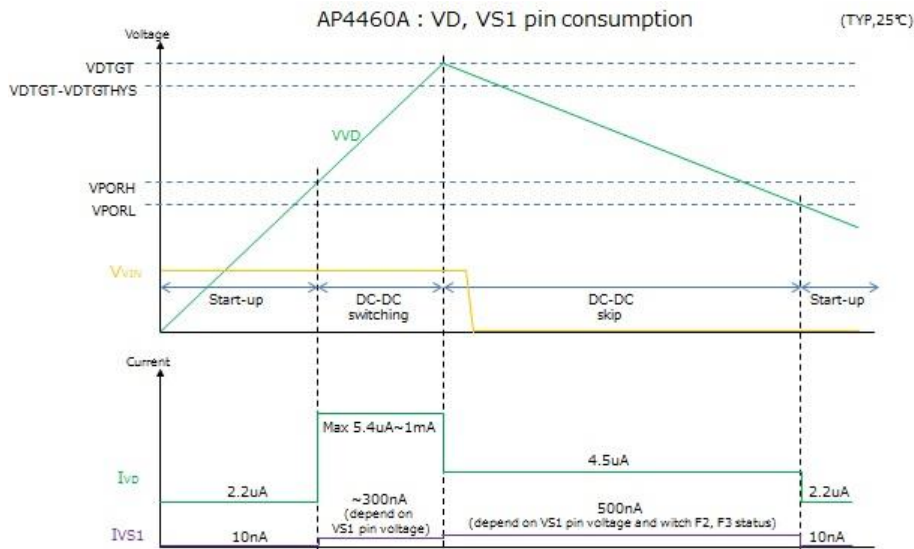
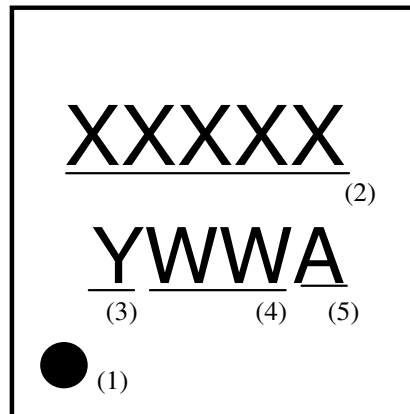


Figure 12. The consumption for VD and VS1 pin

- In the case of Start-up: VD pin current (I_{VD} , inflow into VD pin) is about 2.2uA and VS1 pin current (I_{VS1} , inflow into VS1 pin) is about 10nA before V_{VD} reaches to V_{PORH} voltage. (In case of $V_{VD} < V_{PORL}$, F2 switch= ON, the total internal consumption of VS1 and VS2 pins is 10nA.)
- In the case of DC-DC switching: After V_{VD} reaches to V_{PORH} , until V_{VD} drops to V_{PORL} , I_{VD} is 5.4uA~1mA depends on switching period and V_{VD} voltage.
- In the case of DC-DC skip (intermittent action): After V_{VD} reaches to V_{TGT} , internal current consumption is about 4.7uA. I_{VS1} consumption is determined by VS1 pin voltage and internal resistor. (Maximum I_{VS1} is 500nA when VS1 voltage= 4V) After V_{VD} reaches to V_{TGT} , until V_{VD} drops to $V_{VDTGT}-V_{VDTGTHYS}$, switch F1= OFF, the adverse current (from VS1 pin to VD pin) is not occurred. When V_{VD} reaches V_{PORL} , I_{VD} is about 2.2uA and I_{VS1} is about 10nA.

■ **Marking**



- (1) 1pin Indication
- (2) Market Code : 4460A
- (3) Year Code (last 1 digit)
- (4) Week Code
- (5) Management Code

11 . Revise History

Date (YY/MM/DD)	Revision	Page	Contents
14/12/09	00	-	First edition
15/04/16	01	10	Table 2. error correction

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