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ProASIC^{PLUS}® Flash Family FPGAs



Features and Benefits

High Capacity

Commercial and Industrial

- 75,000 to 1 Million System Gates
- 27 k to 198 kbits of Two-Port SRAM
- 66 to 712 User I/Os

Military

- 300,000 to 1 million System Gates
- 72 k to 198 kbits of Two Port SRAM
- 158 to 712 User I/Os

Reprogrammable Flash Technology

- 0.22 μm 4 LM Flash-Based CMOS Process
- Live At Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- No Configuration Device Required
- Retains Programmed Design during Power-Down/Up Cycles
- Mil/Aero Devices Operate over Full Military Temperature Range

Performance

- 3.3 V, 32-Bit PCI, up to 50 MHz (33 MHz over military temperature)
- Two Integrated PLLs
- External System Performance up to 150 MHz

Secure Programming

- The Industry's Most Effective Security Key (FlashLock[®])

Low Power

- Low Impedance Flash Switches
- Segmented Hierarchical Routing Structure
- Small, Efficient, Configurable (Combinatorial or Sequential) Logic Cells

High Performance Routing Hierarchy

- Ultra-Fast Local and Long-Line Network
- High-Speed Very Long-Line Network
- High-Performance, Low Skew, Splittable Global Network
- 100% Routability and Utilization

I/O

- Schmitt-Trigger Option on Every Input
- 2.5 V/3.3 V Support with Individually-Selectable Voltage and Slew Rate
- Bidirectional Global I/Os
- Compliance with PCI Specification Revision 2.2
- Boundary-Scan Test IEEE Std. 1149.1 (JTAG) Compliant
- Pin Compatible Packages across the ProASIC^{PLUS} Family

Unique Clock Conditioning Circuitry

- PLL with Flexible Phase, Multiply/Divide and Delay Capabilities
- Internal and/or External Dynamic PLL Configuration
- Two LVPECL Differential Pairs for Clock or Data Inputs

Standard FPGA and ASIC Design Flow

- Flexibility with Choice of Industry-Standard Front-End Tools
- Efficient Design through Front-End Timing and Gate Optimization

ISP Support

- In-System Programming (ISP) via JTAG Port

SRAMs and FIFOs

- SmartGen Netlist Generation Ensures Optimal Usage of Embedded Memory Blocks
- 24 SRAM and FIFO Configurations with Synchronous and Asynchronous Operation up to 150 MHz (typical)

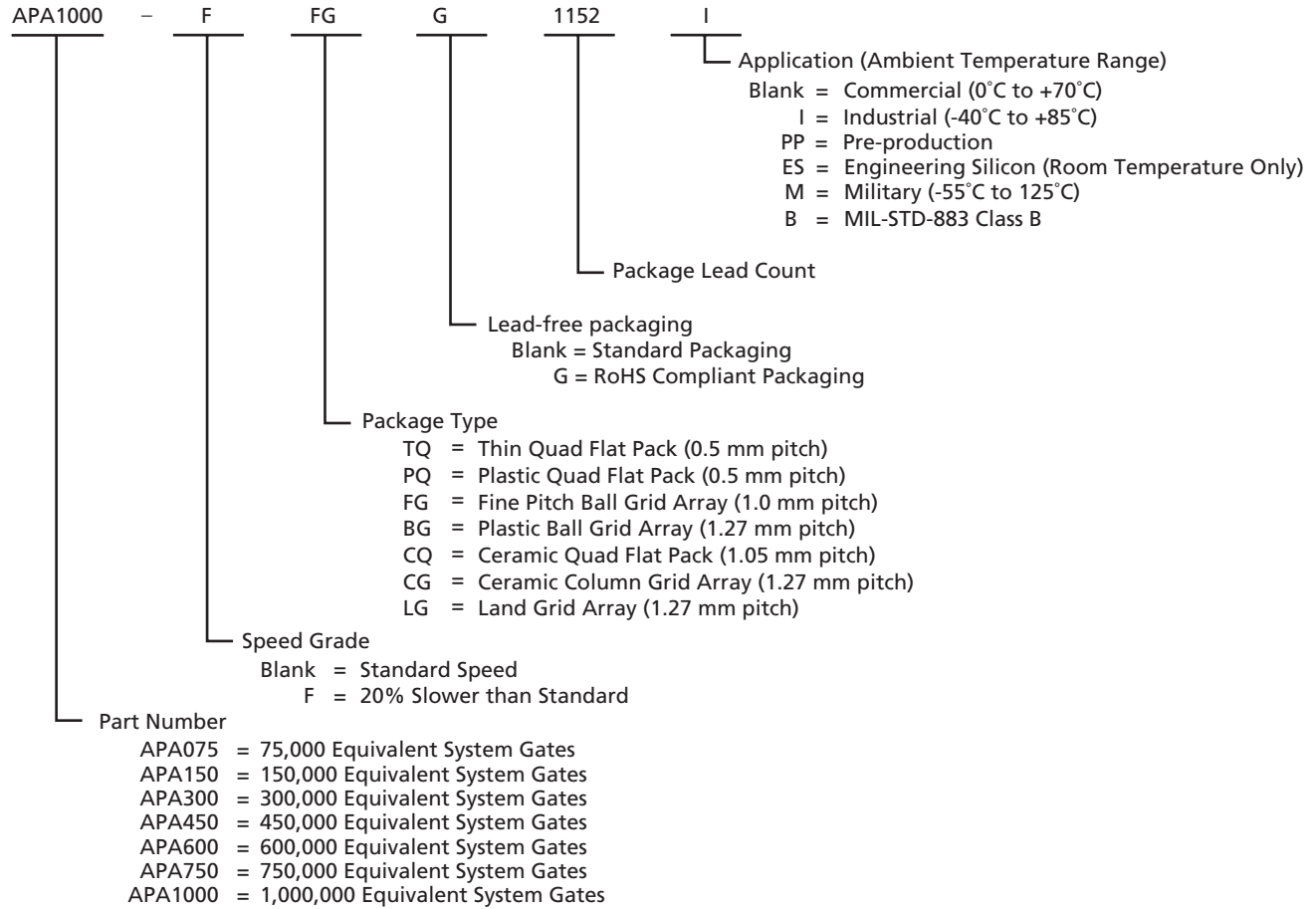
Table 1 • ProASIC^{PLUS} Product Profile

Device	APA075	APA150	APA300 ¹	APA450	APA600 ¹	APA750	APA1000 ¹
Maximum System Gates	75,000	150,000	300,000	450,000	600,000	750,000	1,000,000
Tiles (Registers)	3,072	6,144	8,192	12,288	21,504	32,768	56,320
Embedded RAM Bits (k=1,024 bits)	27 k	36k	72 k	108 k	126 k	144 k	198 k
Embedded RAM Blocks (256x9)	12	16	32	48	56	64	88
LVPECL	2	2	2	2	2	2	2
PLL	2	2	2	2	2	2	2
Global Networks	4	4	4	4	4	4	4
Maximum Clocks	24	32	32	48	56	64	88
Maximum User I/Os	158	242	290	344	454	562	712
JTAG ISP	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Package (by pin count)							
TQFP	100, 144	100	–	–	–	–	–
PQFP	208	208	208	208	208	208	208
PBGA	–	456	456	456	456	456	456
FBGA	144	144, 256	144, 256	144, 256, 484	256, 484, 676	676, 896	896, 1152
CQFP ²			208, 352		208, 352		208, 352
CCGA/LGA ²					624		624

Notes:

1. Available as Commercial/Industrial and Military/ML-STD-883B devices.
2. These packages are available only for Military/ML-STD-883B devices.

Ordering Information



Device Resources

User I/Os ²													
Commercial/Industrial											Military/MIL-STD-883B		
Device	TQFP 100-Pin	TQFP 144-Pin	PQFP 208-Pin	PBGA 456-Pin	FBGA 144-Pin	FBGA 256-Pin	FBGA 484-Pin	FBGA 676-Pin	FBGA 896-Pin	FBGA 1152-Pin	CQFP 208-Pin	CQFP 352-Pin	CCGA/ LGA 624-Pin
APA075	66	107	158		100								
APA150	66		158	242	100	186 ³							
APA300			158 ⁴	290 ⁴	100 ⁴	186 ^{3,4}					158	248	
APA450			158	344	100	186 ³	344 ³						
APA600			158 ⁴	356 ⁴		186 ^{3,4}	370 ³	454			158	248	440
APA750			158	356				454	562 ⁵				
APA1000			158 ⁴	356 ⁴					642 ^{4,5}	712 ⁵	158	248	440

Notes:

1. Package Definitions: TQFP = Thin Quad Flat Pack, PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array, CQFP = Ceramic Quad Flat Pack, CCGA = Ceramic Column Grid Array, LGA = Land Grid Array
2. Each pair of PECL I/Os is counted as one user I/O.
3. FG256 and FG484 are footprint-compatible packages.
4. Military Temperature Plastic Package Offering
5. FG896 and FG1152 are footprint-compatible packages.

General Guideline

Maximum performance numbers in this datasheet are based on characterized data. Actel does not guarantee performance beyond the limits specified within the datasheet.

Temperature Grade Offerings

Package	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
TQ100	C, I	C, I					
TQ144	C, I						
PQ208	C, I	C, I	C, I, M	C, I	C, I, M	C, I	C, I, M
BG456		C, I	C, I, M	C, I	C, I, M	C, I	C, I, M
FG144	C, I	C, I	C, I, M	C, I			
FG256		C, I	C, I, M	C, I	C, I, M		
FG484				C, I	C, I, M		
FG676					C, I, M	C, I	
FG896						C, I	C, I, M
FG1152							C, I
CQ208			M, B		M, B		M, B
CQ352			M, B		M, B		M, B
CG624					M, B		M, B

Note: C = Commercial
 I = Industrial
 M = Military
 B = MIL-STD-883

Speed Grade and Temperature Matrix

	-F	Std.
C	✓	✓
I		✓
M, B		✓

Note: C = Commercial
 I = Industrial
 M = Military
 B = MIL-STD-883

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General Description

The ProASIC^{PLUS} family of devices, Actel's second-generation Flash FPGAs, offers enhanced performance over Actel's ProASIC family. It combines the advantages of ASICs with the benefits of programmable devices through nonvolatile Flash technology. This enables engineers to create high-density systems using existing ASIC or FPGA design flows and tools. In addition, the ProASIC^{PLUS} family offers a unique clock conditioning circuit based on two on-board phase-locked loops (PLLs). The family offers up to one million system gates, supported with up to 198 kbits of two-port SRAM and up to 712 user I/Os, all providing 50 MHz PCI performance.

Advantages to the designer extend beyond performance. Unlike SRAM-based FPGAs, four levels of routing hierarchy simplify routing, while the use of Flash technology allows all functionality to be live at power-up. No external boot PROM is required to support device programming. While on-board security mechanisms prevent access to the program information, reprogramming can be performed in-system to support future design iterations and field upgrades. The device's architecture mitigates the complexity of ASIC migration at higher user volume. This makes ProASIC^{PLUS} a cost-effective solution for applications in the networking, communications, computing, and avionics markets.

The ProASIC^{PLUS} family achieves its nonvolatility and reprogrammability through an advanced Flash-based 0.22 μm LVCMOS process with four layers of metal. Standard CMOS design techniques are used to implement logic and control functions, including the PLLs and LVPECL inputs. This results in predictable performance compatible with gate arrays.

The ProASIC^{PLUS} architecture provides granularity comparable to gate arrays. The device core consists of a Sea-of-Tiles™. Each tile can be configured as a flip-flop, latch, or three-input/one-output logic function by programming the appropriate Flash switches. The

combination of fine granularity, flexible routing resources, and abundant Flash switches allow 100% utilization and over 95% routability for highly congested designs. Tiles and larger functions are interconnected through a four-level routing hierarchy.

Embedded two-port SRAM blocks with built-in FIFO/RAM control logic can have user-defined depths and widths. Users can also select programming for synchronous or asynchronous operation, as well as parity generations or checking.

The unique clock conditioning circuitry in each device includes two clock conditioning blocks. Each block provides a PLL core, delay lines, phase shifts (0° and 180°), and clock multipliers/dividers, as well as the circuitry needed to provide bidirectional access to the PLL. The PLL block contains four programmable frequency dividers which allow the incoming clock signal to be divided by a wide range of factors from 1 to 64. The clock conditioning circuit also delays or advances the incoming reference clock up to 8 ns (in increments of 0.25 ns). The PLL can be configured internally or externally during operation without redesigning or reprogramming the part. In addition to the PLL, there are two LVPECL differential input pairs to accommodate high-speed clock and data inputs.

To support customer needs for more comprehensive, lower-cost, board-level testing, Actel's ProASIC^{PLUS} devices are fully compatible with IEEE Standard 1149.1 for test access port and boundary-scan test architecture. For more information concerning the Flash FPGA implementation, please refer to the "[Boundary Scan \(JTAG\)](#)" section on page 1-11.

ProASIC^{PLUS} devices are available in a variety of high-performance plastic packages. Those packages and the performance features discussed above are described in more detail in the following sections.

ProASIC^{PLUS} Architecture

The proprietary ProASIC^{PLUS} architecture provides granularity comparable to gate arrays.

The ProASIC^{PLUS} device core consists of a Sea-of-Tiles (Figure 1-1). Each tile can be configured as a three-input logic function (e.g., NAND gate, D-Flip-Flop, etc.) by programming the appropriate Flash switch interconnections (Figure 1-2 and Figure 1-3 on page 1-3). Tiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to

the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew global signal distribution throughout the core. Maximum core utilization is possible for virtually any design.

ProASIC^{PLUS} devices also contain embedded, two-port SRAM blocks with built-in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user defined depth and width, and parity generation or checking. Please see the "Embedded Memory Configurations" section on page 1-23 for more information.

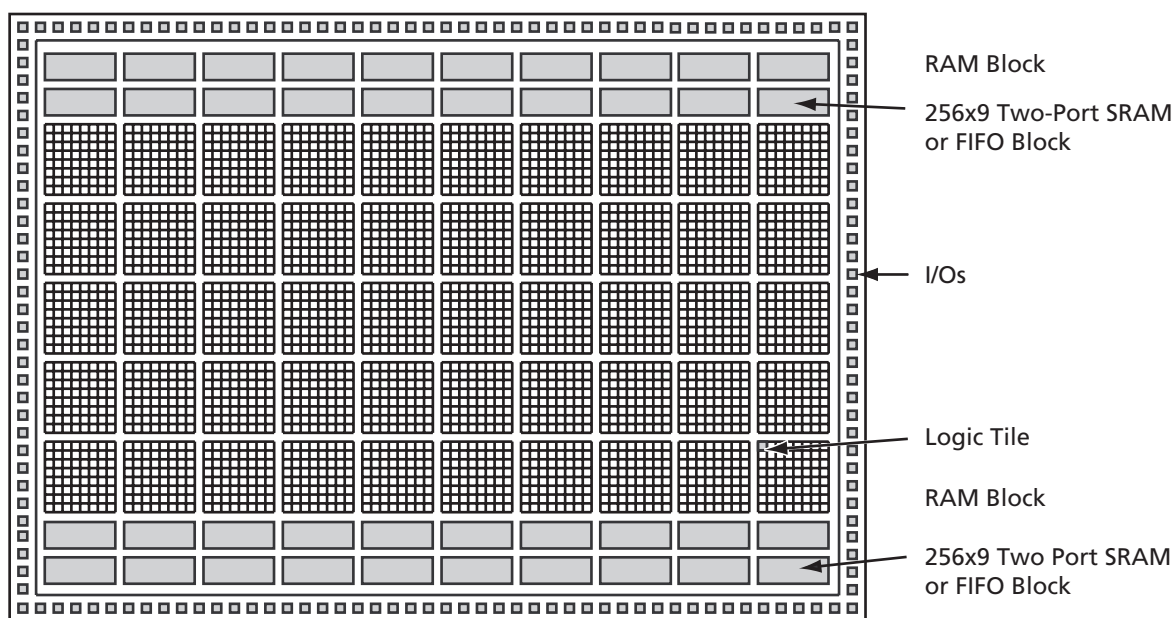


Figure 1-1 • The ProASIC^{PLUS} Device Architecture

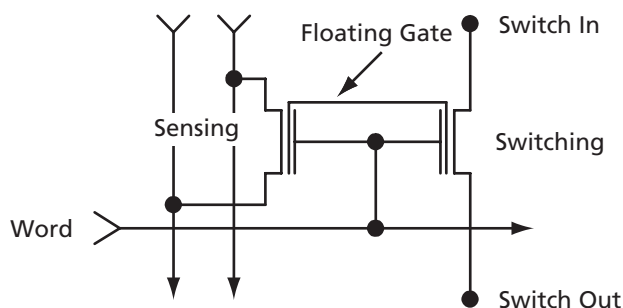


Figure 1-2 • Flash Switch

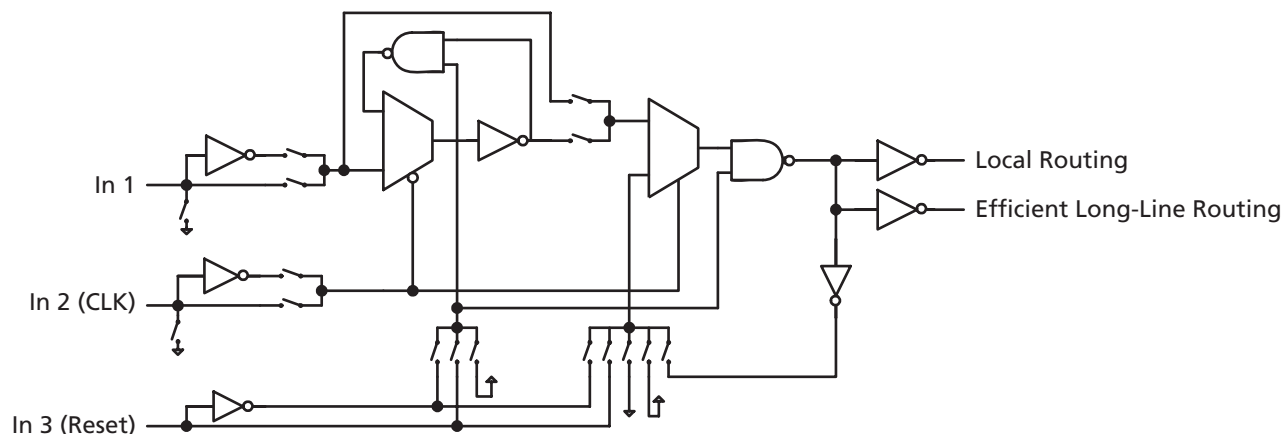


Figure 1-3 • Core Logic Tile

Live at Power-Up

The Actel Flash-based ProASIC^{PLUS} devices support Level 0 of the live at power-up (LAPU) classification standard. This feature helps in system component initialization, executing critical tasks before the processor wakes up, setting up and configuring memory blocks, clock generation, and bus activity management. The LAPU feature of Flash-based ProASIC^{PLUS} devices greatly simplifies total system design and reduces total system cost, often eliminating the need for Complex Programmable Logic Device (CPLD) and clock generation PLLs that are used for this purpose in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC^{PLUS} device's Flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC^{PLUS} devices simplify total system design, and reduce cost and design risk, while increasing system reliability and improving system initialization time.

Flash Switch

Unlike SRAM FPGAs, ProASIC^{PLUS} uses a live-on-power-up ISP Flash switch as its programming element.

In the ProASIC^{PLUS} Flash switch, two transistors share the floating gate, which stores the programming information. One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. It can be used in the architecture to connect/separate routing nets or to configure logic. It is also used to erase the floating gate (Figure 1-2 on page 1-2).

Logic Tile

The logic tile cell (Figure 1-3) has three inputs (any or all of which can be inverted) and one output (which can connect to both ultra-fast local and efficient long-line routing resources). Any three-input, one-output logic function (except a three-input XOR) can be configured as one tile. The tile can be configured as a latch with clear or set or as a flip-flop with clear or set. Thus, the tiles can flexibly map logic and sequential gates of a design.

Routing Resources

The routing structure of ProASIC^{PLUS} devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources, efficient long-line resources, high-speed, very long-line resources, and high performance global networks.

The ultra-fast local resources are dedicated lines that allow the output of each tile to connect directly to every input of the eight surrounding tiles (Figure 1-4).

The efficient long-line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning 1, 2, or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC^{PLUS} device (Figure 1-5 on page 1-5). Each tile can drive signals onto the efficient long-line resources, which

can in turn access every input of every tile. Active buffers are inserted automatically by routing software to limit the loading effects due to distance and fanout.

The high-speed, very long-line resources, which span the entire device with minimal delay, are used to route very long or very high fanout nets. (Figure 1-6 on page 1-6).

The high-performance global networks are low-skew, high fanout nets that are accessible from external pins or from internal logic (Figure 1-7 on page 1-7). These nets are typically used to distribute clocks, resets, and other high fanout nets requiring a minimum skew. The global networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically with signals accessing every input on all tiles.

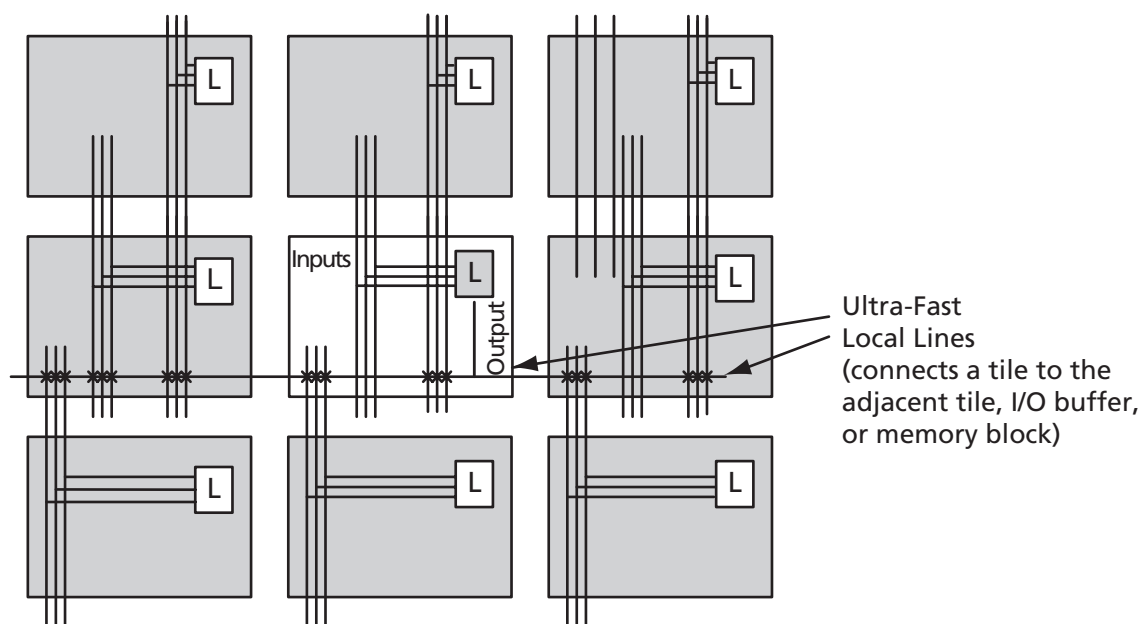


Figure 1-4 • Ultra-Fast Local Resources

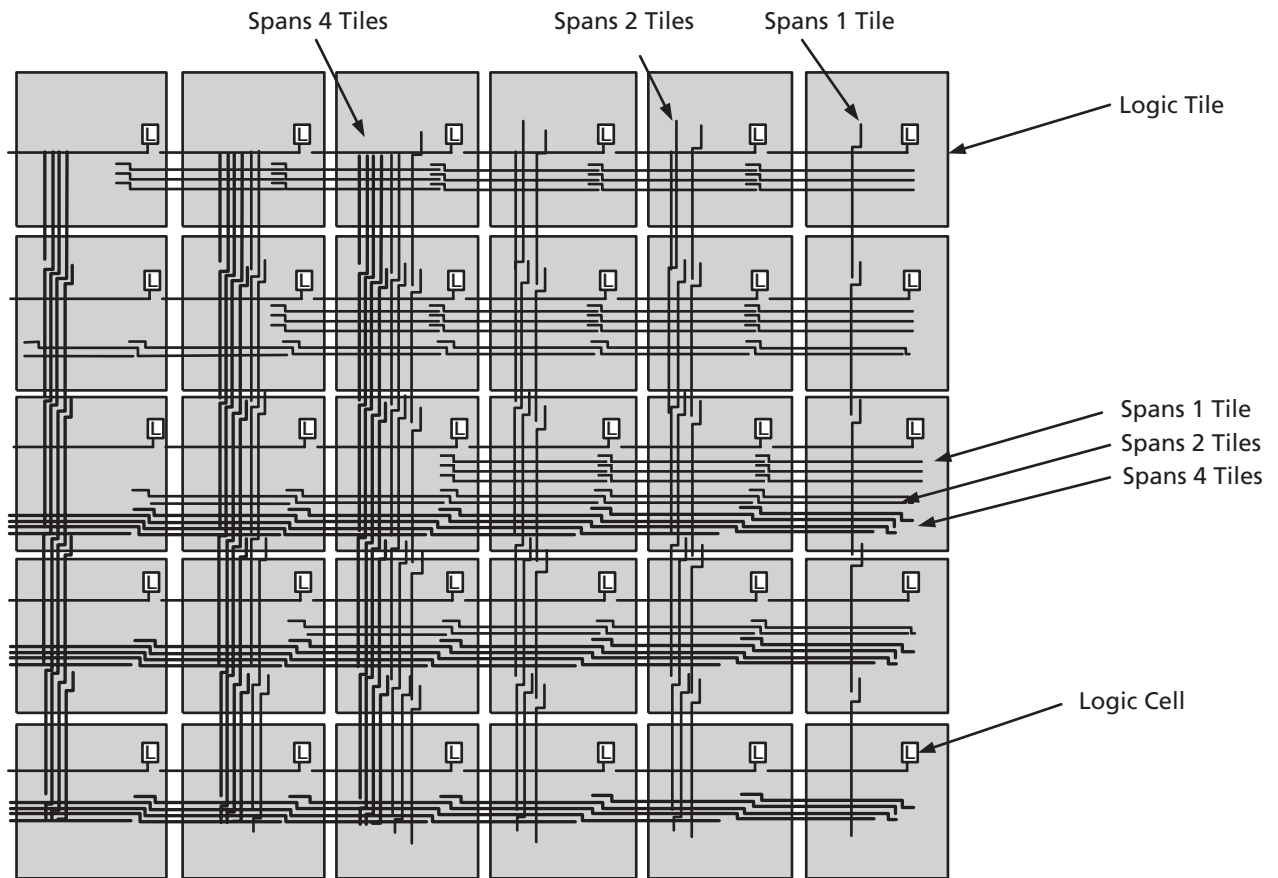


Figure 1-5 • Efficient Long-Line Resources

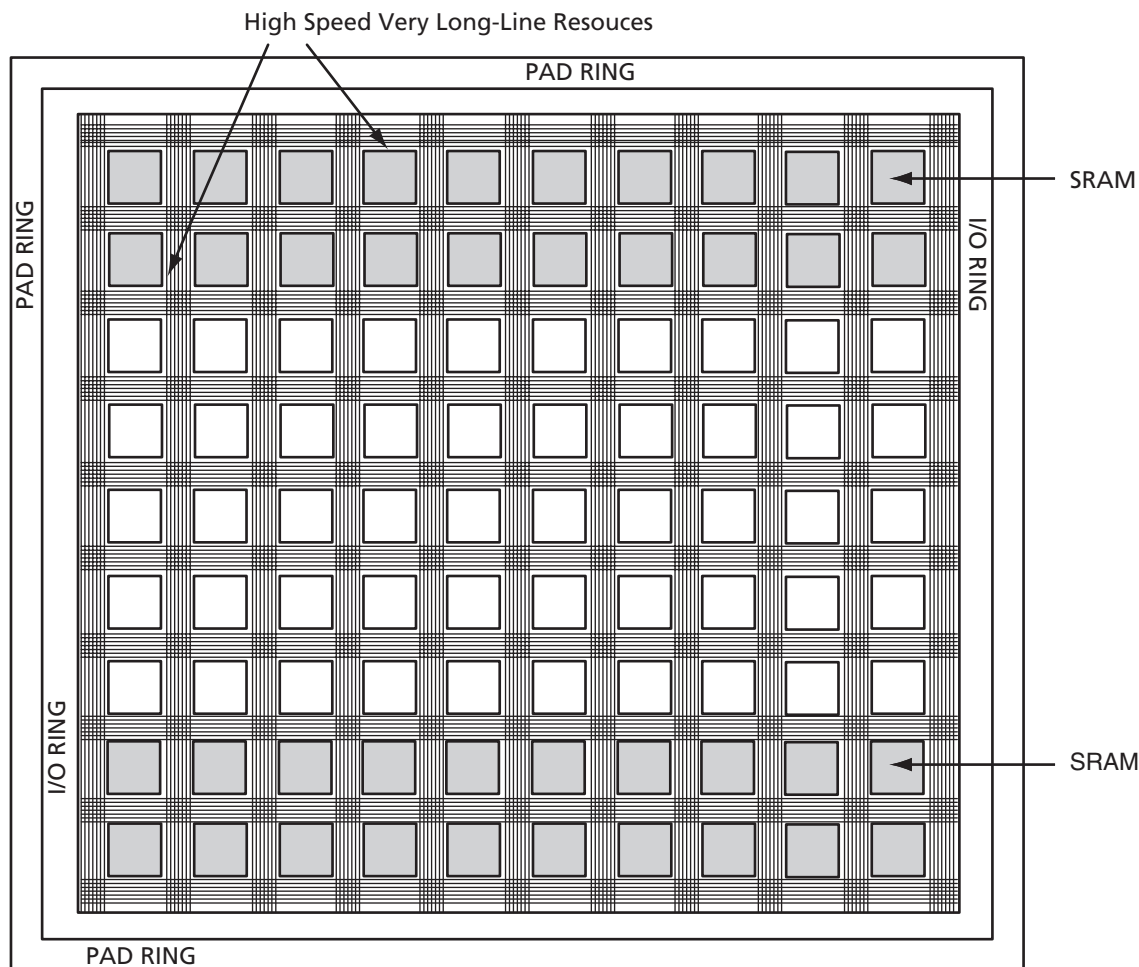


Figure 1-6 • High-Speed, Very Long-Line Resources

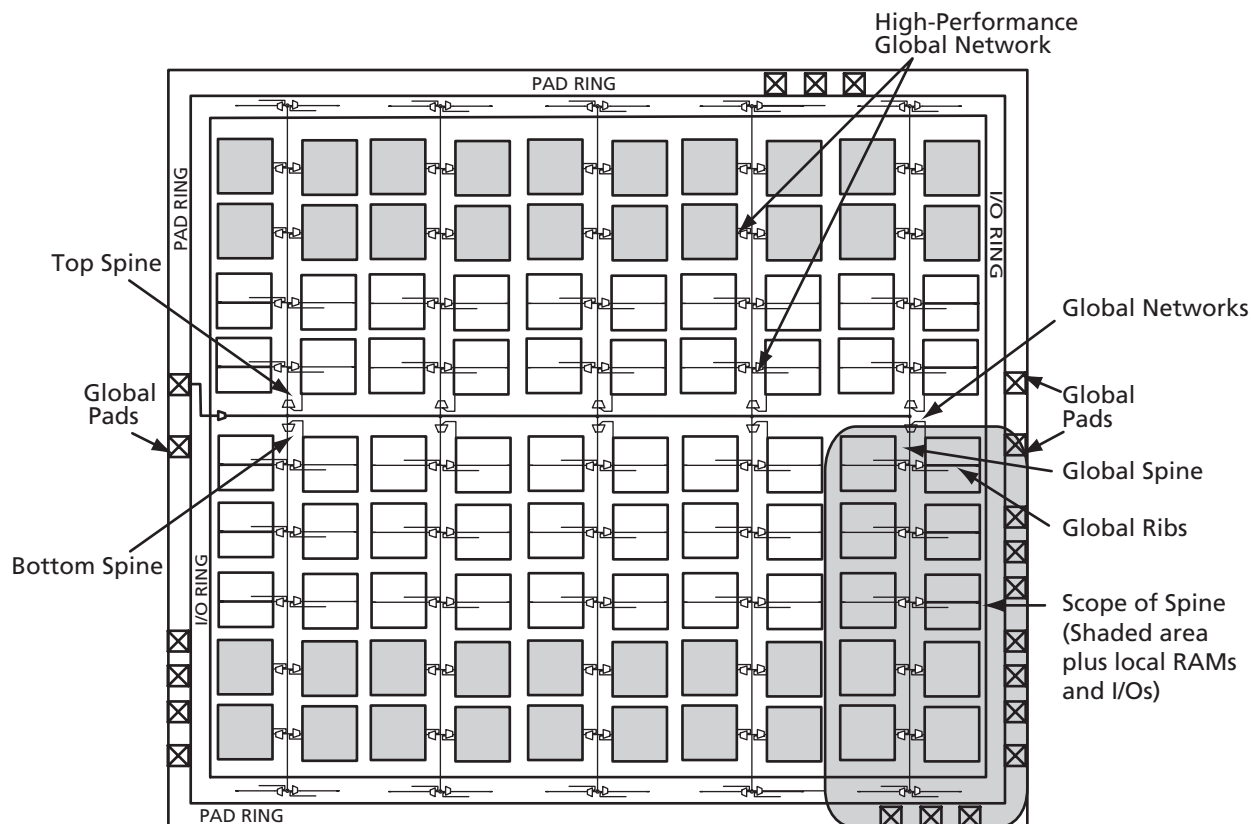
Clock Resources

The ProASIC^{PLUS} family offers powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has two clock conditioning blocks containing a phase-locked loop (PLL) core, delay lines, phase shifter (0° and 180°), clock multiplier/dividers, and all the circuitry needed for the selection and interconnection of inputs to the global network (thus providing bidirectional access to the PLL). This permits the PLL block to drive inputs and/or outputs via the two global lines on each side of the chip (four total lines). This circuitry is discussed in more detail in the "ProASIC^{PLUS} Clock Management System" section on page 1-13.

Clock Trees

One of the main architectural benefits of ProASIC^{PLUS} is the set of power- and delay-friendly global networks. ProASIC^{PLUS} offers four global trees. Each of these trees is based on a network of spines and ribs that reach all the tiles in their regions (Figure 1-7 on page 1-7). This flexible clock tree architecture allows users to map up to 88 different internal/external clocks in an APA1000 device. Details on the clock spines and various numbers of the family are given in Table 1-1 on page 1-7.

The flexible use of the ProASIC^{PLUS} clock spine allows the designer to cope with several design requirements. Users implementing clock-resource intensive applications can easily route external or gated internal clocks using global routing spines. Users can also drastically reduce delay penalties and save buffering resources by mapping critical high fanout nets to spines. For design hints on using these features, refer to Actel's *Efficient Use of ProASIC Clock Trees* application note.



Note: This figure shows routing for only one global path.

Figure 1-7 • High-Performance Global Network

Table 1-1 • Clock Spines

	APA075	APA150	APA300	APA450	APA600	APA750	APA1000
Global Clock Networks (Trees)	4	4	4	4	4	4	4
Clock Spines/Tree	6	8	8	12	14	16	22
Total Spines	24	32	32	48	56	64	88
Top or Bottom Spine Height (Tiles)	16	24	32	32	48	64	80
Tiles in Each Top or Bottom Spine	512	768	1,024	1,024	1,536	2,048	2,560
Total Tiles	3,072	6,144	8,192	12,288	21,504	32,768	56,320

Array Coordinates

During many place-and-route operations in Actel's Designer software tool, it is possible to set constraints that require array coordinates.

Table 1-2 is provided as a reference. The array coordinates are measured from the lower left (0,0). They can be used in region constraints for specific groups of core cells, I/Os, and RAM blocks. Wild cards are also allowed.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O

cells and core cells. In addition, the I/O coordinate system changes depending on the die/package combination.

Core cell coordinates start at the lower left corner (represented as (1,1)) or at (1,5) if memory blocks are present at the bottom. Memory coordinates use the same system and are indicated in Table 1-2. The memory coordinates for an APA1000 are illustrated in Figure 1-8. For more information on how to use constraints, see the *Designer User's Guide* or online help for ProASIC^{PLUS} software tools.

Table 1-2 • Array Coordinates

Device	Logic Tile				Memory Rows		All	
	Min.		Max.		Bottom	Top	Min.	Max.
	x	y	x	y	y	y		
APA075	1	1	96	32	–	(33,33) or (33, 35)	0,0	97, 37
APA150	1	1	128	48	–	(49,49) or (49, 51)	0,0	129, 53
APA300	1	5	128	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	129, 73
APA450	1	5	192	68	(1,1) or (1,3)	(69,69) or (69, 71)	0,0	193, 73
APA600	1	5	224	100	(1,1) or (1,3)	(101,101) or (101, 103)	0,0	225, 105
APA750	1	5	256	132	(1,1) or (1,3)	(133,133) or (133, 135)	0,0	257, 137
APA1000	1	5	352	164	(1,1) or (1,3)	(165,165) or (165, 167)	0,0	353, 169

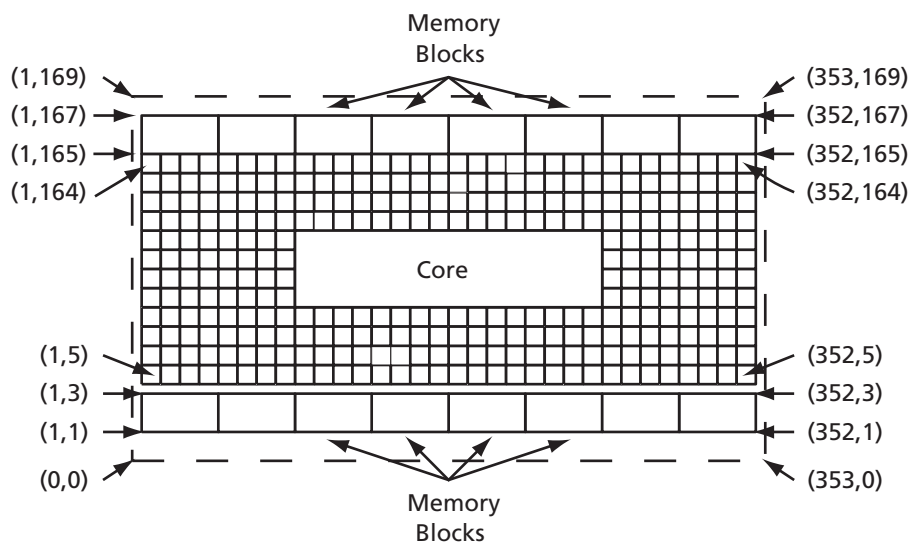


Figure 1-8 • Core Cell Coordinates for the APA1000

Input/Output Blocks

To meet complex system demands, the ProASIC^{PLUS} family offers devices with a large number of user I/O pins, up to 712 on the APA1000. Table 1-3 shows the available supply voltage configurations (the PLL block uses an independent 2.5 V supply on the AVDD and AGND pins). All I/Os include ESD protection circuits. Each I/O has been tested to 2000 V to the human body model (per JESD22 (HBM)).

Six or seven standard I/O pads are grouped with a GND pad and either a V_{DD} (core power) or V_{DDP} (I/O power) pad. Two reference bias signals circle the chip. One protects the cascaded output drivers, while the other creates a virtual V_{DD} supply for the I/O ring.

I/O pads are fully configurable to provide the maximum flexibility and speed. Each pad can be configured as an input, an output, a tristate driver, or a bidirectional buffer (Figure 1-9 and Table 1-4).

Table 1-3 • ProASIC^{PLUS} I/O Power Supply Voltages

	V _{DDP}	
	2.5 V	3.3 V
Input Compatibility	2.5 V	3.3 V
Output Drive	2.5 V	3.3 V

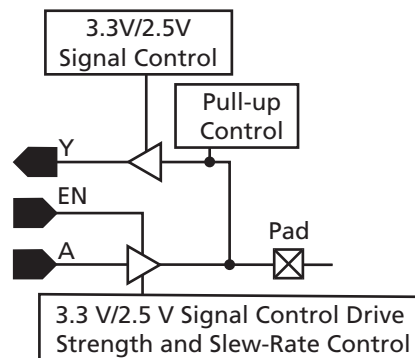


Figure 1-9 • I/O Block Schematic Representation

Table 1-4 • I/O Features

Function	Description
I/O pads configured as inputs	<ul style="list-style-type: none"> Selectable 2.5 V or 3.3 V threshold levels Optional pull-up resistor Optionally configurable as Schmitt trigger input. The Schmitt trigger input option can be configured as an input only, not a bidirectional buffer. This input type may be slower than a standard input under certain conditions and has a typical hysteresis of 0.35 V. I/O macros with an "S" in the standard I/O library have added Schmitt capabilities. 3.3 V PCI Compliant (except Schmitt trigger inputs)
I/O pads configured as outputs	<ul style="list-style-type: none"> Selectable 2.5 V or 3.3 V compliant output signals 2.5 V – JEDEC JESD 8-5 3.3 V – JEDEC JESD 8-A (LVTTTL and LVCMOS) 3.3 V PCI compliant Ability to drive LVTTTL and LVCMOS levels Selectable drive strengths Selectable slew rates Tristate
I/O pads configured as bidirectional buffers	<ul style="list-style-type: none"> Selectable 2.5 V or 3.3 V compliant output signals 2.5 V – JEDEC JESD 8-5 3.3 V – JEDEC JESD 8-A (LVTTTL and LVCMOS) 3.3 V PCI compliant Optional pull-up resistor Selectable drive strengths Selectable slew rates Tristate

Power-Up Sequencing

While ProASIC^{PLUS} devices are live at power-up, the order of V_{DD} and V_{DDP} power-up is important during system start-up. V_{DD} should be powered up simultaneously with V_{DDP} on ProASIC^{PLUS} devices. Failure to follow these guidelines may result in undesirable pin behavior during system start-up. For more information, refer to Actel's *Power-Up Behavior of ProASIC^{PLUS} Devices* application note.

LVPECL Input Pads

In addition to standard I/O pads and power pads, ProASIC^{PLUS} devices have a single LVPECL input pad on both the east and west sides of the device, along with AVDD and AGND pins to power the PLL block. The LVPECL pad cell consists of an input buffer (containing a

low voltage differential amplifier) and a signal and its complement, PPECL (I/P) (PECLN) and NPECL (PECLREF). The LVPECL input pad cell differs from the standard I/O cell in that it is operated from V_{DD} only.

Since it is exclusively an input, it requires no output signal, output enable signal, or output configuration bits. As a special high-speed differential input, it also does not require pull ups. Recommended termination for LVPECL inputs is shown in Figure 1-10. The LVPECL pad cell compares voltages on the PPECL (I/P) pad (as illustrated in Figure 1-11) and the NPECL pad and sends the results to the global MUX (Figure 1-14 on page 1-14). This high-speed, low-skew output essentially controls the clock conditioning circuit.

LVPECLs are designed to meet LVPECL JEDEC receiver standard levels (Table 1-5).

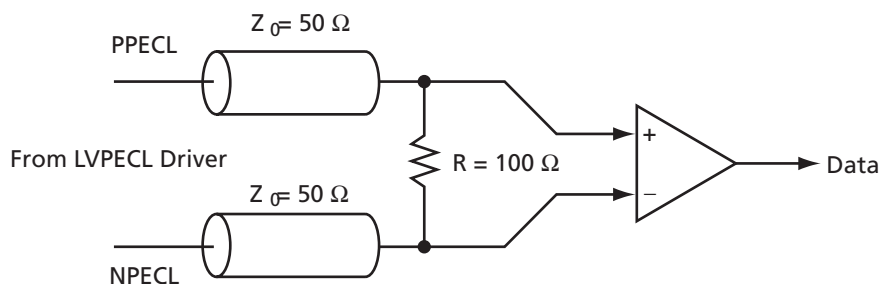


Figure 1-10 • Recommended Termination for LVPECL Inputs

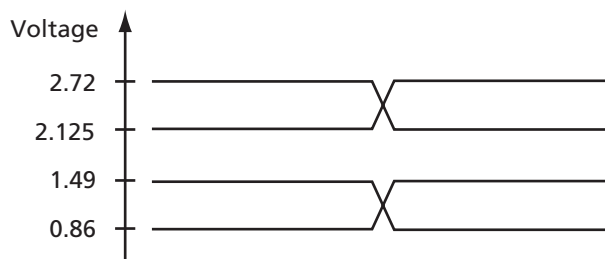


Figure 1-11 • LVPECL High and Low Threshold Values

Table 1-5 • LVPECL Receiver Specifications

Symbol	Parameter	Min.	Max	Units
V_{IH}	Input High Voltage	1.49	2.72	V
V_{IL}	Input Low Voltage	0.86	2.125	V
V_{ID}	Differential Input Voltage	0.3	V_{DD}	V

Boundary Scan (JTAG)

ProASIC^{PLUS} devices are compatible with IEEE Standard 1149.1, which defines a set of hardware architecture and mechanisms for cost-effective, board-level testing. The basic ProASIC^{PLUS} boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers, and instruction register (Figure 1-12). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and the optional IDCODE instruction (Table 1-6).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI and TDO (test data input and output), TMS (test mode selector) and TRST (test reset input). TMS, TDI and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These

pins are dedicated for boundary-scan test usage. Actel recommends that a nominal 20 kΩ pull-up resistor is added to TDO and TCK pins.

The TAP controller is a four-bit state machine (16 states) that operates as shown in Figure 1-13 on page 1-12. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

ProASIC^{PLUS} devices have to be programmed at least once for complete boundary-scan functionality to be available. Prior to being programmed, EXTEST is not available. If boundary-scan functionality is required prior to programming, refer to online [technical support](#) on the Actel website and search for ProASIC^{PLUS} BSDL.

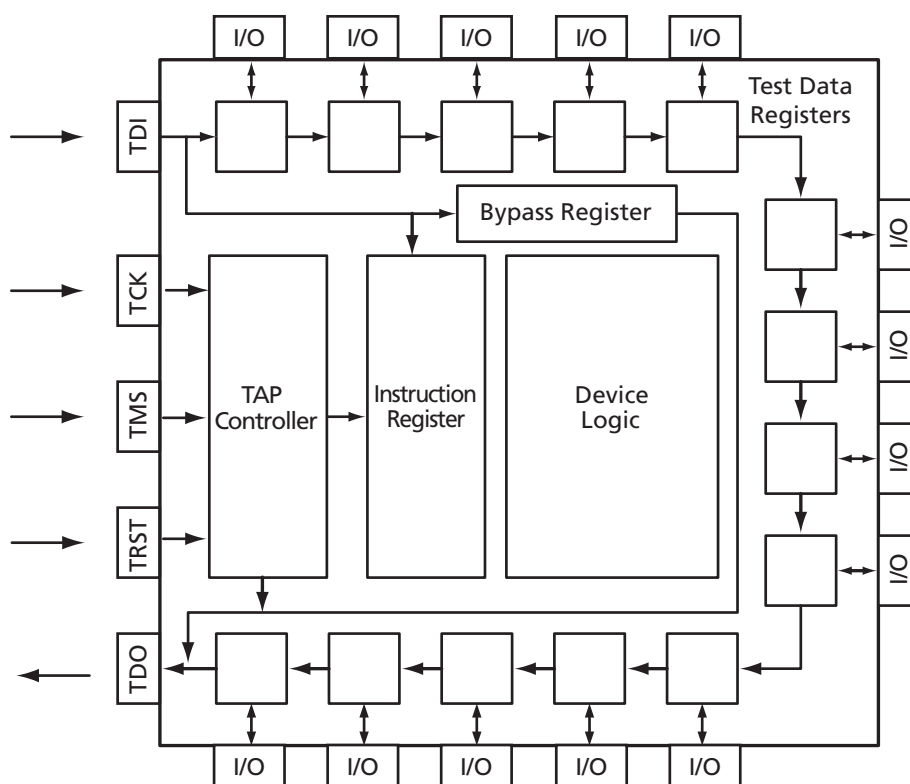


Figure 1-12 • ProASIC^{PLUS} JTAG Boundary Scan Test Logic Circuit

Table 1-6 • Boundary-Scan Opcodes

	Hex Opcode
EXTEST	00
SAMPLE/PRELOAD	01
IDCODE	0F

Table 1-6 • Boundary-Scan Opcodes

	Hex Opcode
CLAMP	05
BYPASS	FF

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles. The TRST pin may also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

ProASIC^{PLUS} devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register

with four fields (lowest significant byte (LSB), ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary-scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

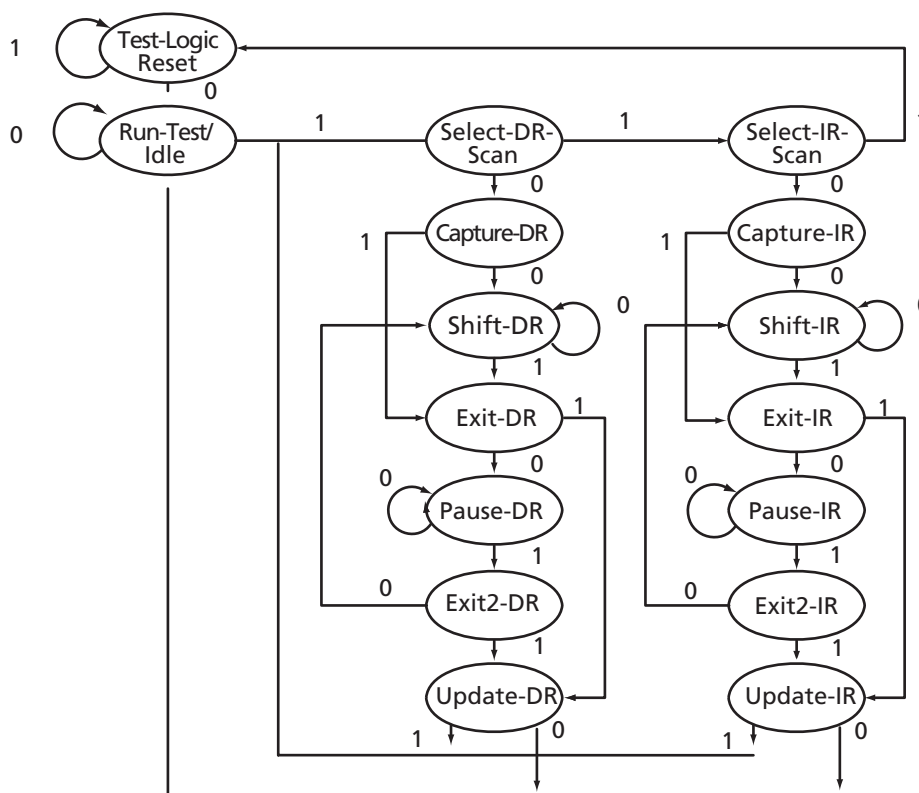


Figure 1-13 • TAP Controller State Diagram

Timing Control and Characteristics

ProASIC^{PLUS} Clock Management System

ProASIC^{PLUS} devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC^{PLUS} family contains two phase-locked loop (PLL) blocks which perform the following functions:

- Clock Phase Adjustment via Programmable Delay (250 ps steps from -7 ns to +8 ns)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range (f_{IN}) = 1.5 to 180 MHz
- Feedback Frequency Range (f_{VCO}) = 24 to 180 MHz
- Output Frequency Range (f_{OUT}) = 8 to 180 MHz
- Output Phase Shift = 0° and 180°
- Output Duty Cycle = 50%
- Low Output Jitter (max at 25°C)
 - $f_{VCO} < 10$ MHz. Jitter $\pm 1\%$ or better
 - $10 \text{ MHz} < f_{VCO} < 60$ MHz. Jitter $\pm 2\%$ or better
 - $f_{VCO} > 60$ MHz. Jitter $\pm 1\%$ or better

Note: Jitter(ps) = Jitter(%)* period

For Example:

Jitter in picoseconds at 100 MHz = $0.01 * (1/100E6) = 100$ ps

- Maximum Acquisition Time = 80 μ s for $f_{VCO} > 40$ MHz
= 30 μ s for $f_{VCO} < 40$ MHz
- Low Power Consumption – 6.9 mW (max – analog supply) + 7.0 μ W/MHz (max – digital supply)

Physical Implementation

Each side of the chip contains a clock conditioning circuit based on a 180 MHz PLL block (Figure 1-14 on page 1-14). Two global multiplexed lines extend along each side of the chip to provide bidirectional access to the PLL on that side (neither MUX can be connected to the opposite side's PLL). Each global line has optional LVPECL input pads (described below). The global lines may be driven by either the LVPECL global input pad or the outputs from the PLL block, or both. Each global line can be driven by a different output from the PLL. Unused global pins can be configured as regular I/Os or left unconnected. They default to an input with pull-up. The two signals available to drive the global networks are as

follows (Figure 1-15 on page 1-15, Table 1-7 on page 1-15, and Table 1-8 on page 1-16):

Global A (secondary clock)

- Output from Global MUX A
- Conditioned version of PLL output (f_{OUT}) – delayed or advanced
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)¹

Global B

- Output from Global MUX B
- Delayed or advanced version of f_{OUT}
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)²

Functional Description

Each PLL block contains four programmable dividers as shown in Figure 1-14 on page 1-14. These allow frequency scaling of the input clock signal as follows:

- The n divider divides the input clock by integer factors from 1 to 32.
- The m divider in the feedback path allows multiplication of the input clock by integer factors ranging from 1 to 64.
- The two dividers together can implement any combination of multiplication and division resulting in a clock frequency between 24 and 180 MHz exiting the PLL core. This clock has a fixed 50% duty cycle.
- The output frequency of the PLL core is given by the formula EQ 1-1 (f_{REF} is the reference clock frequency):

$$f_{OUT} = f_{REF} * m/n$$

EQ 1-1

- The third and fourth dividers (u and v) permit the signals applied to the global network to each be further divided by integer factors ranging from 1 to 4.

The implementations shown in EQ2 and EQ3 enable the user to define a wide range of frequency multiplier and divisors.

$$f_{GLB} = m/(n*u)$$

EQ 1-2

$$f_{GLA} = m/(n*v)$$

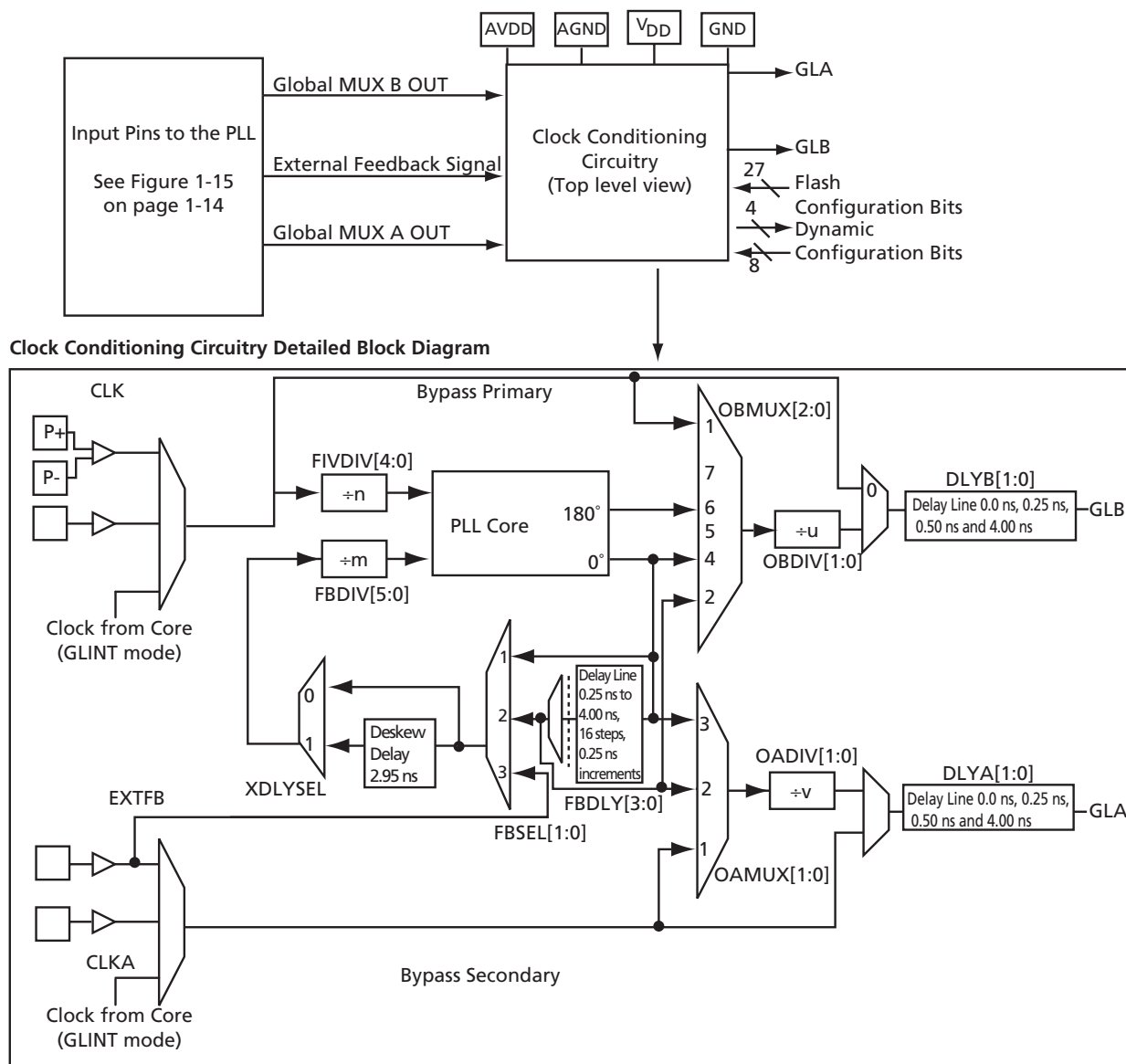
EQ 1-3

1. This mode is available through the delay feature of the Global MUX driver.

enable the user to define a wide range of frequency multipliers and divisors. The clock conditioning circuit can advance or delay the clock up to 8 ns (in increments of 0.25 ns) relative to the positive edge of the incoming reference clock. The system also allows for the selection of output frequency clock phases of 0° and 180°.

Prior to the application of signals to the rib drivers, they pass through programmable delay units, one per global network. These units permit the delaying of global

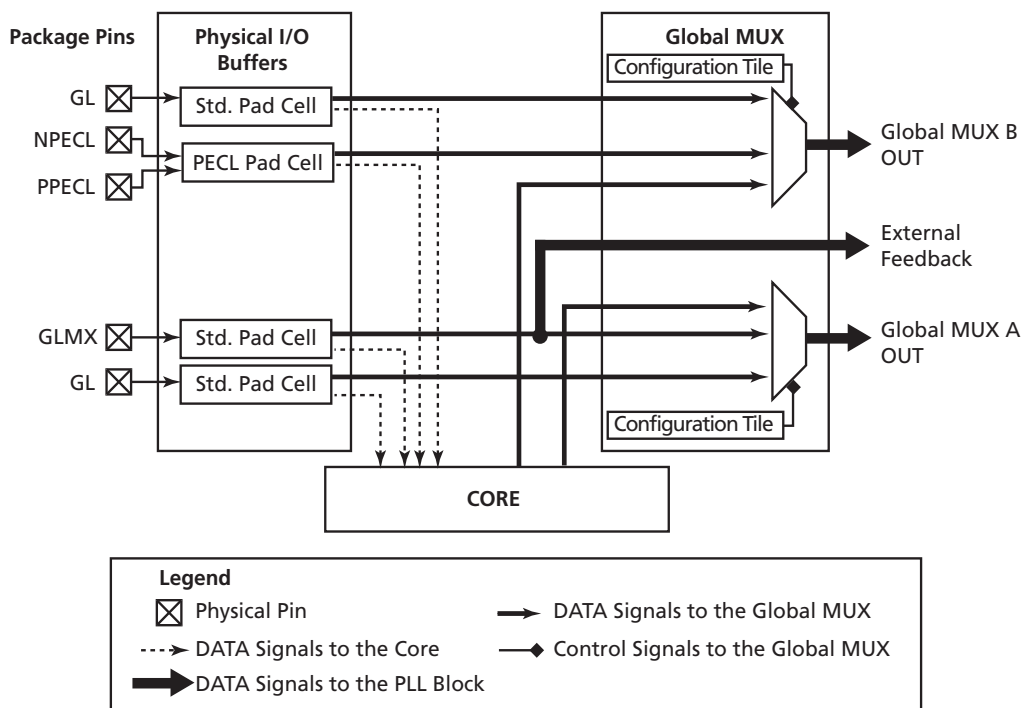
signals relative to other signals to assist in the control of input set-up times. Not all possible combinations of input and output modes can be used. The degrees of freedom available in the bidirectional global pad system and in the clock conditioning circuit have been restricted. This avoids unnecessary and unwieldy design kit and software work.



Notes:

1. FBDLY is a programmable delay line from 0 to 4 ns in 250 ps increments.
2. DLYA and DLYB are programmable delay lines, each with selectable values 0 ps, 250 ps, 500 ps, and 4 ns.
3. OBDIV will also divide the phase-shift since it takes place after the PLL Core.

Figure 1-14 • PLL Block – Top-Level View and Detailed PLL Block Diagram



Note: When a signal from an I/O tile is connected to the core, it cannot be connected to the Global MUX at the same time.

Figure 1-15 • Input Connectors to ProASIC^{PLUS} Clock Conditioning Circuitry

Table 1-7 • Clock-Conditioning Circuitry MUX Settings

MUX	Datapath	Comments
FBSEL		
1	Internal Feedback	
2	Internal Feedback and Advance Clock Using FBDLY	-0.25 to -4 ns in 0.25 ns increments
3	External Feedback (EXTFB)	
XDLYSEL		
0	Feedback Unchanged	
1	Deskew feedback by advancing clock by system delay	Fixed delay of -2.95 ns
OBMUX		
GLB		
0	Primary bypass, no divider	
1	Primary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25 ns increments
4	Phase Shift Clock by 0°	
5	Reserved	
6	Phase Shift Clock by +180°	
7	Reserved	
OAMUX		
GLA		
0	Secondary bypass, no divider	
1	Secondary bypass, use divider	
2	Delay Clock Using FBDLY	+0.25 to +4 ns in 0.25 ns increments
3	Phase Shift Clock by 0°	

Table 1-8 • Clock-Conditioning Circuitry Delay-Line Settings

Delay Line	Delay Value (ns)
DLYB	
0	0
1	+0.25
2	+0.50
3	+4.0
DLYA	
0	0
1	+0.25
2	+0.50
3	+4.0

Lock Signal

An active-high Lock signal (added via the SmartGen PLL development tool) indicates that the PLL has locked to the incoming clock signal. The PLL will acquire and maintain lock even when there is jitter on the incoming clock signal. The PLL will maintain lock with an input jitter up to 5% of the input period, with a maximum of 5 ns. Users can employ the Lock signal as a soft reset of the logic driven by GLB and/or GLA. Note if F_{IN} is not within specified frequencies, then both the F_{OUT} and lock signal are indeterminate.

PLL Configuration Options

The PLL can be configured during design (via Flash-configuration bits set in the programming bitstream) or dynamically during device operation, thus eliminating the need to reprogram the device. The dynamic configuration bits are loaded into a serial-in/parallel-out shift register provided in the clock conditioning circuit. The shift register can be accessed either from user logic within the device or via the JTAG port. Another option is internal dynamic configuration via user-designed hardware. Refer to Actel's [ProASIC^{PLUS} PLL Dynamic Reconfiguration Using JTAG](#) application note for more information.

For information on the clock conditioning circuit, refer to Actel's [Using ProASIC^{PLUS} Clock Conditioning Circuits](#) application note.

Sample Implementations

Frequency Synthesis

Figure 1-16 on page 1-17 illustrates an example where the PLL is used to multiply a 33 MHz external clock up to 133 MHz. Figure 1-17 on page 1-17 uses two dividers to synthesize a 50 MHz output clock from a 40 MHz input reference clock. The input frequency of 40 MHz is multiplied by five and divided by four, giving an output clock (GLB) frequency of 50 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL. For example, in this case the input divider could have been two and the output divider also two, giving us a division of the input frequency by four to go with the feedback loop division (effective multiplication) by five.

Adjustable Clock Delay

Figure 1-18 on page 1-18 illustrates the delay of the input clock by employing one of the adjustable delay lines. This is easily done in ProASIC^{PLUS} by bypassing the PLL core entirely and using the output delay line. Notice also that the output clock can be effectively advanced relative to the input clock by using the delay line in the feedback path. This is shown in Figure 1-19 on page 1-18.

Clock Skew Minimization

Figure 1-20 on page 1-19 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (GLA) feeds a clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to Actel's [Using ProASIC^{PLUS} Clock Conditioning Circuits](#) application note for more information.

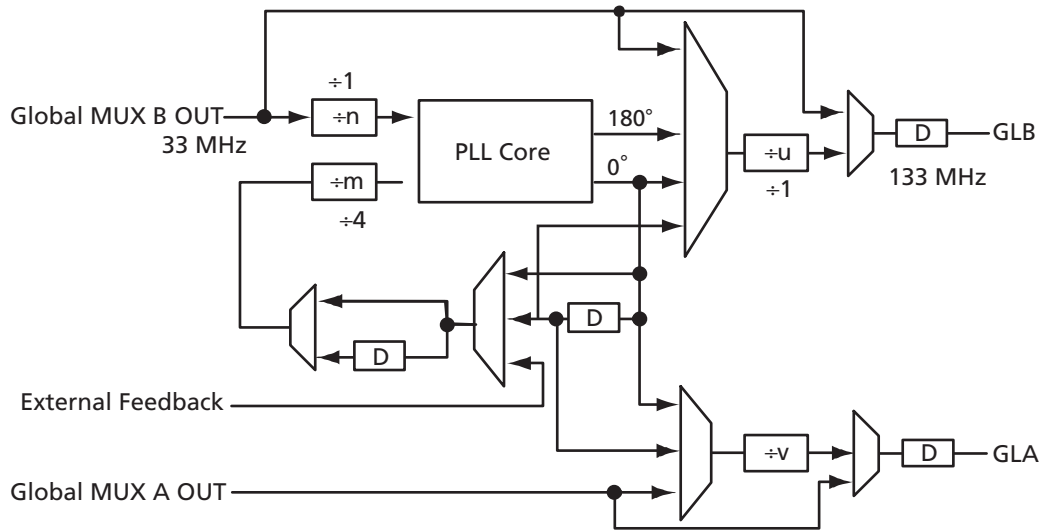


Figure 1-16 • Using the PLL 33 MHz In, 133 MHz Out

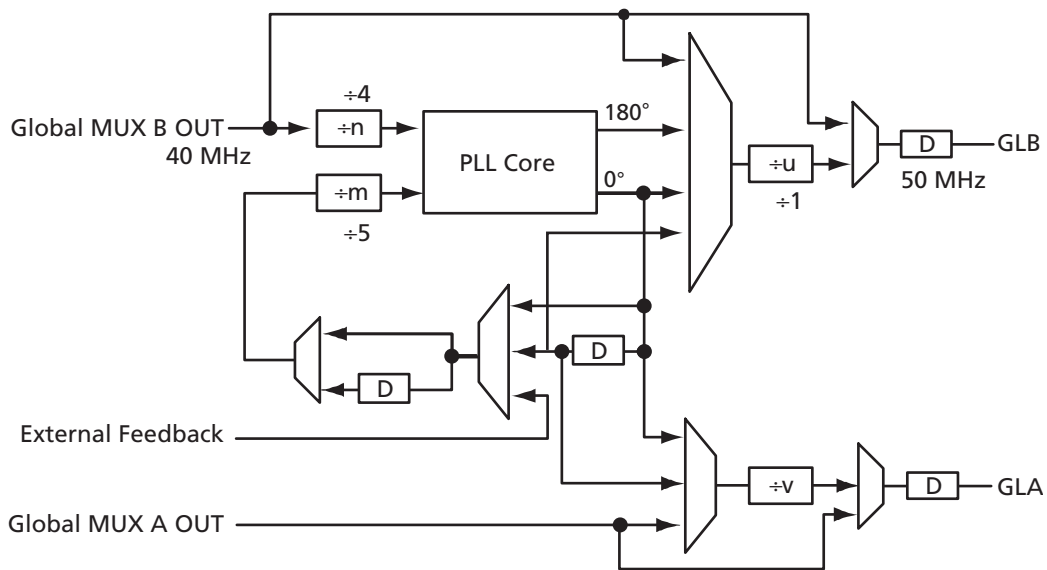


Figure 1-17 • Using the PLL 40 MHz In, 50 MHz Out

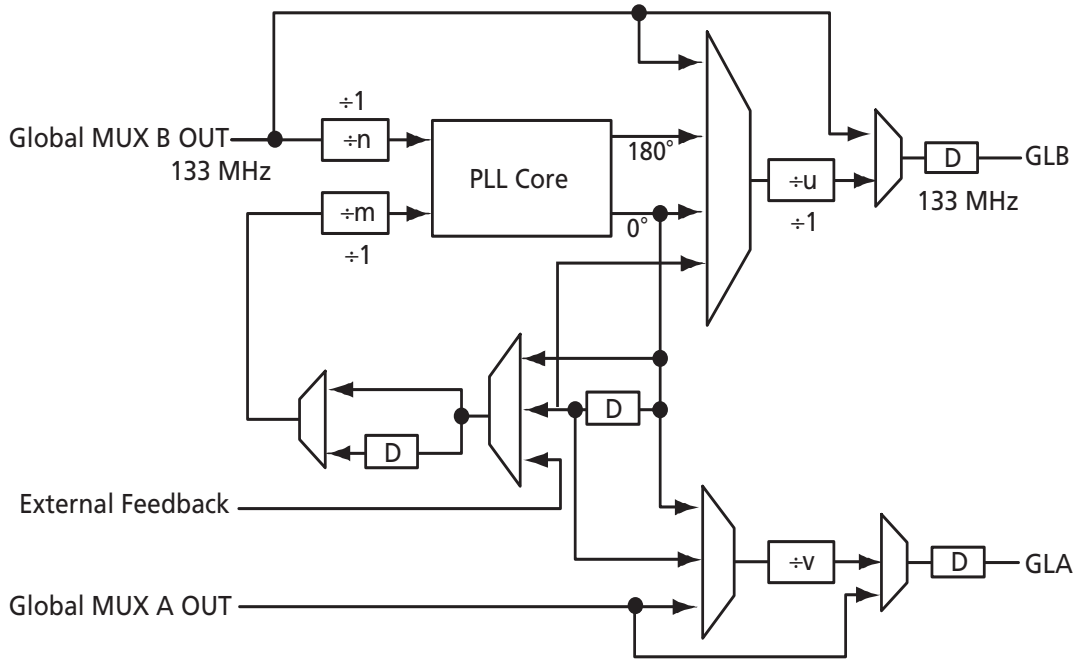


Figure 1-18 • Using the PLL to Delay the Input Clock

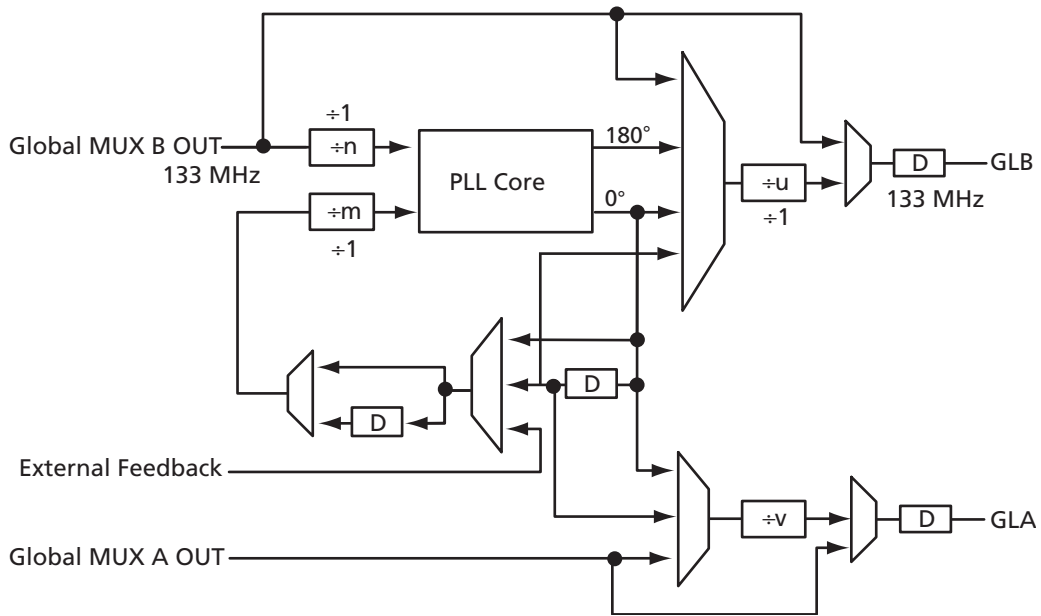


Figure 1-19 • Using the PLL to Advance the Input Clock

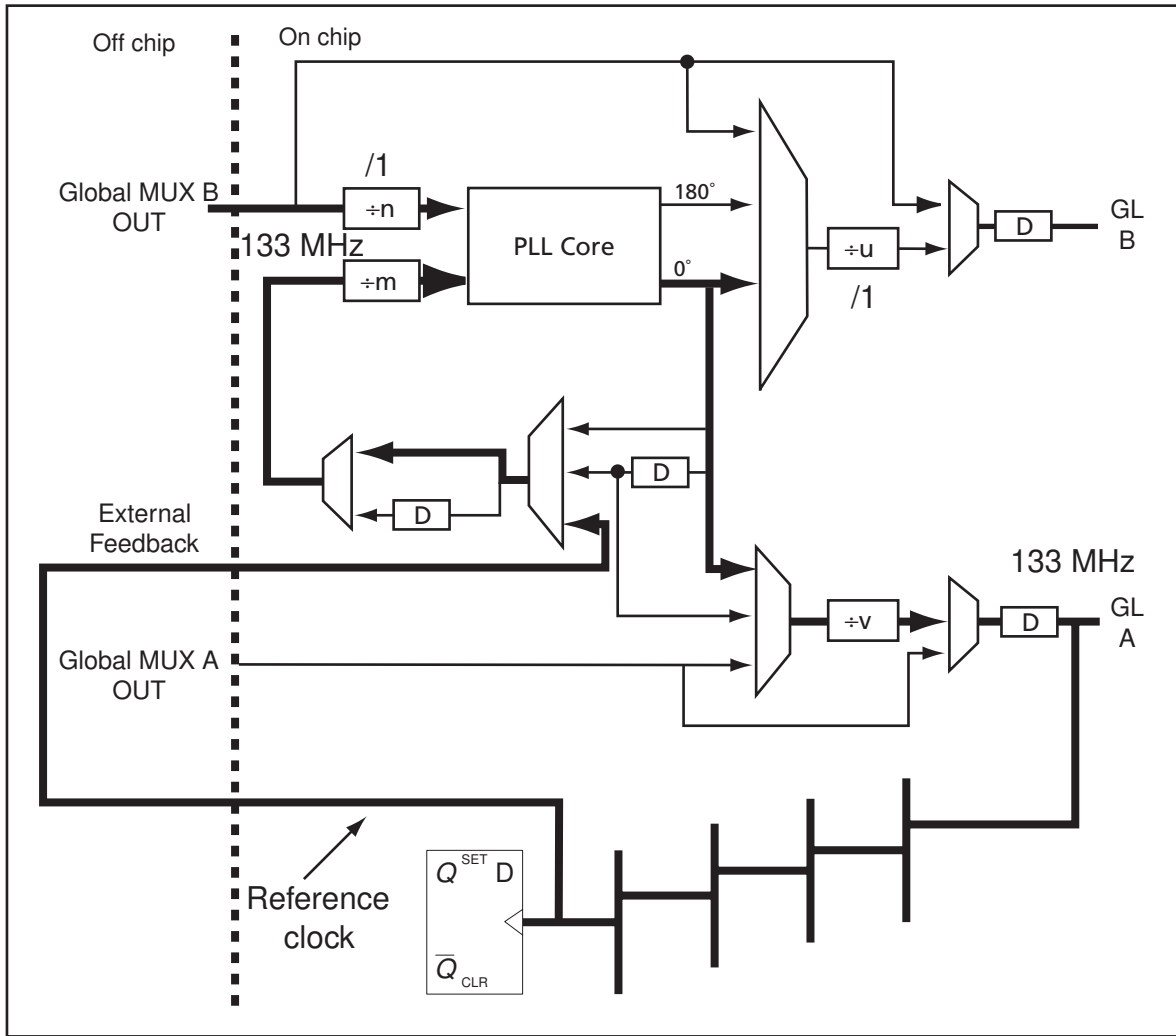


Figure 1-20 • Using the PLL for Clock Deskewing