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56F8014

Data Sheet

Technical Data

56F8000
16-bit Digital Signal Controllers

MC56F8014
Rev. 11
05/2008

freescale.com

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Document Revision History

Version History	Description of Change
Rev 0	Initial release
Rev 1	Updates to **Part 10, Specifications,** **Table 10-1**, added maximum clamp current, per pin **Table 10-11**, clarified variation over temperature table and graph **Table 10-15**, added LIN slave timing
Rev 2	Added alternate pins to **Figure 11-1** and **Table 11-1**.
Rev 3	Corrected bit selects in Timer Channel 3 Input (TC3_INP) bit 9, **Section 6.3.1.7**, clarified **Section 1.4.1**, and simplified notes in **Table 10-9**,
Rev 4	Added clarification on sync inputs in **Section 1.4.1**, added voltage difference specification to **Table 10-1** and **Table 10-4**, deleted formula for Ambient Operating Temperature in **Table 10-4**, and a note for pin group 3, corrected **Table 8-1**, error in Port C peripheral function configuration, updated notes in **Table 10-9**. Added RoHs and “pb-free” language to back cover.
Rev 5	Updates to **Section 10** **Table 10-5**, corrected max values for ADC Input Current High and Low; corrected typ value for pull-up disabled Digital Input Current Low (a) **Table 10-6**, corrected typ and added max values for Standby > Stop and Powerdown modes **Table 10-7**, corrected min value for Low-Voltage Interrupt for 3.3V **Table 10-11**, corrected typ and max values and units for PLL lock time **Table 10-12**, corrected typ values for Relaxation Oscillator output frequency and variation over temperature (also increased temp range to 150 degreesC) and added variation over temperature from 0—105 degreesC Updated **Figure 10-5** **Table 10-19**, updated max values for Integral Non-Linearity full input signal range, Negative Differential Non-Linearity, ADC internal clock, Offset Voltage Internal Ref, Gain Error and Offset Voltage External Ref; updated typ values for Negative Differential Non-Linearity, Offset Voltage Internal Ref, Gain Error and Offset Voltage External Ref; added new min values and corrected typ values for Signal-to-noise ratio, Total Harmonic Distortion, Spurious Free Dynamic Range, Signal-to-noise plus distortion, Effective Number of Bits
Rev 6	Added details to Section 1. Clarified language in State During Reset column in **Table 2-3**; corrected flash data retention temperature in **Table 10-4**; moved input current high/low to**Table 10-19** and location of footnotes in **Table 10-5**; reorganized **Table 10-19**; clarified title of **Figure 10-1**.
Rev. 7	• In **Table 10-4**, added an entry for flash data retention with less than 100 program/erase cycles (minimum 20 years). • In **Table 10-6**, changed the device clock speed in STOP mode from 8MHz to 4MHz. • In **Table 10-12**, changed the typical relaxation oscillator output frequency in Standby mode from 400kHz to 200kHz.
Rev. 8	In **Table 10-19**, changed the maximum ADC internal clock frequency from 8MHz to 5.33MHz.

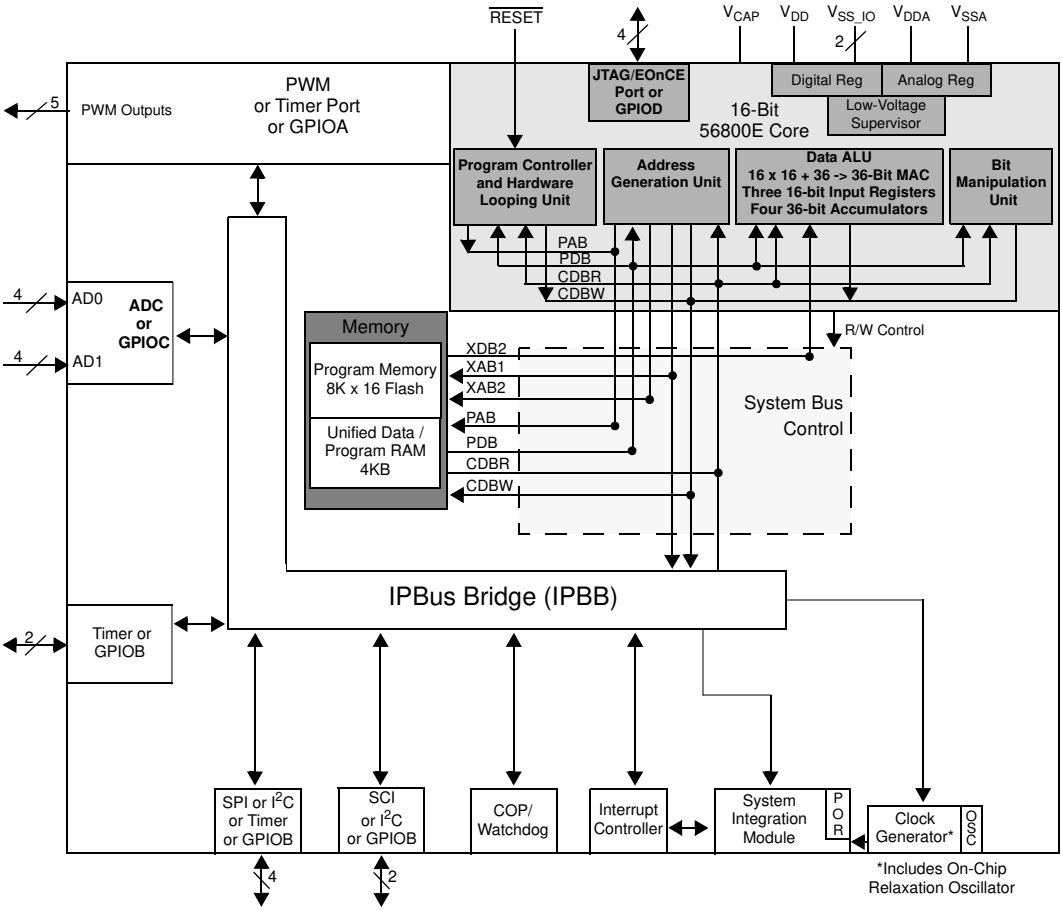
Document Revision History (Continued)

Version History	Description of Change
Rev. 9	Added the following note to the description of the TMS signal in **Table 2-3**: **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
Rev. 10	• In **Table 2-3**, changed V_{CAP} value from 4.7 µF to 2.2 µF. • In **Table 2-3**, changed the input type for FAULT3 (was “Output”, is “Input”). • In **Table 2-3**, changed the input type for FAULT2 (was “Input/Output”, is “Input”). • Revised **Section 7, Security Features**. • Added MC56F8014MFAE to **Section 13, Ordering Information**. • Fixed miscellaneous errors.
Rev.11	• Updated temperature information in **Table 10-1** and **Table 10-4**.

Please see http://www.freescale.com for the most current data sheet revision.

56F8014 General Description

- Up to 32 MIPS at 32MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- 16KB Program Flash
- 4KB Unified Data/Program RAM
- One 5-channel PWM module
- Two 4-channel 12-bit ADCs
- One Serial Communication Interface (SCI) with LIN slave functionality
- One Serial Peripheral Interface (SPI)
- One 16-bit Quad Timer
- One Inter-Integrated Circuit (I^2C) Port
- Computer Operating Properly (COP)/Watchdog
- On-Chip Relaxation Oscillator
- Integrated Power-On Reset and Low-Voltage Interrupt Module
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Up to 26 GPIO lines
- 32-pin LQFP Package



56F8014 Block Diagram

56F8014 Data Sheet Table of Contents

Part 1 Overview

1.1 56F8014 Features

1.1.1 Digital Signal Controller Core

- Efficient 16-bit 56800E family Digital Signal Controller (DSC) engine with dual Harvard architecture
- As many as 32 Million Instructions Per Second (MIPS) at 32MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent, real-time debugging

1.1.2 Memory

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security and protection that prevent unauthorized users from gaining access to the internal Flash
- On-chip memory
  - 16KB of Program Flash
  - 4KB of Unified Data/Program RAM
- EEPROM emulation capability using Flash

1.1.3 Peripheral Circuits for 56F8014

- One multi-function five-output Pulse Width Modulator (PWM) module
  - Up to 96MHz PWM operating clock
  - 15 bits of resolution
  - Center-aligned and Edge-aligned PWM signal mode
  - Three programmable fault inputs with programmable digital filter
  - Double-buffered PWM registers

  - Each complementary PWM signal pair can output a different switching frequency by selecting PWM generation sources from:
    - PWM generator
    - External GPIO
    - Internal timers
    - ADC conversion result of over/under limits:
      When conversion result is greater than high limit, deactivate PWM signal
      When conversion result is less than low limit, activate PWM signal
- Two independent 12-bit Analog-to-Digital Converters (ADCs)
  - 2 x 4 channel inputs
  - Supports both simultaneous and sequential conversions
  - ADC conversions can be synchronized by both PWM and timer modules
  - Sampling rate up to 2.67MSPS
  - 8-word result buffer registers
  - ADC Smart Power Management (Auto-standby, auto-powerdown)
- One 16-bit multi-purpose Quad Timer module (TMR)
  - Up to 96MHz operating clock
  - Four independent 16-bit counter/timers with cascading capability
  - Each timer has capture and compare capability
  - Up to 12 operating modes
- One Serial Communication Interface (SCI) with LIN slave functionality
  - Full-duplex or single-wire operation
  - Two receiver wake-up methods:
    - Idle line
    - Address mark
- One Serial Peripheral Interface (SPI)
  - Full-duplex operation
  - Master and slave modes
  - Programmable length transactions (two to sixteen bits)
- One Inter-Integrated Circuit (I^2C) port
  - Operates up to 400 kbps
  - Supports both master and slave operation
- Computer Operating Properly (COP)/Watchdog timer capable of selecting different clock sources
- Up to 26 General-Purpose I/O (GPIO) pins with 5V tolerance
- Integrated Power-On Reset and Low-Voltage Interrupt Module
- Phase Lock Loop (PLL) provides a high-speed clock to the core and peripherals
- Clock Sources:
  - On-chip relaxation oscillator

— External clock source
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- JTAG/EOnCE debug programming interface for real-time debugging

1.1.4 Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- ADC smart power management
- Each peripheral can be individually disabled to save power

1.2 56F8014 Description

The 56F8014 is a member of the 56800E core-based family of Digital Signal Controllers (DSCs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F8014 is well-suited for many applications. The 56F8014 includes many peripherals that are especially useful for industrial control, motion control, home appliances, general purpose inverters, smart sensors, fire and security systems, switched-mode power supplies, power management, and medical monitoring applications.

The 56800E core is based on a dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The 56F8014 supports program execution from internal memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. The 56F8014 also offers up to 26 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56F8014 Digital Signal Controller includes 16KB of Program Flash and 4KB of Unified Data/Program RAM. Program Flash memory can be independently bulk erased or erased in pages. Program Flash page erase size is 512 Bytes/256 Words.

A full set of programmable peripherals—PWM, ADCs, SCI, SPI, I^2C, Quad Timer—support various applications. Each peripheral can be independently shut down to save power. Any pin in these peripherals can also be used as a General Purpose Input/Outputs (GPIO).

1.3 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs

create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Architecture Block Diagram

The 56F8014's architecture is shown in **Figure 1-1**, **Figure 1-2**, and **Figure 1-3**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories and the IPBus Bridge, as well as showing the internal connections between each unit of the 56800E core. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. **Figure 1-3** details how the device's I/O pins are muxed. The figures do not show the on-board regulator and power and ground signals. They also do not show the multiplexing between peripherals or the dedicated GPIOs. Please see **Part 2 Signal/Connection Descriptions** to see which signals are multiplexed with those of other peripherals.

1.5 Synchronize ADC with PWM

ADC conversion can be synchronized with the PWM module via Quad Timer channel 2 and 3 if needed. Internally, the PWM synch signal — which is generated at every PWM reload —can be connected to the timer channel 3 input, and the timer channel 2 and channel 3 outputs are connected to the ADC sync inputs. Timer channel 3 output is connected to SYNC0 and timer channel 2 is connected to SYNC1. The setting is controlled by the TC3_INP bit in the SIM Control Register; see **Section 6.3.1**.

SYNC0 is the master ADC sync input, used to trigger both ADCA and ADCB in sequence and parallel mode. SYNC1 is used to trigger ADCB in parallel independent mode, while SYNC0 is used to trigger ADCA. See *MC56F8000RM*, the 56F801X Peripheral Reference Manual, for additional information.

1.6 Multiple Frequency PWM Output

When both PWM channels of a complementary pair in software control mode and software control bits are set to 1, each complementary PWM signal pair — PWM 0 and 1; PWM 2 and 3; and PWM 4 and 5 — can select a PWM source from one of the following sources. This will enable each PWM pair and PWM2 to output PWM signals at different frequencies.

- External GPIO input:
  - GPIOB2 input can be used to drive PWM 0 and 1
  - GPIOB3 input can be used to drive PWM 2
  - GPIOB4 input can be used to drive PWM 4 and 5
- Quad Timer output:
  - Timer0 output can be used to drive PWM 0 and 1
  - Timer2 output can be used to drive PWM 2
  - Timer3 output can be used to drive PWM 4 and 5
- ADC conversion result:
  - Signal of over/under limit of ADC sample 0 can be used to drive PWM 0 and 1
  - Signal of over/under limit of ADC sample 1 can be used to drive PWM 2

— Signal of over/under limit of ADC sample 2 can be used to drive PWM 4 and 5

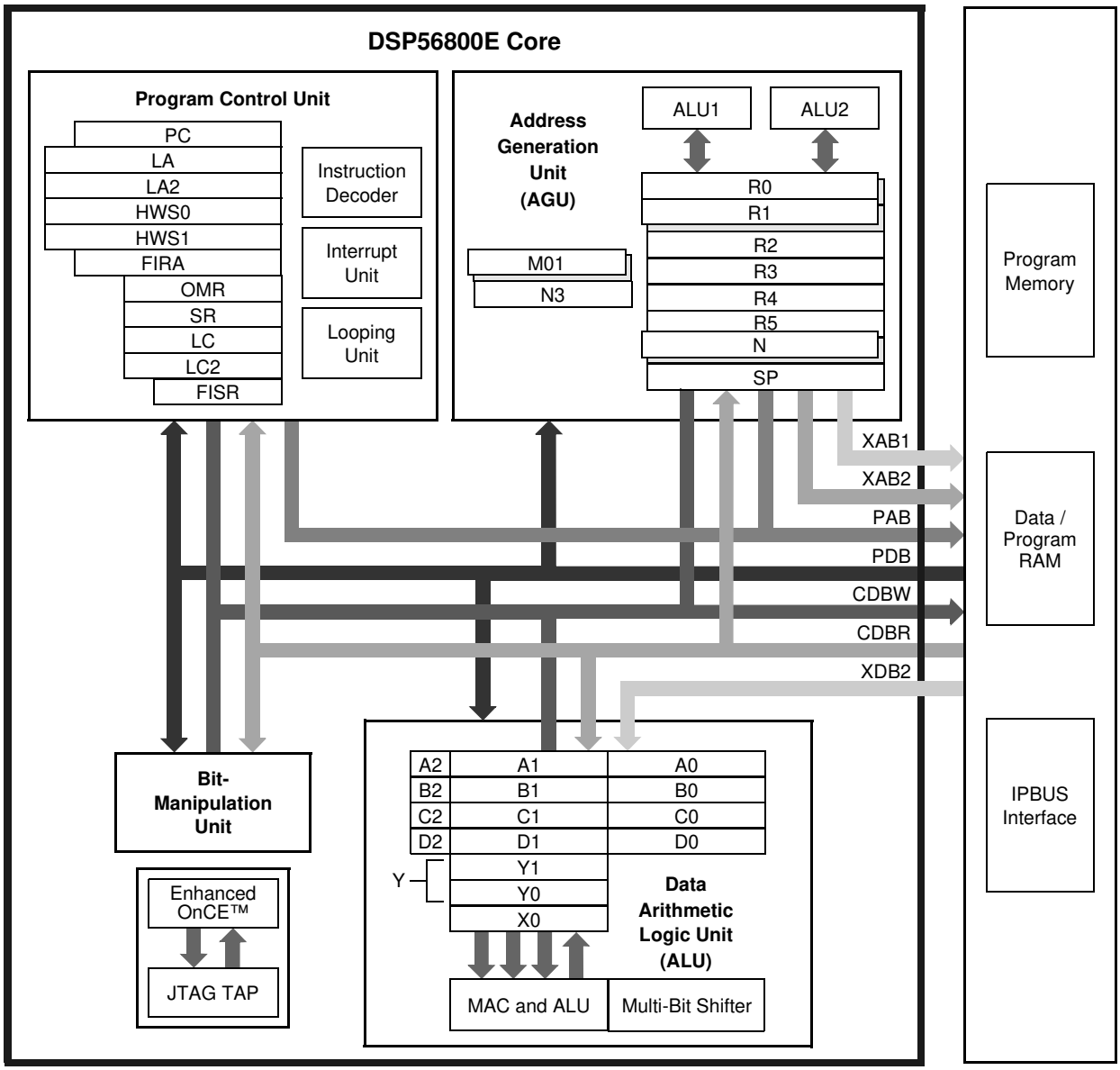


Figure 1-1 56800E Core Block Diagram

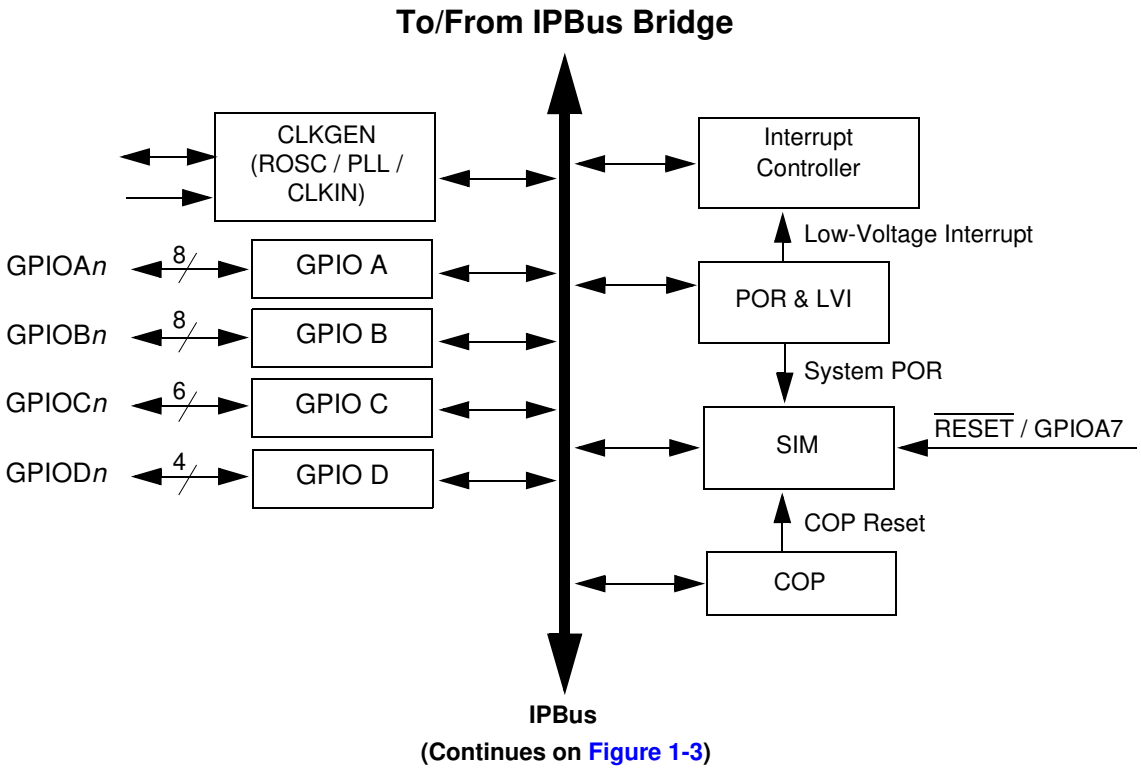


Figure 1-2 Peripheral Subsystem

(Continued from Figure 1-2)

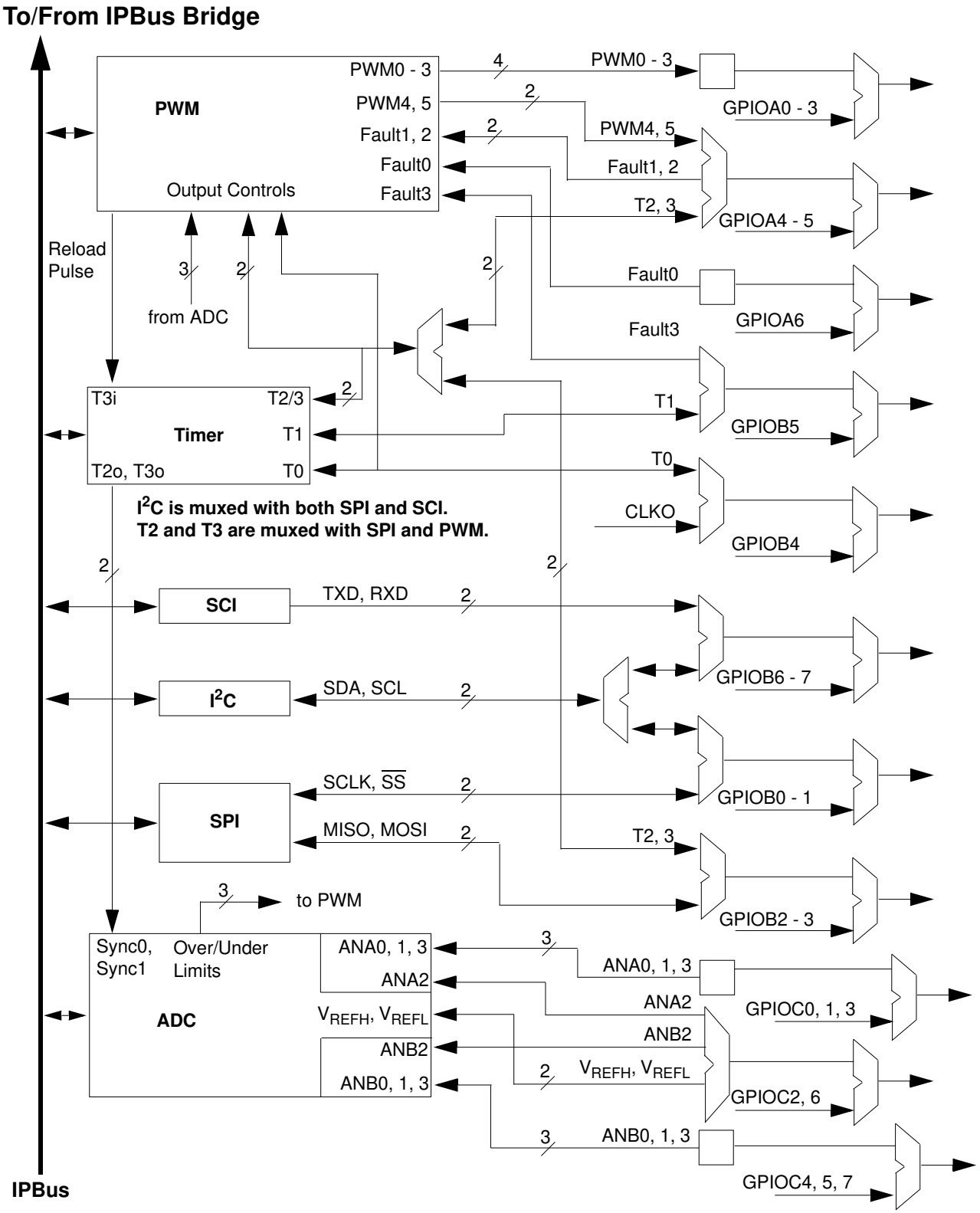


Figure 1-3 56F8014 Peripheral I/O Pin-Out

1.7 Product Documentation

The documents listed in **Table 1-1** are required for a complete description and proper design with the 56F8014. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at:
http://www.freescale.com

Table 1-1 56F8014 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit Digital Signal Controller core processor, and the instruction set	DSP56800ERM
56F801X Peripheral Reference Manual	Detailed description of peripherals of the 56F801X family of devices	MC56F8000RM
56F801x Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F801x family of devices	56F801xBLUG
56F8014 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8014
56F8014 Errata	Details any chip issues that might be present	MC56F8014E

1.8 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
“asserted”	A high true (active high) signal is high or a low true (active low) signal is low.
“deasserted”	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56F8014 are organized into functional groups, as detailed in **Table 2-1**. **Table 2-2** summarizes all device pins. In **Table 2-2**, each table row describes the signal or signals present on a pin, sorted by pin number.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins
Power (V_{DD} or V_{DDA})	2
Ground (V_{SS} or V_{SSA})	3
Supply Capacitors	1
Reset	1
Pulse Width Modulator (PWM) Ports[1]	5
Serial Peripheral Interface (SPI) Ports[2]	4
Analog-to-Digital Converter (ADC) Ports	8
Timer Module Ports[3]	2
Serial Communications Interface (SCI) Ports[4]	2
JTAG/Enhanced On-Chip Emulation (EOnCE)	4

1. Pins in this section can function as TMR and GPIO.
2. Pins in this section can function as TMR, I^2C, and GPIO.
3. Pins can function as PWM and GPIO.
4. Pins in this section can function as I^2C and GPIO.

Table 2-2 56F8014 Pins

			Peripherals:									
LQFP Pin #	**Pin Name**	**Signal Name**	**GPIO**	**I2C**	**SCI**	**SPI**	**ADC**	**PWM**	**Quad Timer**	**Power & Ground**	**JTAG**	**Misc.**
1	**GPIOB1**	GPIOB1, $\overline{SS}$, SDA	**B1**	SDA		$\overline{SS}$						
2	**GPIOB7**	GPIOB7, TXD, SCL	**B7**	SCL	TXD							
3	**GPIOB5**	GPIOB5, T1, FAULT3	**B5**					FAULT3	T1			
4	**ANB0**	ANB0, GPIOC4	C4				**ANB0**					
5	**ANB1**	ANB1, GPIOC5	C5				**ANB1**					
6	**ANB2**	ANB2, V_{REFL}, GPIOC6	C6				**ANB2,** V_{REFL}					
7	**ANB3**	ANB3, GPIOC7	C7				**ANB3**					
8	**VDDA**	V_{DDA}								**V_{DDA}**		
9	**VSSA**	V_{SSA}								**V_{SSA}**		
10	**ANA3**	ANA3, GPIOC3	C3				**ANA3**					
11	**ANA2**	ANA2, V_{REFH}, GPIOC2	C2				**ANA2,** V_{REFH}					
12	**ANA1**	ANA1, GPIOC1	C1				**ANA1**					
13	**ANA0**	ANA0, GPIOC0	C0				**ANA0**					
14	**VSS_IO**	V_{SS_IO}								**V_{SS_IO}**		
15	**TCK**	TCK, GPIOD2	D2								**TCK**	
16	**RESET**	$\overline{RESET}$, GPIOA7	A7									**$\overline{RESET}$**
17	**GPIOB3**	GPIOB3, MOSI, T3	**B3**			MOSI			T3			
18	**GPIOB2**	GPIOB2, MISO, T2	**B2**			MISO			T2			
19	**GPIOB4**	GPIOB4, T0, CLKO	**B4**						T0			CLKO
20	**GPIOA5**	GPIOA5, PWM5, FAULT2, T3	**A5**					PWM5, FAULT2	T3			
21	**GPIOB0**	GPIOB0, SCLK, SCL	**B0**	SCL		SCLK						
22	**GPIOA4**	GPIOA4, PWM4, FAULT1, T2	**A4**					PWM4, FAULT1	T2			
23	**GPIOA2**	GPIOA2, PWM2	**A2**					PWM2				
24	**VCAP**	V_{CAP}								**V_{CAP}**		

Table 2-2 56F8014 Pins (Continued)

			Peripherals:									
LQFP Pin #	**Pin Name**	**Signal Name**	**GPIO**	**I2C**	**SCI**	**SPI**	**ADC**	**PWM**	**Quad Timer**	**Power & Ground**	**JTAG**	**Misc.**
25	**VDD_IO**	V_{DD_IO}								**V_{DD_IO}**		
26	**VSS_IO**	V_{SS_IO}								**V_{SS_IO}**		
27	**GPIOA1**	GPIOA1, PWM1	**A1**					PWM1				
28	**GPIOA0**	GPIOA0, PWM0	**A0**					PWM0				
29	**TDI**	TDI, GPIOD0	D0								**TDI**	
30	**TMS**	TMS, GPIOD3	D3								**TMS**	
31	**TDO**	TDO, GPIOD1	D1								**TDO**	
32	**GPIOB6**	GPIOB6, RXD, SDA, CLKIN	**B6**	SDA	RXD							CLKIN

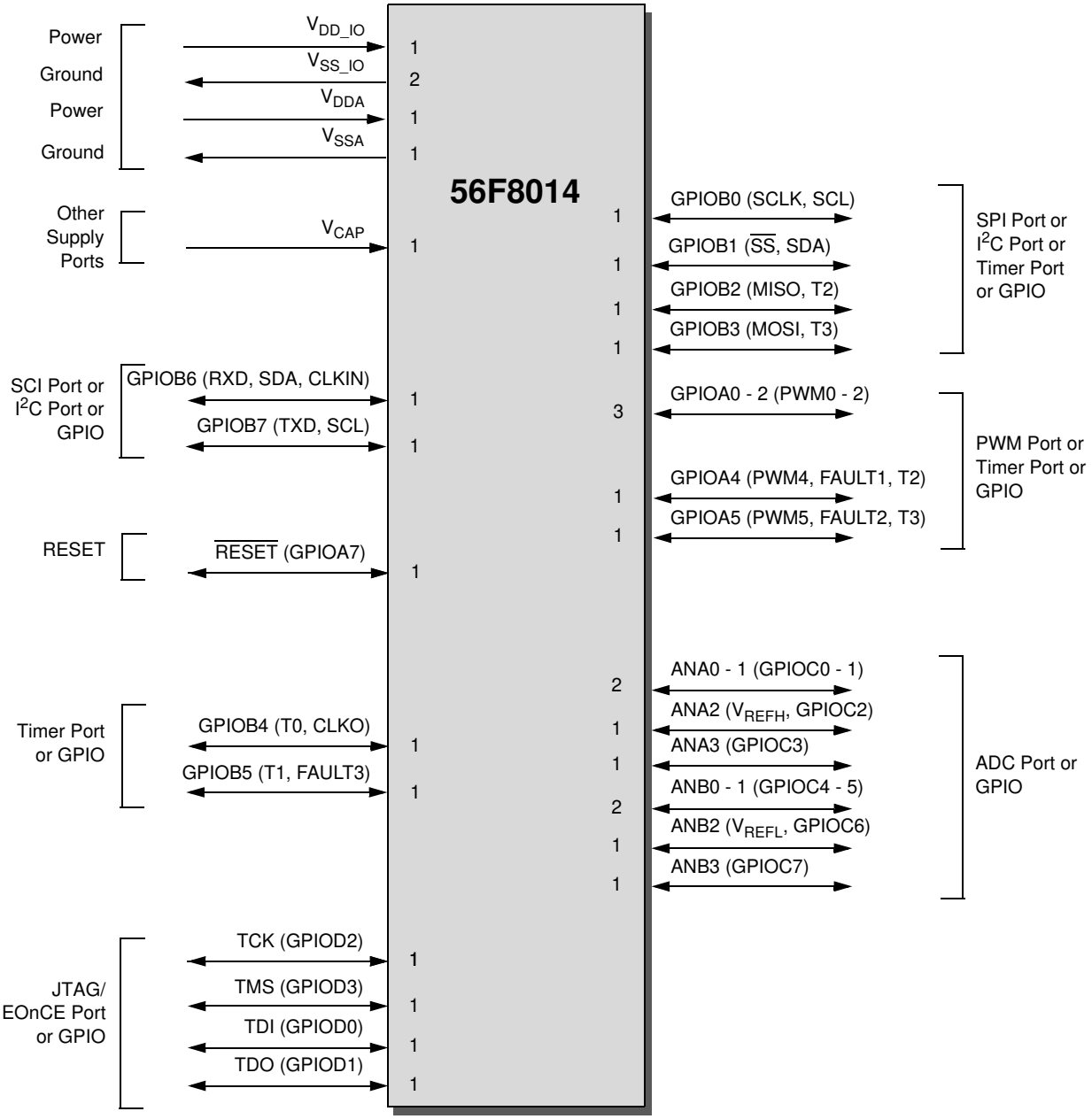


Figure 2-1 56F8014 Signals Identified by Functional Group (32-Pin LQFP)

2.2 56F8014 Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternate functionality must be programmed.

Table 2-3 56F8014 Signal and Package Information for the 32-Pin LQFP

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
V_{DD_IO}	25	Supply	Supply	**I/O Power** — This pin supplies 3.3V power to the chip I/O interface.
V_{SS_IO}	14	Supply	Supply	**V_{SS}** — These pins provide ground for chip logic and I/O drivers.
V_{SS_IO}	26			
V_{DDA}	8	Supply	Supply	**ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply.
V_{SSA}	9	Supply	Supply	**ADC Analog Ground** — This pin supplies an analog ground to the ADC modules.
V_{CAP}	24	Supply	Supply	**V_{CAP}** — Connect a 2.2 µF or greater bypass capacitor between this pin and VSS_IO, which is required by the internal voltage regulator for proper chip operation. See **Section 10.2.1**.
GPIOB6 **(RXD)** **(SDA[1])** **(CLKIN)**	32	Input/ Output Input Input/ Output Input	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. **Receive Data** — SCI receive data input. **Serial Data** — This pin serves as the I^2C serial data line. **Clock Input** — This pin serves as an optional external clock input. After reset, the default state is GPIOB6. The alternative peripheral functionality is controlled via the SIM (See **Section 6.3.8**) and the CLKMODE bit of the OCCS Oscillator Control Register.

1. This signal is also brought out on the GPIOB1 pin.

Return to Table 2-2

Table 2-3 56F8014 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOB7	2	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(TXD)		Input/ Output		**Transmit Data** — SCI transmit data output or transmit / receive in single wire opeation.
(SCL[2])		Input/ Output		**Serial Clock** — This pin serves as the I^2C serial clock. After reset, the default state is GPIOB7. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
2. This signal is also brought out on the GPIOB0 pin.				
$\overline{\text{RESET}}$	16	Input	Input with internal pull-up enabled	**Reset** — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the chip is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. The internal reset signal will be deasserted synchronous with the internal clocks after a fixed number of internal clocks.
(GPIOA7)		Input/Open Drain Output		**Port A GPIO** — This GPIO pin can be individually programmed as an input or open drain output pin. Note that $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can only be reset via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.
GPIOB4	19	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(T0)		Input/ Output		**T0** — Timer, Channel 0
(CLKO)		Output		**Clock Output** — This is a buffered clock signal. Using the SIM_CLKO Select Register (SIM_CLKOSR), this pin can be programmed as any of the following: disabled (logic 0), CLK_MSTR (system clock), IPBus clock, or oscillator output. See **Section 6.3.7**. After reset, the default state is GPIOB4. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.

Return to Table 2-2

Table 2-3 56F8014 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOB5 **(T1)** **(FAULT3)**	3	Input/ Output Input/ Output Input	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. **T1** — Timer, Channel 1 **FAULT3** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip. After reset, the default state is GPIOB5. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
TCK **(GPIOD2)**	15	Input Input/ Output	Input with internal pull-up enabled	**Test Clock Input** — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pull-up resistor. A Schmitt trigger input is used for noise immunity. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TCK.
TMS **(GPIOD3)**	30	Input Input/ Output	Input with internal pull-up enabled	**Test Mode Select Input** — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TMS. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor if this pin is configured as TMS.
TDI **(GPIOD0)**	29	Input Input/ Output	Input with internal pull-up enabled	**Test Data Input** — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDI.

Return to Table 2-2

Table 2-3 56F8014 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
TDO	31	Output	Output	**Test Data Output** — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK.
(GPIOD1)		Input/ Output		**Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDO.
GPIOB0	21	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(SCLK)		Input/ Output		**SPI Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity.
(SCL[3])		Input/ Output		**Serial Data** — This pin serves as the I^2C serial clock. After reset, the default state is GPIOB0. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
3. This signal is also brought out on the GPIOB7 pin.				
GPIOB1	1	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
($\overline{SS}$)		Input		**SPI Slave Select** — $\overline{SS}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received.
(SDA[4])		Input/ Output		**Serial Clock** — This pin serves as the I^2C serial data line. After reset, the default state is GPIOB1. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
4. This signal is also brought out on the GPIOB6 pin.				

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Table 2-3 56F8014 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOB2	18	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(MISO)		Input/ Output		**SPI Master In/Slave Out** — This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The slave device places data on the MISO line a half-cycle before the clock edge the master device uses to latch the data.
(T2[5])		Input/ Output		**T2** — Timer, Channel 2 After reset, the default state is GPIOB2. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
5. This signal is also brought out on the GPIOA4 pin.				
GPIOB3	17	Input/ Output	Input with internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(MOSI)		Input/ Output		**SPI Master Out/Slave In**— This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data.
(T3[6])		Input/ Output		**T3** — Timer, Channel 3 After reset, the default state is GPIOB3. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
6. This signal is also brought out on the GPIOA5 pin.				
GPIOA0	28	Input/ Output	Input with internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(PWM0)		Output		**PWM0** — This is one of the six PWM output pins. After reset, the default state is GPIOA0.

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Table 2-3 56F8014 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOA1 **(PWM1)**	27	Input/ Output Output	Input with internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM1** — This is one of the six PWM output pins. After reset, the default state is GPIOA1.
GPIOA2 **(PWM2)**	23	Input/ Output Output	Input with internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM2** — This is one of the six PWM output pins. After reset, the default state is GPIOA2.
GPIOA4 **(PWM4)** **(FAULT1)** **(T2[7])**	22	Input/ Output Output Input Input/ Output	Input with internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM4** — This is one of the six PWM output pins. **Fault1** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip. **T2** — Timer, Channel 2 After reset, the default state is GPIOA4. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
7. This signal is also brought out on the GPIOB2 pin.				
GPIOA5 **(PWM5)** **(FAULT2)** **(T3[8])**	20	Input/ Output Output Input Input/ Output	Input with internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM5** — This is one of the six PWM output pins. **Fault2** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip. **T3** — Timer, Channel 3 After reset, the default state is GPIOA5. The alternative peripheral functionality is controlled via the SIM. See **Section 6.3.8**.
8. This signal is also brought out on the GPIOB3 pin.				

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Table 2-3 56F8014 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
ANA0 **(GPIOC0)**	13	Input Input/ Output	Analog Input	**ANA0** — Analog input to ADC A, channel 0 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is ANA0.
ANA1 **(GPIOC1)**	12	Input Input/ Output	Analog Input	**ANA1** — Analog input to ADC A, channel 1 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is ANA1.
ANA2 **(V_{REFH})** **(GPIOC2)**	11	Input Input Input/ Output	Analog Input	**ANA2** — Analog input to ADC A, channel 2 **V_{REFH}** — Analog reference voltage high **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is ANA2.
ANA3 **(GPIOC3)**	10	Input Input/ Output	Analog Input	**ANA3** — Analog input to ADC A, channel 3 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is ANA3.
ANB0 **(GPIOC4)**	4	Input Input/ Output	Analog Input	**ANB0** — Analog input to ADC B, channel 0 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is ANB0.

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Table 2-3 56F8014 Signal and Package Information for the 32-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
ANB1 **(GPIOC5)**	5	Input Input/ Output	Analog Input	**ANB1** — Analog input to ADC B, channel 1 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is ANB1.
ANB2 **(V_{REFL})** **(GPIOC6)**	6	Input Input Input/ Output	Analog Input	**ANB2** — Analog input to ADC B, channel 2 **V_{REFL}** — Analog reference voltage low. This should normally be connected to a low-noise V_{SS}. **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is ANB2.
ANB3 **(GPIOC7)**	7	Input Input/ Output	Analog Input	**ANB3** — Analog input to ADC B, channel 3 **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is ANB3.

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