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APX4 – WIRELESS SYSTEM-ON-MODULE

DATA SHEET

Tuesday, 23 July 2013

Version 1.01

bluegiga

VERSION HISTORY

Version	Comment
0.1	First draft
0.2	Defined screws and attachment to motherboard
0.3.1	Some small fixes and additions
0.3	TBDs defined
0.4	Review
0.4.1	Small fix to part number clarification
0.4.2	Updated document name, product description and contact information
0.4.3	Added *Bluetooth* RF specifications
0.5	Clarified pins etc.
0.6	Fixed layout. Removed software version from part number.
0.7	Styles updated and fixed Added notes about missing information
0.8	Added Mouser part number for the SO-DIMM receptacle
0.9	Chapter 6.5.1 removed
1.0	Added FCC/IC texts, removed battery related texts
1.01	Typos

TABLE OF CONTENTS

DESCRIPTION

The Bluegiga APx4 is a small form factor, low power system-on-module that includes the latest wireless connectivity standards: 802.11 b/g/n and *Bluetooth* 4.0. APx4 is based on Freescale's i.MX28 processor family and runs an embedded Linux operating system based on the Yocto Project™. In addition to integrating the 454MHz ARM9 processor, the wireless connectivity technologies, Linux operating system the APx4 also includes with several built in applications, such as the 802.11 and *Bluetooth* 4.0 stacks, Continua v.1.5 compliant IEEE manager and many more. This combination provides an ideal platform for designing multi-radio wireless gateways that enables fast time-to-market and minimum R&D risks.

The Bluegiga APx4 software can be easily extended or tailored customizing the Linux operating system with applications. The motherboards for the APx4 can be easily extended to include almost anything from 3G modems to Ethernet and audio interfaces to and touch screen displays.

The Bluegiga APx4 is an ideal product for applications requiring wireless or wired connectivity technologies and the processing power of the ARM9 processor, such as health and fitness gateways, building and home automation gateways, M2M, point-of-sale and industrial connectivity.

APPLICATIONS:

- Health gateways
- M2M connectivity
- Fitness gateways
- Home and building automation
- Point-of-sale gateways
- People and asset tracking

KEY FEATURES

APx4 is a computing platform:

- 454MHz ARM9 core (Freescale i.MX28)
- 64MB RAM
- 128MB Flash
- Real Time Clock
- Linux operating system
- SO-DIMM form factor

A connectivity platform:

- *Bluetooth* 4.0 dual-mode radio
- 2.4GHz 802.11 b/g/n radio
- Wi-Fi Access Point mode
- 10/100 Ethernet
- USB 2.0 High Speed

With many extension options:

- Up to 800 x 480, 24bit display
- Resistive touch screen
- MMC/SDIO
- Multiple SPI, UART and I²C
- I²S
- PWM, GPIO and AIO

Linux operating system:

- Based on the Yocto Project(TM)
- Thousands of open source software packets available

Qualifications:

- *Bluetooth*
- CE
- FCC and IC

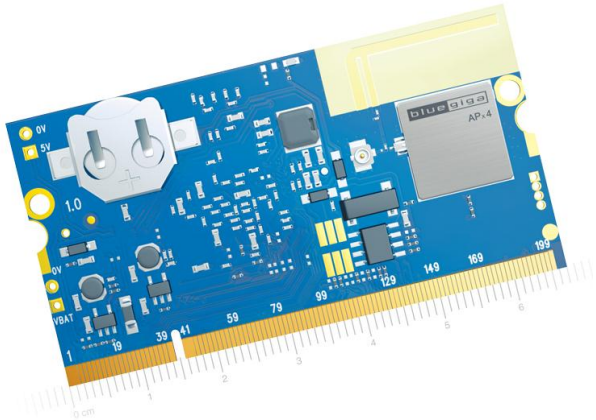
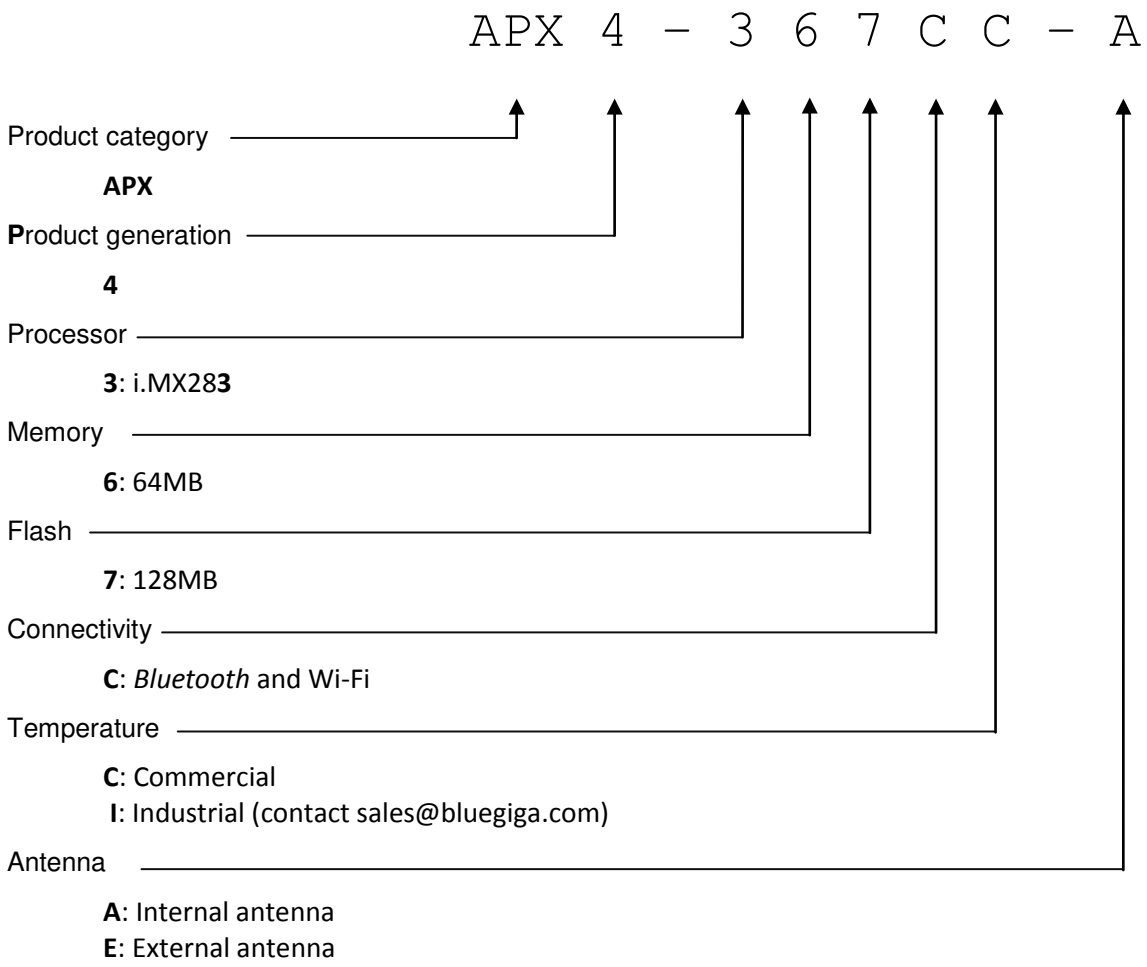


Figure 1: Physical outlook

1 Ordering Information

Product code	CPU and memories	Connectivity	Antenna	Temperature range
APX4-367CC-A	i.MX283 64MB DDR2 128MB Flash	*Bluetooth* + Wi-Fi	Internal antenna	-10 – 50°C

1.1 Part number decoder



Note: Not all variants are available. Minimum order quantities and lead times may apply for special variants. Please contact Bluegiga Technologies Oy for more information.

2 APx4 pin descriptions

The APX4 connector uses a standard DDR1 SO-DIMM connector with 2.5V keying.

- Odd numbered pins are located on top layer
- Even numbered pins are located on bottom layer

There is a ½ pitch (0.3mm) offset from top layer pins to bottom layer pins.

Note that most receptacles also have 0.3mm offset from odd pins to even pins.

2.1 Receptacle

Suitable receptacles are available from multiple vendors. For example TE Connectivity's part number 1473005-1, Mouser part number: 571-1473005-1 and Digi-Key's part number: A99605-ND.

PCB footprint and schematic symbol for the mentioned part number will be available for download from Techforum in Mentor Graphics' PADS format.

2.2 Power contacts on the left side

In addition to the 200 pins/finger contacts there are two pairs of plated through holes on the left side of the module which can be used for powering the module stand-alone (not assembled on any motherboard). The pitch between the holes is 2.54mm. Leave the holes unconnected if the module is assembled on a motherboard.

Name	Function
GND	Ground
VIN	+5V input
GND	Ground
VBATTERY	Battery positive input/output

Table 1: Power supply pins

2.3 Debug UART on the right side

On the right side there are four plated through holes for PWM or debug port stand-alone (not assembled on any motherboard). The vertical distance between the holes is 1.27mm:

Name	Function
3V3	3.3V output (for current limits, see Table 50)
PWM1/DUART TxD	Debug UART data transmit, logic level 3.3V
PWM0/DUART RxD	Debug UART data receive, logic level 3.3V
GND	Ground

Table 2: Debug UART pins

2.4 SO-DIMM connection pin descriptions

Note: Signals/nets marked with a star (*) are not present on standard version

Pin#	Default function	Net name	Note
1	5V input	VIN	
2	5V input	VIN	
3	5V input	VIN	
4	5V input	VIN	
5	Battery input/output	VBATTERY	
6	Battery input/output	VBATTERY	
7	Battery input/output	VBATTERY	
8	Bootmode	BOOTMODE	
9	3.3V output	3V3	Pins 9-10 may source up to 200mA combined.
10	3.3V output	3V3	Pins 9-10 may source up to 200mA combined.
11	3.3V output	3V3	Pins 9-10 may source up to 200mA combined.
12	3.3V output	3V3	Pins 9-10 may source up to 200mA combined.
13	RTC battery	VBACKUP	
14	PS switch	PSWITCH_OUT	
15	NC	NC	
16	NC	NC	
17	Reset in - Master reset	RESETN	
18	Ground	GND	

Table 3: Main power pins

Pin#	Default function	Net name
19	Ethernet TX -	ETN_TXN
20	GND	GND
21	Ethernet TX +	ETN_TXP
22	3.3V output	3V3
23	Ethernet RX -	ETN_RXN
24	Ethernet LED	ETN_LED1N*
25	Ethernet RX +	ETN_RXP
26	GND	GND

Table 4: Ethernet

* See 6.1 for detailed function.

Pin#	Default function	Net name
27	USB External VBUS enable	SPDIF*
28		NC
29	USB D-	USB1DM
30		NC
31	USB D+	USB1DP
32	Ground	GND

Table 5: USB Host

Pin#	Default function	Net name
33	USB OTG id	USB0_ID
34		NC
35	USB D-	USB0DM
36		NC
37	USB D+	USB0DP
38		NC
39	Ground	GND

Table 6: USB On-the-go

Pin#	Default function	Net name
40	I^2C Data	I2C0_SDA
41	I^2C Clock	I2C0_SCL

Table 7: I^2C 0

Pin#	Default function	Net name
42	PWM (Backlight)	PWM4
43	Status led	PWM3

Table 8: Dedicated PWMs

Pin#	Default function	Net name
44	Slave select 1	SDIO_DAT1_OUT*
45	Slave select 2	SDIO_DAT2_OUT*
46	Command - Master out, slave in	SDIO_CMD_OUT*
47	Data 0, Master in, slave out	SDIO_DAT0_OUT*
48	Clock	SDIO_CLK_OUT*
49	Ready - Slave select 0	SDIO_DAT3_OUT*
50	Ground	GND

Table 9: SSP2 – SDIO/MMC/SPI

Pin#	Default function	Net name
51	Card detect	SSP0_DETECT
52	Data 0	SSP0_DATA0
53	Data 1	SSP0_DATA1
54	Data 2	SSP0_DATA2
55	Data 3	SSP0_DATA3
56	Command	SSP0_CMD
57	Clock	SSP0_SCK
58	Ground	GND

Table 10: SSP0 – SDIO/MMC/SPI

Pin#	Default function	Net name
59	UART transmit	AUART0_TX
60	UART receive	AUART0_RX
61	UART clear-to-send	AUART0_CTS
62	UART request-to-send	AUART0_RTS

Table 11: UART 0

Pin#	Default function	Net name
63	UART transmit	SSP2_MOSI
64	UART receive	SSP2_SCK
65		NC
66		NC

Table 12: UART 2

Pin#	Default function	Net name
67	UART transmit	SSP2_SS0
68	UART receive	SSP2_MISO
69		NC
70		NC
71	Ground	GND

Table 13: UART 3

Pin#	Default function	Net name
72	*Bluetooth* GPIO	BT_PIO7
73	*Bluetooth* GPIO	BT_PIO8
74	*Bluetooth* GPIO	BT_PIO9
75	*Bluetooth* GPIO	BT_PIO25

Table 14: *Bluetooth* GPIO

Pin#	Default function	Net name
76	CAN 0 transmit	GPMI_RDY2*
77	Ground	GND
78	CAN 1 transmit	GPMI_CE2N*
79	CAN 1 receive	GPMI_CE3*
80	Ground	GND
81	CAN 0 receive	GPMI_RDY3*
82	Ground	GND

Table 15: CAN

Pin#	Default function	Net name
83	MCLK	SAIF0_MCLK
84	Data line 1	SAIF1_SDATA0
85	Data line 0	SAIF0_SDATA0
86	Bit clock	SAIF0_BITCLK
87	Left/Right clock	SAIF0_LRCLK
88	GND	GND

Table 16: Primary audio / UART 4

Pin#	Default function	Net name
89		NC
90		NC
91		NC
92		NC
93		NC
94	Ground	GND
95		NC
96		NC
97		NC
98		NC
99		NC
100		NC

Table 17: Reserved group 1

Pin#	Default function	Net name
101		NC
102	Ground	GND
103		NC
104		NC
105		NC
106		NC
107	1.4V output*	1V4_CPU
108	1.8V output*	1V8
109	4.2V output*	4V2_CPU
110		NC
111		GND
112		NC
113		NC
114		NC
115		NC
116	Ground	GND

Table 18: Reserved group 2

*__Important:__ Pins 107-109 are only meant for manufacturing test. Please leave unconnected. Do not pull any current from these outputs. Doing so may create a black hole in the universe.

Pin#	Default function	Net name
117	Data 0	LCD_D0
118	Data 1	LCD_D1
119	Data 2	LCD_D2
120	Data 3	LCD_D3
121	Data 4	LCD_D4
122	Data 5	LCD_D5
123	Data 6	LCD_D6
124	Data 7	LCD_D7
125	Data 8	LCD_D8
126	Data 9	LCD_D9
127	Data 10	LCD_D10
128	Data 11	LCD_D11
129	Ground	GND
130	Data 12	LCD_D12
131	Data 13	LCD_D13
132	Data 14	LCD_D14
133	Data 15	LCD_D15
134	Data 16	LCD_D16
135	Data 17	LCD_D17
136	Data 18	LCD_D18
137	Data 19	LCD_D19
138	Data 20	LCD_D20
139	Data 21	LCD_D21
140	Data 22	LCD_D22
141	Data 23	LCD_D23
142	Ground	GND

Table 19 LCD data lines

Pin#	Default function	Net name
143	Horizontal Sync	LCD_WR_RWN
144	Vertical Sync	LCD_RD_E
145	LCD Enable	LCD_CS
146	Dot clock	LCD_RS
147	Ground	GND

Table 20: LCD control lines

Pin#	Function	Net name
148	Debug UART RX or I2C1_SDA	PWM0 (also connected to PTH pins on right side)
149	Debug UART TX or I2C1_SCL	PWM1 (also connected to PTH pins on right side)
150	LCD reset / GPIO	LCD_RESET
151		NC

Table 21: Debug UART / PWM / I2C1 / GPIO

Pin#	Function	Net name
152		NC
153		NC
154		NC
155		NC
156		NC
157		NC
158		NC
159	Ground	GND
160	Ground	GND
161		NC
162		NC
163	Ground	GND
164	Ground	GND
165		NC
166		NC
167	Ground	GND
168	Ground	GND
169		NC
170	WiFi Activity	WIFI_ACT
171	Ground	GND

Table 22: Reserved group 3

Pin#	Function	Net name
172	Wi-Fi Debug SPI - MISO	SPI_WIFI_MISO
173	Wi-Fi Debug SPI – CLK	SPI_WIFI_CLK
174	Wi-Fi Debug SPI – MOSI	SPI_WIFI_MOSI
175	Wi-Fi Debug SPI - CS	SPI_WIFI_CS
176	RTC interrupt	INT_EXT_RTC_N
177	Factory reset button / JTAG return clock	JTAG_RTCK
178	JTAG test clock	JTAG_TCK
179	JTAG test data in	JTAG_TDI
180	JTAG test data out	JTAG_TDO
181	JTAG test mode state	JTAG_TMS
182	JTAG test reset	JTAG_TRST
183	Ground	GND
184	JTAG enable boundary scan	DEBUG

Table 23: Misc

Pin#	Function	Net name
185	Touch controller XN	LRADC4
186	Touch controller XP	LRADC2
187	Touch controller YN	LRADC5
188	Touch controller YP	LRADC3
189	Touch controller WIPER	LRADC6
190	Generic ADC 0	LRADC0
191	Generic ADC 1	LRADC1
192	High speed ADC	HSADC0
193	Ground	GND
194	Ground	GND

Table 24: ADC

Pin #	Function	Net name
195	*Bluetooth* debug enable	BT_SPI_PCM1N
196	PCM in	BT_PCM1_IN
197	PCM out	BT_PCM1_OUT
198	PCM clock	BT_PCM1_CLK
199	PCM sync	BT_PCM1_SYNC
200	Ground	GND

Table 25: *Bluetooth* audio

3 Power subsystem

Pin#	Function	APx4 net name	Description
1-4	5V input	VIN	Main power input
5-7	Battery input/output	VBATTERY	A rechargeable battery can be connected
9-12, 22	3.3V output	3V3	For maximum current draw, see Table 50
13	RTC battery	VBACKUP	RTC battery backup power
14	Power switch	PSWITCH_OUT	Power switch
17	Reset in - Master reset	RESETN	Active low master reset. Resets the entire board.

Table 26: Power supply pins

The module is powered through the 5V input. It is recommended that all the pins (1-4) are connected together on the application board.

The external battery connectable to VBATTERY is currently not supported.

VBACKUP is connected to the Real-Time clock battery and the VDD input of the Real Time Clock. This pin can be used to power the real time clock in cases where the battery is not placed on the module.

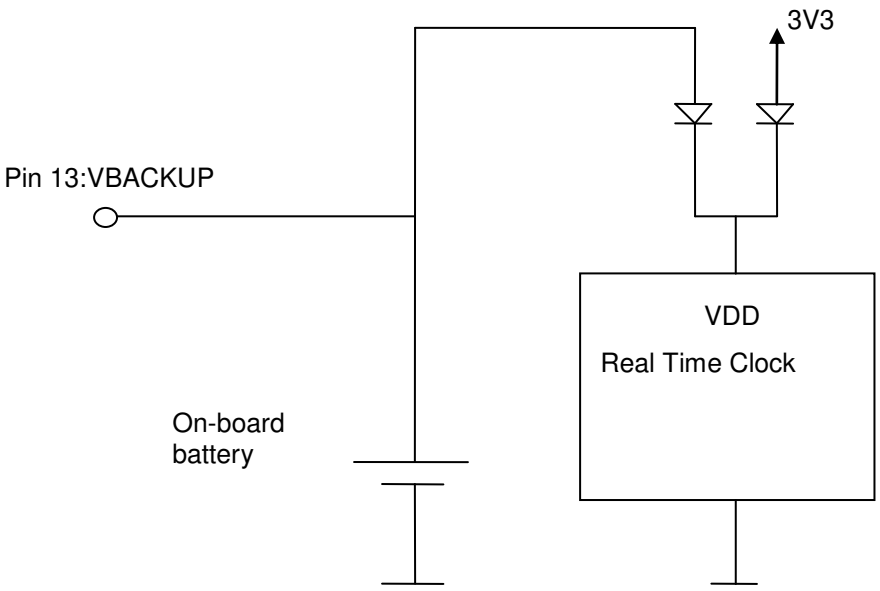


Figure 2: VBACKUP and battery connection

3.1 PSWITCH_OUT pin 14

***Note*: In most cases the user can ignore the PSWITCH pin. Leave unconnected for normal operation.**

The ÅSWITCH_OUT (pin 14) has three levels: low, mid and high. A 10kΩ pull-up to mid-level is applied on the module to the PSWITCH line, causing the device to start booting immediately once power is applied. Boot-up requires a mid-level voltage to be present for >100ms.

If the PSWITCH is pulled high for over 5 seconds, for example by connecting it to 3.3V, a special Freescale USB recovery mode is entered. For further details about the power switch, refer to Freescale's Reference Manual, Section 11.4. This mode can also be entered using the BOOTMODE pin.

3.2 RESETN

Power-on reset is generated internally. If a reset from external pins is required use the RESETN pin. RESETN is internally pulled up to 3.3V.

The RESETN pin must be kept low for at least 100ms and then released in order to guarantee a proper reset.

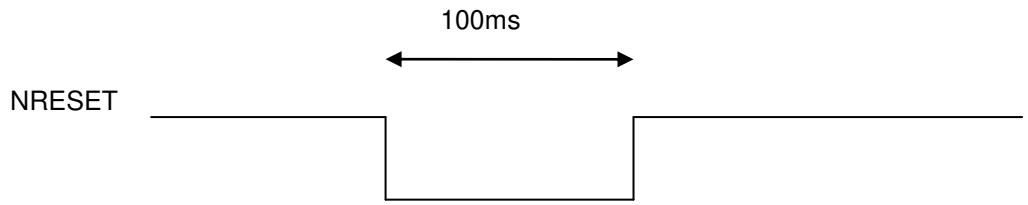


Figure 3: NRESET

4 Processor subsystem

The processor belongs to the Freescale i.MX28-family and integrates an ARM9 core operating at 454MHz. The standard APX4 variant uses the i.MX283 processor. The module also has 128MB of SLC NAND flash and 64MB of DDR2-400 memory. For more details regarding the features the processor offers, please see the Freescale Reference Manual.

By default the module boots from the NAND flash into the U-Boot boot loader environment. From there the boot loader loads a Linux kernel which boots into the Bluegiga Linux userspace.

4.1 Bootmodes

The module supports booting from multiple different media including NAND Flash, Secure Digital (SD) cards, MMC cards, I^2C EEPROM and USB (in a device mode). The selected boot media can be selected using the LCD_DATA[0-3] signals or in the case of USB recovery boot, by tying the BOOTMODE pin to ground.

By default the module boots from internal NAND flash, meaning that LCD_DATA[3], LCD_DATA[1] and LCD_DATA[0] have pull-downs on the module and LCD_DATA[2] has a pull-up.

Default boot mode in bold face. The module has pull-ups and pull-downs so that when LCD_DATA[0]..LCD_DATA[3] are left unconnected the module boots from internal NAND. After boot the LCD_DATA lines can be used fro any purpose.

LCD_DATA[3]	LCD_DATA[2]	LCD_DATA[1]	LCD_DATA[0]	Port
0	0	0	0	USB0 device mode boot
0	0	0	1	EEPROM connected to I2C0
0	0	1	0	SPI flash on SSP2 (non-Wi-Fi version only)
0	0	1	1	SPI flash on SSP3 (not available on standard versions)
0	**1**	**0**	**0**	**Module's internal NAND Flash**
0	1	1	0	Wait for JTAG connection
1	0	0	0	SPI EEPROM on SSP3 (not available on standard versions)
1	0	0	1	SD/MMC card on SSP0
1	0	1	0	SD/MMC on SSP1 (not available on standard versions)

Table 27: Bootmodes

5 Wireless interfaces

The wireless connectivity on the module is implemented using two separate chips which share a 2.4GHz antenna.

5.1 *Bluetooth*

The module is a fully qualified *Bluetooth* 4.0, Class 1, system, supporting both classical *Bluetooth* as well as *Bluetooth Smart* (*Bluetooth* low energy) devices simultaneously.

5.1.1 *Bluetooth* GPIOs

Pin#	Function	Net name
72	*Bluetooth* GPIO 7	BT_PIO7
73	*Bluetooth* GPIO 8	BT_PIO8
74	*Bluetooth* GPIO 9	BT_PIO9
75	*Bluetooth* GPIO 25	BT_PIO25

Table 28: *Bluetooth* GPIO

These GPIOs are controlled by the *Bluetooth* baseband chip. The main processor can read and write them by issuing special commands to the *Bluetooth* chip, making them suitable for use as status indicators, but not for high speed signals. For the current status of software support, please refer to the software documentation. Contact support if needed.

The pins are bidirectional pins with internal programmable strength pull-up or pull-down. By default they are inputs with a weak pull-down.

5.1.2 *Bluetooth* Audio interface

Pin #	Net name	PCM function	I^2S function	Debug interface
195	BT_SPI_PCM1N	Select Audio: GND	Select Audio: GND	Select Debug: +3.3V
196	BT_PCM1_IN	PCM in	Serial in (SD_IN)	MOSI
197	BT_PCM1_OUT	PCM out	Serial out (SD_OUT)	MISO
198	BT_PCM1_CLK	PCM clock	Serial clock (SCK)	Clock
199	BT_PCM1_SYNC	PCM sync	Write sync (WS)	Chip select (active low)

Table 29: *Bluetooth* audio and debug interface

The *Bluetooth* audio functionality can be configured to work in either I^2S or PCM mode. In addition, the *Bluetooth* chip's debug interface is multiplexed with the audio pins.

The audio interface supports continuous transmission and reception of PCM audio data over *Bluetooth*. Operation in either master or slave mode are supported and many different clock modes can be supported. A maximum of 3 SCO audio links can be transmitted through the PCM interface at any one time.