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ON Semiconductor®

1/3-Inch CMOS Digital Image Sensor

AR0132AT Datasheet, Rev. 9

For the latest data sheet, please visit www.onsemi.com

Features

- Superior low-light performance
- HD video (720p60)
- Linear or high dynamic range capture
- Video/Single Frame modes
- On-chip AE and statistics engine
- Parallel and serial output
- Auto black level calibration
- Context switching
- Temperature Sensor

Applications

- Automotive imaging
- Video surveillance
- 720p60 video applications
- High dynamic range imaging

General Description

ON Semiconductor's AR0132AT is a 1/3-inch CMOS digital image sensor with an active-pixel array of 1280H x 960V. It captures images in either linear or high dynamic range modes, with a rolling-shutter readout. It includes sophisticated camera functions such as auto exposure control, windowing, and both video and single frame modes. It is designed for both low light and high dynamic range scene performance. It is programmable through a simple two-wire serial interface. The AR0132AT produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including surveillance and HD video.

Table 1: Key Parameters

Parameter		Typical Value
Optical format		1/3-inch (6 mm)
Active pixels		1280 x 960 = 1.2 Mp
Pixel size		3.75 μm
Color filter array		RGB Bayer, or monochrome
Shutter type		Electronic rolling shutter
Input clock range		6 – 50 MHz
Output clock maximum		74.25 MHz
Output	Serial	HiSPi 12-, 14-, or 20-bit
	Parallel	12-bit
Frame rate	Full resolution	45 fps
	720p	60 fps
Responsivity		5.48 V/lux-sec
SNR_{MAX}		43.9 dB
Maximum dynamic range		>115 dB
Supply voltage	I/O	1.8 or 2.8 V*
	Digital	1.8 V
	Analog	2.8 V
	HiSPi	0.4V or 1.8V
Power consumption (typical)		270 mW (1280 x 720 60 fps Parallel output Linear Mode)
		460 mW (1280x720 60 fps Parallel output HDR Mode)
Operating temperature		−40°C to + 105° C (ambient) −40°C to + 120° C (junction)
Package options		9x9 mm iBGA
		Bare die

Note: *1.8V V_{DD}_IO is recommended for better row noise performance

1

Ordering Information

Table 2:   Available Part Numbers

Part Number	Product Description	Orderable Product Attribute Description
AR0132AT6C00XPEA0-DPBR1	RGB, 0deg CRA, iBGA Package	Drypack, Protective Film, Anti-Reflective Glass
AR0132AT6C00XPEA0-DRBR1	RGB, 0deg CRA, iBGA Package	Drypack, Anti-Reflective Glass
AR0132AT6C00XPEA0-TPBR	RGB, 0deg CRA, iBGA Package	Tape & Reel, Protective Film, Anti-Reflective Glass
AR0132AT6C00XPEA0-TRBR	RGB, 0deg CRA, iBGA Package	Tape & Reel, Anti-Reflective Glass
AR0132AT6C00XPD20	RGB, 0deg CRA, Reconstruct Die	
AR0132AT6C00XPW90	RGB, 0deg CRA, Wafer	
AR0132AT6B00XPEA0-DRBR1	RCCB, 0deg CRA, iBGA Package	Drypack, Anti-Reflective Glass
AR0132AT6B00XPW90	RCCB, 0deg CRA, Wafer	
AR0132AT6G00XPEA0-DPBR1	RGBC, 0deg CRA, iBGA Package	Drypack, Protective Film, Anti-Reflective Glass
AR0132AT6G00XPEA0-DRBR1	RGBC, 0deg CRA, iBGA Package	Drypack, Anti-Reflective Glass
AR0132AT6G00XPEA0-TPBR	RGBC, 0deg CRA, iBGA Package	Tape & Reel, Protective Film, Anti-Reflective Glass
AR0132AT6G00XPEA0-TRBR	RGBC, 0deg CRA, iBGA Package	Tape & Reel, Anti-Reflective Glass
AR0132AT6M00XPEA0-DPBR1	Mono, 0deg CRA, iBGA Package	Drypack, Protective Film, Anti-Reflective Glass
AR0132AT6M00XPEA0-DRBR1	Mono, 0deg CRA, iBGA Package	Drypack, Anti-Reflective Glass
AR0132AT6M00XPEA0-TPBR	Mono, 0deg CRA, iBGA Package	Tape & Reel, Protective Film, Anti-Reflective Glass
AR0132AT6M00XPW90	Mono, 0deg CRA, Wafer	
AR0132AT6R00XPEA0-DPBR1	RCCC, 0deg CRA, iBGA Package	Drypack, Protective Film, Anti-Reflective Glass
AR0132AT6R00XPEA0-DRBR1	RCCC, 0deg CRA, iBGA Package	Drypack, Anti-Reflective Glass
AR0132AT6R00XPEA0-TPBR	RCCC, 0deg CRA, iBGA Package	Tape & Reel, Protective Film, Anti-Reflective Glass
AR0132AT6R00XPEA0-TRBR	RCCC, 0deg CRA, iBGA Package	Tape & Reel, Anti-Reflective Glass
AR0132AT6R00XPW90	RCCC, 0deg CRA, Wafer	
AR0132AT6C00XPEAD3-GEVK	RGB Demo Kit, Sunex DSL945D	
AR0132AT6C00XPEAH3-GEVB	RGB Headboard, Sunex DSL945D	
AR0132AT6C00XPEAD3-S215-GEVK	RGB Demo Kit, Sunex DSL215	
AR0132AT6C00XPEAH3-S215-GEVB	RGB Headboard, Sunex DSL215	
AR0132AT6B00XPEAD3-GEVK	RCCB Demo Kit, Sunex DSL945D	
AR0132AT6B00XPEAH3-GEVB	RCCB Headboard, Sunex DSL945D	
AR0132AT6G00XPEAD3-GEVK	RGBC Demo Kit, Sunex DSL945D	
AR0132AT6G00XPEAH3-GEVB	RGBC Headboard, Sunex DSL945D	
AR0132AT6M00XPEAD3-GEVK	Mono Demo Kit, Sunex DSL945D	
AR0132AT6M00XPEAH3-GEVB	Mono Headboard, Sunex DSL945D	
AR0132AT6R00XPEAD3-GEVK	RCCC Demo Kit, Sunex DSL945D	
AR0132AT6R00XPEAH3-GEVB	RCCC Headboard, Sunex DSL945D	

See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

Table of Contents

General Description

The ON Semiconductor AR0132AT can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 960p-resolution image at 45 frames per second (fps). In linear mode, it outputs 12-bit raw data, using either the parallel or serial (HiSPi) output ports. In high dynamic range mode, it outputs 12-bit compressed data using parallel output, or 12-bit or 14-bit compressed or 20-bit linearized data using the HiSPi port. The device may be operated in video (master) mode or in single frame trigger mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock in parallel mode.

The AR0132AT includes additional features to allow application-specific tuning: windowing and offset, adjustable auto-exposure control, auto black level correction, and on-board temperature sensor. Optional register information and histogram statistic information can be embedded in first and last two lines of the image frame.

The sensor is designed to operate in a wide temperature range (–40°C to +105°C).

Functional Overview

The AR0132AT is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 50 MHz. The maximum output pixel rate is 74.25 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor.

Figure 1:   Block Diagram
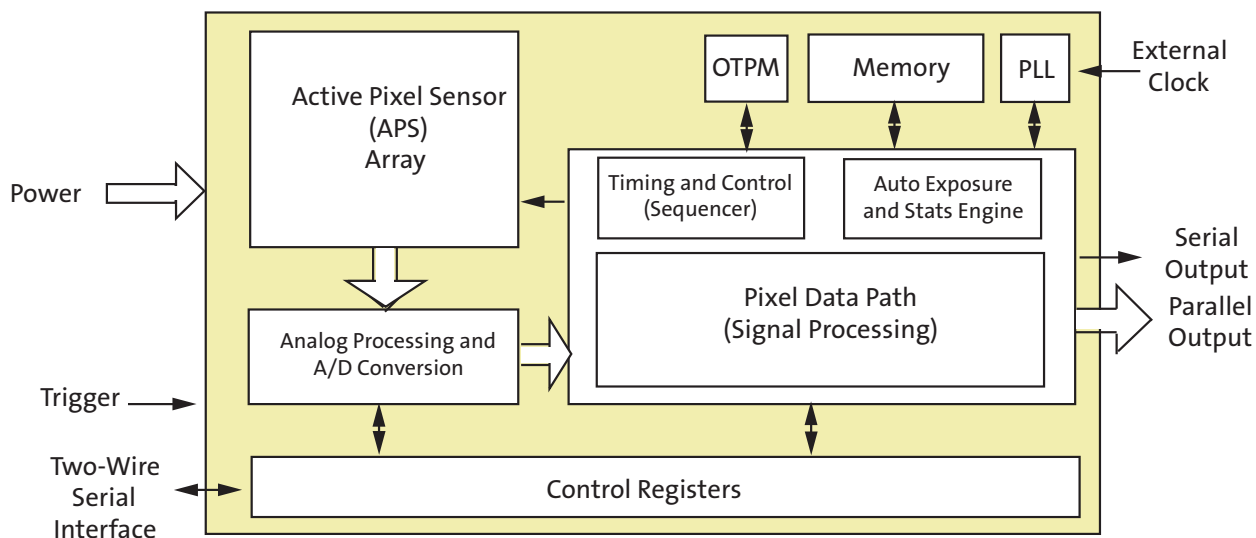
User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.2 Mp Active-Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and

readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor also offers a high dynamic range mode of operation where multiple images are combined on-chip to produce a single image at 20-bit per pixel value. A compressing mode is further offered to allow this 20-bit pixel value to be transmitted to the host system as a 12- or 14-bit value with close to zero loss in image quality. The pixel data are output at a rate of up to 74.25 Mp/s, in parallel to frame and line synchronization signals.

Figure 2:   Typical Configuration: Serial Four-Lane HiSPi Interface
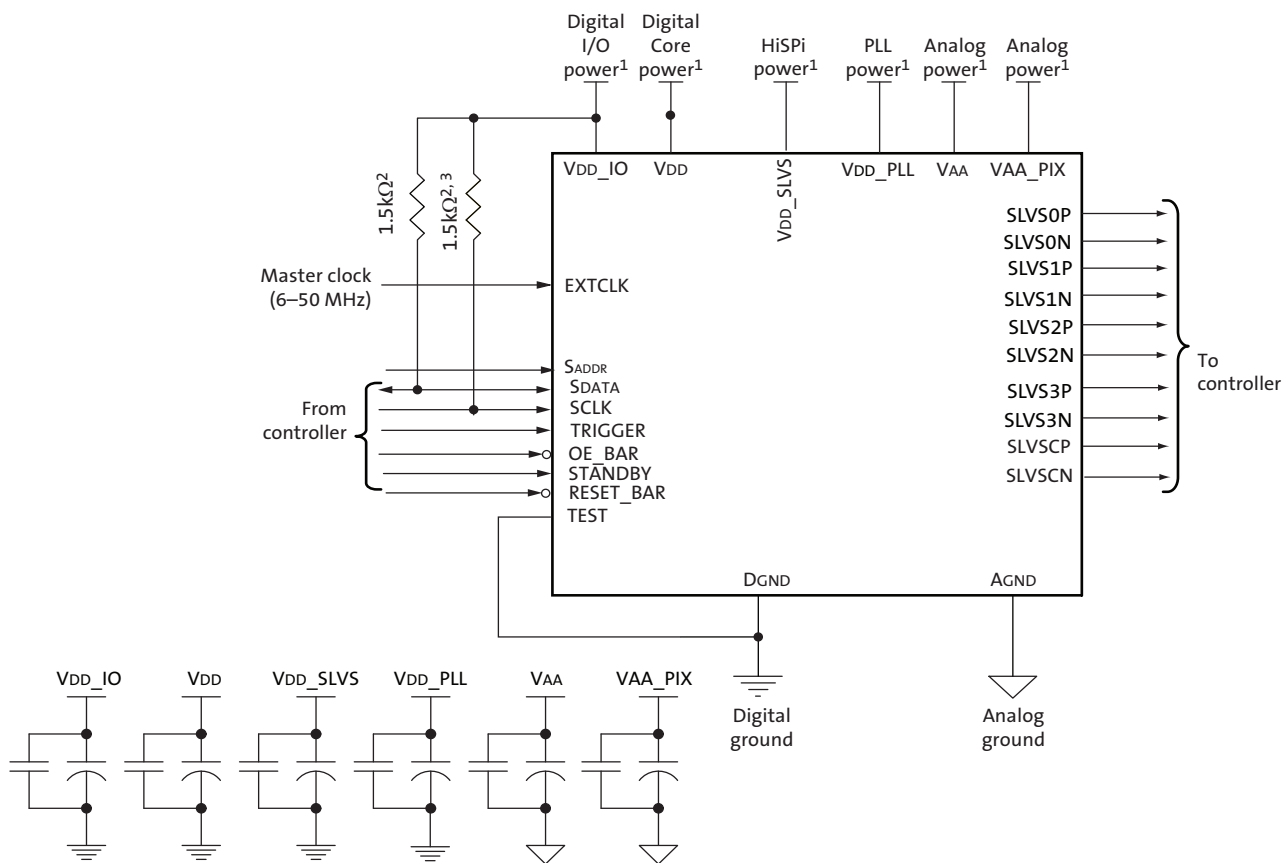
Notes: 1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on S$_{CLK}$ at all times.
4. The parallel interface output pads can be left unconnected if the serial output interface is used.
5. ON Semiconductor recommends that 0.1μF and 10μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Check the AR0132AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match V$_{DD}$_IO voltage to minimize any leakage currents.

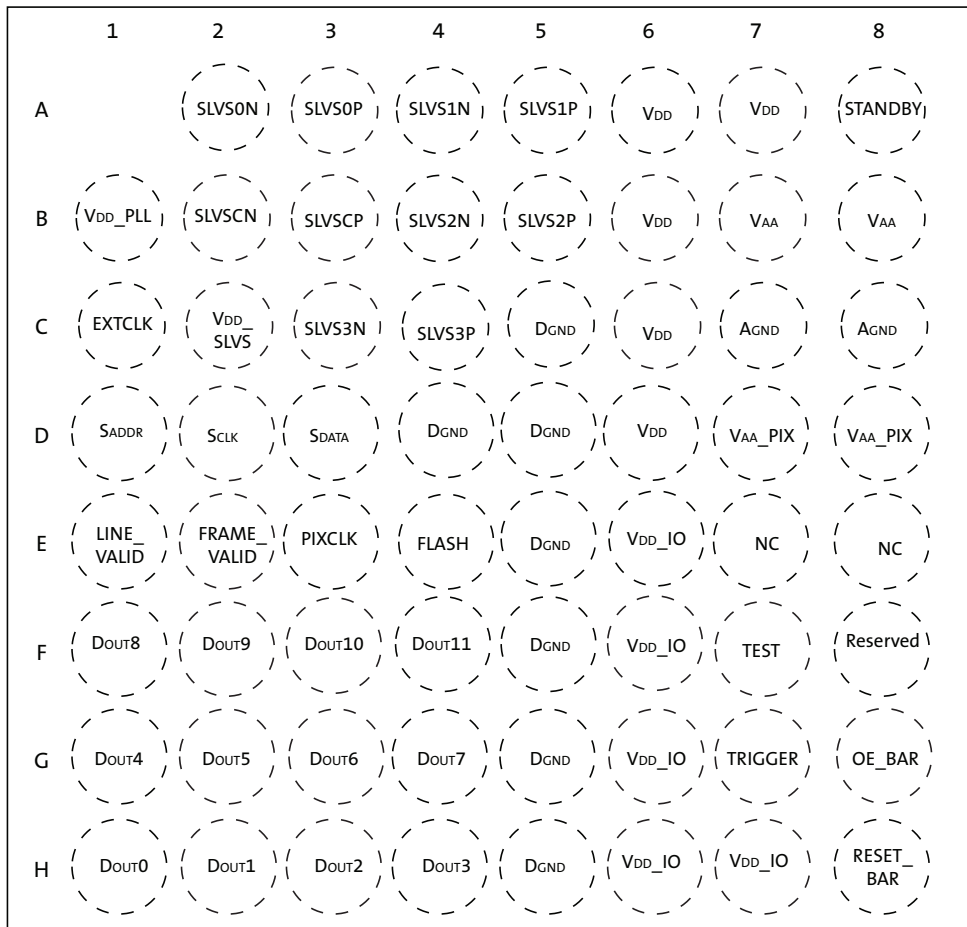**Figure 3:   Typical Configuration: Parallel Pixel Data Interface**
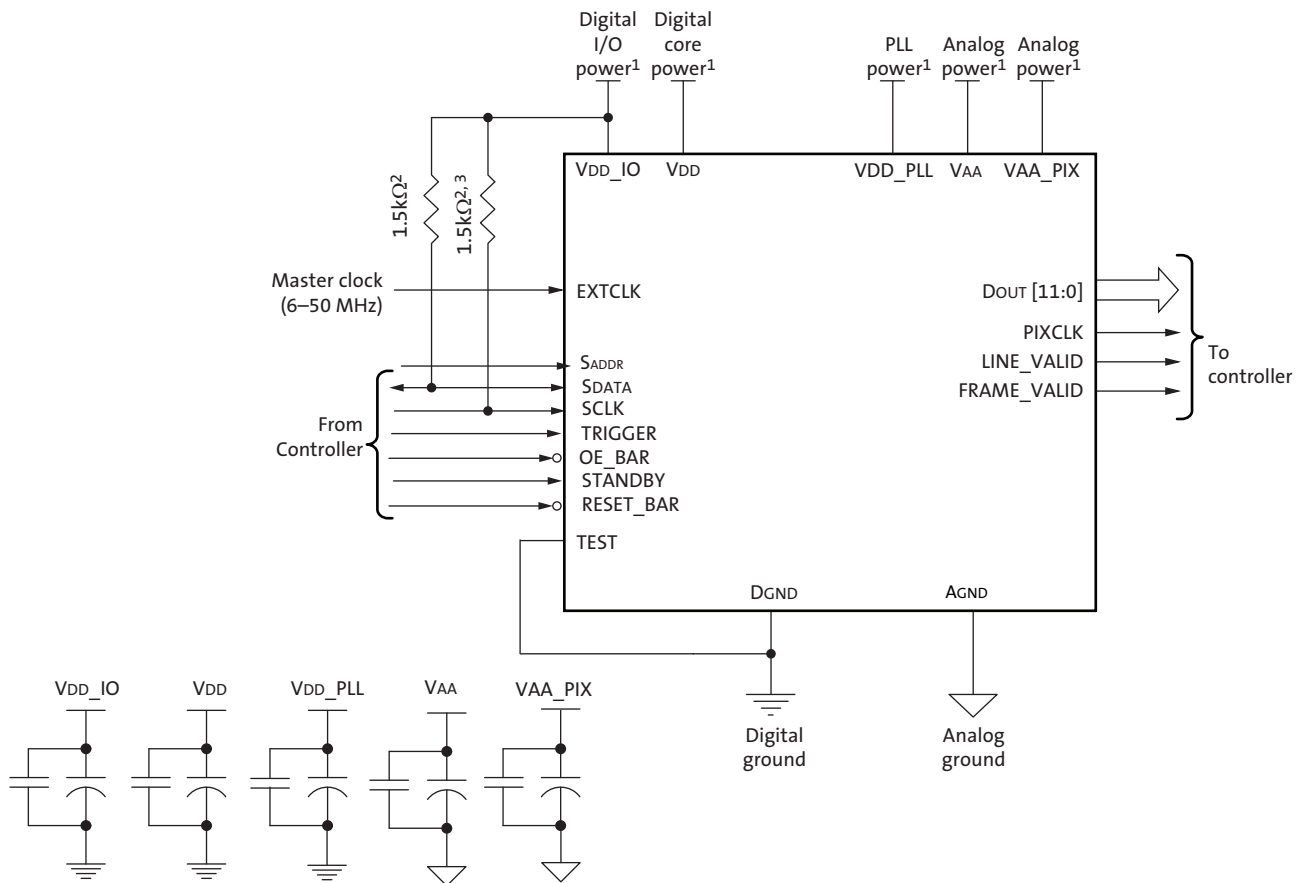
Notes: 1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on S_{CLK} at all times.
4. The serial interface output pads and $V_{DD}SLVS$ can be left unconnected if the parallel output interface is used.
5. ON Semiconductor recommends that 0.1μF and 10μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Check the AR0132AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.

Table 3:   Pin Descriptions, 9 x 9 mm, 63-ball iBGA

Name	iBGA Pin	Type	Description
SLVS0N	A2	Output	HiSPi serial data, lane 0, differential N.
SLVS0P	A3	Output	HiSPi serial data, lane 0, differential P.
SLVS1N	A4	Output	HiSPi serial data, lane 1, differential N.
SLVS1P	A5	Output	HiSPi serial data, lane 1, differential P.
STANDBY	A8	Input	Standby-mode enable pin (active HIGH).
V_{DD_PLL}	B1	Power	PLL power.
SLVSCN	B2	Output	HiSPi serial DDR clock differential N.
SLVSCP	B3	Output	HiSPi serial DDR clock differential P.
SLVS2N	B4	Output	HiSPi serial data, lane 2, differential N.
SLVS2P	B5	Output	HiSPi serial data, lane 2, differential P.
V_{AA}	B7, B8	Power	Analog power.
EXTCLK	C1	Input	External input clock.
V_{DD_SLVS}	C2	Power	HiSPi power.
SLVS3N	C3	Output	HiSPi serial data, lane 3, differential N.
SLVS3P	C4	Output	HiSPi serial data, lane 3, differential P.
D_{GND}	C5, D4, D5, E5, F5, G5, H5	Power	Digital ground.
V_{DD}	A6, A7, B6, C6, D6	Power	Digital power.
A_{GND}	C7, C8	Power	Analog ground.
S_{ADDR}	D1	Input	Two-Wire Serial address select.
S_{CLK}	D2	Input	Two-Wire Serial clock input.
S_{DATA}	D3	I/O	Two-Wire Serial data I/O.
V_{AA_PIX}	D7, D8	Power	Pixel power.
LINE_VALID	E1	Output	Asserted when D_{OUT} line data is valid.
FRAME_VALID	E2	Output	Asserted when D_{OUT} frame data is valid.
PIXCLK	E3	Output	Pixel clock out. D_{OUT} is valid on rising edge of this clock.
V_{DD_IO}	E6, F6, G6, H6, H7	Power	I/O supply power.
$D_{OUT}8$	F1	Output	Parallel pixel data output.
$D_{OUT}9$	F2	Output	Parallel pixel data output.
$D_{OUT}10$	F3	Output	Parallel pixel data output.
$D_{OUT}11$	F4	Output	Parallel pixel data output (MSB)
TEST	F7	Input.	Manufacturing test enable pin (connect to D_{GND}).
$D_{OUT}4$	G1	Output	Parallel pixel data output.
$D_{OUT}5$	G2	Output	Parallel pixel data output.
$D_{OUT}6$	G3	Output	Parallel pixel data output.
$D_{OUT}7$	G4	Output	Parallel pixel data output.
TRIGGER	G7	Input	Exposure synchronization input.
OE_BAR	G8	Input	Output enable (active LOW).
$D_{OUT}0$	H1	Output	Parallel pixel data output (LSB)
$D_{OUT}1$	H2	Output	Parallel pixel data output.
$D_{OUT}2$	H3	Output	Parallel pixel data output.
$D_{OUT}3$	H4	Output	Parallel pixel data output.
RESET_BAR	H8	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
FLASH	E4	Output	Flash control output.
NC	E7, E8		No connection.
Reserved	F8		No connection. Must be left floating for normal operation.

**Figure 4:   9 x 9 mm 63-Ball IBGA Package**

	1	2	3	4	5	6	7	8
A		SLVS0N	SLVS0P	SLVS1N	SLVS1P	V$_{DD}$	V$_{DD}$	STANDBY
B	V$_{DD}$_PLL	SLVSCN	SLVSCP	SLVS2N	SLVS2P	V$_{DD}$	V$_{AA}$	V$_{AA}$
C	EXTCLK	V$_{DD}$_SLVS	SLVS3N	SLVS3P	D$_{GND}$	V$_{DD}$	A$_{GND}$	A$_{GND}$
D	S$_{ADDR}$	S$_{CLK}$	S$_{DATA}$	D$_{GND}$	D$_{GND}$	V$_{DD}$	V$_{AA}$_PIX	V$_{AA}$_PIX
E	LINE_VALID	FRAME_VALID	PIXCLK	FLASH	D$_{GND}$	V$_{DD}$_IO	NC	NC
F	D$_{OUT}$8	D$_{OUT}$9	D$_{OUT}$10	D$_{OUT}$11	D$_{GND}$	V$_{DD}$_IO	TEST	Reserved
G	D$_{OUT}$4	D$_{OUT}$5	D$_{OUT}$6	D$_{OUT}$7	D$_{GND}$	V$_{DD}$_IO	TRIGGER	OE_BAR
H	D$_{OUT}$0	D$_{OUT}$1	D$_{OUT}$2	D$_{OUT}$3	D$_{GND}$	V$_{DD}$_IO	V$_{DD}$_IO	RESET_BAR

Top View
(Ball Down)

Note: No ball on A1 pin, 63 balls in total in actual iBGA package.

Pixel Data Format

Pixel Array Structure

The AR0132AT pixel array is configured as 1412 columns by 1028 rows, (see Figure 5). The dark pixels are optically black and are used internally to monitor black level. Of the right 96 columns, 64 are dark pixels used for row noise correction. Of the top 24 rows of pixels, 12 of the dark rows are used for black level correction. There are 1288 columns by 972 rows of optically active pixels that can be readable. While the sensor's format is 1280 x 960, the additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for monochrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

Figure 5:   Pixel Array Description
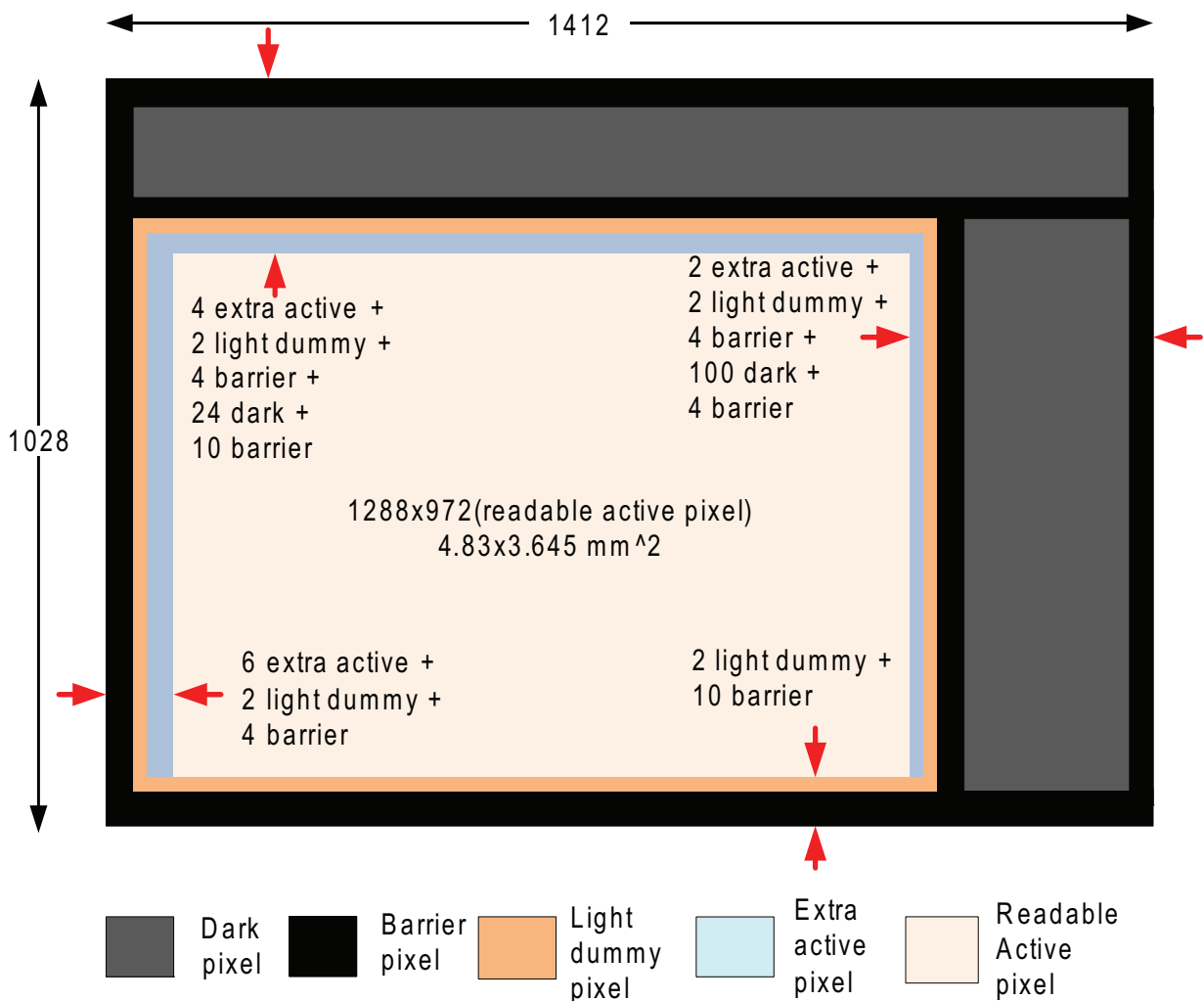
**Figure 6:   Pixel Color Pattern Detail (Top Right Corner)**
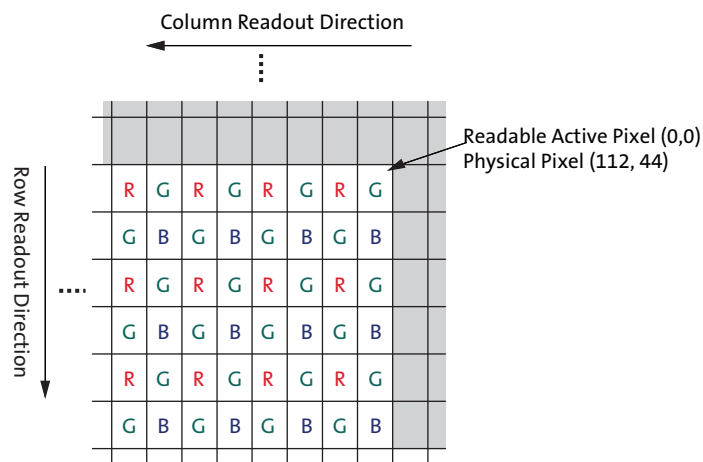
Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right 2corner (see Figure 6). This reflects the actual layout of the array on the die. Also, the first readable pixel location of the sensor in default condition is that of physical pixel address(112, 44). This first readable pixel location corresponds to the register x_addr_start(R0x3004)=0x0000 and the register y_addr_start(R0x3002)=0x0000.

The optical center of the readable pixel array is the location of the register x_addr_end(R0x3008)=643 and the register y_addr_end(R0x3006)=485.

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 7. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 7 on page 10.

Figure 7:   Imaging a Scene
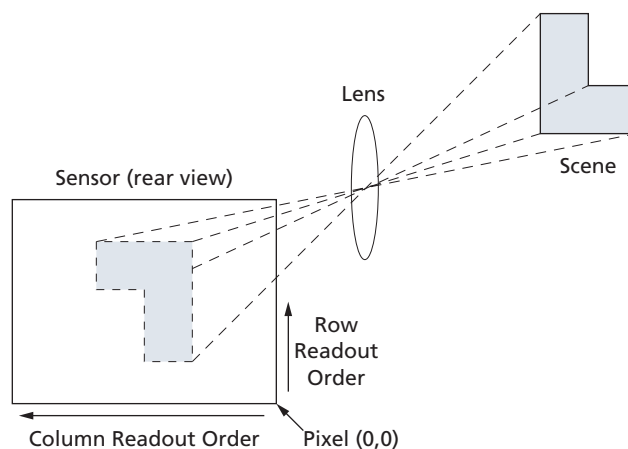
Digital Gain Control

AR0132AT supports four digital gains for the color channels: Red, Green1 (green pixels on the red rows), Green2 (green pixels on the blue rows), and Blue. Digital gain control of the AR0132AT is dependent on the configuration of the x_addr_start register. Table 4 illustrates how the digital gains are applied when x_addr_start is even or odd number.

Table 4:   Digital Gain Control for odd and even x_addr_start (R0x3004)

Pixels	x_addr_start	Gain	Register
Red	Even	red_gain	R0x305A
	Odd	green1_gain	R0x3056
Green1 (on Red rows)	Even	green1_gain	R0x3056
	Odd	red_gain	R0x305A
Green2 (on Blue rows)	Even	green2_gain	R0x305C
	Odd	blue_gain	R0x3058
Blue	Even	blue_gain	R0x3058
	Odd	green2_gain	R0x305C

Output Data Format

The AR0132AT image data is read out in a progressive scan. Valid image data is surrounded by horizontal and vertical blanking (see Figure 8). The amount of horizontal row time (in clocks) is programmable through R0x300C. The amount of vertical frame time (in rows) is programmable through R0x300A. LINE_VALID (LV) is HIGH during the shaded region of Figure 8. Optional Embedded Register setup information and Histogram statistics information are available in first two and last row of image data.

**Figure 8: Spatial Illustration of Image Readout**
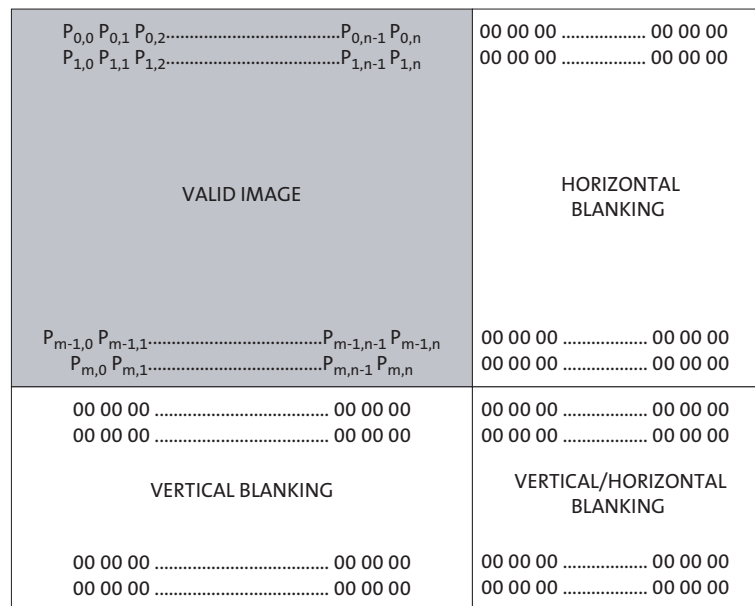
Readout Sequence

Typically, the readout window is set to a region including only active pixels. The user has the option of reading out dark regions of the array, but if this is done, consideration must be given to how the sensor reads the dark regions for its own purposes.

Parallel Output Data Timing

The output images are divided into frames, which are further divided into lines. By default, the sensor produces 968 rows of 1284 columns each. The FRAME_VALID (FV) and LINE_VALID (LV) signals indicate the boundaries between frames and lines, respectively. PIXCLK can be used as a clock to latch the data. For each PIXCLK cycle, with respect to the falling edge, one 12-bit pixel datum outputs on the DOUT pins. When both FV and LV are asserted, the pixel is valid. PIXCLK cycles that occur when FV is deasserted are called vertical blanking. PIXCLK cycles that occur when only LV is deasserted are called horizontal blanking.

Figure 9: Default Pixel Output Timing

| Vertical Blanking | Horizontal Blanking | Valid Image Data | Horizontal Blanking | Vertical Blanking |
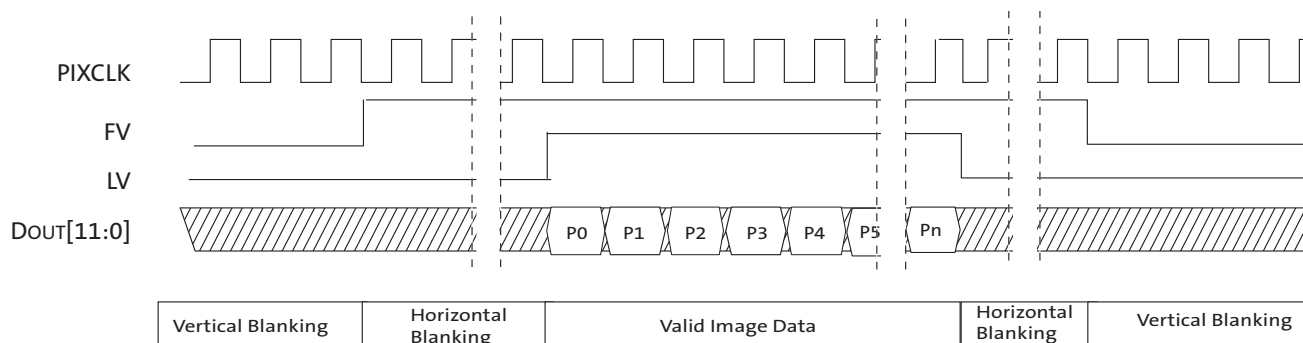
LV and FV

The timing of the FV and LV outputs is closely related to the row time and the frame time.

FV will be asserted for an integral number of row times, which will normally be equal to the height of the output image.

LV will be asserted during the valid pixels of each row. The leading edge of LV will be offset from the leading edge of FV by six PIXCLKs. Normally, LV will only be asserted if FV is asserted; this is configurable as described below.

LV Format Options

The default situation is for LV to be de-asserted when FV is de-asserted. By configuring R0x306E[1:0], the LV signal can take two different output formats. The formats for reading out four lines and two vertical blanking lines are shown in Figure 10.

**Figure 10:   LV Format Options**
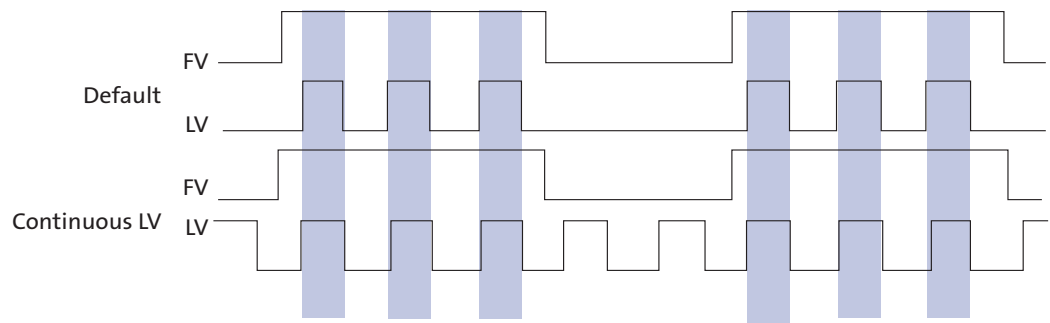
The timing of an entire frame is shown in Figure 16: "Line Timing and FRAME_VALID/ LINE_VALID Signals," on page 17.

Serial Output Data Timing

The AR0132AT also uses ON Semiconductor's High-Speed Serial Pixel Interface ("HiSPi"). The physical interface comprises differential serial data lines and a differential clock line. The protocol layer formats the data and synchronization signals separately, with Sync codes defined for active image boundaries. Figure 11 shows the configuration between the HiSPi transmitter and the receiver. There are two options for HiSPi output: SLVS or HiVCM mode selectable through register 0x306E bit 9. Setting this bit to 0 selects SLVS; setting the bit to 1 selects HiVCM.

Figure 11:   HiSPi Transmitter and Receiver Interface Block Diagram
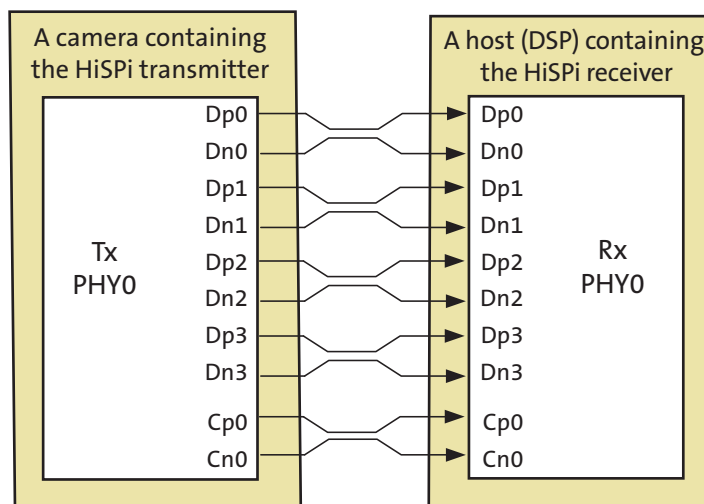
HiSPi Physical Layer

The HiSPi physical layer has four data lanes and an associated clock lane. Depending on the sensor operating mode and data rate, it can be configured to use either 2, 3, or 4 lanes. The PHY will serialize a 12- to 20-bit data word and transmit each bit of data centered on a rising edge of the clock, the second on the following falling edge of clock. Figure 12 shows bit transmission. In this example, the word is transmitted in order of MSB to LSB. The receiver latches data at the rising and falling edge of the clock.
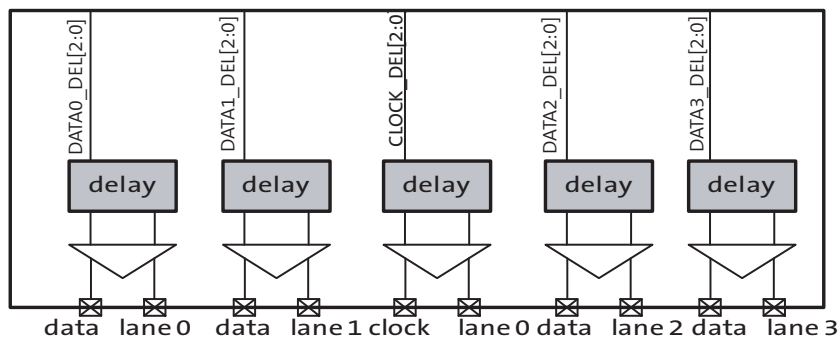
Figure 12:   Timing Diagram
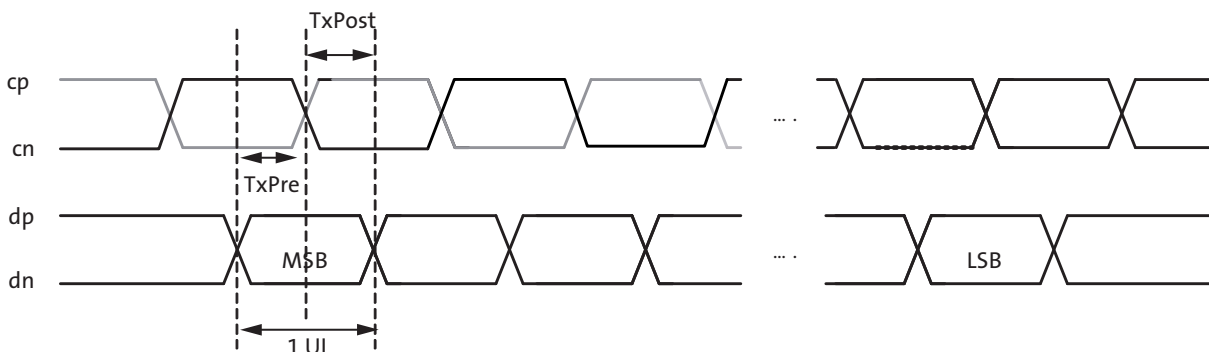
DLL Timing Adjustment

The AR0132AT includes a DLL to compensate for differences in group delay for each data lane. The DLL is connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. Once the DLL has gained phase lock, each lane can be delayed in 1/8 unit interval (UI) steps. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design.
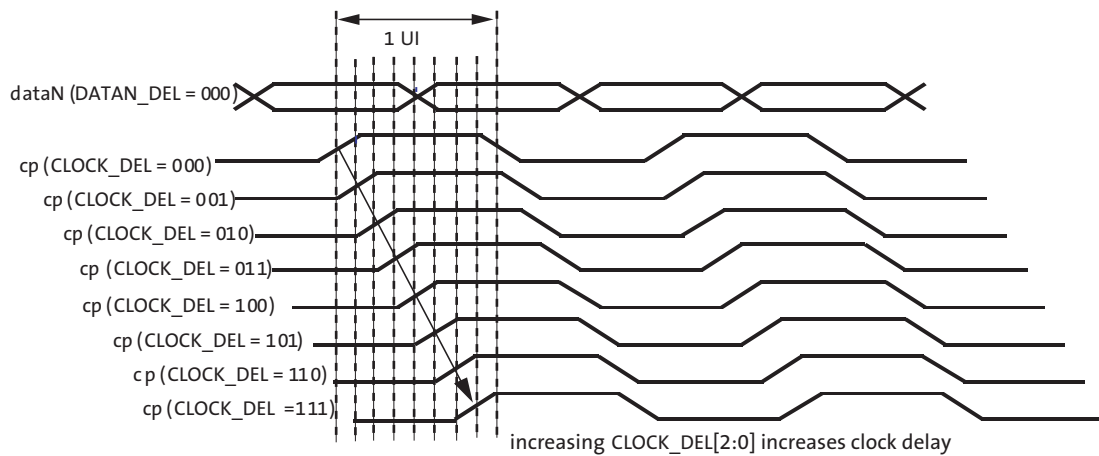
Delay compensation may be set for clock and/or data lines in the hispi_timing register R0x31C0. If the DLL timing adjustment is not required, the data and clock lane delay settings should be set to a default code of 0x000 to reduce jitter, skew, and power dissipation.

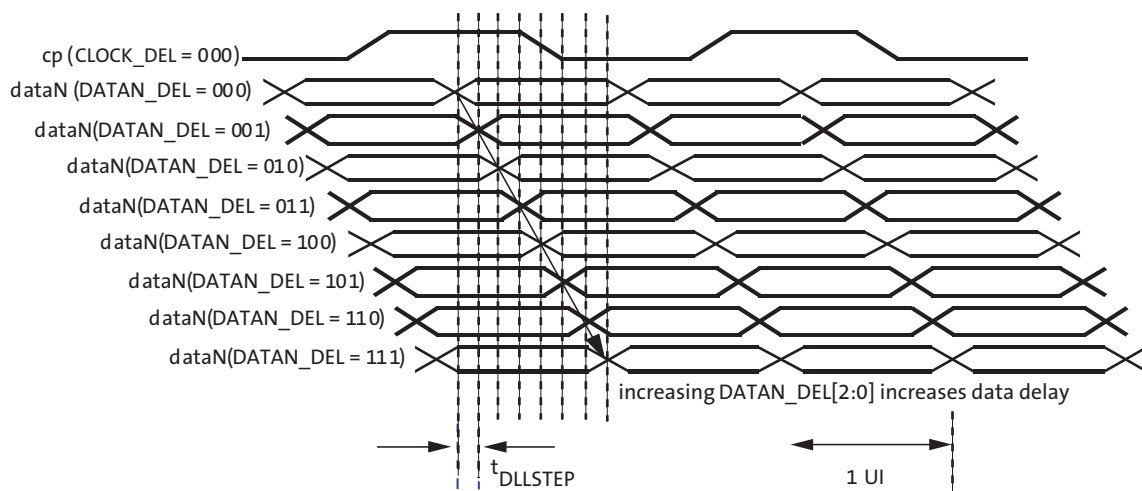**Figure 13:   Block Diagram of DLL Timing Adjustment**

Figure 14:   Delaying the Clock with Respect to Data

dataN (DATAN_DEL = 000)
cp (CLOCK_DEL = 000)
cp (CLOCK_DEL = 001)
cp (CLOCK_DEL = 010)
cp (CLOCK_DEL = 011)
cp (CLOCK_DEL = 100)
cp (CLOCK_DEL = 101)
c p (CLOCK_DEL = 110)
cp (CLOCK_DEL =111)

1 UI

increasing CLOCK_DEL[2:0] increases clock delay

Figure 15:   Delaying Data with Respect to the Clock

cp (CLOCK_DEL = 000)
dataN (DATAN_DEL = 000)
dataN (DATAN_DEL = 001)
dataN (DATAN_DEL = 010)
dataN (DATAN_DEL = 011)
dataN (DATAN_DEL = 100)
dataN (DATAN_DEL = 101)
dataN (DATAN_DEL = 110)
dataN (DATAN_DEL = 111)

increasing DATAN_DEL[2:0] increases data delay

$t_{DLLSTEP}$

1 UI

HiSPi Protocol Layer

> The HiSPi protocol is described the HiSPi Protocol Specification document. Contact your local Field Applications Engineer or sales representative to get a copy.

Frame Time

The pixel clock (PIXCLK) represents the time needed to sample 1 pixel from the array. The sensor outputs data at the maximum rate of 1 pixel per PIXCLK. One row time (t_{ROW}) is the period from the first pixel output in a row to the first pixel output in the next row. The row time and frame time are defined by equations in Table 5.

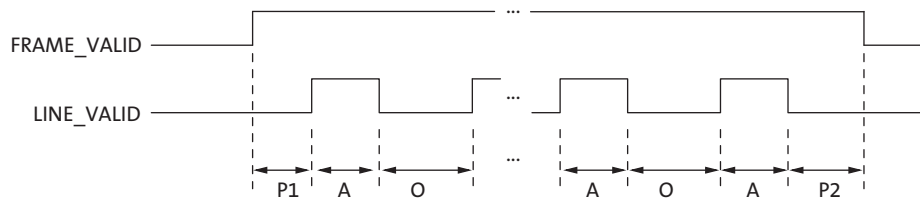**Figure 16: Line Timing and FRAME_VALID/LINE_VALID Signals**

Table 5: Frame Time (Example Based on 1280 x 960, 45 Frames Per Second)

Parameter	Name	Equation	Default Timing at 74.25 MHz
A	Active data time	Context A: R0x3008 - R0x3004 + 1 Context B: R0x308E - R0x308A + 1	1280 pixel clocks = 17.23μs
P1	Frame start blanking	6 (fixed)	6 pixel clocks = 0.08μs
P2	Frame end blanking	6 (fixed)	6 pixel clocks = 0.08μs
Q	Horizontal blanking	R0x300C - A	370 pixel clocks = 4.98μs
A+Q (t_{ROW})	Line (Row) time	R0x300C	1650 pixel clocks = 22.22μs
V	Vertical blanking	Context A: (R0x300A-(R0x3006-R0x3002+1)) x (A + Q) Context B: ((R0x30AA-(R0x3090-R0x308C+1)) x (A + Q)	49,500 pixel clocks = 666.66μs
Nrows x (A + Q)	Frame valid time	Context A: ((R0x3006-R0x3002+1)*(A+Q))-Q+P1+P2 Context B: ((R0x3090-R0x308C+1)*(A+Q))-Q+P1+P2	1,584,000 pixel clocks = 21.33ms
F	Total frame time	V + (N rows x (A + Q))	1,633,500 pixel clocks = 22.22ms

Sensor timing is shown in terms of pixel clock cycles (see Figure 8 on page 12). The recommended pixel clock frequency is 74.25 MHz. The vertical blanking and the total frame time equations assume that the integration time (coarse integration time plus fine integration time) is less than the number of active lines plus the blanking lines:

Window Height + Vertical Blanking   (EQ 1)

If this is not the case, the number of integration lines must be used instead to determine the frame time, (see Table 6). In this example, it is assumed that the coarse integration time control is programmed with 2000 rows and the fine integration time total is zero.

For master mode, if the integration time registers exceed the total readout time, then the vertical blanking time is internally extended automatically to adjust for the additional integration time required. This extended value is **not** written back to the frame_length_lines register. The frame_length_lines register can be used to adjust frame-to-frame readout time. This register does not affect the exposure time but it may extend the readout time.

Table 6: **Frame Time: Long Integration Time**

Parameter	Name	Equation (Number of Pixel Clock Cycles)	Default Timing at 74.25 MHz
F'	Total frame time (long integration time)	Context A: (R0x3012 x (A + Q)) + R0x3014 + P1 + P2 Context B: (R0x3016 x (A + Q)) + V R0x3018 + P1 + P2	3,300,012 pixel clocks = 44.44ms

Note: The AR0132AT uses column parallel analog-digital converters; thus short line timing is not possible. The minimum total line time is 1650 columns (horizontal width + horizontal blanking). The minimum horizontal blanking is 370.

Exposure

Total integration time is the result of Coarse_Integration_Time and Fine_Integration_-Time registers in Linear mode and is the result of Coarse_Integration_Time in HDR mode, and it depends also on whether manual or automatic exposure is selected.

The actual total integration time, t_{INT} is defined as:

$$t_{INT} = t_{INTCoarse} - 410 - t_{INTFine} \qquad\qquad (EQ\ 2)$$

= (number_of_lines_of_integration x line_time) - ((410 + number_of_pixels_of_integration) x pixel_time)

where:
- Number of Lines of Integration (Auto Exposure Control: Enabled)
  When automatic exposure control (AEC) is enabled, the number of lines of integration may vary from frame to frame, with the limits controlled by R0x311E (minimum auto exposure time) and R0x311C (maximum auto exposure time).
- Number of Lines of Integration (Auto Exposure Control: Disabled)
  If AEC is disabled, the number of lines of integration equals the value in R0x3012 (context A) or R0x3016 (context B).
- Number of Pixels of Integration
  The number of fine integration time pixels is independent of AEC mode (enabled or disabled):
  - Context A: the number of pixels of integration equals the value in R0x3014.
  - Context B: the number of pixels of integration equals the value in R0x3018.
 - where < Fine_Integration_Time < (Line_Length_Pck - 545) in linear mode.

Typically, the value of the Coarse_Integration_Time register is limited to the number of lines per frame (which includes vertical blanking lines), such that the frame rate is not affected by the integration time. For more information on coarse and fine integration time settings limits, please refer to the Register Reference document.

Note: In HDR mode, there are specific limitations on coarse_integration_time due to the number of line buffers available. Please refer to the section called "HDR Specific Exposure Settings" on page 21.

High Dynamic Range Mode

By default, the sensor powers up in Linear Mode, however, the AR0132AT can be configured to run in HDR mode. The HDR scheme used is multi-exposure HDR. This allows the sensor to handle 120dB of dynamic range. The sensor also features a linear mode. In HDR mode, the sensor sequentially captures three exposures by maintaining three separate read and reset pointers that are interleaved within the rolling shutter readout. The intermediate pixel values are stored in line buffers while waiting for the three exposure values to be present. As soon as a pixel's three exposure values are available, they are combined to create a linearized 20-bit value for each pixel's response. This 20-bit value is then optionally compressed back to a 12- or 14-bit value for output. For 14-bit mode, the compressing is lossless. In 12-bit mode, there is minimal data loss. Figure 17 shows the HDR data compression:

Figure 17:   HDR Data Compression
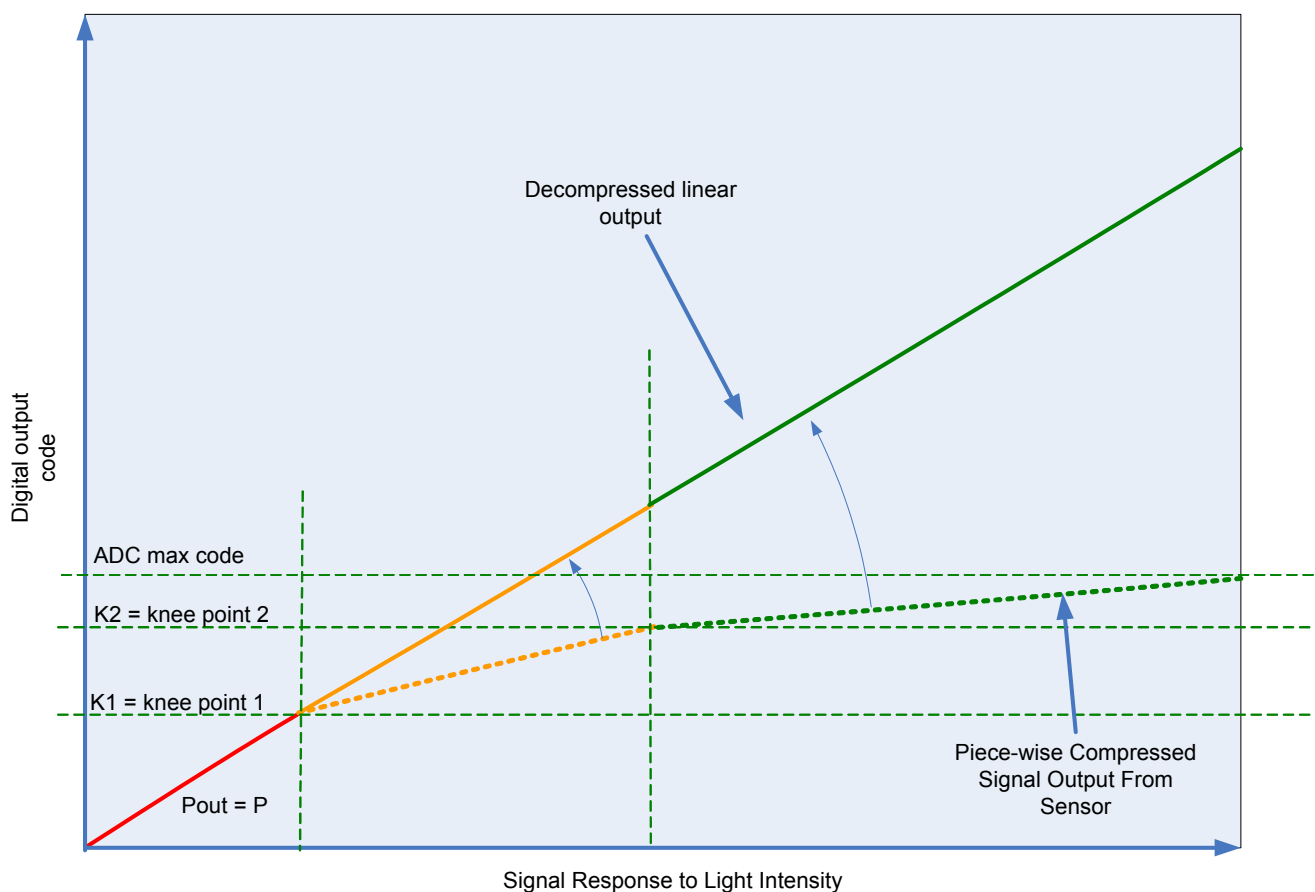
The HDR mode is selected when Operation_Mode_Ctrl, R0x3082[1:0] = 0. Further controls on exposure time limits and compressing are controlled by R0x3082[5:2] and R0x31D0. More details can be found in the AR0132AT Register Reference.

In HDR mode, when compression is used, there are two types of knee-points: (i) T1/T2 and T2/T3 capture knee-points and (ii) POUT and POUT2 compression knee-points (Figure 17). Aligning the capture knee-points on top of the compression knee-points,

19

can avoid code losses (SNR loss) in the compression. Table 7 and Table 8 below show the knee points for the different modes. Alternatively, the sensor automatically reports the knee points and can be read directly from registers R0x319A and R0x319C.

Table 7:   **Knee Points for Compression to 14 Bits**

T1/T2 Exposure Ratio (R1) R0x3082[3:2]	P1	P_{OUT1} = P1	P2	P_{OUT2} = (P2 - P1)/ R1 + P_{OUT1}	T2/T3 Exposure Ratio (R2) R0x3082[5:4]	P_{MAX}	P_{OUTMAX} = (P_{MAX} - P2)/ (R1*R2) + P_{OUT2}
4x	2^{12}	4096	2^{14}	7168	4x	2^{16}	10240
					8x	2^{17}	10752
					16x	2^{18}	11008
8x	2^{12}	4096	2^{15}	7680	4x	2^{17}	10752
					8x	2^{18}	11264
					16x	2^{19}	11520
16x	2^{12}	4096	2^{16}	7936	4x	2^{18}	11008
					8x	2^{19}	11520
					16x	2^{20}	11776

Table 8:   **Knee Points for Compression to 12 Bits**

T1/T2 Exposure Ratio (R1) R0x3082[3:2]	P1	P_{OUT1} = P1	P2	P_{OUT2} = (P2 - P1)/ (R1* 4)+ P_{OUT1}	T2/T3 Exposure Ratio (R2) R0x3082[5:4]	P_{MAX}	P_{OUTMAX} = (P_{MAX} - P2)/ (R1*R2*4) + P_{OUT2}
4x	2^{11}	2048	2^{14}	2944	4x	2^{16}	3712
					8x	2^{17}	3840
					16x	2^{18}	3904
8x	2^{11}	2048	2^{15}	3008	4x	2^{17}	3776
					8x	2^{18}	3904
					16x	2^{19}	3968
16x	2^{11}	2048	2^{16}	3040	4x	2^{18}	3808
					8x	2^{19}	3936
					16x	2^{20}	4000

HDR Specific Exposure Settings

In HDR mode, pixel values are stored in line buffers while waiting for all 3 exposures to be available for final pixel data combination. There are 42 line buffers used to store intermediate T1 data. Due to this limitation, the maximum coarse integration time possible is equal to 42*T1/T2 lines.

For example, if R0x3082[3:2] = 2, the sensor is set to have T1/T2 ratio = 16x. Therefore the maximum number of integration lines is 42*16 = 672 lines. If coarse integration time is greater than this, the T2 integration time will stay at 42 lines. The sensor calculates the ratio internally, enabling the linearization to be performed. If companding is being used then relinearization would still follow the programmed ratio. For example, if the T1/T2 ratio was programmed to 16x but coarse integration was increased beyond 672 then one would still use the 16x relinearization formulas.

An additional limitation is the maximum number of exposure lines in relation to the frame_length_lines register. In Linear mode, as described on page 20, maximum coarse_integration_time = frame_length_lines - 1. However in HDR mode, since the coarse integration time register controls T1, the max coarse_integration time is frame_length_lines - 45.

Putting the two criteria listed above together, it can be summarized as follows:

$$maximum\ coarse\_integration\_time\ =\ minimum(42 \times T1/T2,\ frame\_length\_lines - 45) \qquad \text{(EQ 3)}$$

In HDR mode, subline integration is not utilized. As such, fine integration time register changes will have no effect on the image.

There is also a limitation of the minimum number of exposure lines that can be used. This is summarized in the following formula:

$$minimum\ coarse\_integration\_time\ =\ (0.5)*(T1/T2)*(T2/T3) \qquad \text{(EQ 4)}$$

Due to limitation on the internal floating point calculation, the exact ratio specified by the RATIO_T2_T3 (R0x3082[5:4]) may not be achievable.

Motion Compensation

In typical multi-exposure HDR systems, motion artifacts can be created when objects move during the T1, T2 or T3 integration time. When this happens, edge artifacts can potentially be visible and might look like a ghosting effect.

To correct this feature, the AR0132AT has special 2D motion compensation circuitry that detects motion artifacts and corrects the image accordingly.

There are two motion compensation options available. One using the default HDR motion compensation feature can be enabled by setting R0x318C[14] = 1. Additional parameters are available to control the extent of motion detection and correction as per the requirements of the specific application. These can be set in R0x318C–R0x3190. The other is using the DLO method of HDR combination. When using DLO, R0x318C[14] is ignored. DLO is enabled by setting R0x3190[13] = 1. Noise filtering is enabled by setting R0x3190[14] = 1. For more information, please refer to the AR0132AT Register Reference document.

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Real-Time Context Switching

In the AR0132AT, the user may switch between two full register sets (listed in Table 9) by writing to a context switch change bit in R0x30B0[13]. This context switch will change all registers (no shadowing) at the frame start time and have the new values apply to the immediate next exposure and readout time.

Table 9:   Real-Time Context-Switch Registers

Register Description	Register Number	
	Context A	Context B
Y_Addr_Start	R0x3002	R0x308C
X_Addr_Start	R0x3004	R0x308A
Y_Addr_End	R0x3006	R0x3090
X_Addr_End	R0x3008	R0x308E
Coarse_Integration_Time	R0x3012	R0x3016
Fine_Integration_Time	R0x3014	R0x3018
Y_Odd_Inc	R0x30A6	R0x30A8
Column Gain	R0x30B0[5:4]	R0x30B0[9:8]
Green1_Gain (GreenR)	R0x3056	R0x30BC
Blue_Gain	R0x3058	R0x30BE
Red_Gain	R0x305A	R0x30C0
Green2_Gain (GreenB)	R0x305C	R0x30C2
Global_Gain	R0x305E	R0x30C4
Frame_Length_Lines	R0x300A	R0x30AA
Digital_Binning	R0x3032[1:0]	R0x3032[5:4]
Operation_Mode_Ctrl	0x3082	0x3084

Features

See the AR0132AT Register Reference for additional details.

Reset

The AR0132AT may be reset by using RESET_BAR (active LOW) or the reset register.

Hard Reset of Logic

The RESET_BAR pin can be connected to an external RC circuit for simplicity. The recommended RC circuit uses a 10kΩ resistor and a 0.1μF capacitor. The rise time for the RC circuit is 1μs maximum.

Soft Reset of Logic

Soft reset of logic is controlled by the R0x301A Reset register. Bit 0 is used to reset the digital logic of the sensor while preserving the existing two-wire serial interface configuration. Furthermore, by asserting the soft reset, the sensor aborts the current frame it is processing and starts a new frame. This bit is a self-resetting bit and also returns to "0" during two-wire serial interface reads.

Clocks

The AR0132AT requires one clock input (EXTCLK).

PLL-Generated Master Clock

The PLL contains a prescaler to divide the input clock applied on EXTCLK, a VCO to multiply the prescaler output, and two divider stages to generate the output clock. The clocking structure is shown in Figure 18. PLL control registers can be programmed to generate desired master clock frequency.

Note: The PLL control registers must be programmed while the sensor is in the software Standby state. The effect of programming the PLL divisors while the sensor is in the streaming state is undefined.

Figure 18:   PLL-Generated Master Clock PLL Setup
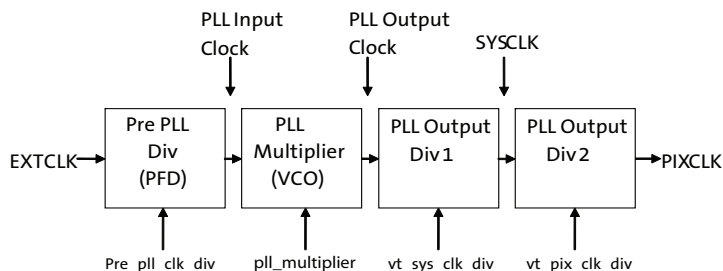
The PLL is enabled by default on the AR0132AT.

To configure and use the PLL:

1. Bring the AR0132AT up as normal; make sure that f_{EXTCLK} is between 6 and 50MHz and ensure the sensor is in software standby (R0x301A-B[2]= 0). PLL control registers must be set in software standby.
2. Set pll_multiplier, pre_pll_clk_div, vt_sys_clk_siv, and vt_pix_clk_div based on the desired input (f_{EXTCLK}) and output (f_{PIXCLK}) frequencies. Determine the M, N, P1, and P2 values to achieve the desired f_{PIXCLK} using this formula:

$f_{PIXCLK}= (f_{EXTCLK} \times M) / (N \times P1 \text{ x } P2)$
where
M = PLL_Multiplier
N = Pre_PLL_Clk_Div
P1 = Vt_Sys_Clk_Div
P2 = Vt_PIX_Clk_Div

3. Wait 1ms to ensure that the VCO has locked.
4. Set R0x301A[2]=1 to enable streaming and to switch from EXTCLK to the PLL-generated clock.

Notes: **1.** The PLL can be bypassed at any time (sensor will run directly off EXTCLK) by setting R0x30B0[14]=1. However, only the parallel data interface is supported with the PLL bypassed. The PLL is always bypassed in software standby mode. To disable the PLL, the sensor must be in standby mode (R0x301A[2] = 0)

2. The following restrictions apply to the PLL tuning parameters:

$32 \leq M \leq 255$

$$1 \leq N \leq 63$$

$$P1 \ = \ 1, \ 2, \ 4, \ 6, \ 8, \ 10, \ 12, \ 14, \ 16$$

$$4 \leq P2 \leq 16$$

3. The VCO frequency, defined as $f_{VCO} \ = \ f_{EXTCLK} \times M / N$ must be within 384-768 MHz.
4. When PLL_Multiplier is odd, 2 MHz $\leq$ f_{EXTCLK} / N $\leq$ 24 MHz.
5. If using HiSPi output mode, use the following settings for P2 (Vt_Pix_Clk_Div).
   5a. If 20-bit mode (4 lanes): set P2 (R0x302A) = 5
   5b. If 12-/14-bit mode (3 lanes): set P2 (R0x302A) = 5
   5c. If 12-bit mode (2 lanes): set P2 (R0x302A) = 6
   5d. If 14-bit mode (2 lanes): set P2 (R0x302A) = 7

The user can utilize the Register Wizard tool accompanying DevWare to generate PLL settings given a supplied input clock and desired output frequency.

Spread-Spectrum Clocking

To facilitate improved EMI performance, the external clock input allows for spread spectrum sources, with no impact on image quality. Limits of the spread spectrum input clock are:
- 5% maximum clock modulation
- 35 KHz maximum modulation frequency
- Accepts triangle wave modulation, as well as sine or modified triangle modulations.

Stream/Standby Control

The sensor supports two standby modes: Hard Standby and Soft Standby. In both modes, external clock can be optionally disabled to further minimize power consumption. If this is done, then the "Power-Up Sequence" on page 51 must be followed.

Soft Standby

Soft Standby is a low power state that is controlled through register R0x301A[2]. Depending on the value of R0x301A[4], the sensor will go to standby after completion of the current frame readout (default behavior) or after the completion of the current row readout. When the sensor comes back from Soft Standby, previously written register settings are still maintained. Soft standby will not occur if the TRIGGER pin is held high.

A specific sequence needs to be followed to enter and exit from Soft Standby.

Entering Soft Standby:
1. R0x301A[12] = 1 if serial mode was used
2. Set R0x301A[2] = 0 and drive the TRIGGER pin LOW.
3. External clock can be turned off to further minimize power consumption (Optional)

Exiting Soft Standby:
1. Enable external clock if it was turned off
2. R0x301A[2] = 1 or drive the TRIGGER pin HIGH.
3. R0x301A[12] = 0 if serial mode is used

Hard Standby

Hard Standby puts the sensor in lower power state; previously written register settings are still maintained.

A specific sequence needs to be followed to enter and exit from Hard Standby.

Entering Hard Standby:
1. R0x301A[8] = 1
2. R0x301A[12] = 1 if serial mode was used
3. Assert STANDBY pin
4. External clock can be turned off to further minimize power consumption (Optional)

Exiting Hard Standby:
1. Enable external clock if it was turned off
2. De-assert STANDBY pin
3. Set R0x301A[8] = 0

Window Control

Registers x_addr_start, x_addr_end, y_addr_start, and y_addr_end control the size and starting coordinates of the image window.

The exact window height and width out of the sensor is determined by the difference between the Y address start and end registers or the X address start and end registers, respectively.

The AR0132AT allows different window sizes for context A and context B.

Blanking Control

Horizontal blank and vertical blank times are controlled by the line_length_pck and frame_length_lines registers, respectively.
- Horizontal blanking is specified in terms of pixel clocks. It is calculated by subtracting the X window size from the line_length_pck register. The minimum horizontal blanking is 370 pixel clocks.
- Vertical blanking is specified in terms of numbers of lines. It is calculated by subtracting the Y window size from the frame_length_lines register. The minimum vertical blanking is 26 lines.

The actual imager timing can be calculated using Table 5 on page 17 and Table 6 on page 18, which describe the Line Timing and FV/LV signals.

When in HDR mode, the maximum size is 1280 x 960.