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AR0330CM

1/3-inch CMOS Digital Image Sensor

ON Semiconductor®

CLCC48
CASE 848AU

ODCSP64
CASE 570BH

Description

The AR0330 from ON Semiconductor is a 1/3-inch CMOS digital image sensor with an active-pixel array of 2304 (H) × 1536 (V). It can support 3.15 Mp (2048 (H) × 1536 (V)) digital still image capture and a 1080p60 + 20% EIS (2304 (H) × 1296 (V)) digital video mode. It incorporates sophisticated on-chip camera functions such as windowing, mirroring, column and row sub-sampling modes, and snapshot modes.
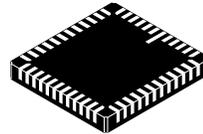
ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Table 1. KEY PERFORMANCE PARAMETERS

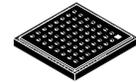| Parameter	Typical Value
Optical Format	1/3-inch (6.0 mm) Entire Array: 6.09 mm Still Image: 5.63 mm (4:3) HD Image: 5.82 mm (16:9)
Active Pixels	2304 (H) × 1536 (V): (Entire Array) 5.07mm (H) × 3.38mm (V) 2048 (H) × 1536 (V) (4:3, Still Mode) 2304 (H) × 1296 (V) (16:9, HD Mode)
Pixel Size	2.2 × 2.2 μm
Color Filter Array	RGB Bayer
Shutter Type	ERS and GRR
Input Clock Range	6–27 MHz
Output Clock Maximum	196 Mp/s (4-lane HiSPi or MIPI)
Output Video – 4-lane HiSPi	2304 × 1296 at 60 fps < 450 mW (V_{CM} 0.2 V, 198 MP/s) 2304 × 1296 at 30 fps < 300 mW (V_{CM} 0.2 V, 98 MP/s)
Responsivity	2.0 V/lux–sec
SNR_{MAX}	39 dB
Dynamic Range	69.5 dB

Supply Voltage
    Digital
    Analog
    HiSPi PHY
    HiSPi I/O (SLVS)
    HiSPi I/O (HiVCM)
    I/O/Digital
	
	1.7–1.9 V (1.8 V Nominal)
	2.7–2.9 V
	1.7–1.9 V (1.8 V Nominal)
	0.3–0.9 V (0.4 or 0.8 V Nominal)
	1.7–1.9 V (1.8 V Nominal)
	1.7–1.9 V (1.8 V Nominal) or
	2.4–3.1 V (2.8 V Nominal)

Operating Temperature (Junction) – T_J	–30°C to + 70°C
Package Options	CLCC – 11.4 mm × 11.4mm CSP – 6.28 mm × 6.65 mm Bare Die

Features

- 2.2 μm Pixel with A–Pix™ Technology
- Full HD support at 60 fps (2304 (H) × 1296 (V)) for Maximum Video Performance
- Superior Low-light Performance
- 3.4 Mp (3:2) and 3.15 Mp (4:3) Still Images
- Support for External Mechanical Shutter
- Support for External LED or Xenon Flash
- Data Interfaces: Four-lane Serial High-speed Pixel Interface (HiSPi) Differential Signaling (SLVS), Four-lane Serial MIPI Interface, or Parallel
- On-chip Phase-locked Loop (PLL) Oscillator
- Simple Two-wire Serial Interface
- Auto Black Level Calibration
- 12-to-10 Bit Output A–Law Compression
- Slave Mode for Precise Frame-rate Control and for Synchronizing Two Sensors

Applications

- 1080p High-definition Digital Video Camcorder
- Web Cameras and Video Conferencing Cameras
- Security

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
AR0330CM1C00SHAA0−DP	3 MP 1/3″ CIS	Dry Pack with Protective Film
AR0330CM1C00SHAA0−DR	3 MP 1/3″ CIS	Dry Pack without Protective Film
AR0330CM1C00SHAA0−TP	3 MP 1/3″ CIS	Tape & Reel with Protective Film
AR0330CM1C00SHKA0−CP	3 MP 1/3″ CIS	Chip Tray with Protective Film
AR0330CM1C00SHKA0−CR	3 MP 1/3″ CIS	Chip Tray without Protective Film
AR0330CM1C12SHAA0−DP	3 MP 1/3″ CIS	Dry Pack with Protective Film
AR0330CM1C12SHAA0−DR	3 MP 1/3″ CIS	Dry Pack without Protective Film
AR0330CM1C12SHKA0−CP	3 MP 1/3″ CIS	Chip Tray with Protective Film
AR0330CM1C12SHKA0−CR	3 MP 1/3″ CIS	Chip Tray without Protective Film
AR0330CM1C21SHKA0−CP	3 MP 1/3″ CIS	Chip Tray with Protective Film
AR0330CM1C21SHKA0−CR	3 MP 1/3″ CIS	Chip Tray without Protective Film

GENERAL DESCRIPTION

The AR0330 can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 2304×1296 image at 60 frames per second (fps). The sensor outputs 10- or 12-bit raw data, using either the parallel or serial (HiSPi, MIPI) output ports.

FUNCTIONAL OVERVIEW

The AR0330 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can generate all internal clocks from a single master input clock running between 6 and 27 MHz. The maximum output pixel rate is 196 Mp/s using a 4-lane HiSPi or MIPI serial interface and 98 Mp/s using the parallel interface.
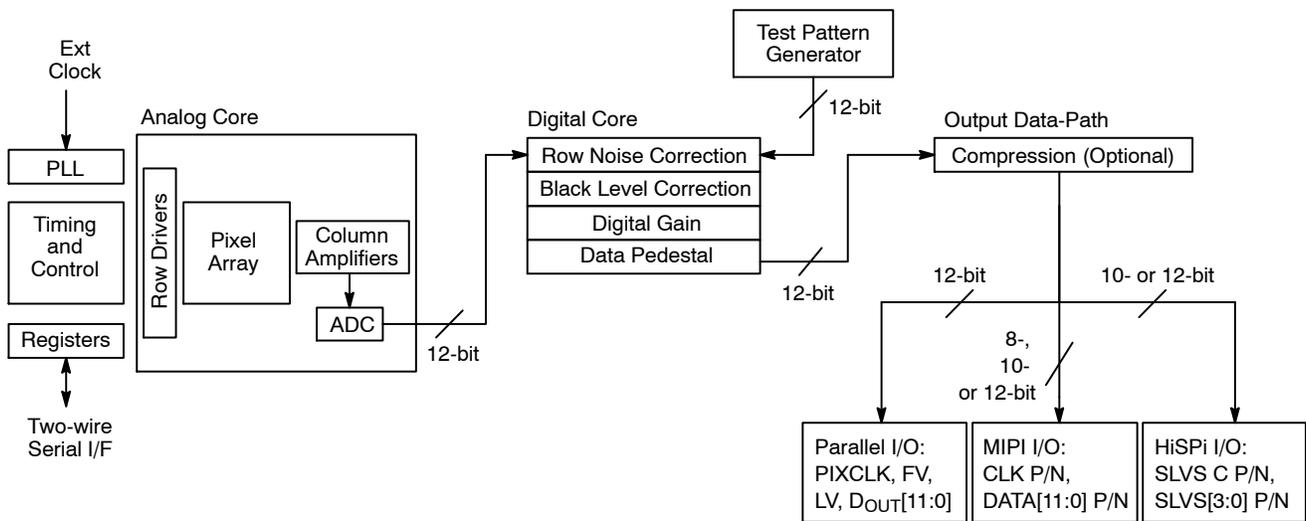

Figure 1. Block Diagram

User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 3.4 Mp active-pixel sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the signal from the column is amplified in a column amplifier and then digitized in an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain).

AR0330CM

WORKING MODES

The AR0330 sensor working modes are specified from the following aspect ratios:

Table 3. AVAILABLE ASPECT RATIOS IN THE AR0330 SENSOR

Aspect Ratio		Sensor Array Usage
3:2	Still Format #1	2256 (H) × 1504 (V)
4:3	Still Format #2	2048 (H) × 1536 (V)
16:10	Still Format #3	2256 (H) × 1440 (V)
16:9	HD Format	2304 (H) × 1296 (V)

The AR0330 supports the following working modes. To operate the sensor at full speed (196 Mp/s) the sensor must use the 4-lane HiSPi or MIPI interface. The sensor will operate at half-speed (98 Mp/s) when using the parallel interface.

Table 4. AVAILABLE WORKING MODES IN THE AR0330 SENSOR

Mode	Aspect Ratio	Active Readout Window	Sensor Output Resolution	FPS (4-lane MIPI/ HiSPi Interface)	FPS (Parallel Interface)	Subsampling	FOV
1080p + EIS	16:9	2304 × 1296	2304 × 1296	60	N/A	–	100%
				30	30	–	100%
3M Still	4:3	2048 × 1536	2048 × 1536	30	25	–	100%
	3:2	2256 × 1504	2256 × 1504	30	25	–	100%
WVGA + EIS	16:9	2304 × 1296	1152 × 648	60	60	2×2	100%
WVGA + EIS Slow-motion	16:9	2304 × 1296	1152 × 648	120	N/A	2×2	100%
VGA Video	16:10	2256 × 1440	752 × 480	60	60	3×3	96%
VGA Video Slow-motion	16:10	2256 × 1440	752 × 480	215	107	3×3	96%

HiSPi POWER SUPPLY CONNECTIONS

The HiSPi interface requires two power supplies. The V_{DD}_HiSPi powers the digital logic while the V_{DD}_HiSPi_TX powers the output drivers. The digital logic supply is a nominal 1.8 V and ranges from 1.7 to 1.9 V. The HiSPi drivers can receive a supply voltage of 0.4 to 0.8 V or 1.7 to 1.9 V.
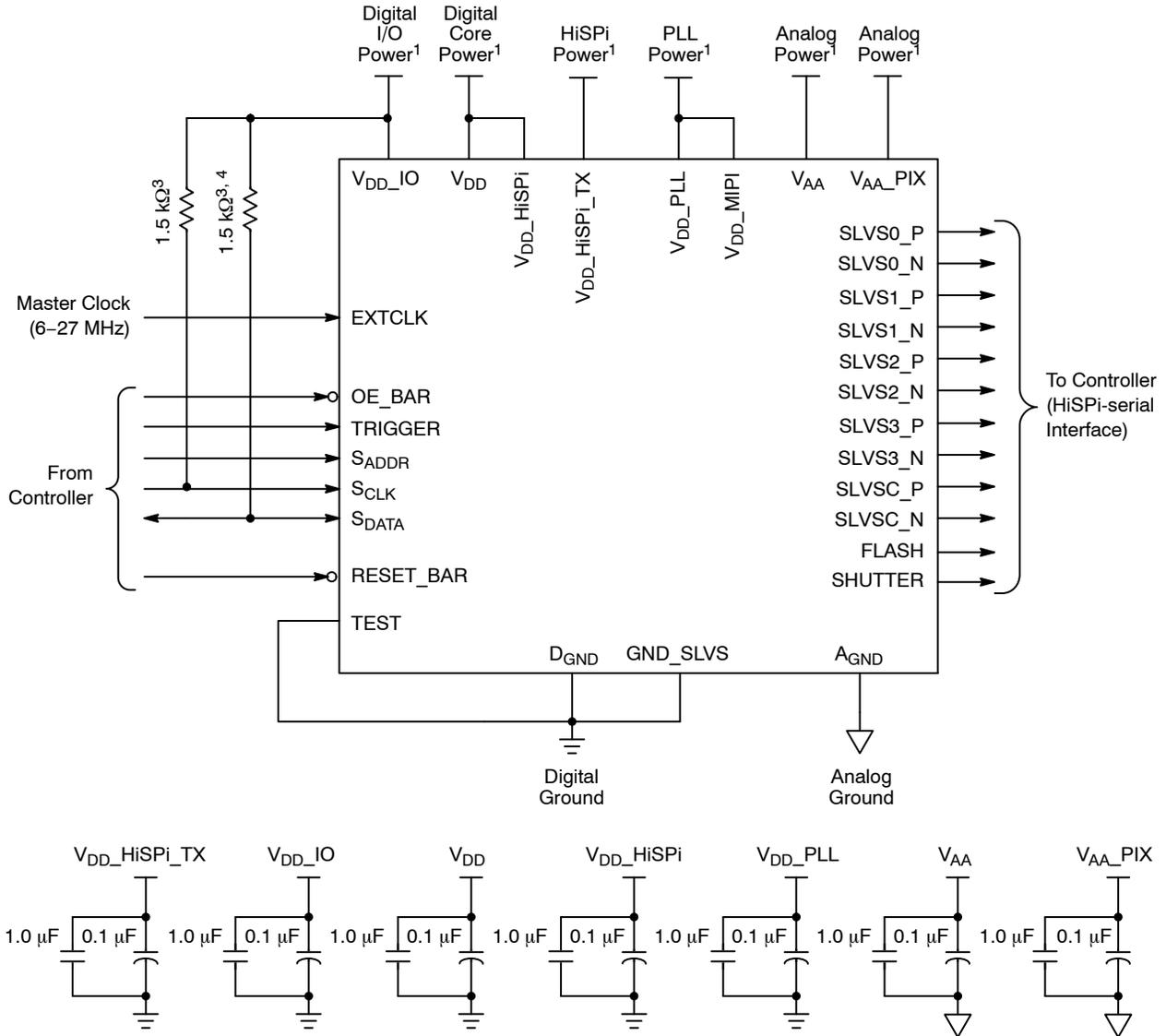
The common mode voltage is derived as half of the V_{DD}_HiSPi _TX supply. Two settings are available for the output common mode voltage:

1. SLVS Mode:
   The V_{DD}_HiSPi_Tx supply must be in the range of 0.4 to 0.8 V and the high_vcm register bit R0x306E[9] must be set to "0".
   The output common mode voltage will be in the range of 0.2 to 0.4 V.
2. HiVCM Mode:
   The V_{DD}_HiSPi_Tx supply must be in the range of 1.7 to 1.9 V and the high_vcm register bit R0x306E[9] must be set to "1". The output common mode voltage will be in the range of 0.76 to 1.07 V.

Two prior naming conventions have also been used with the V_{DD}_HiSPi and V_{DD}_HiSPi_TX pins:

1. Digital logic supply was named V_{DD}_SLVS while the driver supply was named V_{DD}_SLVS_TX.
2. Digital logic supply was named V_{DD}_PHY while the driver supply was named V_{DD}_SLVS.

TYPICAL CONFIGURATIONS

Digital I/O Power[1] Digital Core Power[1] HiSPi Power[1] PLL Power[1] Analog Power[1] Analog Power[1]

$1.5\ k\Omega^3$ $1.5\ k\Omega^{3,\ 4}$

V_{DD_IO} V_{DD} V_{DD_HiSPi} $V_{DD\_HiSPi\_TX}$ V_{DD_PLL} V_{DD_MIPI} V_{AA} V_{AA_PIX}

Master Clock (6–27 MHz) → EXTCLK

From Controller:
OE_BAR
TRIGGER
S_{ADDR}
S_{CLK}
S_{DATA}
RESET_BAR
TEST

SLVS0_P
SLVS0_N
SLVS1_P
SLVS1_N
SLVS2_P
SLVS2_N
SLVS3_P
SLVS3_N
SLVSC_P
SLVSC_N
FLASH
SHUTTER

To Controller (HiSPi-serial Interface)

D_{GND} GND_SLVS A_{GND}

Digital Ground Analog Ground

$V_{DD\_HiSPi\_TX}$ 1.0 μF 0.1 μF
V_{DD_IO} 1.0 μF 0.1 μF
V_{DD} 1.0 μF 0.1 μF
V_{DD_HiSPi} 1.0 μF 0.1 μF
V_{DD_PLL} 1.0 μF 0.1 μF
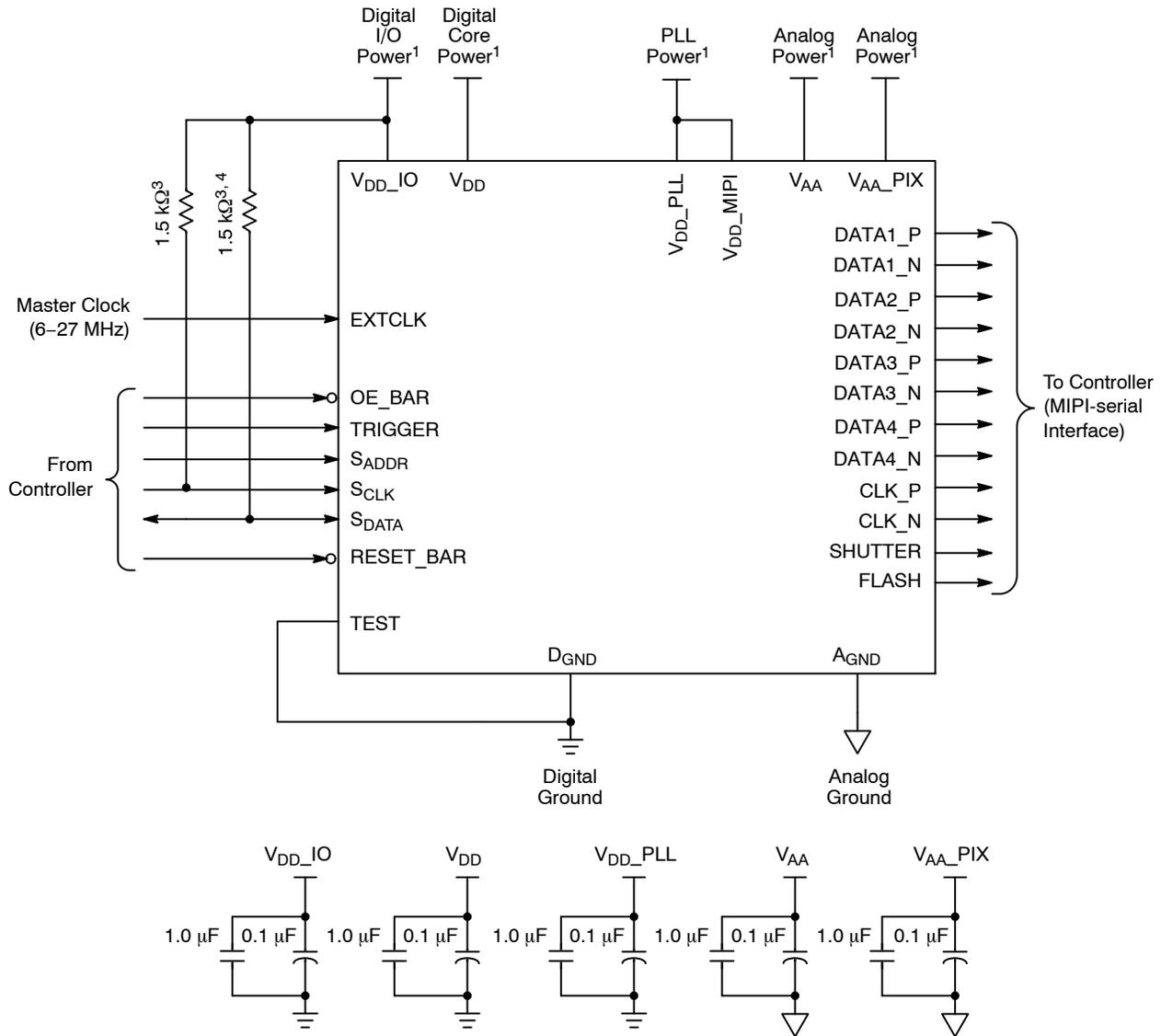V_{AA} 1.0 μF 0.1 μF
V_{AA_PIX} 1.0 μF 0.1 μF

Notes:
1. All power supplies must be adequately decoupled. ON Semiconductor recommends having 1.0 μF and 0.1 μF decoupling capacitors for every power supply. If space is a concern, then priority must be given in the following order: V_{AA}, V_{AA_PIX}, V_{DD_PLL}, V_{DD_IO}, and V_{DD}. Actual values and results may vary depending on layout and design considerations.
2. To allow for space constraints, ON Semiconductor recommends having 0.1 μF decoupling capacitor inside the module as close to the pads as possible. In addition, place a 10 μF capacitor for each supply off-module but close to each supply.
3. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
4. This pull-up resistor is not required if the controller drives a valid logic level on S_{CLK} at all times.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. TEST pin should be tied to D_{GND}.
7. Set High_VCM (R0x306E[9]) to 0 (default) to use the $V_{DD\_HiSPi\_TX}$ in the range of 0.4–0.8 V. Set High_VCM to 1 to use a range of 1.7–1.9 V.
8. The package pins or die pads used for the MIPI data and clock as well as the parallel interface must be left floating.
9. The V_{DD_MIPI} package pin and sensor die pad should be connected to a 2.8 V supply as V_{DD_MIPI} is tied to the V_{DD_PLL} supply both in the package routing and also within the sensor die itself.
10. If the SHUTTER or FLASH pins or pads are not used, then they must be left floating.
11. If the TRIGGER pin or pad is not used then it should be tied to D_{GND}.
12. The GND_SLVS pad must be tied to D_{GND}. It is connected this way in the CLCC and CSP packages.

Figure 2. Serial 4-lane HiSPi Interface

AR0330CM

Digital I/O Power[1] Digital Core Power[1] PLL Power[1] Analog Power[1] Analog Power[1]

1.5 kΩ[3]   1.5 kΩ[3, 4]

V_{DD_IO} V_{DD} V_{DD_PLL} V_{DD_MIPI} V_{AA} V_{AA_PIX}

Master Clock (6–27 MHz) → EXTCLK

From Controller
- OE_BAR
- TRIGGER
- S_{ADDR}
- S_{CLK}
- S_{DATA}
- RESET_BAR

TEST

D_{GND} A_{GND}

DATA1_P
DATA1_N
DATA2_P
DATA2_N
DATA3_P
DATA3_N
DATA4_P
DATA4_N
CLK_P
CLK_N
SHUTTER
FLASH

To Controller (MIPI-serial Interface)

Digital Ground   Analog Ground

V_{DD_IO} V_{DD} V_{DD_PLL} V_{AA} V_{AA_PIX}

1.0 μF 0.1 μF   1.0 μF 0.1 μF   1.0 μF 0.1 μF   1.0 μF 0.1 μF   1.0 μF 0.1 μF
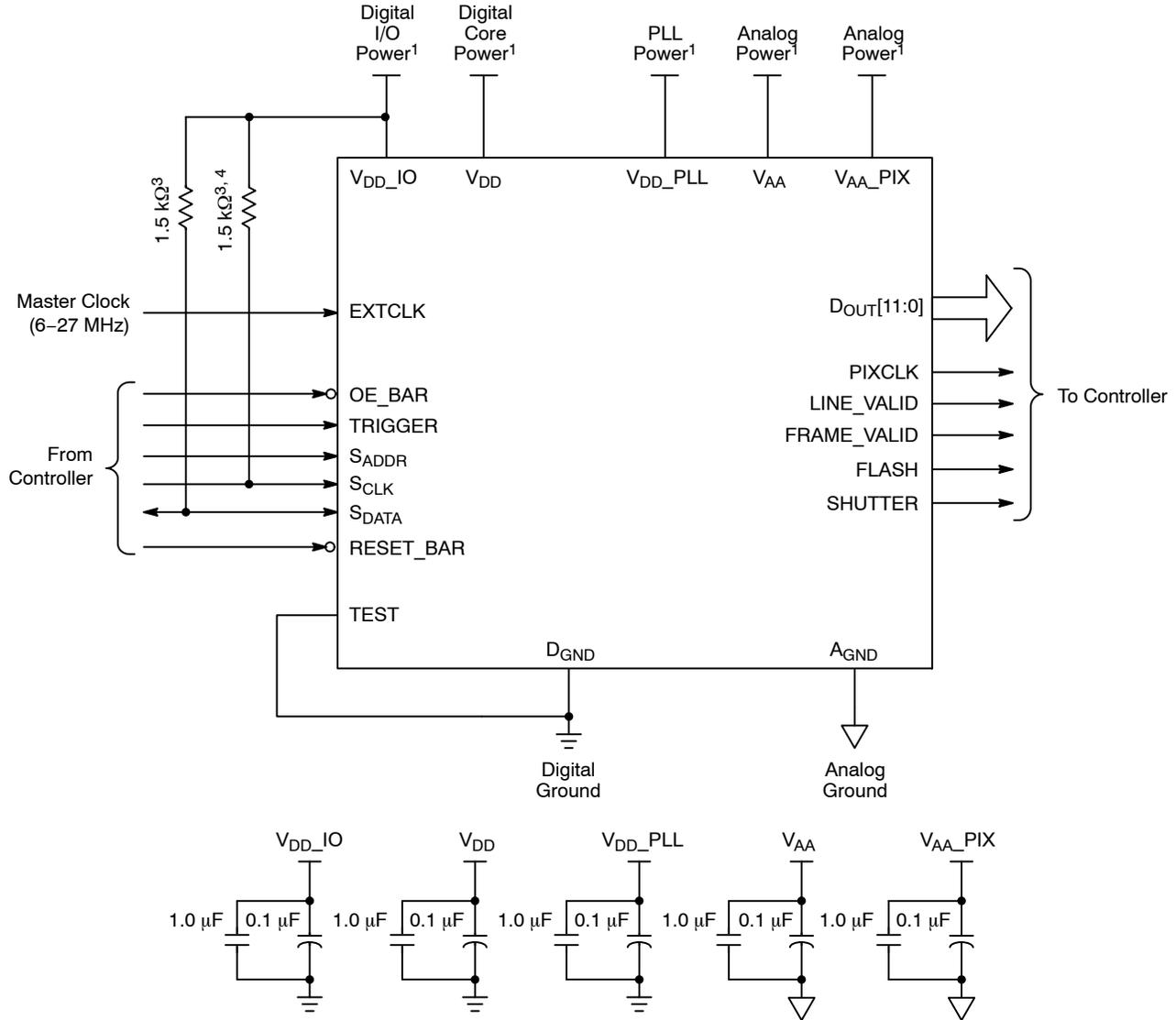
Notes:
1. All power supplies must be adequately decoupled. ON Semiconductor recommends having 1.0 μF and 0.1 μF decoupling capacitors for every power supply. If space is a concern, then priority must be given in the following order: V_{AA}, V_{AA_PIX}, V_{DD_PLL}, V_{DD_MIPI}, V_{DD_IO}, and V_{DD}. Actual values and results may vary depending on layout and design considerations.
2. To allow for space constraints, ON Semiconductor recommends having 0.1 μF decoupling capacitor inside the module as close to the pads as possible. In addition, place a 10 μF capacitor for each supply off-module but close to each supply.
3. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
4. This pull-up resistor is not required if the controller drives a valid logic level on S_{CLK} at all times.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. TEST pin must be tied to D_{GND} for the MIPI configuration.
7. ON Semiconductor recommends that GND_MIPI be tied to D_{GND}.
8. V_{DD_MIPI} is tied to V_{DD_PLL} in both the CLCC and the CSP package. ON Semiconductor strongly recommends that V_{DD_MIPI} must be connected to a V_{DD_PLL} in a module design since V_{DD_PLL} and V_{DD_MIPI} are tied together in the die.
9. The package pins or die pads used for the HiSPi data and clock as well as the parallel interface must be left floating.
10. HiSPi Power Supplies (V_{DD_HISPI} and $V_{DD\_HISPI\_TX}$) can be tied to ground.
11. If the SHUTTER or FLASH pins or pads are not used, then they must be left floating.
12. If the TRIGGER pin or pad is not used then it should be tied to D_{GND}.

Figure 3. Serial MIPI

AR0330CM

Figure 4. Parallel Pixel Data Interface

Notes:
1. All power supplies must be adequately decoupled. ON Semiconductor recommends having 1.0 μF and 0.1 μF decoupling capacitors for every power supply. If space is a concern, then priority must be given in the following order: V_{AA}, V_{AA}_PIX, V_{DD}_PLL, V_{DD}_IO, and V_{DD}. Actual values and results may vary depending on layout and design considerations.
2. To allow for space constraints, ON Semiconductor recommends having 0.1 μF decoupling capacitor inside the module as close to the pads as possible. In addition, place a 10 μF capacitor for each supply off-module but close to each supply.
3. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
4. This pull-up resistor is not required if the controller drives a valid logic level on S_{CLK} at all times.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. TEST pin should be tied to the ground.
7. The data and clock package pins or die pads used for the HiSPi and MIPI interface must be left floating.
8. The V_{DD}_MIPI package pin and sensor die pad should be connected to a 2.8 V supply as it is tied to the V_{DD}_PLL supply both in the package routing and also within the sensor die itself. HiSPi Power Supplies (V_{DD}_HISPI and $V_{DD}\_HISPI\_TX$) can be tied to ground.
9. If the SHUTTER or FLASH pins or pads are not used, then they must be left floating.
10. If the TRIGGER pin or pad is not used then it should be tied to D_{GND}.

PIN DESCRIPTIONS

Table 5. PIN DESCRIPTIONS

| Name	Type	Description
RESET_BAR	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
EXTCLK	Input	Master input clock, range 6−27 MHz.
OE_BAR	Input	Output enable (active LOW). Only available on bare die version.
TRIGGER	Input	Receives slave mode VD signal for frame rate synchronization and trigger to start a GRR frame.
S_{ADDR}	Input	Two-wire serial address select.
S_{CLK}	Input	Two-wire serial clock input.
S_{DATA}	I/O	Two-wire serial data I/O.
PIXCLK	Output	Pixel clock out. D_{OUT} is valid on rising edge of this clock.
$D_{OUT}[11:0]$	Output	Parallel pixel data output.
FLASH	Output	Flash output. Synchronization pulse for external light source. Can be left floating if not used.
FRAME_VALID	Output	Asserted when D_{OUT} data is valid.
LINE_VALID	Output	Asserted when D_{OUT} data is valid.
V_{DD}	Power	Digital power.
V_{DD}_IO	Power	IO supply power.
V_{DD}_PLL	Power	PLL power supply. The MIPI power supply (V_{DD}_MIPI) is tied to V_{DD}_PLL in both packages.
D_{GND}	Power	Digital GND.
V_{AA}	Power	Analog power.
V_{AA}_PIX	Power	Pixel power.
A_{GND}	Power	Analog GND.
TEST	Input	Enable manufacturing test modes. Tie to D_{GND} for normal sensor operation.
SHUTTER	Output	Control for external mechanical shutter. Can be left floating if not used.
SLVS0_P	Output	HiSPi serial data, lane 0, differential P.
SLVS0_N	Output	HiSPi serial data, lane 0, differential N.
SLVS1_P	Output	HiSPi serial data, lane 1, differential P.
SLVS1_N	Output	HiSPi serial data, lane 1, differential N.
SLVS2_P	Output	HiSPi serial data, lane 2, differential P.
SLVS2_N	Output	HiSPi serial data, lane 2, differential N.
SLVS3_P	Output	HiSPi serial data, lane 3, differential P.
SLVS3_N	Output	HiSPi serial data, lane 3, differential N.
SLVSC_P	Output	HiSPi serial DDR clock differential P.
SLVSC_N	Output	HiSPi serial DDR clock differential N.
DATA1_P	Output	MIPI serial data, lane 1, differential P.
DATA1_N	Output	MIPI serial data, lane 1, differential N.
DATA2_P	Output	MIPI serial data, lane 2, differential P.
DATA2_N	Output	MIPI serial data, lane 2, differential N.
DATA3_P	Output	MIPI serial data, lane 3, differential P.
DATA3_N	Output	MIPI serial data, lane 3, differential N.
DATA4_P	Output	MIPI serial data, lane 4, differential P.
DATA4_N	Output	MIPI serial data, lane 4, differential N.

Table 5. PIN DESCRIPTIONS (continued)

Name	Type	Description
CLK_P	Output	Output MIPI serial clock, differential P.
CLK_N	Output	Output MIPI serial clock, differential N.
V_{DD}_HiSPi	Power	1.8 V power port to HiSPi digital logic.
V_{DD}_HiSPi_TX	Power	0.4−0.8 V or 1.7−1.9 V. Refer to "HiSPi Power Supply Connections".
V_{AA}_HV_NPIX	Power	Power supply pin used to program the sensor OTPM (one-time programmable memory). This pin should be open if OTPM is not used.

Table 6. CSP (HiSPi/MIPI) PACKAGE PINOUT

	1	2	3	4	5	6	7	8
A	V_{AA}	V_{AA}_HV_NPIX	A_{GND}	A_{GND}	V_{AA}	V_{DD}	TEST	D_{GND}
B	D_{GND}	NC	V_{AA}_PIX	D_{GND}	V_{DD}_IO	TRIGGER	RESET_BAR	EXTCLK
C	V_{DD}	SHUTTER	D_{GND}	SLVSC_P	SLVS3_P	SLVS3_N	SLVS2_N	SLVS2_P
D	S_{ADDR}	S_{CLK}	SDATA	FLASH	SLVSC_N	SLVS1_P	V_{DD}_HiSPi_TX	V_{DD}_HiSPi
E	V_{DD}_IO	V_{DD}_IO	CLK_N	CLK_P	D_{GND}	SLVS1_N	SLVS0_N	SLVS0_P
F	D_{GND}	V_{DD}_IO	D_{GND}	D_{GND}	DATA4_P	DATA_N	DATA_P	V_{DD}_PLL
G	V_{DD}_IO	V_{DD}	D_{GND}	V_{DD}_IO	DATA4_N	DATA3_N	DATA2_N	V_{DD}
H	D_{GND}	V_{DD}_IO	V_{DD}_IO	D_{GND}	V_{DD}_PLL	DATA3_P	DATA2_P	V_{DD}_PLL

NOTE: NC = No Connection.
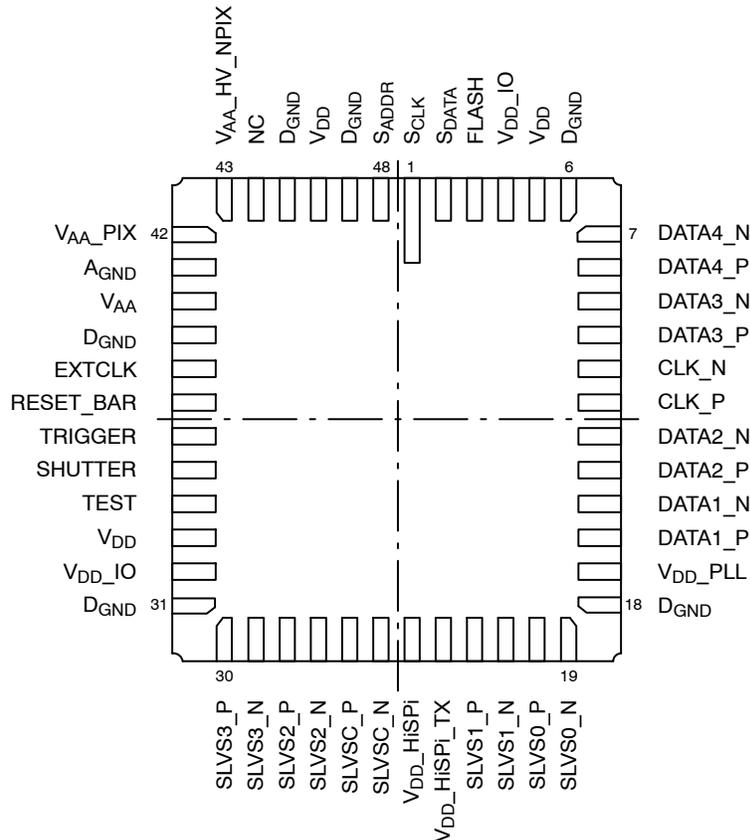
NOTE: Pins labeled NC (Not Connected) should be tied to ground.

**Figure 5. CLCC Package Pin Descriptions**

SENSOR INITIALIZATION

Power-Up Sequence

The recommended power-up sequence for the AR0330CS is shown in Figure 6. The available power supplies (V_{DD_IO}, V_{DD_PLL}, V_{DD_MIPI}, V_{AA}, V_{AA_PIX}) must have the separation specified below.

1. Turn on V_{DD_PLL} and V_{DD_MIPI} power supplies.
2. After 100 μs, turn on V_{AA} and V_{AA_PIX} power supply.
3. After 100 μs, turn on V_{DD} power supply.
4. After 100 μs, turn on V_{DD_IO} power supply.
5. After the last power supply is stable, enable EXTCLK.

6. Assert RESET_BAR for at least 1 ms.
7. Wait 150,000 EXTCLK periods (for internal initialization into software standby.
8. Write R0x3152 = 0xA114 to configure the internal register initialization process.
9. Write R0x304A = 0x0070 to start the internal register initialization process.
10. Wait 150,000 EXTCLK periods.
11. Configure PLL, output, and image settings to desired values.
12. Wait 1ms for the PLL to lock.
13. Set streaming mode (R0x301A[2] = 1).
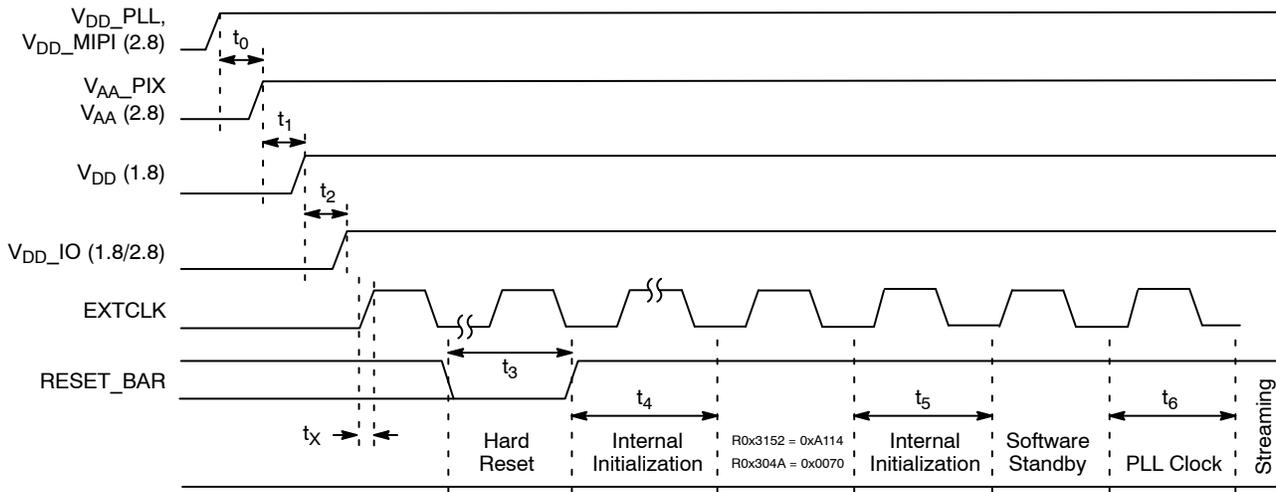
Notes:
1. A software reset (R0x301A[0] = 1) is not necessary after the procedure described above since a Hard Reset will automatically triggers a software reset. Independently executing a software reset, should be followed by steps seven through thirteen above.
2. The sensor must be receiving the external input clock (EXTCLK) before the reset pin is toggled. The sensor will begin an internal initialization sequence when the reset pin toggle from LOW to HIGH. This initialization sequence will run using the external input clock. Power on default state is software standby state, need to apply two-wire serial commands to start streaming. Above power up sequence is a general power up sequence. For different interface configurations, MIPI, and Parallel, some power rails are not needed. Those not needed power rails should be ignored in the general power up sequence.

Figure 6. Power Up

Table 7. POWER-UP SEQUENCE

Symbol	Definition	Min	Typ	Max	Unit
t_0	V_{DD_PLL}, V_{DD_MIPI} to V_{AA}/V_{AA_PIX} (Note 3)	0	100	–	μs
t_1	V_{AA}/V_{AA_PIX} to V_{DD}	0	100	–	μs
t_2	V_{DD} to V_{DD_IO}	0	100	–	μs
t_X	External Clock Settling Time (Note 1)	–	30	–	ms
t_3	Hard Reset (Note 2)	1	–	–	ms
t_4	Internal Initialization	150000	–	–	EXTCLKs
t_5	Internal Initialization	150000	–	–	EXTCLKs
t_6	PLL Lock Time	1	–	–	ms

1. External clock settling time is component-dependent, usually taking about 10–100 ms.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
3. It is critical that V_{DD_PLL} is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that V_{DD_PLL} is powered after other supplies then sensor may have functionality issues and will experience high current draw on this supply.
4. V_{DD_MIPI} is tied to V_{DD_PLL} in the both the CLCC and CSP packages and must be powered to 2.8 V. The V_{DD_HiSPi} and $V_{DD\_HiSPi\_TX}$ supplies do not need to be turned on if the sensor is configured to use the MIPI or parallel interface.

Power-Down Sequence

The recommended power-down sequence for the AR0330 is shown in Figure 7. The available power supplies (V_{DD}_IO, V_{DD}_HiSPi, $V_{DD}\_HiSPi\_TX$, V_{DD}_PLL, V_{DD}_MIPI, V_{AA}, V_{AA}_PIX) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0.

2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off $V_{DD}\_HiSPi\_TX$.
4. Turn off V_{DD}_IO.
5. Turn off V_{DD} and V_{DD}_HiSPi.
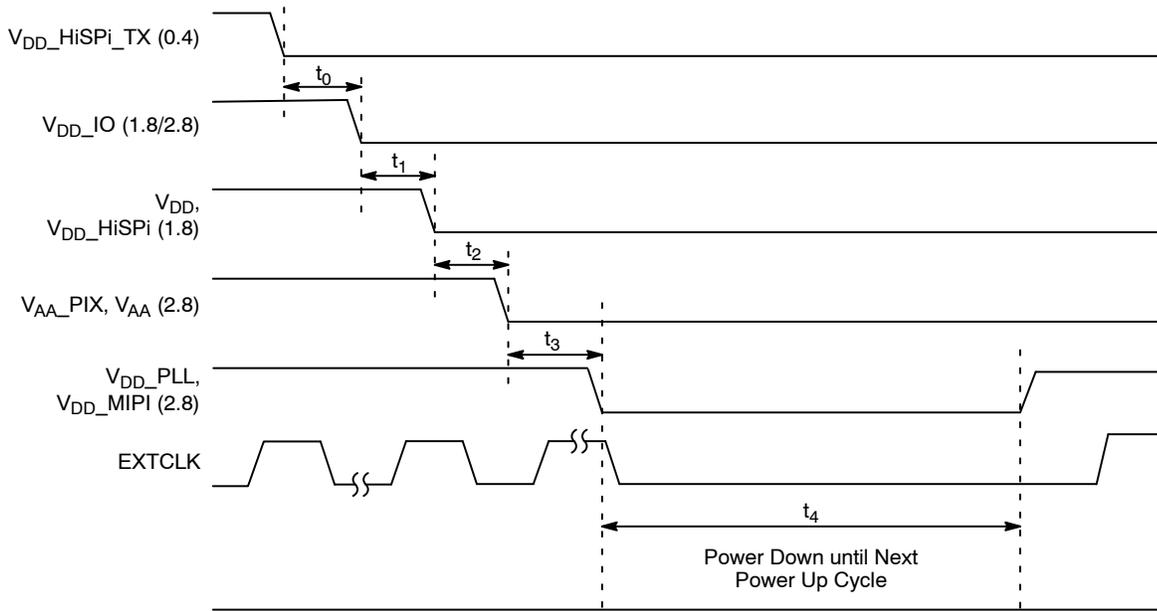6. Turn off V_{AA}/V_{AA}_PIX.
7. Turn off V_{DD}_PLL, V_{DD}_MIPI.

Figure 7. Power Down

Table 8. POWER-DOWN SEQUENCE

Symbol	Parameter	Min	Typ	Max	Unit
t_0	$V_{DD}\_HiSPi\_TX$ to V_{DD}_IO	0	–	–	μs
t_1	V_{DD}_IO to V_{DD} and V_{DD}_HiSPi	0	–	–	μs
t_2	V_{DD} and V_{DD}_HiSPi to V_{AA}/V_{AA}_PIX	0	–	–	μs
t_3	V_{AA}/V_{AA}_PIX to V_{DD}_PLL	0	–	–	μs
t_4	PwrDn until Next PwrUp Time	100	–	–	ms

NOTE: t_4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

ELECTRICAL CHARACTERISTICS

Table 9. DC ELECTRICAL DEFINITIONS AND CHARACTERISTICS (MIPI MODE)

(f_{EXTCLK} = 24 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 1.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; Output Load = 68.5 pF; T_J = 60°C; Data Rate = 588 Mbps; 2304 × 1296 at 60 fps)

Symbol	Definition	Min	Typ	Max	Unit
V_{DD}	Core Digital Voltage	1.7	1.8	1.9	V
V_{DD}_IO	I/O Digital Voltage	1.7 2.4	1.8 2.8	1.9 3.1	V
V_{AA}	Analog Voltage	2.7	2.8	2.9	V
V_{AA}_PIX	Pixel Supply Voltage	2.7	2.8	2.9	V
V_{DD}_PLL	PLL Supply Voltage	2.7	2.8	2.9	V
V_{DD}_MIPI	MIPI Supply Voltage	2.7	2.8	2.9	V
I (V_{DD})	Digital Operating Current	–	114	136	mA
I (V_{DD}_IO)	I/O Digital Operating Current	–	0	0	mA
I (V_{AA})	Analog Operating Current	–	41	53	mA
I (V_{AA}_PIX)	Pixel Supply Current	–	9.9	12	mA
I (V_{DD}_PLL)	PLL Supply Current	–	15	27	mA
I (V_{DD}_MIPI)	MIPI Digital Operating Current	–	35	49	mA

Table 10. DC ELECTRICAL DEFINITIONS AND CHARACTERISTICS (HiSPi MODE)

(f_{EXTCLK} = 24 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 1.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_HiSPi = 1.8 V, V_{DD}_HiSPi_TX = 0.4 V; Output Load = 68.5 pF; T_J = 60°C; Data Rate = 588 Mbps; DLL Set to 0; 2304 × 1296 at 60 fps)

Symbol	Definition	Min	Typ	Max	Unit
V_{DD}	Core Digital Voltage	1.7	1.8	1.9	V
V_{DD}_IO	I/O Digital Voltage	1.7 2.4	1.8 2.8	1.9 3.1	V
V_{AA}	Analog Voltage	2.7	2.8	2.9	V
V_{AA}_PIX	Pixel Supply Voltage	2.7	2.8	2.9	V
V_{DD}_PLL	PLL Supply Voltage	2.7	2.8	2.9	V
V_{DD}_HiSPi	HiSPi Digital Voltage	1.7	1.8	1.9	V
V_{DD}_HiSPi_TX	HiSPi I/O Digital Voltage	0.3 1.7	0.4 1.8	0.9 1.9	V
I (V_{DD})	Digital Operating Current	–	96.3	137	mA
I (V_{DD}_IO)	I/O Digital Operating Current	–	0	0	mA
I (V_{AA})	Analog Operating Current	–	45.1	53	mA
I (V_{AA}_PIX)	Pixel Supply Current	–	10.5	12	mA
I (V_{DD}_PLL)	PLL Supply Current	–	6.4	11	mA
I (V_{DD}_HiSPi)	HiSPi Digital Operating Current	–	21.8	36	mA
I (V_{DD}_HiSPi_TX)	HiSPi I/O Digital Operating Current	–	22.3	40	mA

Table 11. DC ELECTRICAL DEFINITIONS AND CHARACTERISTICS (PARALLEL MODE)

(f_{EXTCLK} = 24 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 1.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; Output Load = 68.5 pF; T_J = 60°C; 2304 × 1296 at 30 fps)

Symbol	Definition	Min	Typ	Max	Unit
V_{DD}	Core Digital Voltage	1.7	1.8	1.9	V
V_{DD}_IO	I/O Digital Voltage	1.7 2.4	1.8 2.8	1.9 3.1	V
V_{AA}	Analog Voltage	2.7	2.8	2.9	V
V_{AA}_PIX	Pixel Supply Voltage	2.7	2.8	2.9	V
V_{DD}_PLL	PLL Supply Voltage	2.7	2.8	2.9	V
I (V_{DD})	Digital Operating Current	–	66.5	75	mA
I (V_{DD}_IO)	I/O Digital Operating Current	–	24	35	mA
I (V_{AA})	Analog Operating Current	–	36	44	mA
I (V_{AA}_PIX)	Pixel Supply Current	–	10.5	18	mA
I (V_{DD}_PLL)	PLL Supply Current	–	6	11	mA

Table 12. STANDBY POWER

(f_{EXTCLK} = 24 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 1.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; Output Load = 68.5 pF; T_J = 60°C)

	Power	Typ	Max	Unit
Hard Standby (CLK OFF)	Digital	19.8	35.8	µA
	Analog	5.8	7.0	µA
Soft Standby (CLK OFF)	Digital	23.5	39.7	µA
	Analog	5.4	5.9	µA
Soft Standby (CLK ON)	Digital	15700	16900	µA
	Analog	5.5	5.7	µA

CAUTION: Stresses greater than those listed in Table 13 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Table 13. ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min	Max	Unit
V_{DD}_MAX	Core Digital Voltage	−0.3	2.4	V
V_{DD}_IO_MAX	I/O Digital Voltage	−0.3	4	V
V_{AA}_MAX	Analog Voltage	−0.3	4	V
V_{AA}_PIX	Pixel Supply Voltage	−0.3	4	V
V_{DD}_PLL	PLL Supply Voltage	−0.3	4	V
V_{DD}_MIPI	MIPI Supply Voltage	−0.3	4	V
V_{DD}_HiSPi_MAX	HiSPi Digital Voltage	−0.3	2.4	V
V_{DD}_HiSPi_TX_MAX	HiSPi I/O Digital Voltage	−0.3	2.4	V
t_{ST}	Storage Temperature	−40	85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (S_{CLK}, S_{DATA}) are shown in Figure 8 and Table 14.
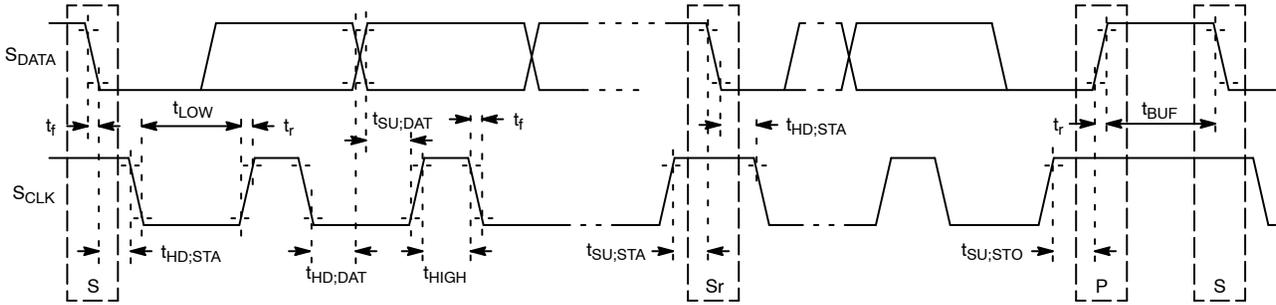
NOTE: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Figure 8. Two-Wire Serial Bus Timing Parameters

Table 14. TWO-WIRE SERIAL BUS CHARACTERISTICS

(f_{EXTCLK} = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
S_{CLK} Clock Frequency	t_{SCL}	0	100	0	400	kHz
Hold Time (Repeated) START Condition						
After this Period, the First Clock Pulse is Generated	$t_{HD;STA}$	4.0	–	0.6	–	μs
LOW Period of the S_{CLK} Clock	t_{LOW}	4.7	–	1.3	–	μs
HIGH Period of the S_{CLK} Clock	t_{HIGH}	4.0	–	0.6	–	μs
Set-up Time for a Repeated START Condition	$t_{SU;STA}$	4.7	–	0.6	–	μs
Data Hold Time	$t_{HD;DAT}$	0 (Note 4)	3.45 (Note 5)	0 (Note 6)	0.9 (Note 5)	μs
Data Set-up Time	$t_{SU;DAT}$	250	–	100 (Note 6)	–	ns
Rise Time of both S_{DATA} and S_{CLK} Signals	t_r	–	1000	20 + 0.1 Cb (Note 7)	300	ns
Fall Time of both S_{DATA} and S_{CLK} Signals	t_f	–	300	20 + 0.1 Cb (Note 7)	300	ns
Set-up Time for STOP Condition	$t_{SU;STO}$	4.0	–	0.6	–	μs
Bus Free Time between a STOP and START Condition	t_{BUF}	4.7	–	1.3	–	μs
Capacitive Load for Each Bus Line	Cb	–	400	–	400	pF
Serial Interface Input Pin Capacitance	CIN_SI	–	3.3	–	3.3	pF
S_{DATA} Max Load Capacitance	CLOAD_SD	–	30	–	30	pF
S_{DATA} Pull-up Resistor	RSD	1.5	4.7	1.5	4.7	kΩ

1. This table is based on I2C standard (v2.1 January 2000). Philips Semiconductor.
2. Two-wire control is I2C-compatible.
3. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1 V_{DD} levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the S_{DATA} signal to bridge the undefined region of the falling edge of S_{CLK}.
5. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the S_{CLK} signal.
6. A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the S_{CLK} signal. If such a device does stretch the LOW period of the S_{CLK} signal, it must output the next data bit to the S_{DATA} line t_r max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the S_{CLK} line is released.
7. Cb = total capacitance of one bus line in pF.

AR0330CM
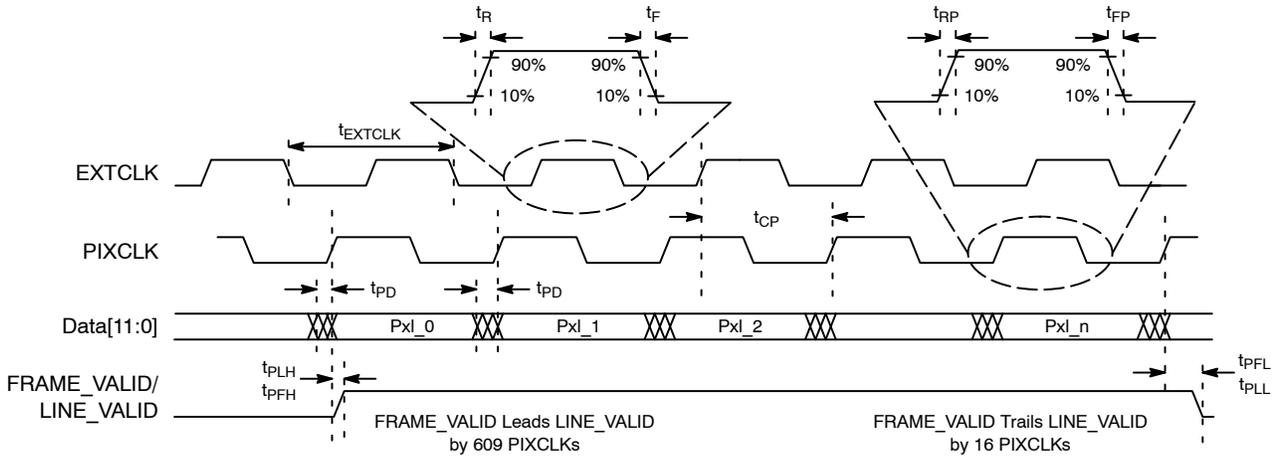
NOTE: PLL disabled for t_{CP}.

Figure 9. I/O Timing Diagram

Table 15. I/O PARAMETERS

(f_{EXTCLK} = 24 MHz; V_{DD} = 1.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; Output Load = 68.5 pF; T_J = 60°C; CLK_OP = 98 Mp/s)

Symbol	Definition	Condition	Min	Max	Unit
V_{IH}	Input HIGH Voltage	V_{DD}_IO = 1.8 V V_{DD}_IO = 2.8 V	1.4 2.4	V_{DD}_IO + 0.3 V_{DD}_IO + 0.3	V
V_{IL}	Input LOW Voltage	V_{DD}_IO = 1.8 V V_{DD}_IO = 2.8 V	GND − 0.3 GND − 0.3	0.4 0.8	μV
I_{IN}	Input Leakage Current	No Pull-up Resistor; V_{IN} = V_{DD} OR D_{GND}	−20	20	μA
V_{OH}	Output HIGH Voltage	At Specified I_{OH}	V_{DD}_IO – 0.4	–	V
V_{OL}	Output LOW Voltage	At Specified I_{OL}	–	0.4	V
I_{OH}	Output HIGH Current	At Specified V_{OH}	–	−12	mA
I_{OL}	Output LOW Current	At Specified V_{OL}	–	9	mA
I_{OZ}	Tri-state Output Leakage Current		–	10	μA

Table 16. I/O TIMING

(f_{EXTCLK} = 24 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 1.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; Output load = 68.5 pF; T_J = 60°C; CLK_OP = 98 Mp/s)

Symbol	Definition	Conditions	Min	Typ	Max	Unit
f_{EXTCLK}	Input Clock Frequency	PLL Enabled	6	24	27	MHz
t_{EXTCLK}	Input Clock Period	PLL Enabled	166	41	20	ns
t_R	Input Clock Rise Time		0.5	–	Sine Wave Rise Time	ns
t_F	Input Clock Fall Time		0.5	–	Sine Wave Fall Time	ns
	Clock Duty Cycle		45	50	55	%
t_{JITTER}	Input Clock Jitter		–	–	0.3	ns
Output Pin Slew	Fastest	C_{LOAD} = 15 pF	–	0.7	–	V/ns
f_{PIXCLK}	PIXCLK frequency	Default	–	80	–	MHz
t_{PD}	PIXCLK to data valid	Default	–	–	3	ns
t_{PFH}	PIXCLK to FRAME_VALID HIGH	Default	–	–	3	ns
t_{PLH}	PIXCLK to LINE_VALID HIGH	Default	–	–	3	ns
t_{PFL}	PIXCLK to FRAME_VALID LOW	Default	–	–	3	ns
t_{PLL}	PIXCLK to LINE_VALID LOW	Default	–	–	3	ns

Table 17. PARALLEL I/O RISE SLEW RATE

(f_{EXTCLK} = 24 MHz; V_{DD} = 1.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; Output Load = 68.5 pF; T_J = 60°C; CLK_OP = 98 Mp/s)

VDD_IO	Parallel Slew Rate (R0x306E[15:13])								Unit
	0	1	2	3	4	5	6	7	
1.70 V	0.069	0.115	0.172	0.239	0.325	0.43	0.558	0.836	V/ns
1.80 V	0.078	0.131	0.195	0.276	0.375	0.507	0.667	1.018	
1.95 V	0.093	0.156	0.233	0.331	0.456	0.62	0.839	1.283	
2.50 V	0.15	0.252	0.377	0.539	0.759	1.07	1.531	2.666	
2.80 V	0.181	0.305	0.458	0.659	0.936	1.347	1.917	3.497	
3.10 V	0.212	0.361	0.543	0.78	1.114	1.618	2.349	4.14	

HiSPi TRANSMITTER

NOTE: Refer to "High-Speed Serial Pixel Interface Physical Layer Specification v2.00.00" for further explanation of the HiSPi transmitter specification.

SLVS Electrical Specifications

Table 18. POWER SUPPLY AND OPERATING TEMPERATURE

(f_{EXTCLK} = 24 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 1.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; Output load = 68.5 pF; T_J = 60°C; CLK_OP = 98 Mp/s)

Symbol	Parameter	Min	Typ	Max	Unit
I_{DD}_HiSPi_TX	SLVS Current Consumption (Notes 1, 2)	–	–	$n \times 18$	mA
I_{DD}_HiSPi	HiSPi PHY Current Consumption (Notes 1, 2, 3)	–	–	$n \times 45$	mA
T_J	Operating Temperature (Note 4)	–30	–	70	°C

1. Where 'n' is the number of PHYs.
2. Temperature of 25°C.
3. Up to 700 Mbps.
4. Specification values may be exceeded when outside this temperature range.

Table 19. SLVS ELECTRICAL DC SPECIFICATION (T_J = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CM}	SLVS DC Mean Common Mode Voltage	$0.45 * V_{DD}\_TX$	$0.5 * V_{DD}\_TX$	$0.55 * V_{DD}\_TX$	V
$|V_{OD}|$	SLVS DC Mean Differential Output Voltage	$0.36 * V_{DD}\_TX$	$0.5 * V_{DD}\_TX$	$0.64 * V_{DD}\_TX$	V
ΔV_{CM}	Change in V_{CM} between Logic 1 and 0	–	–	25	mV
$|V_{OD}|$	Change in $|V_{OD}|$ between Logic 1 and 0	–	–	25	mV
NM	V_{OD} Noise Margin	–	–	±30	%
$|\Delta V_{CM}|$	Difference in V_{CM} between any Two Channels	–	–	50	mV
$|\Delta V_{OD}|$	Difference in V_{OD} between any Two Channels	–	–	100	mV
V_{CM_AC}	Common-mode AC Voltage (pk) without VCM Cap Termination	–	–	50	mV
V_{CM_AC}	Common-mode AC Voltage (pk) with VCM Cap Termination	–	–	30	mV
V_{OD_AC}	Maximum Overshoot Peak $|V_{OD}|$	–	–	$1.3 * |V_{OD}|$	V
V_{Diff_pk-pk}	Maximum Overshoot V_{Diff_pk-pk}	–	–	$2.6 * V_{OD}$	V
R_O	Single-ended Output Impedance	35	50	70	Ω
ΔR_O	Output Impedance Mismatch	–	–	20	%

AR0330CM

Table 20. SLVS ELECTRICAL TIMING SPECIFICATION

Symbol	Parameter	Min	Max	Unit
1/UI	Data Rate (Note 1)	280	700	Mbps
t_{PW}	Bitrate Period (Note 1)	1.43	3.57	ns
t_{PRE}	Max Setup Time from Transmitter (Notes 1, 2)	0.3	–	UI
t_{POST}	Max Hold Time from Transmitter (Notes 1, 2)	0.3	–	UI
t_{EYE}	Eye Width (Notes 1, 2)	–	0.6	UI
$t_{TOTALJIT}$	Data Total Jitter (pk-pk) @1e–9 (Notes 1, 2)	–	0.2	UI
t_{CKJIT}	Clock Period Jitter (RMS) (Note 2)	–	50	ps
t_{CYCJIT}	Clock Cycle-to-Cycle Jitter (RMS) (Note 2)	–	100	ps
t_R	Rise Time (20–80%) (Note 3)	150 ps	0.25	UI
t_F	Fall Time (20–80%) (Note 3)	150 ps	0.25	UI
DCYC	Clock Duty Cycle (Note 2)	45	55	%
t_{CHSKEW}	Mean Clock to Data Skew (Notes 1, 4)	–0.1	0.1	UI
$t_{PHYSKEW}$	PHY-to-PHY Skew (Notes 1, 5)	–	2.1	UI
$t_{DIFFSKEW}$	Mean Differential Skew (Note 6)	–100	100	ps

1. One UI is defined as the normalized mean time between one edge and the following edge of the clock.
2. Taken from the 0 V crossing point with the DLL off.
3. Also defined with a maximum loading capacitance of 10 pF on any pin. The loading capacitance may also need to be less for higher bitrates so the rise and fall times do not exceed the maximum 0.3 UI.
4. The absolute mean skew between the Clock lane and any Data Lane in the same PHY between any edges.
5. The absolute skew between any Clock in one PHY and any Data lane in any other PHY between any edges.
6. Differential skew is defined as the skew between complementary outputs. It is measured as the absolute time between the two complementary edges at mean VCM point. Note that differential skew also is related to the ΔVCM_AC spec which also must not be exceeded.

HiVCM Electrical Specifications

The HiSPi 2.0 specification also defines an alternative signaling level mode called HiVCM. Both V_{OD} and V_{CM} are still scalable with $V_{DD}\_HiSPi\_TX$, but with $V_{DD}\_HiSPi\_TX$ nominal set to 1.8 V the common-mode is elevated to around 0.9 V.

Table 21. HiVCM POWER SUPPLY AND OPERATING TEMPERATURES

Symbol	Parameter	Min	Typ	Max	Unit
$I_{DD}\_HiSPi\_TX$	HiVCM Current Consumption (Notes 1, 2)	–	–	n * 34	mA
I_{DD}_HiSPi	HiSPi PHY Current Consumption (Notes 1, 2, 3)	–	–	n * 45	mA
T_J	Operating Temperature (Note 4)	–30	–	70	°C

1. Where 'n' is the number of PHYs.
2. Temperature of 25°C.
3. Up to 700 Mbps.
4. Specification values may be exceeded when outside this temperature range.

AR0330CM

Table 22. HiVCM ELECTRICAL VOLTAGE AND IMPEDANCE SPECIFICATION ($T_J = 25°C$)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CM}	HiVCM DC Mean Common Mode Voltage	0.76	0.90	1.07	V
$|V_{OD}|$	HiVCM DC Mean Differential Output Voltage	200	280	350	mV
ΔV_{CM}	Change in V_{CM} between Logic 1 and 0	–	–	25	mV
$|V_{OD}|$	Change in $|V_{OD}|$ between Logic 1 and 0	–	–	25	mV
NM	V_{OD} Noise Margin	–	–	±30	%
$|\Delta V_{CM}|$	Difference in V_{CM} between any Two Channels	–	–	50	mV
$|\Delta V_{OD}|$	Difference in V_{OD} between any Two Channels	–	–	100	mV
ΔV_{CM_AC}	Common-mode AC Voltage (pk) without V_{CM} Cap Termination	–	–	50	mV
ΔV_{CM_AC}	Common-mode AC Voltage (pk) with V_{CM} Cap Termination	–	–	30	mV
V_{OD_AC}	Maximum Overshoot Peak $|V_{OD}|$	–	–	1.3 * $|V_{OD}|$	V
V_{Diff_pk-pk}	Maximum Overshoot $V_{Diff\ pk-pk}$	–	–	2.6 * V_{OD}	V
R_O	Single-ended Output Impedance	40	70	100	Ω
ΔR_O	Output Impedance Mismatch	–	–	20	%

Table 23. HiVCM ELECTRICAL AC SPECIFICATION

Symbol	Parameter	Min	Max	Unit
1/UI	Data Rate (Note 1)	280	700	Mbps
t_{PW}	Bitrate Period (Note 1)	1.43	3.57	ns
t_{PRE}	Max Setup Time from Transmitter (Notes 1, 2)	0.3	–	UI
t_{POST}	Max Gold Time from Transmitter (Notes 1, 2)	0.3	–	UI
t_{EYE}	Eye Width (Notes 1, 2)	–	0.6	UI
$t_{TOTALJIT}$	Data Total Jitter (pk-pk) @1e−9 (Notes 1, 2)	–	0.2	UI
t_{CKJIT}	Clock Period Jitter (RMS) (Note 2)	–	50	ps
t_{CYCJIT}	Clock Cycle-to-Cycle Jitter (RMS) (Note 2)	–	100	ps
t_R	Rise Time (20–80%) (Note 3)	150 ps	0.3	UI
t_F	Fall Time (20–80%) (Note 3)	150 ps	0.3	UI
D_{CYC}	Clock Duty Cycle (Note 2)	45	55	%
t_{CHSKEW}	Clock to Data Skew (Notes 1, 4)	−0.1	0.1	UI
$t_{PHYSKEW}$	PHY-to-PHY Skew (Notes 1, 5)	–	2.1	UI
$t_{DIFFSKEW}$	Mean Differential Skew (Note 6)	−100	100	ps

1. One UI is defined as the normalized mean time between one edge and the following edge of the clock.
2. Taken from the 0 V crossing point with the DLL off.
3. Also defined with a maximum loading capacitance of 10 pF on any pin. The loading capacitance may also need to be less for higher bitrates so the rise and fall times do not exceed the maximum 0.3 UI.
4. The absolute mean skew between the Clock lane and any Data Lane in the same PHY between any edges.
5. The absolute mean skew between any Clock in one PHY and any Data lane in any other PHY between any edges.
6. Differential skew is defined as the skew between complementary outputs. It is measured as the absolute time between the two complementary edges at mean V_{CM} point. Note that differential skew also is related to the ΔVCM_AC spec which also must not be exceeded.

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17

Electrical Definitions

Figure 10 is the diagram defining differential amplitude V_{OD}, V_{CM}, and rise and fall times. To measure V_{OD} and V_{CM} use the DC test circuit shown in Figure 11 and set the HiSPi PHY to constant Logic 1 and Logic 0. Measure V_{oa}, V_{ob} and V_{CM} with voltmeters for both Logic 1 and Logic 0.
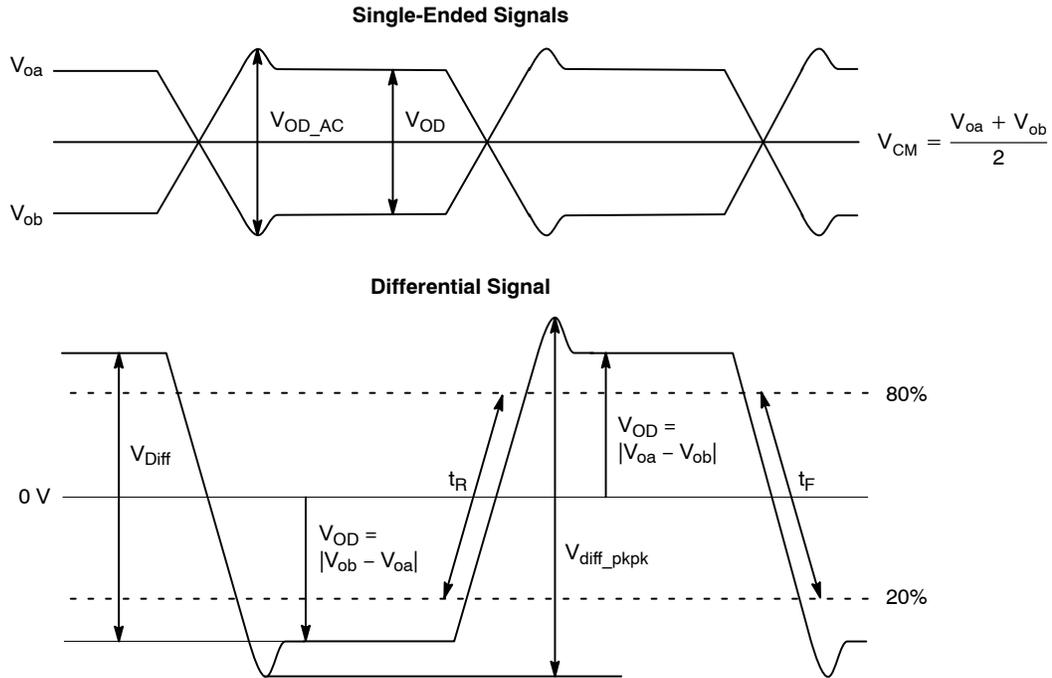
Single-Ended Signals

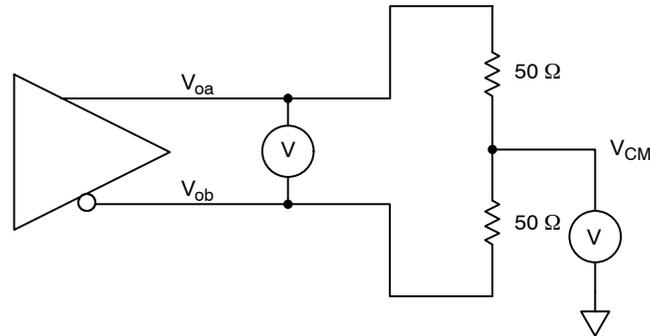$$V_{CM} = \frac{V_{oa} + V_{ob}}{2}$$

Differential Signal

Figure 10. Single-Ended and Differential Signals

Figure 11. DC Test Circuit

$$V_{OD}(m) = \left| V_{oa}(m) - V_{ob}(m) \right| \qquad \text{(eq. 1)}$$

Where *m* is either "1" for logic 1 or "0" for logic 0.

$$V_{OD} = \frac{V_{OD}(1) + V_{OD}(0)}{2} \qquad \text{(eq. 2)}$$

$$V_{Diff} = V_{OD}(1) + V_{OD}(0) \qquad \text{(eq. 3)}$$

$$\Delta V_{OD} = \left| V_{OD}(1) - V_{OD}(0) \right| \qquad \text{(eq. 4)}$$

$$V_{CM} = \frac{V_{CM}(1) + V_{CM}(0)}{2} \qquad \text{(eq. 5)}$$

$$\Delta V_{CM} = \left| V_{CM}(1) - V_{CM}(0) \right| \qquad \text{(eq. 6)}$$

Both V_{OD} and V_{CM} are measured for all output channels. The worst case ΔV_{OD} is defined as the largest difference in V_{OD} between all channels regardless of logic level. And the worst case ΔV_{CM} is similarly defined as the largest difference in V_{CM} between all channels regardless of logic level.

Timing Definitions

1. Timing measurements are to be taken using the Square Wave test mode.
2. Rise and fall times are measured between 20% to 80% positions on the differential waveform, as shown in Figure 10.
3. Mean Clock-to-Data skew should be measured from the 0 V crossing point on Clock to the 0 V crossing point on any Data channel regardless of edge, as shown in Figure 12. This time is compared with the ideal Data transition point of 0.5 UI with the difference being the Clock-to-Data Skew (see Equation 7).

$$t_{CHSKEW}(ps) = \Delta t - \frac{t_{pw}}{2} \qquad \text{(eq. 7)}$$

$$t_{CHSKEW}(UI) = \frac{\Delta t}{t_{pw}} - 0.5 \qquad \text{(eq. 8)}$$
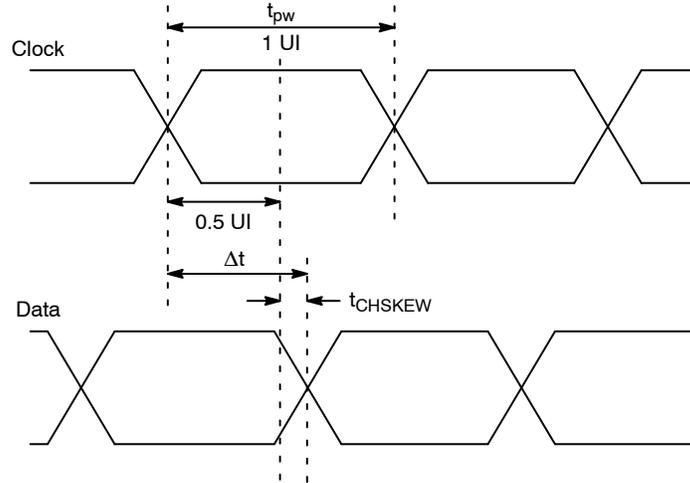
Figure 12. Clock-to-Data Skew Timing Diagram

4. The differential skew is measured on the two single-ended signals for any channel. The time is taken from a transition on V_{oa} signal to corresponding transition on V_{ob} signal at V_{CM} crossing point.
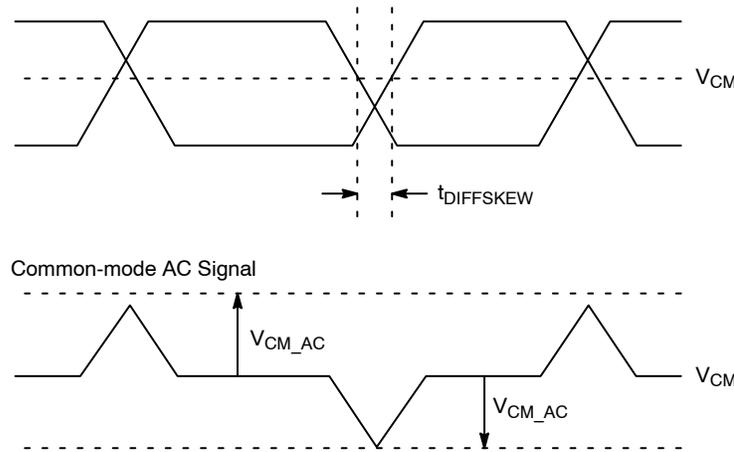
Figure 13. Differential Skew

Figure 13 also shows the corresponding AC V_{CM} common-mode signal. Differential skew between the V_{oa} and V_{ob} signals can cause spikes in the common-mode, which the receiver needs to be able to reject. V_{CM_AC} is measured as the absolute peak deviation from the mean DC V_{CM} common-mode.
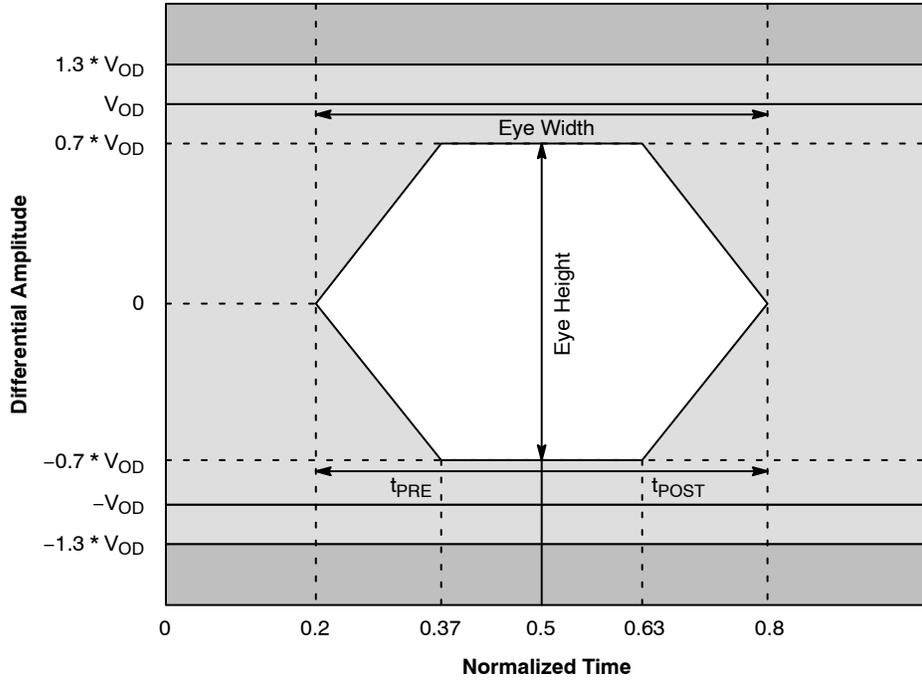
Transmitter Eye Mask

Figure 14. Transmitter Eye Mask

Figure 14 defines the *eye mask* for the transmitter. 0.5 UI point is the instantaneous crossing point of the Clock. The area in white shows the area Data is prohibited from crossing into. The *eye mask* also defines the minimum eye height, the data t_{PRE} and t_{POST} times, and the *total jitter pk-pk +mean skew (t_{TJSKEW})* for Data.

Clock Signal

t_{HCLK} is defined as the high clock period, and t_{LCLK} is defined as the low clock period as shown in Figure 15. The clock duty cycle D_{CYC} is defined as the percentage time the clock is either high (t_{HCLK}) or low (t_{LCLK}) compared with the clock period T.
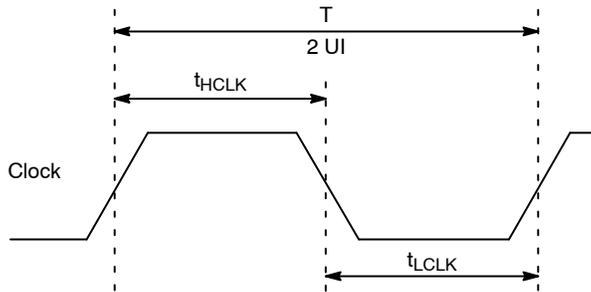

Figure 15. Clock Duty Cycle

$$D_{CYC}(1) = \frac{t_{HCLK}}{T} \qquad \text{(eq. 9)}$$

$$D_{CYC}(0) = \frac{t_{LCLK}}{T} \qquad \text{(eq. 10)}$$

$$t_{pw} = \frac{T}{2} \quad \text{(i.e, 1 UI)} \qquad \text{(eq. 11)}$$

$$\text{Bitrate} = \frac{1}{t_{pw}} \qquad \text{(eq. 12)}$$

Figure 16 shows the definition of clock jitter for both the period and the cycle-to-cycle jitter.
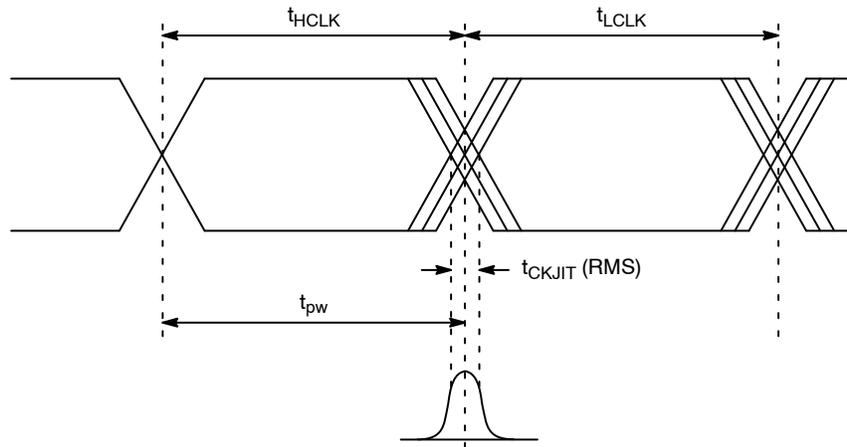

Figure 16. Clock Jitter

Period Jitter (t_{CKJIT}) is defined as the deviation of the instantaneous clock t_{PW} from an ideal 1 UI. This should be measured for both the clock high period variation Δt_{HCLK}, and the clock low period variation Δt_{LCLK} taking the RMS or 1-sigma standard deviation and quoting the worse case jitter between Δt_{HCLK} and Δt_{LCLK}.

Cycle-to-cycle jitter (t_{CYCJIT}) is defined as the difference in time between consecutive clock high and clock low periods t_{HCLK} and t_{LCLK}, quoting the RMS value of the variation $\Delta(t_{HCLK} - t_{LCLK})$.

If pk-pk jitter is also measured, this should be limited to ±3-sigma.

Table 24. HiVCM ELECTRICAL AC SPECIFICATION

Symbol	Parameter	Min	Max	Unit
1/UI	Data Rate (Note 1)	280	700	Mbps
t_{PW}	Bitrate Period (Note 1)	1.43	3.57	ns
t_{PRE}	Max Setup Time from Transmitter (Notes 1, 2)	0.3	–	UI
t_{POST}	Max Gold Time from Transmitter (Notes 1, 2)	0.3	–	UI
t_{EYE}	Eye Width (Notes 1, 2)	–	0.6	UI
$t_{TOTALJIT}$	Data Total Jitter (pk-pk) @1e–9 (Notes 1, 2)	–	0.2	UI
t_{CKJIT}	Clock Period Jitter (RMS) (Note 2)	–	50	ps
t_{CYCJIT}	Clock Cycle-to-Cycle Jitter (RMS) (Note 2)	–	100	ps
t_R	Rise Time (20–80%) (Note 3)	150 ps	0.3	UI
t_F	Fall Time (20–80%) (Note 3)	150 ps	0.3	UI
D_{CYC}	Clock Duty Cycle (Note 2)	45	55	%
t_{CHSKEW}	Clock to Data Skew (Notes 1, 4)	–0.1	0.1	UI
$t_{PHYSKEW}$	PHY-to-PHY Skew (Notes 1, 5)	–	2.1	UI
$t_{DIFFSKEW}$	Mean Differential Skew (Note 6)	–100	100	ps

1. One UI is defined as the normalized mean time between one edge and the following edge of the clock.
2. Taken from the 0 V crossing point with the DLL off.
3. Also defined with a maximum loading capacitance of 10 pF on any pin. The loading capacitance may also need to be less for higher bitrates so the rise and fall times do not exceed the maximum 0.3 UI.
4. The absolute mean skew between the Clock lane and any Data Lane in the same PHY between any edges.
5. The absolute mean skew between any Clock in one PHY and any Data lane in any other PHY between any edges.
6. Differential skew is defined as the skew between complementary outputs. It is measured as the absolute time between the two complementary edges at mean V_{CM} point. Note that differential skew also is related to the ΔVCM_AC spec which also must not be exceeded.

SEQUENCER

The sequencer digital block determines the order and timing of operations required to sample pixel data from the array during each row period. It is controlled by an instruction set that is programmed into RAM from the sensor OTPM (One Time Programmable Memory). The OTPM is configured during production.

The instruction set determines the length of the sequencer operation that determines the "ADC Readout Limitation" (Equation 5) listed in the Sensor Frame Rate section. The instruction set can be shortened through register writes in order to achieve faster frame rates. Instructions for shortening the sequencer can be found in the AR0330 Developer Guide.

The sequencer digital block can be reprogrammed using the following instructions:

Program a new sequencer.
1. Place the sensor in standby.
2. Write 0x8000 to R0x3088 ("seq_ctrl_port").
3. Write each instruction incrementally to R0x3086. Each write must be 16-bit consisting of two bytes {Byte[N], Byte[N+1]}.
4. If the sequencer consists of an odd number of bytes, set the last byte to "0".

Read the instructions stored in the sequencer.
1. Place the sensor in standby.
2. Write 0xC000 to R0x3088 ("seq_ctrl_port").
3. Sequentially read one byte at a time from R0x3086 with 8-bit read command.

SENSOR PLL

VCO

The sensor contains a phase-locked loop (PLL) that is used for timing generation and control. The required VCO clock frequency is attained through the use of a pre-PLL clock divider followed by a multiplier (see Figure 17). The multiplier is followed by set of dividers used to generate the output clocks required for the sensor array, the pixel analog and digital readout paths, and the output parallel and serial interfaces.

Dual Readout Paths

There are two readout paths within the sensor digital block (see Figure 18).

The sensor row timing calculations refers to each data-path individually. For example, the sensor default configuration uses 1248 clocks per row (line_length_pck) to output 2304 active pixels per row. The aggregate clocks per row seen by the receiver will be 2496 clocks (1248 × 2 readout paths).
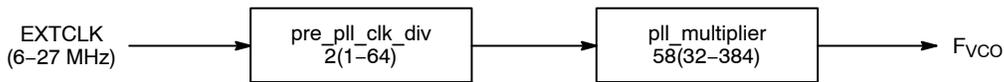

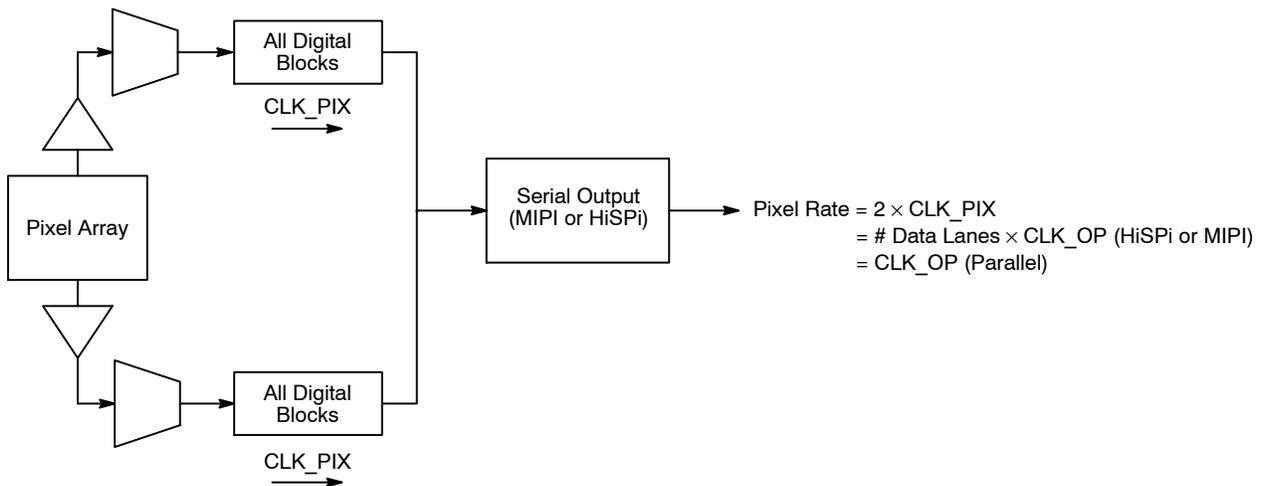**Figure 17. Relationship between Readout Clock and Peak Pixel Rate**

Figure 18. Sensor Dual Readout Paths
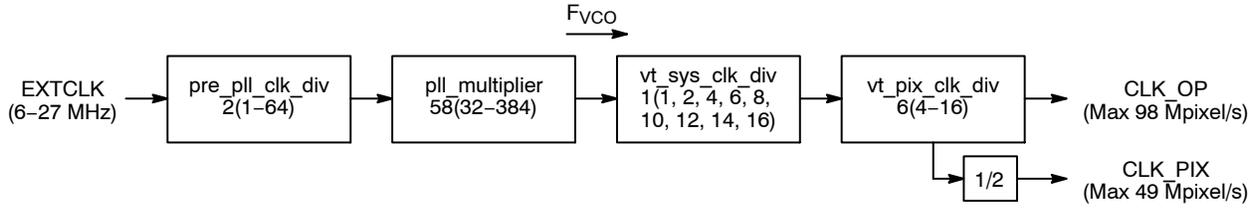
Parallel PLL Configuration

Figure 19. PLL for the Parallel Interface
(The parallel interface has a maximum output data-rate of 98 Mpixel/s)

The maximum output of the parallel interface is 98 Mpixel/s (CLK_OP). This will limit the readout clock (CLK_PIX) to 49 Mpixel/s. The sensor will not use the F_{SERIAL}, F_{SERIAL_CLK}, or CLK_OP when configured to use the parallel interface.

Table 25. PLL PARAMETERS FOR THE PARALLEL INTERFACE

Symbol	Parameter	Min	Max	Unit
EXTCLK	External Clock	6	27	MHz
F_{VCO}	VCO Clock	384	768	MHz
CLK_PIX	Readout Clock		49	Mpixel/s
CLK_OP	Output Clock		98	Mpixel/s

Table 26. EXAMPLE PLL CONFIGURATION FOR THE PARALLEL INTERFACE

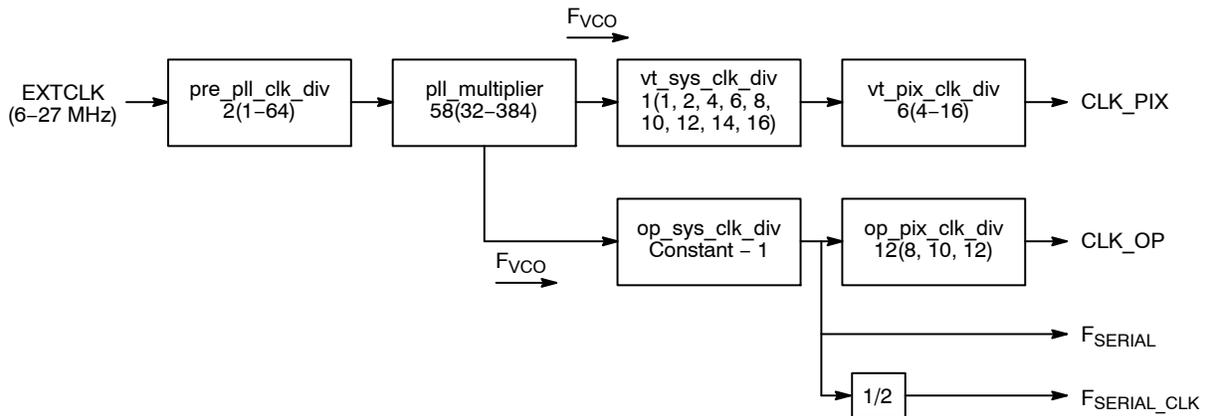| Parameter	Value	Output
F_{VCO}		588 MHz (Max)
vt_sys_clk_div	1	
vt_pix_clk_div	6	
CLK_PIX		49 Mpixel/s (= 588 MHz/12)
CLK_OP		98 Mpixel/s (= 588 MHz/6)
Output Pixel Rate		98 Mpixel/s

Serial PLL Configuration

Figure 20. PLL for the Serial Interface

The sensor will use op_sys_clk_div and op_pix_clk_div to configure the output clock per lane (CLK_OP). The configuration will depend on the number of active lanes (1, 2, or 4) configured. To configure the sensor protocol and number of lanes, refer to "Serial Configuration".

Table 27. PLL PARAMETERS FOR THE SERIAL INTERFACE

Symbol	Parameter	Min	Max	Unit
EXTCLK	External Clock	6	27	MHz
F_{VCO}	VCO Clock	384	768	MHz
CLK_PIX	Readout Clock	–	98	Mpixel/s
CLK_OP	Output Clock	–	98	Mpixel/s
F_{SERIAL}	Output Serial Data Rate Per Lane HiSPi MIPI	300 384	700 768	Mbps
F_{SERIAL_CLK}	Output Serial Clock Speed Per Lane HiSPIi MIPI	150 192	350 384	MHz

The serial output should be configured so that it adheres to the following rules:

- The maximum data-rate per lane (F_{SERIAL}) is 768 Mbps/lane (MIPI) and 700 Mbps/lane (HiSPi).
- The output pixel rate per lane (CLK_OP) should be configured so that the sensor output pixel rate matches the peak pixel rate ($2 \times$ CLK_PIX):

- 4-lane: $4 \times$ CLK_OP = $2 \times$ CLK_PIX = Pixel Rate (max: 196 Mpixel/s)
- 2-lane: $2 \times$ CLK_OP = $2 \times$ CLK_PIX = Pixel Rate (max: 98 Mpixel/s)
- 1-lane: $1 \times$ CLK_OP = $2 \times$ CLK_PIX = Pixel Rate (max: 76 Mpixel/s)

Table 28. EXAMPLE PLL CONFIGURATIONS FOR THE SERIAL INTERFACE

Parameter	4-lane		2-lane		1-lane			Unit
	12-bit	10-bit	12-bit	10-bit	12-bit	10-bit	8-bit	
F_{VCO}	588	490	588	490	768	768	768	MHz
vt_sys_clk_div	1	1	2	2	4	4	4	
vt_pix_clk_div	6	5	6	5	6	5	4	
op_sys_clk_div	1	1	1	1	1	1	1	
op_pix_clk_div	12	10	12	10	12	10	8	
F_{SERIAL}	588	490	588	490	768	768	768	MHz
F_{SERIAL_CLK}	294	245	294	245	384	384	384	MHz
CLK_PIX	98	98	49	49	32	38.4	48	Mpixel/s
CLK_OP	49	49	49	49	64	76.8	96	Mpixel/s
Pixel Rate	196	196	98	98	64	76.8	96	Mpixel/s

PIXEL OUTPUT INTERFACES

Parallel Interface

The parallel pixel data interface uses these output-only signals:

- FV
- LV
- PIXCLK
- $D_{OUT}[11:0]$

The parallel pixel data interface is disabled by default at power up and after reset. It can be enabled by programming R0x301A. Table 30 shows the recommended settings.

When the parallel pixel data interface is in use, the serial data output signals can be left unconnected. Set reset_register[12] to disable the serializer while in parallel output mode.

Output Enable Control

When the parallel pixel data interface is enabled, its signals can be switched asynchronously between the driven and High−Z under pin or register control, as shown in Table 29. OE_BAR pin is only available on the bare die version.

Table 29. OUTPUT ENABLE CONTROL

OE_BAR Pin	Drive Signals R0x301A−B[6]	Description
Disabled	0	Interface High−Z
Disabled	1	Interface Driven
1	0	Interface High−Z
X	1	Interface Driven
0	X	Interface Driven

Configuration of the Pixel Data Interface

Fields in R0x301A are used to configure the operation of the pixel data interface. The supported combinations are shown in Table 30.

Table 30. CONFIGURATION OF THE PIXEL DATA INTERFACE

Serializer Disable R0x301A−B[12]	Parallel Enable R0x301A−B[7]	Standby End-of-Frame R0x301A−B[7]	Description
0	0	1	Power up default. Serial pixel data interface and its clocks are enabled. Transitions to soft standby are synchronized to the end of frames on the serial pixel data interface.
1	1	0	Parallel pixel data interface, sensor core data output. Serial pixel data interface and its clocks disabled to save power. Transitions to soft standby are synchronized to the end of the current row readout on the parallel pixel data interface.
1	1	1	Parallel pixel data interface, sensor core data output. Serial pixel data interface and its clocks disabled to save power. Transitions to soft standby are synchronized to the end of frames in the parallel pixel data interface.

High Speed Serial Pixel Data Interface

The High Speed Serial Pixel (HiSPi) interface uses four data and one clock low voltage differential signaling (LVDS) outputs.

- SLVSC_P
- SLVSC_N
- SLVS0_P
- SLVS0_N
- SLVS1_P
- SLVS1_N
- SLVS2_P
- SLVS2_N
- SLVS3_P
- SLVS3_N

The HiSPi interface supports three protocols, Streaming S, Streaming SP, and Packetized SP. The streaming protocols conform to a standard video application where each line of active or intra-frame blanking provided by the sensor is transmitted at the same length. The Packetized SP protocol will transmit only the active data ignoring line-to-line and frame-to-frame blanking data.

These protocols are further described in the High-Speed Serial Pixel (HiSPi) Interface Protocol Specification V1.00.00.

The HiSPi interface building block is a unidirectional differential serial interface with four data and one double data rate (DDR) clock lanes. One clock for every four serial data lanes is provided for phase alignment across multiple lanes. Figure 21 shows the configuration between the HiSPi transmitter and the receiver.