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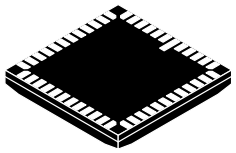
AR0331

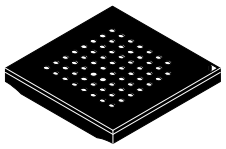
AR0331 1/3-Inch 3.1 Mp/Full HD Digital Image Sensor

ON Semiconductor®

www.onsemi.com



ILCC48 10x10
CASE 847AG



IBGA52 9x9
CASE 503AA

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

General Description

The ON Semiconductor AR0331 is a 1/3-inch CMOS digital image sensor with an active-pixel array of 2048 (H) x 1536 (V). It captures images in either linear or high dynamic range modes, with a rolling-shutter readout. It includes sophisticated camera functions such as in-pixel binning, windowing and both video and single frame modes. It is designed for both low light and high dynamic range scene performance. It is programmable through a simple two-wire serial interface. The AR0331 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including surveillance and HD video.

The ON Semiconductor AR0331 can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 1080p-resolution image at 60 frames per second (fps). In linear mode, it outputs 12-bit or 10-bit A-Law compressed raw data, using either the parallel or serial (HiSPi) output ports. In high dynamic range mode, it outputs 12-bit compressed data using parallel output. In HiSPi mode, 12- or 14-bit compressed, or 16-bit linearized data may be output. The device may be operated in video (master) mode or in single frame trigger mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock in parallel mode.

The AR0331 includes additional features to allow application-specific tuning: windowing and offset, auto black level correction, and on-board temperature sensor. Optional register information and histogram statistic information can be embedded in the first and last 2 lines of the image frame.

The sensor is designed to operate in a wide temperature range (–30°C to +85°C).

Features

- Superior Low-light Performance
- Latest 2.2 μm Pixel with ON Semiconductor A-Pix™ Technology
- Full HD Support at 1080 P 60 fps for Superior Video Performance
- Linear or High Dynamic Range Capture
- 3.1 M (4:3) and 1080 P Full HD (16:9) Images
- Optional Adaptive Local Tone Mapping (ALTM)
- Interleaved T1/T2 Output
- Support for External Mechanical Shutter
- Support for External LED or Xenon Flash
- Slow-motion Video (VGA 120 fps)
- On-chip Phase-locked Loop (PLL) Oscillator
- Integrated Position-based Color and Lens Shading Correction
- Slave Mode for Precise Frame-rate Control
- Stereo/3D Camera Support
- Statistics Engine
- Data Interfaces: Four-lane Serial High-speed Pixel Interface (HiSPi) Differential Signaling (SLVS and HiVCM), or Parallel
- Auto Black Level Calibration
- High-speed Context Switching
- Temperature Sensor

Applications

- Video Surveillance
- Stereo Vision
- Smart Vision
- Automation
- Machine Vision
- 1080p60 Video Applications
- High Dynamic Range Imaging

Table 1. KEY PARAMETERS

Parameter		Typical Value
Optical Format		1/3-inch (5.8 mm) Note: Sensor optical format will also work with lenses designed for 1/3.2" format.
Active Pixels		2048 (H) x 1536 (V) (4:3, mode)
Pixel Size		2.2 μm x 2.2 μm
Color Filter Array		RGB Bayer
Shutter Type		Electronic rolling shutter and GRR
Input Clock Range		6 – 48 MHz
Output Clock Maximum		148.5 Mp/s (4-lane HiSPi) 74.25 Mp/s (Parallel)
Output	Serial	HiSPi 10-, 12-, 14-, or 16-bit
	Parallel	10-, 12-bit
Frame Rate	Full Resolution	30 fps
	1080p	60 fps
Responsivity		1.9 V/lux-sec
SNR_{MAX}		39 dB
Max Dynamic Range		Up to 100 dB
Supply Voltage	I/O	1.8 or 2.8 V
	Digital	1.8 V
	Analog	2.8 V
	HiSPi	0.3 V–0.6 V, 1.7 V–1.9 V
Power Consumption (Typical)		<780 mW
Operating Temperature (Ambient)		–30°C to +85° C
Package Options		10 x 10 mm 48 pin iLCC 9.5 x 9.5 mm 63-pin iBGA

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
AR0331SRSC00SHCA0-DRBR	48-pin iLCC HiSPi, 0° CRA	Dry Pack without Protective Film, Double Side BBAR Glass
AR0331SRSC00SHCAD3-GEVK	48-pin iLCC HiSPi, 0° CRA	Demo Kit 3
AR0331SRSC00SHCAD-GEVK	48-pin iLCC HiSPi, 0° CRA	Demo Kit
AR0331SRSC00SHCAH-GEVB	48-pin iLCC HiSPi, 0° CRA	Demo Board
AR0331SRSC00SUCA0-DPBR	48-pin iLCC Parallel, 0° CRA	Dry Pack with Protective Film, Double Side BBAR Glass
AR0331SRSC00SUCA0-DRBR	48-pin iLCC Parallel, 0° CRA	Dry Pack without Protective Film, Double Side BBAR Glass
AR0331SRSC00SUCAD3-GEVK	48-pin iLCC Parallel, 0° CRA	Demo Kit 3
AR0331SRSC00SUCAD-GEVK	48-pin iLCC Parallel, 0° CRA	Demo Kit
AR0331SRSC00SUCAH-GEVB	48-pin iLCC Parallel, 0° CRA	Demo Board
AR0331SRSC00XUEAD3-GEVK	63-pin iBGA	Demo Kit 3
AR0331SRSC00XUEAD-GEVK	63-pin iBGA	Demo Kit
AR0331SRSC00XUEAH-GEVB	63-pin iBGA	Demo Board
AR0331SRSC00XUEE0–BY–DRBR	63-pin iBGA, 0° CRA	Dry Pack without Protective Film, Double Side BBAR Glass
AR0331SRSC00XUEE0-DPBR	63-pin iBGA, 0° CRA	Dry Pack with Protective Film, Double Side BBAR Glass
AR0331SRSC00XUEE0-DRBR	63-pin iBGA, 0° CRA	Dry Pack without Protective Film, Double Side BBAR Glass
AR0331SRSC00XUEE0-DRBR1	63-pin iBGA, 0° CRA	Dry Pack without Protective Film, Double Side BBAR Glass

FUNCTIONAL OVERVIEW

The AR0331 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 48 MHz. The maximum output pixel rate is 148.5 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor.

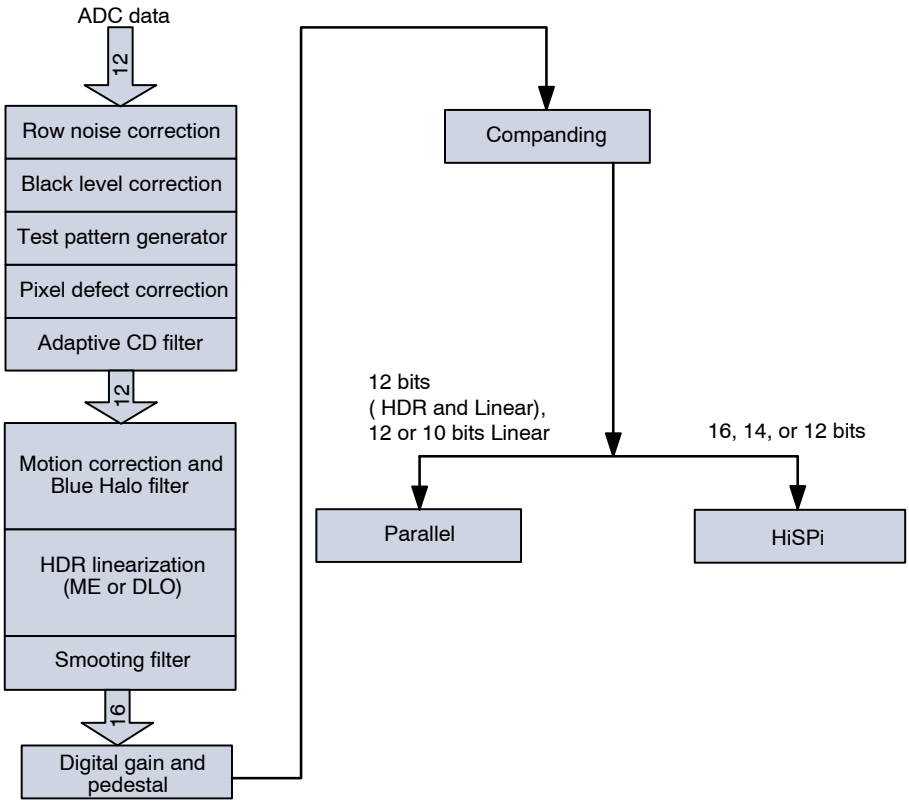
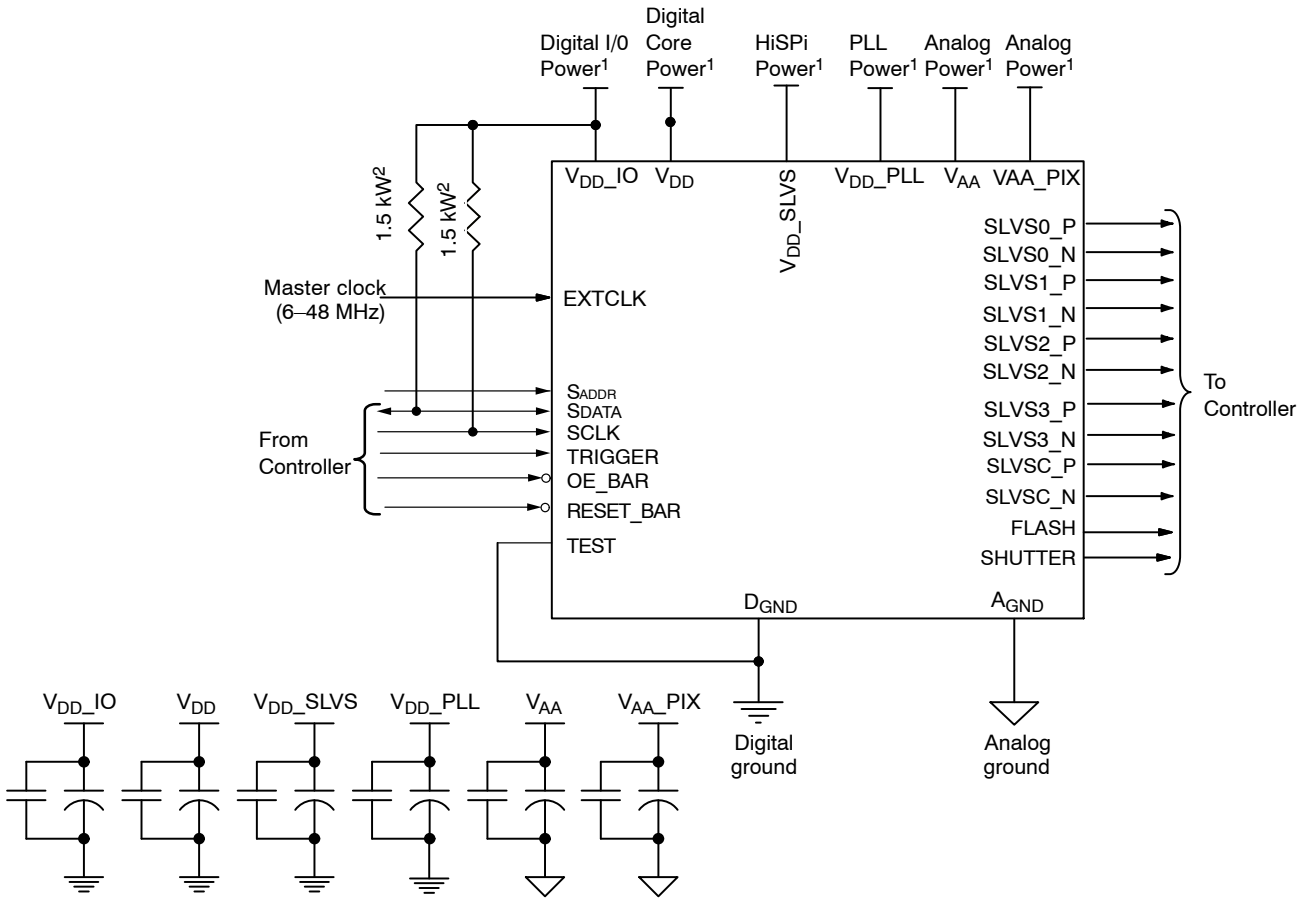


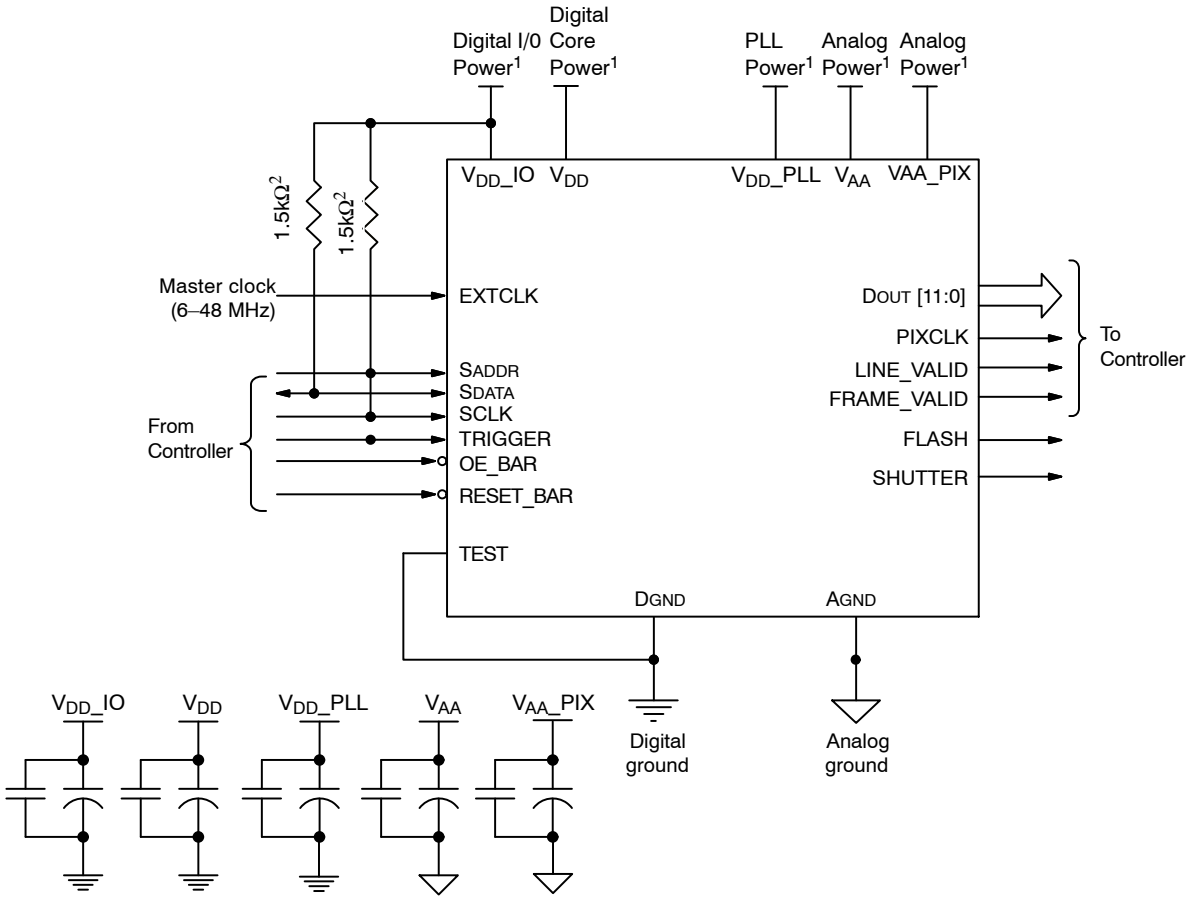
Figure 1. Block Diagram

User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 3.1 Mp Active-pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor also offers a high dynamic range mode of operation where multiple images are combined on-chip to produce a single image at 16-bit per pixel value. A compression mode is further offered to allow the 16-bit pixel value to be transmitted to the host system as a 12-bit value with close to zero loss in image quality.



Notes:
1. All power supplies should be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. The parallel interface output pads can be left unconnected if the serial output interface is used.
4. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0331 demo headboard schematics for circuit recommendations.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match VDD_IO voltage to minimize any leakage currents.

Figure 2. Typical Configuration: Serial Four-Lane HiSPi Interface



Notes:
1. All power supplies should be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. The serial interface output pads and VDDSLVS can be left unconnected if the parallel output interface is used.
4. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0331 demo headboard schematics for circuit recommendations.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match VDD_IO voltage to minimize any leakage currents.
7. The EXTCLK input is limited to 6–48 MHz.

Figure 3. Typical Configuration: Parallel Pixel Data Interface

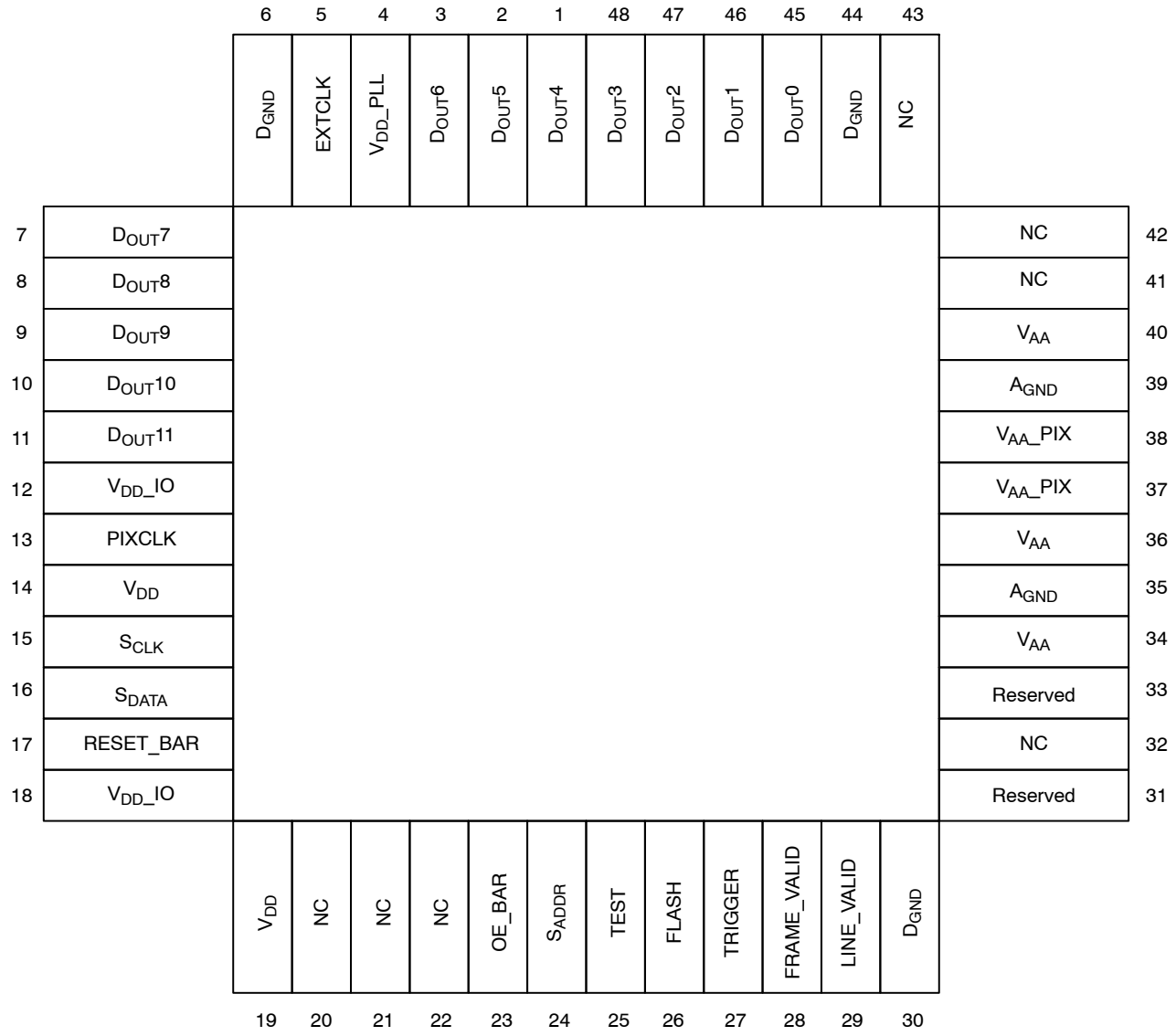


Figure 4. 48 iLCC Package, Parallel Output

Table 3. PIN DESCRIPTION

Pin Number	Name	Type	Description
1	DOUT4	Output	Parallel Pixel Data Output
2	DOUT5	Output	Parallel Pixel Data Output
3	DOUT6	Output	Parallel Pixel Data Output
4	VDD_PLL	Power	PLL Power
5	EXTCLK	Input	External Input Clock
6	DGND	Power	Digital Ground
7	DOUT7	Output	Parallel Pixel Data Output
8	DOUT8	Output	Parallel Pixel Data Output
9	DOUT9	Output	Parallel Pixel Data Output
10	DOUT10	Output	Parallel Pixel Data Output

Table 3. PIN DESCRIPTION (continued)

Pin Number	Name	Type	Description
11	DOUT11	Output	Parallel Pixel Data Output (MSB)
12	VDD_IO	Power	I/O Supply Power
13	PIXCLK	Output	Pixel Clock Out. DOUT is Valid on Rising Edge of this Clock
14	VDD	Power	Digital Power
15	SCLK	Input	Two-wire Serial Clock Input
16	SDATA	I/O	Two-wire Serial Data I/O
17	RESET_BAR	Input	Asynchronous Reset (Active LOW). All Settings are Restored to Factory Default
18	VDD_IO	Power	I/O Supply Power
19	VDD	Power	Digital Power
20	NC		
21	NC		
22	NC		
23	OE_BAR	Input	Output Enable (Active LOW)
24	SADDR	Input	Two-wire Serial Address Select. 0: 0x20. 1: 0x30
25	TEST	Input	Manufacturing Test Enable Pin (Connect to DGND)
26	FLASH	Output	Flash Output Control
27	TRIGGER	Input	Receives Slave Mode VD Signal for Frame Rate Synchronization and Trigger to Start a GRR Frame
28	FRAME_VALID	Output	Asserted when DOUT Frame Data is Valid
29	LINE_VALID	Output	Asserted when DOUT Line Data is Valid.
30	DGND	Power	Digital Ground
31	Reserved		
32	SHUTTER	Output	Control for External Mechanical Shutter. Can be Left Floating if not Used
33	Reserved		
34	VAA	Power	Analog Power
35	AGND	Power	Analog Ground
36	VAA	Power	Analog Power
37	VAA_PIX	Power	Pixel Power
38	VAA_PIX	Power	Pixel Power
39	AGND	Power	Analog Ground
40	VAA	Power	Analog Power
41	NC		
42	NC		
43	NC		
44	DGND	Power	Digital Ground
45	DOUT0	Output	Parallel Pixel Data Output (LSB)
46	DOUT1	Output	Parallel Pixel Data Output
47	DOUT2	Output	Parallel Pixel Data Output
48	DOUT3	Output	Parallel Pixel Data Output

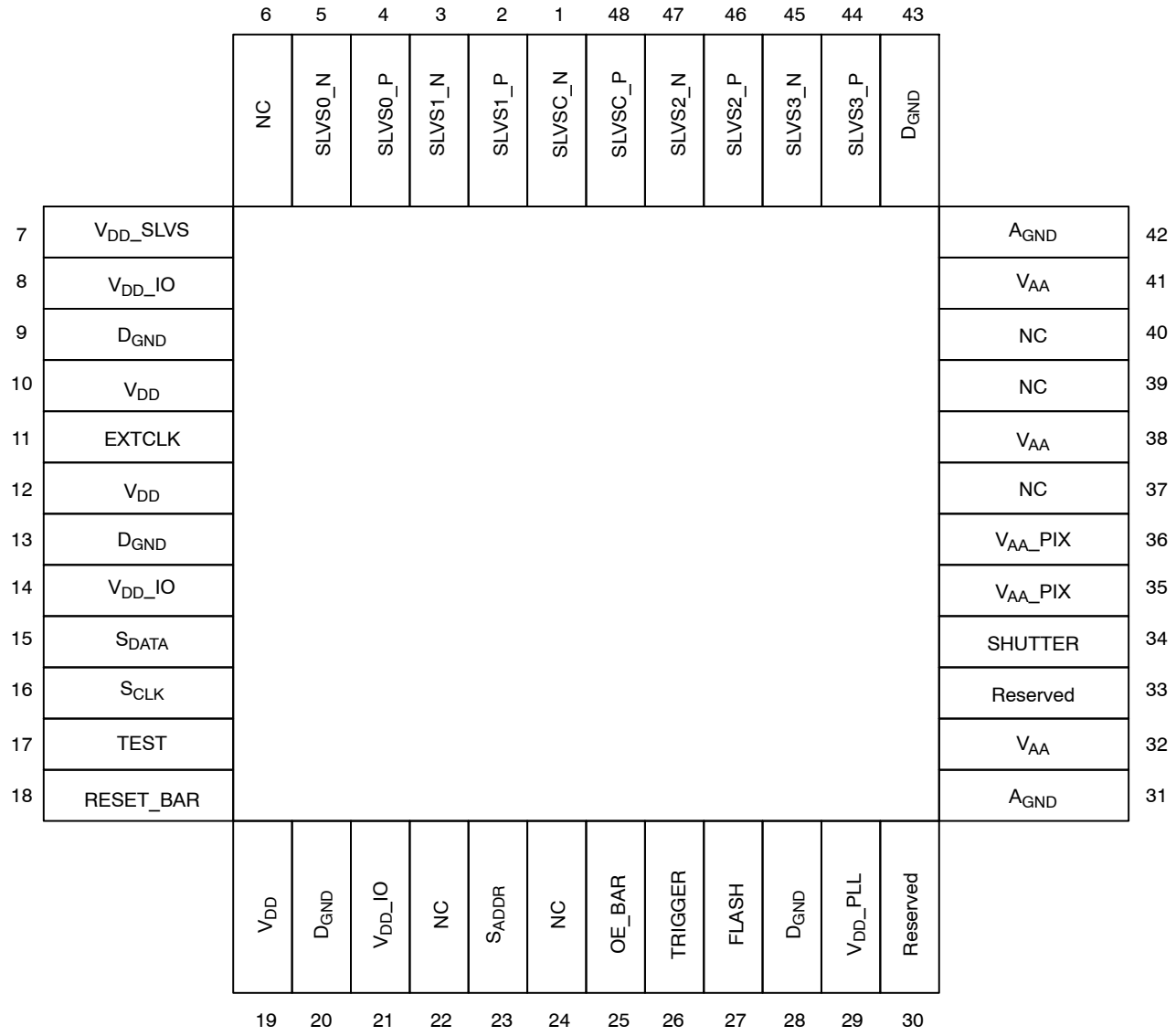


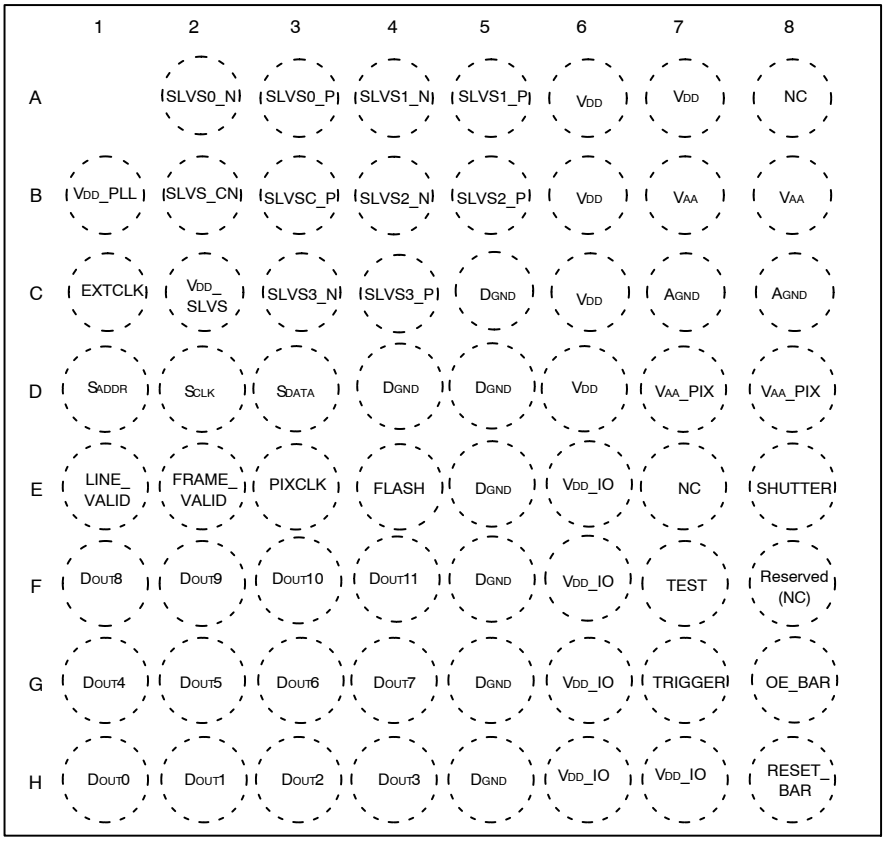
Figure 5. 48 iLCC Package, HiSPi Output

Table 4. PIN DESCRIPTION, 48 ILCC

Pin Number	Name	Type	Description
1	SLVSC_N	Output	HiSPi Serial DDR Clock Differential N
2	SLVS1_P	Output	HiSPi Serial Data, Lane 1, Differential P
3	SLVS1_N	Output	HiSPi Serial Data, Lane 1, Differential N
4	SLVS0_P	Output	HiSPi Serial Data, Lane 0, Differential P
5	SLVS0_N	Output	HiSPi Serial Data, Lane 0, Differential N
6	NC		
7	VDD_SLVS	Power	0.3 V−0.6 V or 1.7 V−1.9 V Port to HiSPi Output Driver. Set the High_VCM (R0x306E[9]) Bit to 1 when Configuring VDD_SLVS to 1.7−1.9 V
8	VDD_IO	Power	I/O Supply Power
9	DGND	Power	Digital Ground
10	VDD	Power	Digital Power

Table 4. PIN DESCRIPTION, 48 ILCC (continued)

Pin Number	Name	Type	Description
11	EXTCLK	Input	External Input Clock
12	VDD	Power	Digital Power
13	DGND		Digital Ground
14	VDD_IO	Power	I/O Supply Power
15	SDATA	I/O	Two-wire Serial Data I/O
16	SCLK	Input	Two-wire Serial Clock Input
17	TEST		Manufacturing Test Enable Pin (Connect to DGND)
18	RESET_BAR	Input	Asynchronous Reset (Active LOW). All Settings are Restored to Factory Default
19	VDD	Power	Digital Power
20	DGND	Power	Digital Ground
21	VDD_IO	Power	I/O Supply Power
22	NC		
23	SADDR	Input	Two-wire Serial Address Select. 0: 0x20. 1: 0x30
24	NC		
25	OE_BAR		Output Enable (active LOW)
26	TRIGGER	Input	Receives Slave Mode VD Signal for Frame Rate Synchronization and Trigger to Start a GRR Frame
27	FLASH	Output	Flash Output Control
28	DGND	Power	
29	VDD_PLL	Power	PLL Power
30	Reserved		
31	AGND	Power	Analog Ground
32	VAA	Power	Analog Power
33	Reserved		
34	SHUTTER	Output	Control for External Mechanical Shutter. Can be Left Floating if not Used
35	VAA_PIX	Power	Pixel Power
36	VAA_PIX	Power	Pixel Power
37	NC		
38	VAA	Power	Analog Power
39	NC		
40	NC		
41	VAA	Power	Analog Power
42	AGND	Power	Analog Ground
43	DGND	Power	Digital Ground
44	SLVS3_P	Output	HiSPi Serial Data, Lane 3, Differential P
45	SLVS3_N	Output	HiSPi Serial Data, Lane 3, Differential N
46	SLVS2_P	Output	HiSPi Serial Data, Lane 2, Differential P
47	SLVS2_N	Output	HiSPi Serial Data, Lane 2, Differential N
48	SLVSC_P	Output	HiSPi Serial DDR Clock Differential P



Top View
(Ball Down)

Figure 6. 9.5 x 9.5 mm 63−Ball IBGA Package

Table 5. PIN DESCRIPTIONS, 9.5 x 9.5 mm, 63-BALL IBGA

Name	iBGA Pin	Type	Description
SLVS0_N	A2	Output	HiSPi Serial Data, Lane 0, Differential N
SLVS0_P	A3	Output	HiSPi Serial Data, Lane 0, Differential P
SLVS1_N	A4	Output	HiSPi Serial Data, Lane 1, Differential N
SLVS1_P	A5	Output	HiSPi Serial Data, Lane 1, Differential P
VDD_PLL	B1	Power	PLL power.
SLVSC_N	B2	Output	HiSPi Serial DDR Clock Differential N
SLVSC_P	B3	Output	HiSPi Serial DDR Clock Differential P
SLVS2_N	B4	Output	HiSPi Serial Data, Lane 2, Differential N
SLVS2_P	B5	Output	HiSPi Serial Data, Lane 2, Differential P
VAA	B7, B8	Power	Analog Power
EXTCLK	C1	Input	External Input Clock.
VDD_SLVS	C2	Power	0.3 V−0.6 V or 1.7 V−1.9 V port to HiSPi Output Driver. Set the High_VCM (R0x306E[9]) bit to 1 when configuring VDD_SLVS to 1.7−1.9 V
SLVS3_N	C3	Output	HiSPi Serial Data, Lane 3, Differential N
SLVS3_P	C4	Output	HiSPi Serial Data, Lane 3, Differential P
DGND	C5, D4, D5, E5, F5, G5, H5	Power	Digital Ground

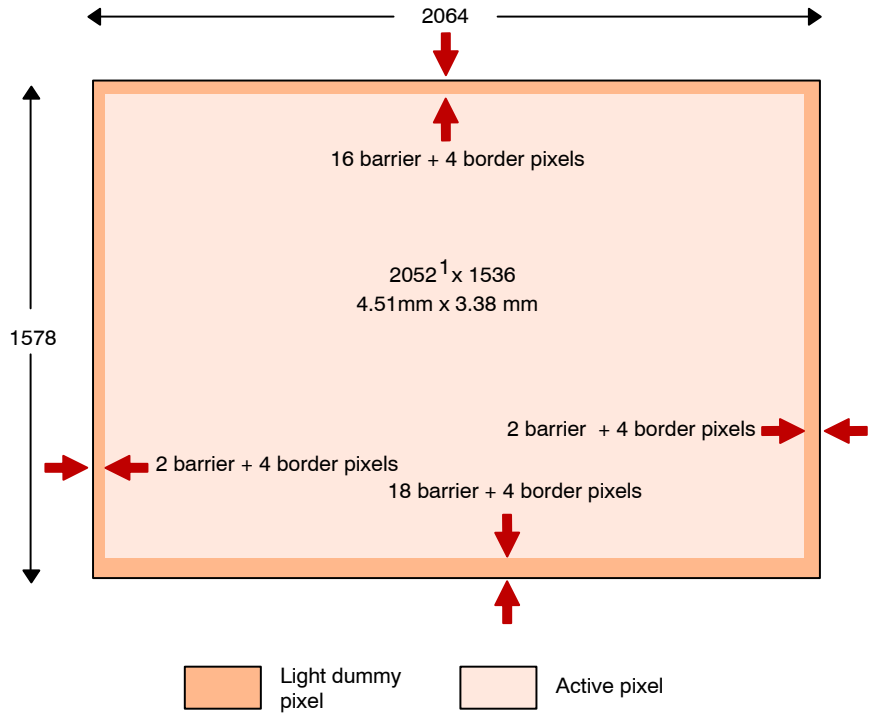
Table 5. PIN DESCRIPTIONS, 9.5 x 9.5 mm, 63-BALL IBGA (continued)

Name	iBGA Pin	Type	Description
VDD	A6, A7, B6, C6, D6	Power	Digital Power
AGND	C7, C8	Power	Analog Ground
SADDR	D1	Input	Two-wire Serial Address Select. 0: 0x20. 1: 0x30
SCLK	D2	Input	Two-wire Serial Clock Input
SDATA	D3	I/O	Two-Wire Serial Data I/O
VAA_PIX	D7, D8	Power	Pixel Power
LINE_VALID	E1	Output	Asserted when DOUT Line Data is Valid
FRAME_VALID	E2	Output	Asserted when DOUT Frame Data is Valid.
PIXCLK	E3	Output	Pixel Clock Out. DOUT is Valid on Rising Edge of this Clock.
VDD_IO	E6, F6, G6, H6, H7	Power	I/O Supply Power
DOUT8	F1	Output	Parallel Pixel Data Output
DOUT9	F2	Output	Parallel Pixel Data Output
DOUT10	F3	Output	Parallel Pixel Data Output
DOUT11	F4	Output	Parallel Pixel Data Output (MSB)
TEST	F7	Input.	Manufacturing Test Enable Pin (Connect to DGND)
DOUT4	G1	Output	Parallel Pixel Data Output
DOUT5	G2	Output	Parallel Pixel Data Output
DOUT6	G3	Output	Parallel Pixel Data Output
DOUT7	G4	Output	Parallel Pixel Data Output
TRIGGER	G7	Input	Exposure Synchronization Input
OE_BAR	G8	Input	Output Enable (Active LOW)
DOUT0	H1	Output	Parallel Pixel Data Output (LSB)
DOUT1	H2	Output	Parallel Pixel Data Output
DOUT2	H3	Output	Parallel Pixel Data Output
DOUT3	H4	Output	Parallel Pixel Data Output
RESET_BAR	H8	Input	Asynchronous reset (active LOW). All settings are restored to factory default
SHUTTER	E8	Output	Control for external mechanical shutter. Can be left floating if not used
FLASH	E4	Output	Flash Control Output
NC	A8, E7		
Reserved	F8		

PIXEL DATA FORMAT

Pixel Array Structure

While the sensor's format is 2048 x 1536, additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for monochrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.



1. Maximum of 2048 columns is supported. Additional columns included for mirroring operations.

Figure 7. Pixel Array Description

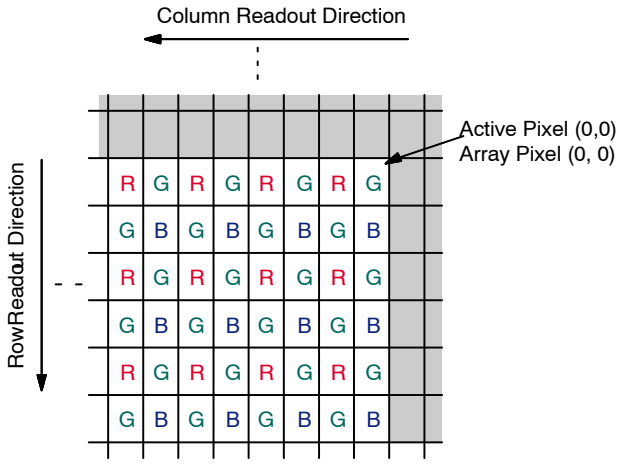


Figure 8. Pixel Color Pattern Detail (Top Right Corner)

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 8). This reflects the actual layout of the array on the die. Also, the first pixel data read out of the sensor in default condition is that of pixel (0, 0).

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 9. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 9.

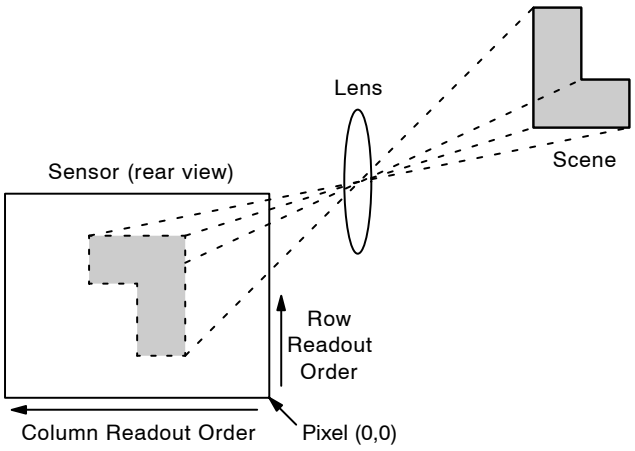


Figure 9. Imaging a Scene

PIXEL OUTPUT INTERFACES

Parallel Interface

The parallel pixel data interface uses these output-only signals:

- FRAME_VALID
- LINE_VALID
- PIXCLK
- DOUT[11:0]

The parallel pixel data interface is disabled by default at power up and after reset. It can be enabled by programming R0x301A. Table 7 shows the recommended settings.

When the parallel pixel data interface is in use, the serial data output signals can be left unconnected. Set reset_register [bit 12 (R0x301A[12] = 1)] to disable the serializer while in parallel output mode.

Output Enable Control

When the parallel pixel data interface is enabled, its signals can be switched asynchronously between the driven and High-Z under pin or register control, as shown in Table 6.

Table 6. OUTPUT ENABLE CONTROL

OE_BAR Pin	Drive Pins R0x301A[6]	Description
1	0	Interface High-Z
X	1	Interface Driven
0	X	Interface Driven

Configuration of the Pixel Data Interface

Fields in R0x301A are used to configure the operation of the pixel data interface. The supported combinations are shown in Table 7.

Table 7. CONFIGURATION OF THE PIXEL DATA INTERFACE

Serializer Disable R0x301 A[12]	Parallel Enable R0x301 A[7]	Description
0	0	Power up default Serial pixel data interface and its clocks are enabled. Transitions to soft standby are synchronized to the end of frames on the serial pixel data interface
1	1	Parallel pixel data interface, sensor core data output. Serial pixel data interface and its clocks disabled to save power. Transitions to soft standby are synchronized to the end of frames in the parallel pixel data interface

High Speed Serial Pixel Data Interface

The High Speed Serial Pixel (HiSPi) interface uses four data lanes and one clock as output.

- SLVSC_P
- SLVSC_N
- SLVS0_P
- SLVS0_N
- SLVS1_P
- SLVS1_N
- SLVS2_P
- SLVS2_N
- SLVS3_P
- SLVS3_N

The HiSPi interface supports three protocols, Streaming-S, Streaming-SP, and Packetized SP. The streaming protocols conform to a standard video application where each line of active or intra-frame blanking provided by the sensor is transmitted at the same length. The Packetized SP protocol will transmit only the active data ignoring line-to-line and frame-to-frame blanking data.

These protocols are further described in the High-Speed Serial Pixel (HiSPi) Interface Protocol Specification V1.50.00.

The HiSPi interface building block is a unidirectional differential serial interface with four data and one double data rate (DDR) clock lanes. One clock for every four serial data lanes is provided for phase alignment across multiple lanes. Figure 10 shows the configuration between the HiSPi transmitter and the receiver.

The HiSPi interface building block is a unidirectional differential serial interface with four data and one double data rate (DDR) clock lanes. One clock for every four serial data lanes is provided for phase alignment across multiple lanes. Figure 10 shows the configuration between the HiSPi transmitter and the receiver.

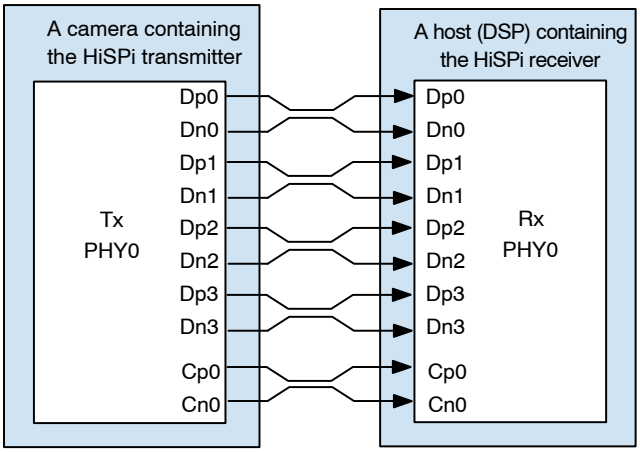


Figure 10. HiSPi Transmitter and Receiver Interface Block Diagram

HiSPi Physical Layer

The HiSPi physical layer is partitioned into blocks of four data lanes and an associated clock lane. Any reference to the PHY in the remainder of this document is referring to this minimum building block.

The PHY will serialize 10-, 12-, 14-, or 16-bit data words and transmit each bit of data centered on a rising edge of the clock, the second on the falling edge of the clock. Figure 11 shows bit transmission. In this example, the word is transmitted in order of MSB to LSB. The receiver latches data at the rising and falling edge of the clock.

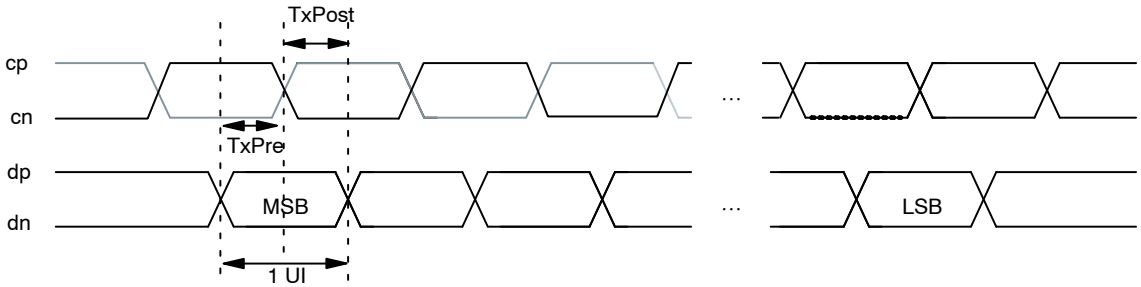


Figure 11. Timing Diagram

DLL Timing Adjustment

The specification includes a DLL to compensate for differences in group delay for each data lane. The DLL is connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. Once the DLL has gained phase lock, each lane can be delayed in 1/8 unit interval (UI) steps. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design.

Delay compensation may be set for clock and/or data lines in the hispi_timing register R0x31C0. If the DLL timing adjustment is not required, the data and clock lane delay settings should be set to a default code of 0x000 to reduce jitter, skew, and power dissipation.

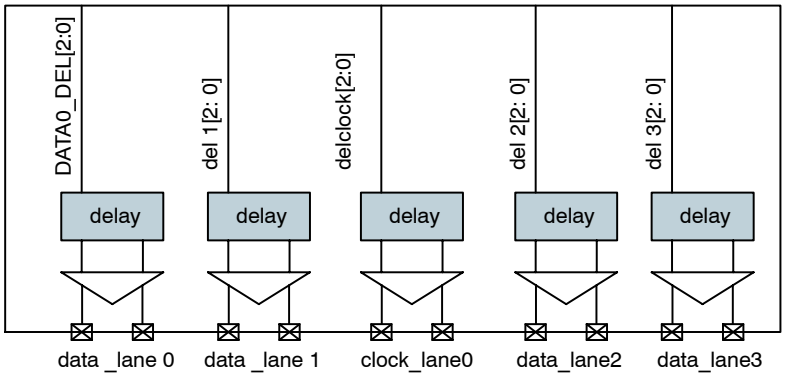


Figure 12. Block Diagram of DLL Timing Adjustment

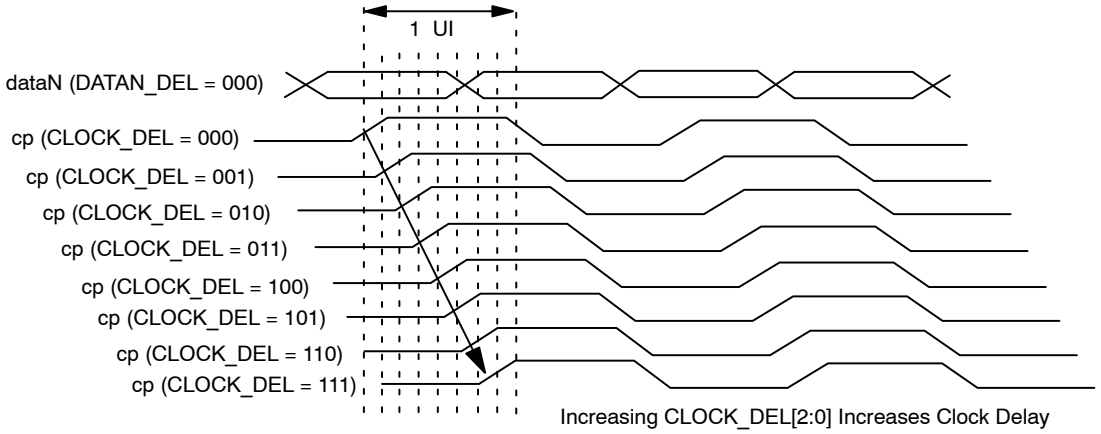


Figure 13. Delaying the Clock with Respect to Data

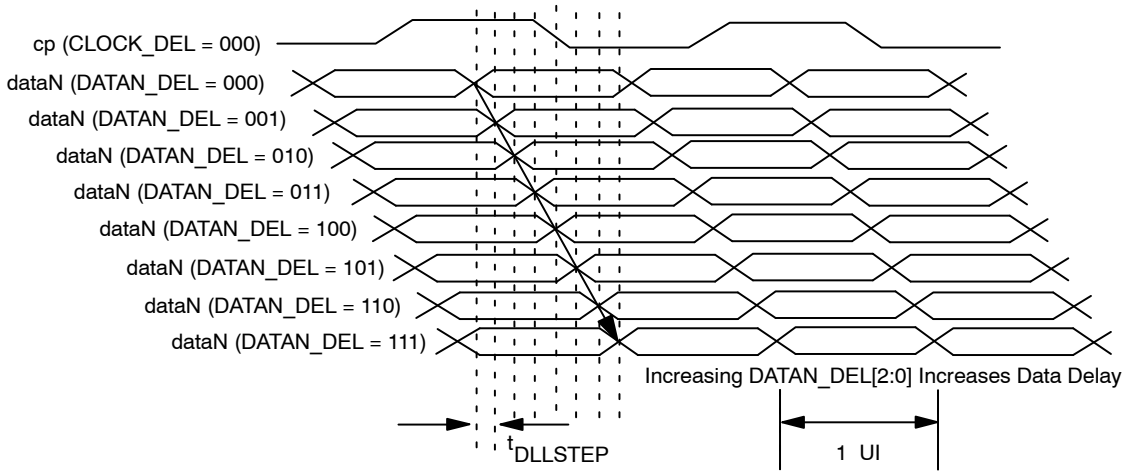


Figure 14. Delaying Data with Respect to the Clock

HiSPi Protocol Layer

The HiSPi protocol is described the HiSPi Protocol Specification document.

Serial Configuration

The serial format should be configured using R0x31AC. Refer to the AR0331 Register Reference document for more detail regarding this register.

The serial_format register (R0x31AE) controls which serial format is in use when the serial interface is enabled (reset_register[12] = 0). The following serial formats are supported:

- 0x0304 – Sensor supports quad-lane HiSPi operation
- 0x0302 – Sensor supports dual-lane HiSPi operation
- 0x0301 – Sensor supports single-lane HiSPi operation

PIXEL SENSITIVITY

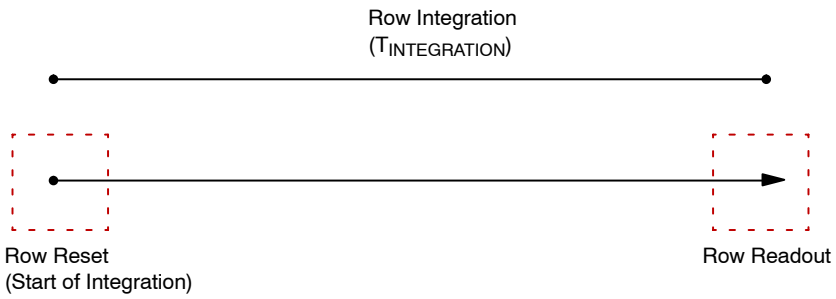


Figure 15. Integration Control in ERS Readout

A pixel's integration time is defined by the number of clock periods between a row's reset and read operation. Both the read followed by the reset operations occur within a row period (T_{ROW}) where the read and reset may be applied to different rows. The read and reset operations will be applied to the rows of the pixel array in a consecutive order.

The coarse integration time is defined by the number of row periods (T_{ROW}) between a row's reset and the row read. The row period is defined as the time between row read operations (see Sensor Frame Rate).

$$T_{COARSE} = T_{ROW} \times coarse\_integration\_time \quad \text{(eq. 1)}$$

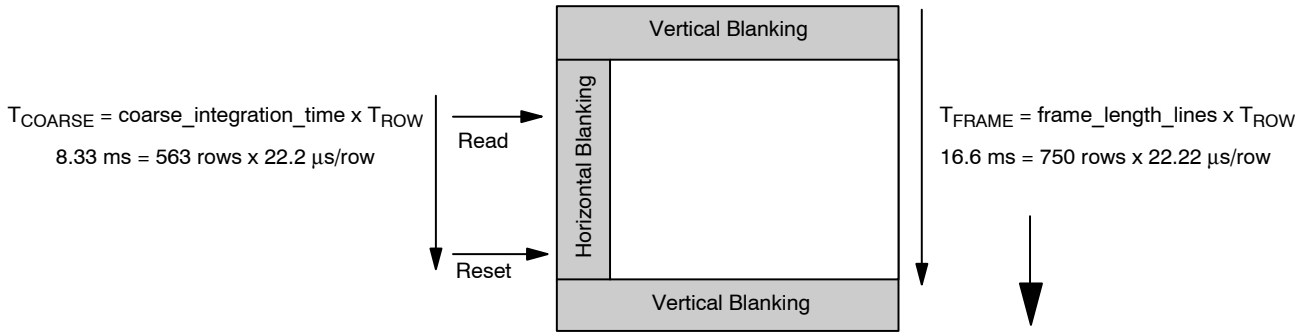


Figure 16. Example of 8.33 ms Integration in 16.6 ms Frame

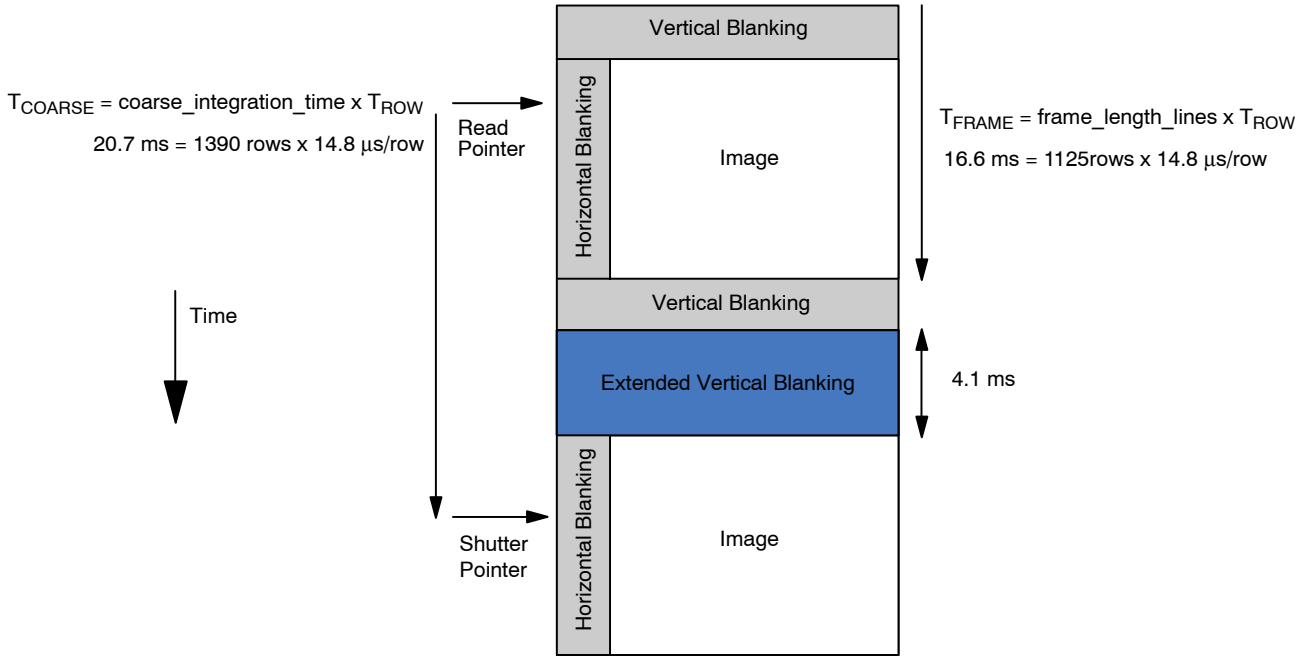


Figure 17. The Row Integration Time is Greater Than the Frame Readout Time

The minimum frame-time is defined by the number of row periods per frame and the row period. The sensor frame-time will increase if the coarse_integration_time is set to a value equal to or greater than the frame_length_lines.

GAIN STAGES

The analog gain stages of the AR0331 sensor are shown in Figure 18. The sensor analog gain stage consists of a variable ADC reference. The sensor will apply the same analog gain to each color channel. Digital gain can be configured to separate levels for each color channel.

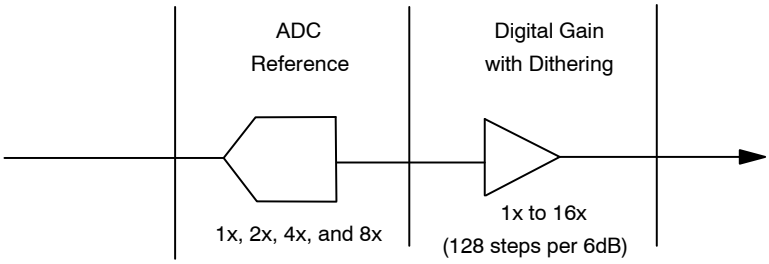


Figure 18. Gain Stages in AR0331 Sensor

The level of analog gain applied is controlled by the coarse_gain register. The recommended analog gain settings are listed in Table 8. A minimum analog gain of 1.23x is recommended. Changes to these registers should be done prior to streaming images.

Table 8. RECOMMENDED SENSOR GAIN

coarse_gain(0x3060[5:4])/ coarse_gain_cb (0x3060[13:12])	fine_gain (0x3060[3:0])/ fine_gain_cb (0x3060[11:8])	ADC Gain
0	6	1.23
0	7	1.28
0	8	1.34
0	9	1.39
0	10	1.45
0	11	1.52
0	12	1.60
0	13	1.69
0	14	1.78
0	15	1.88
1	0	2.00
1	2	2.14
1	4	2.28
1	6	2.47
1	8	2.67
1	10	2.91
1	12	3.20
1	14	3.56
2	0	4
2	4	4.56
2	8	5.34
2	12	6.41
3	0	8

Each digital gain can be configured from a gain of 0 to 15.992. The digital gain supports 128 gain steps per 6dB of gain. The format of each digital gain register is “xxxx.yyyyyyy” where “xxxx” refers an integer gain of 1 to 15 and “yyyyyyy” is a fractional gain ranging from 0/128 to 127/128.

The sensor includes a digital dithering feature to reduce quantization noise resulting from using digital gain. It can be disabled by setting R0x30BA[5] to 0. The default value is 1.

PEDESTALS

There are two types of constant offset pedestals that may be adjusted at the end of the datapath.

The data pedestal is a constant offset that is added to pixel values at the end of the datapath. The default offset when ALTM is disabled is 168 and is a 12-bit offset. This offset matches the maximum range used by the corrections in the digital readout path. The purpose of the data pedestal is to convert negative values generated by the digital datapath into positive output data. It is recommended that the data pedestal be set to 16 when ALTM is enabled.

The data pedestal value can be changed from its default value by adjusting register R0x301E.

The ALTM pedestal (R0x2450) is also located at the end of the datapath. The ALTM pedestal default offset is 0.

HIGH DYNAMIC RANGE MODE

By default, the sensor powers up in HDR Mode. The HDR scheme used is multi-exposure HDR. This allows the sensor to handle up to 100 dB of dynamic range. In HDR mode, the sensor sequentially captures two exposures by maintaining two separate read and reset pointers that are interleaved within the rolling shutter readout. The intermediate pixel values are stored in line buffers while waiting for the two exposure values to be present. As soon as a pixel's two exposure values are available, they are combined to create a linearized 16-bit value for each pixel's response. Depending on whether HiSPi or Parallel mode is selected, the full 16 bit value may be output, it can be compressed to 12 bits using Adaptive Local Tone Mapping (ALTM), or companded to 12 or 14 bits.

Adaptive Local Tone Mapping

Real- world scenes often have a very high dynamic range (HDR) that far exceeds the electrical dynamic range of the imager. Dynamic range is defined as the luminance ratio between the brightest and the darkest objects in a scene. Even though the AR0331 can capture full dynamic range images, the images are still limited by the low dynamic range of display devices. Today's typical LCD monitor has a contrast ratio around 1000:1 while it is not atypical for an HDR image having a contrast ratio of around 250000:1. Therefore, in order to reproduce HDR images on a low dynamic range display device, the captured high dynamic range must be compressed to the available range of the display device. This is commonly called tone mapping. The AR0331 has implemented an adaptive local tone mapping (ALTM) feature to reproduce visually appealing images that increase the local contrast and the visibility of the images. When ALTM is enabled, the gamma in the backend ISP should be set to 1 for proper display.

See the AR0331 Developer Guide for more information on ALTM.

Companding

The 16-bit linearized HDR image may be compressed to 12 bits using on-chip companding. Figure 19 illustrates the compression from 16- to 12-bits. Companding is enabled by setting R0x31D0. Table 10 shows the knee points for the different modes.

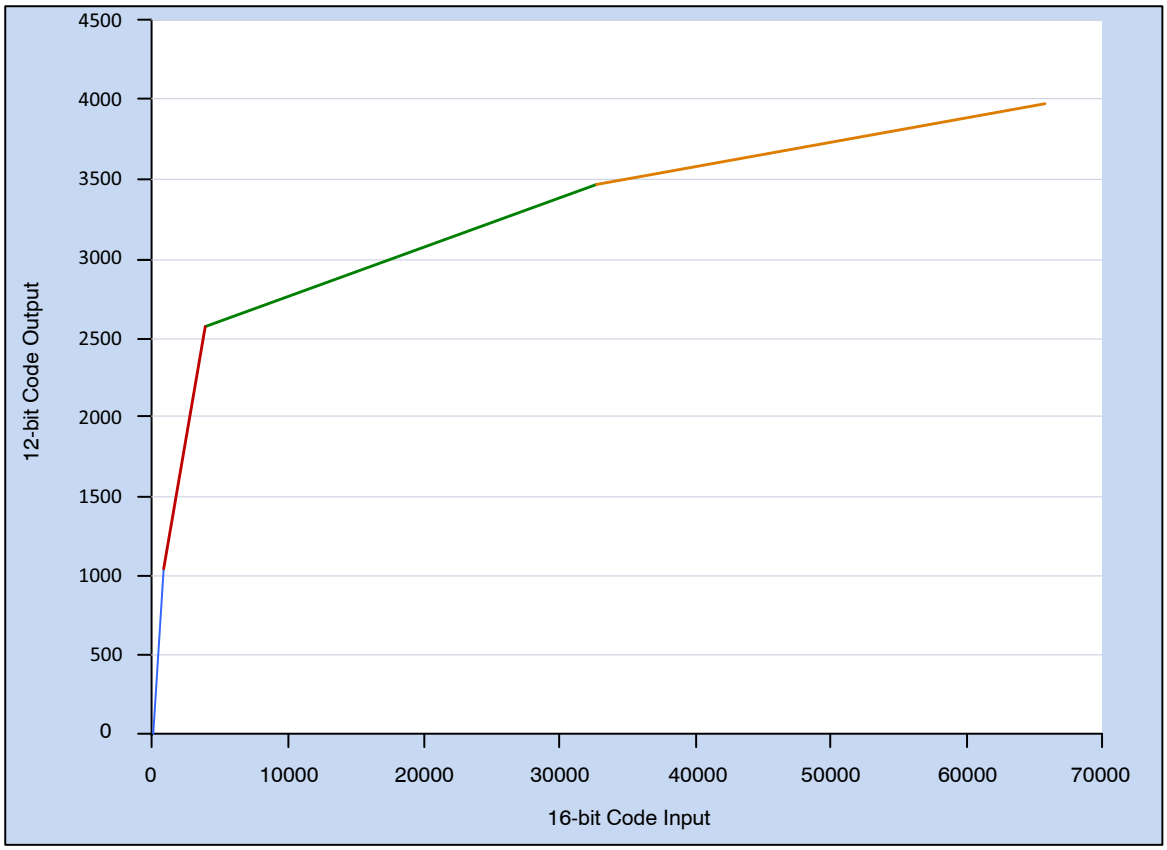


Figure 19. HDR Data Compression

Table 9. COMPANDING TABLE

	Segment 1	Segment 2	Segment 3	Segment 4
Input Code Range	0 to 1023	1024 to 4095	4096 to 32767	32768 to 65535
Output Code Range	0 to 1023	1024 to 2559	2560 to 3455	3456 to 3967
Companding Formula	$P_{out} = P_{in}$	$P_{out} = (P_{in} - 1024)/2 + 1024$	$P_{out} = (P_{in} - 4096)/32 + 2560$	$P_{out} = (P_{in} - 32768)/64 + 3456$
Decompanding Formula	$P_{out} = P_{in}$	$P_{out} = (P_{in} - 1024)*2 + 1024$	$P_{out} = (P_{in} - 2560)*32 + 4096$	$P_{out} = (P_{in} - 3456)*64 + 32768$

Table 9 illustrates the input and output codes as well as companding and decompanding formulas for each of the four colored segments in Figure 19.

Table 10. KNEE POINTS FOR COMPRESSION FROM 16 BITS TO 12 BITS

T1/T2 Exposure Ratio (R1) R0x3082[3:2]	P1	POUT1 = P1	P2	POUT2= (P2 – P1)/2 + 1024	P3	POUT3= (P3 – P2)/32 + 2560	PMAX	POUTMAX = (PMAX – P3)/64 + 3456
4x, 8x, 16x, 32x	2^{10}	1024	2^{12}	2560	2^{15}	3456	2^{16}	3968

As described in Table 10, the AR0331 companding block operates on 16-bit input only. For the exposure ratios that do not result in 16-bits, bit shifting occurs before the data enters the companding block. As a result of the bit shift, data needs to be unshifted after linearization in order to obtain the proper image. Table 11 provides the bit operation that should occur to the data after linearization.

Table 11. BIT OPERATION AFTER LINEARIZATION

ratio_t1_t2 (R0x3082[3:2])/ratio_t1_t2_cb (R0x3084[3:2])	Bit Shift Operation after Linearization
4x	Right Shift 2 Bits
8x	Right Shift 1 Bit
16x	No Shift
32x	Left Shift 1 Bit

HDR-Specific Exposure Settings

In HDR mode, pixel values are stored in line buffers while waiting for both exposures to be available for final pixel data combination. There are 70 line buffers used to store intermediate T1 data. Due to this limitation, the maximum coarse integration time possible for a given exposure ratio is equal to 70*T1/T2 lines.

For example, if R0x3082[3:2] = 2, the sensor is set to have T1/T2 ratio = 16x. Therefore the maximum number of integration lines is 70*16 = 1120 lines. If coarse integration time is greater than this, the T2 integration time will stay at 70. The sensor will calculate the ratio internally, enabling the linearization to be performed. If companding is being used, then relinearization would still follow the programmed ratio. For example if the T1/T2 ratio was programmed to 16x but coarse integration was increased beyond 1120 then one would still use the 16x relinearization formulas.

An additional limitation is the maximum number of exposure lines in relation to the frame_length_lines register. In linear mode, maximum coarse_integration_time = frame_length_lines – 1. However in HDR mode, since the coarse integration time register controls T1, the max coarse integration time is frame_length_lines – 71.

Putting the two criteria listed above together, the formula is as follows:

$$\text{maximum coarse\_integration\_time} = \text{minimum}\left(70 \times \frac{T1}{T2}, \text{frame\_length\_lines} - 71\right) \quad \text{(eq. 2)}$$

There is a limitation of the minimum number of exposure lines, which is one row time for linear mode. In HDR mode, the minimum number of rows required is half of the ratio T1/T2.

Motion Compensation

In typical multi-exposure HDR systems, motion artifacts can be created when objects move during the T1 or T2 integration time. When this happens, edge artifacts can potentially be visible and might look like a ghosting effect.

To correct this, the AR0331 has special 2D motion compensation circuitry that detects motion artifacts and corrects the image.

The motion compensation feature can be enabled by setting R0x318C[14] = 1. Additional parameters are available to control the extent of motion detection and correction as per the requirements of the specific application. For more information, refer to the AR0331 Register Reference document and the AR0331 Developer Guide.

RESET

The AR0331 may be reset by the RESET_BAR pin (active LOW) or the reset register.

Hard Reset of Logic

The RESET_BAR pin can be connected to an external RC circuit for simplicity. The recommended RC circuit uses a 10 kΩ resistor and a 0.1 μF capacitor. The rise time for the RC circuit is 1 μs maximum.

Soft Reset of Logic

Soft reset of logic is controlled by the R0x301A Reset register. Bit 0 is used to reset the digital logic of the sensor. Furthermore, by asserting the soft reset, the sensor aborts the current frame it is processing and starts a new frame. This bit is a self-resetting bit and also returns to “0” during two-wire serial interface reads.

SENSOR PLL

VCO

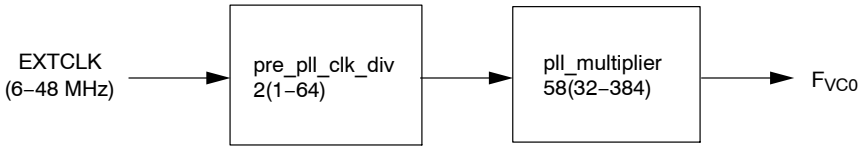


Figure 20. PLL Dividers Affecting VCO Frequency

The sensor contains a phase-locked loop (PLL) that is used for timing generation and control. The required VCO clock frequency is attained through the use of a pre-PLL clock divider followed by a multiplier. The PLL multiplier should be an even integer. If an odd integer (M) is programmed, the PLL will default to the lower (M−1) value to maintain an even multiplier value. The multiplier is followed by a set of dividers used to generate the output clocks required for the sensor array, the pixel analog and digital readout paths, and the output parallel and serial interfaces. Use of the PLL is required when using the HiSPi interface.

Dual Readout Paths

There are two readout paths within the sensor digital block. The sensor PLL should be configured such that the total pixel rate across both readout paths is equal to the output pixel rate. For example, if CLK_PIX is 74.25 MHz in a 4-lane HiSPi configuration, the CLK_OP should be equal to 37.125 MHz.

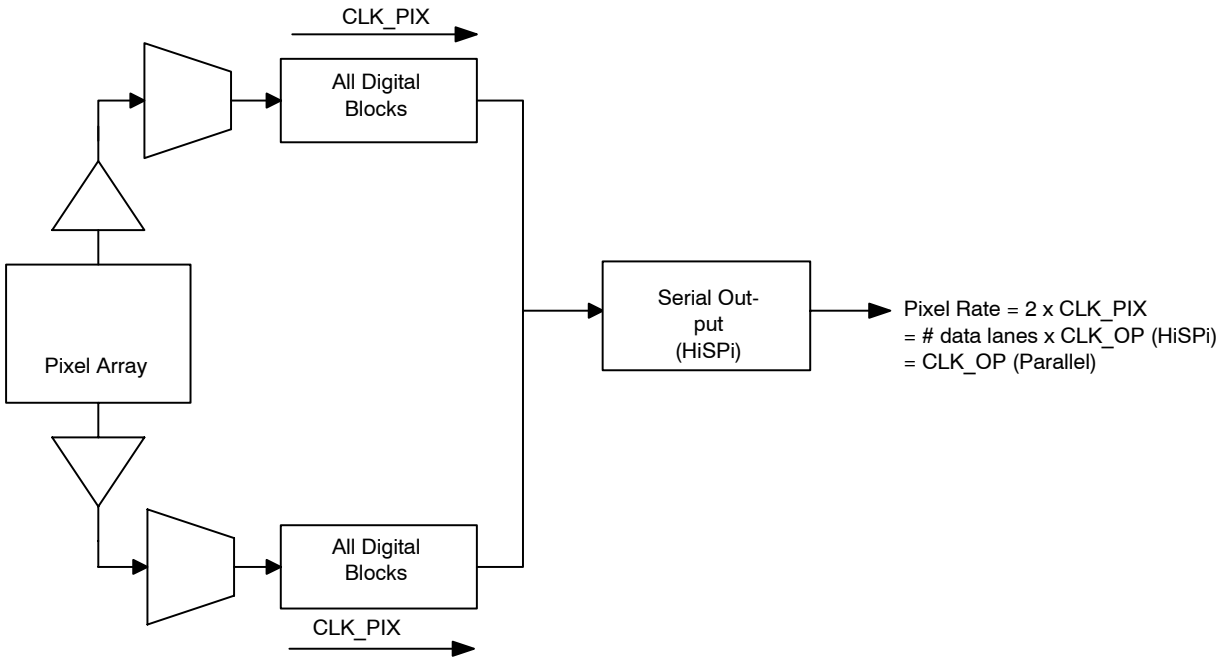


Figure 21. Sensor Dual Readout Paths

The sensor row timing calculation refers to each data-path individually. For example, the sensor default configuration uses 1100 clocks per row (line_length_pck) to output 1928 active pixels per row. The aggregate clocks per row seen by the receiver will be 2200 clocks (1100 x 2 readout paths).

Parallel PLL Configuration

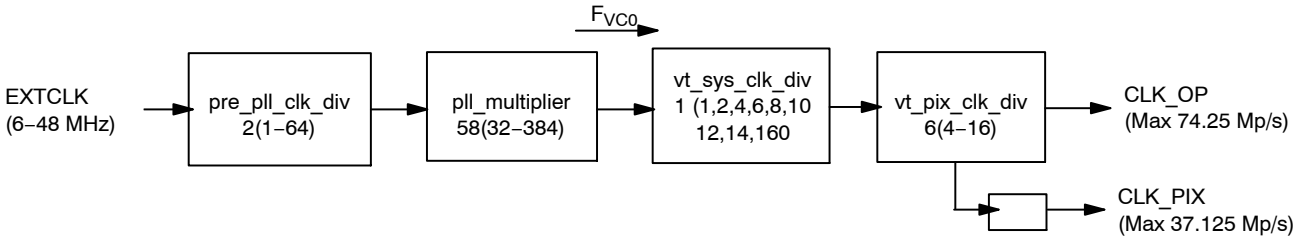


Figure 22. PLL for the Parallel Interface

The maximum output of the parallel interface is 74.25 MPixel/s. This will limit the readout clock (CLK_PIX) to 37.125 MPixel/s. The sensor will not use the F_{SERIAL}, F_{SERIAL_CLK}, or CLK_OP when configured to use the parallel interface.

Table 12. PLL PARAMETERS FOR THE PARALLEL INTERFACE

Parameter	Symbol	Min	Max	Unit
External Clock	EXTCLK	6	48	MHz
VCO Clock	F_{VCO}	384	768	MHz
Readout Clock	CLK_PIX		37.125	Mpixel/s
Output Clock	CLK_OP		74.25	Mpixel/s

Table 13. EXAMPLE PLL CONFIGURATION FOR THE PARALLEL INTERFACE

Parameter	Value	Output
F_{VCO}		445.5 MHz (Max)
vt_sys_clk_div	1	
vt_pix_clk_div	6	
CLK_PIX		37.125 MPixel/s (= 445.5 MHz / 12)
CLK_OP		74.25 MPixel/s (= 445.5 MHz / 6)
Output pixel rate		74.25 MPixel/s

Serial PLL Configuration

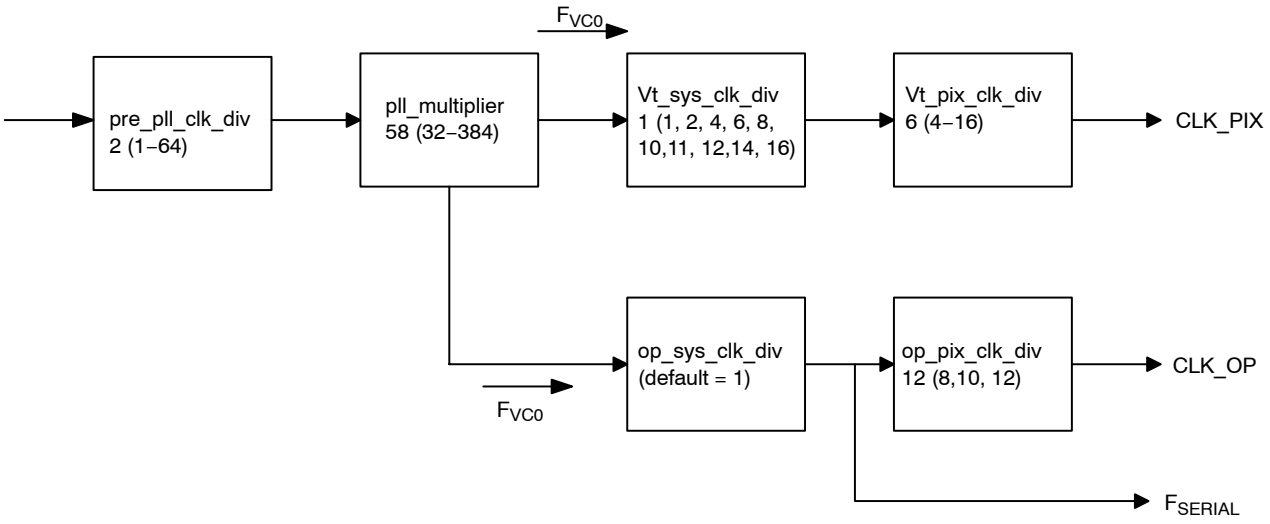


Figure 23. PLL for the Serial Interface

The PLL must be enabled when HiSPi mode is selected. The sensor will use op_sys_clk_div and op_pix_clk_div to configure the output clock per lane (CLK_OP). The configuration will depend on the number of active lanes (1, 2, or 4) configured. To configure the sensor protocol and number of lanes, refer to “Serial Configuration”.

Table 14. PLL PARAMETERS FOR THE SERIAL INTERFACE

Parameter	Symbol	Min	Max	Unit
External Clock	EXTCLK	6	48	MHz
External Clock	EXTCLK	6	48	MHz
VCO Clock	F_{VCO}	384	768	MHz
Readout Clock	CLK_PIX		74.25	Mpixel/s
Output Clock	CLK_OP		37.125	Mpixel/s
Output Serial Data Rate Per Lane	F_{SERIAL}	300 (HiSPi)	700 (HiSPi)	Mbps
Output Serial Clock Speed Per Lane	F_{SERIAL_CLK}	150 (HiSPi)	350 (HiSPi)	MHz

Configure the serial output so that it adheres to the following rules:

- The maximum data-rate per lane (F_{SERIAL}) is 700 Mbps/lane (HiSPi).
- Configure the output pixel rate per lane (CLK_OP) so that the sensor output pixel rate matches the peak pixel rate (2 x CLK_PIX).
  - 4-lane: 4 x CLK_OP = 2 x CLK_PIX = Pixel Rate (max: 148.5 Mpixel/s)
  - 2-lane: 2 x CLK_OP = 2 x CLK_PIX = Pixel Rate (max: 74.25 Mpixel/s)
  - 1-lane: 1 x CLK_OP = 2 x CLK_PIX = Pixel Rate (max: 37.125 Mpixel/s)

Table 15. EXAMPLE PLL CONFIGURATIONS FOR THE SERIAL INTERFACE

Parameter	4-lane				2-lane		1-lane	Units
	16-bit	14-bit	12-bit	10-bit	12-bit	10-bit	10-bit	
F_{VCO}	594	519.75	445.5	742.5	445.5	742.5	742.5	MHz
vt_sys_clk_div	1	1	1	2	1	2	4	
vt_pix_clk_div	8	7	6	5	12	10	10	
op_sys_clk_div	1	1	1	2	1	2	2	
op_pix_clk_div	16	14	12	10	12	10	10	
F_{SERIAL}	594	519.75	445.5	371.25	445.5	371.25	371.25	MHz
F_{SERIAL_CLK}	297	259.875	222.75	185.63	222.75	185.63	185.63	MHz
CLK_PIX	74.25	74.25	74.25	74.25	37.125	37.125	18.563	Mpixel/s
CLK_OP	37.125	37.125	37.125	37.125	37.125	37.125	37.125	Mpixel/s
Pixel Rate	148.5	148.5	148.5	148.5	74.25	74.25	37.125	Mpixel/s

Stream/Standby Control

The sensor supports a soft standby mode. In this mode, the external clock can be optionally disabled to further minimize power consumption. If this is done, then the "Power-Up Sequence" must be followed. When the external clock is disabled, the sensor will be unresponsive to register writes and other operations.

Soft Standby is a low-power state that is controlled through register R0x301A[2]. The sensor will go to Standby after completion of the current frame readout. When the sensor comes back from Soft Standby, previously written register settings are still maintained. Soft Standby will not occur if the Trigger pin is held high.

A specific sequence needs to be followed to enter and exit from Soft Standby.

Entering Soft Standby:

1. Set R0x301A[12] = 1 if serial mode was used
2. Set R0x301A[2] = 0 and drive Trigger pin low.
3. Turn off external clock to further minimize power consumption

Exiting Soft Standby:

1. Enable external clock if it was turned off
2. Set R0x301A[2] = 1 or drive Trigger pin high.
3. Set R0x301A[12] = 0 if serial mode is used