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1/4-Inch 5 Mp CMOS Digital Image Sensor

AR0543 Data Sheet, Rev. F

For the latest data sheet, please visit www.onsemi.com

Features

- Low dark current
- Simple two-wire serial interface
- Auto black level calibration
- Support for external LED or xenon flash
- High frame rate preview mode with arbitrary down-size scaling from maximum resolution
- Programmable controls: gain, horizontal and vertical blanking, auto black level offset correction, frame size/rate, exposure, left–right and top–bottom image reversal, window size, and panning
- Data interfaces: single/dual lanes serial mobile industry processor interface (MIPI)
- On-die phase-locked loop (PLL) oscillator
- Bayer pattern down-size scaler
- Superior low-light performance
- 4 Kb one-time programmable memory (OTPM) for storing shading correction coefficients and module information
- Integrated position and color-based shading correction
- Extended Flash duration that is up to start of frame readout

Applications

- Cellular phones
- Digital still cameras
- PC cameras
- PDAs

General Description

The ON Semiconductor AR0543 is a 1/4-inch CMOS active-pixel digital image sensor with a pixel array of 2592H x 1944V (2608H x 1960V including border pixels). It incorporates sophisticated on-chip camera functions such as windowing, mirroring, column and row skip modes, and snapshot mode. It is programmable through a simple two-wire serial interface and has very low power consumption.

Table 1: Key Performance Parameters

Parameter		Value
Optical format		1/4-inch (4:3)
Active imager size		3.63mm(H)x2.72(V):4.54mm diagonal
Active pixels		2592H x 1944V
Pixel size		1.4 µm x 1.4µm
Chief ray angle		25.0°
Color filter array		RGB Bayer pattern
Shutter type		Electronic rolling shutter (ERS)
Input clock frequency		6–27 MHz
Maximum data rate	MIPI	840 Mbps per lane
Frame rate	Full resolution (2592 x1944)	15 fps
	1080P	19.8 fps(100% FOV, crop to 16:9) 30 fps(77% FOV, crop to 16:9)
	720P	30 fps(98% FOV, crop to 16:9, bin2) 60 fps(98% FOV, crop to 16:9, skip2)
	VGA (640x480)	60 fps(100% FOV, bin2skip2) 115 fps(100% FOV, skip4)
ADC resolution		10-bit, on-die
Responsivity		0.82 V/lux-sec (550nm)
Dynamic range		66 dB
SNR_{MAX}		36.5 dB
Supply voltage	Digital I/O	1.7–1.9 V (1.8 V nominal) or 2.4–3.1 V (2.8 V nominal)
	Digital Core	1.15-1.25(1.2 V nominal)
	Analog	2.6–3.1V (2.8 V nominal)
	Digital 1.8V	1.7–1.9V (1.8 V nominal)
Power Consumption	Full resolution	MIPI: 215 mW at 70°C (TYP)
	Standby	25µW at 70°C (TYP)
Package		Bare die 5.256 x 5.065 mm 45-pin CSP
Operating temperature		–30°C to +70°C (at junction)

Ordering Information

Table 2: Available Part Numbers

Part Number	Product Description	Orderable Product Attribute Description
AR0543CSSC25SMKA0-CR	5 MP 1/4" CIS HB	Chip Tray without Protective Film

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General Description

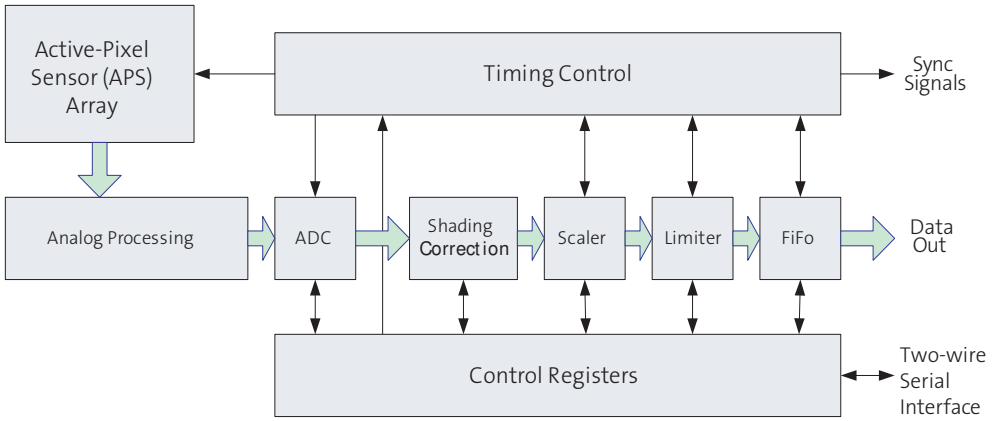
The AR0543 digital image sensor features ON Semiconductor's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The AR0543 sensor can generate full resolution image at up to 15 frames per second (fps). An on-chip analog-to-digital converter (ADC) generates a 10-bit value for each pixel.

Functional Overview

The AR0543 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) to generate all internal clocks from a single master input clock running between 6 and 27 MHz. The maximum pixel rate is 84 Mp/s, corresponding to a pixel clock rate of 84 MHz. A block diagram of the sensor is shown in Figure 1.

Figure 1: Block Diagram



The core of the sensor is a 5Mp active-pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns are sequenced through an analog signal chain (providing offset correction and gain), and then through an ADC. The output from the ADC is a 10-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain).

The pixel array contains optically active and light-shielded ("dark") pixels. The dark pixels are used to provide data for on-chip offset-correction algorithms ("black level" control).

The sensor contains a set of control and status registers that can be used to control many aspects of the sensor behavior including the frame size, exposure, and gain setting. These registers can be accessed through a two-wire serial interface.

The output from the sensor is a Bayer pattern; alternate rows are a sequence of either green and red pixels or blue and green pixels. The offset and gain stages of the analog signal chain provide per-color control of the pixel data.

The control registers, timing and control, and digital processing functions shown in Figure 1 on page 6 are partitioned into three logical parts:

- A sensor core that provides array control and data path corrections. The output of the sensor core is a 10-bit pixel data stream qualified by an output data clock.
- A digital shading correction block to compensate for color/brightness shading introduced by the lens or chief ray angle (CRA) curve mismatch.
- Additional functionality is provided. This includes a horizontal and vertical image scaler, a limiter, a data compressor, an output FIFO, and a serializer.

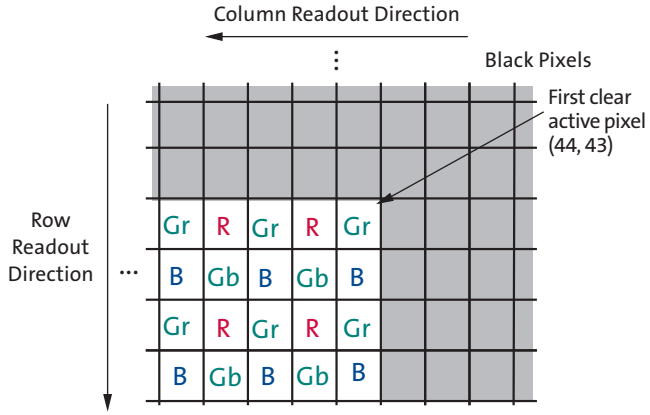
The output FIFO is present to prevent data bursts by keeping the data rate continuous. Programmable slew rates are also available to reduce the effect of electromagnetic interference from the output interface.

A flash output signal is provided to allow an external xenon or LED light source to synchronize with the sensor exposure time.

Pixel Array

The sensor core uses a Bayer color pattern, as shown in Figure 2. The even-numbered rows contain green and red pixels; odd-numbered rows contain blue and green pixels. Even-numbered columns contain green and blue pixels; odd-numbered columns contain red and green pixels.

Figure 2: Pixel Color Pattern Detail (Top Right Corner)



Operating Modes

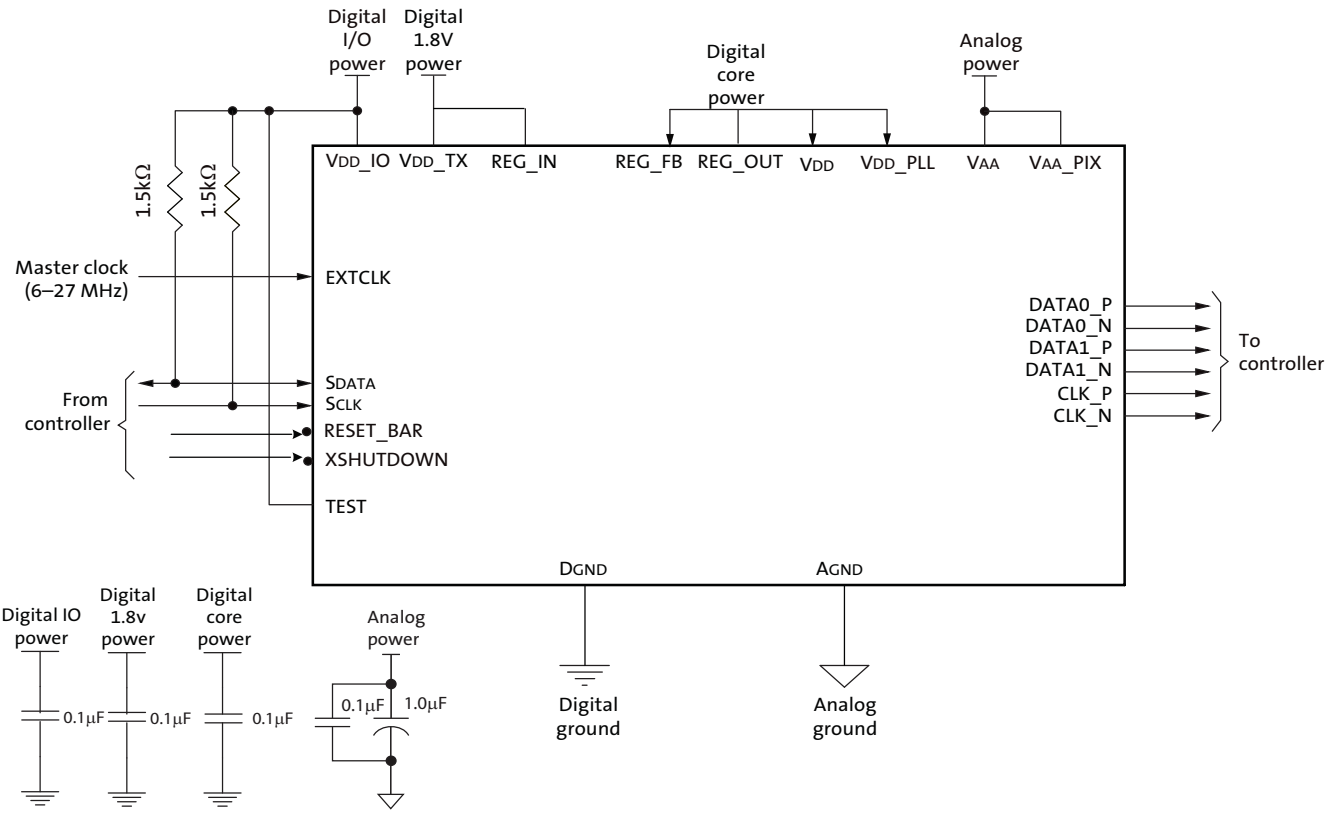
By default, the AR0543 powers up with the serial pixel data interface enabled. The sensor can operate in serial MIPI mode. This mode is preconfigured at the factory. In either case, the sensor has a SMIA-compatible register interface while the two-wire serial device address is compliant with SMIA or MIPI requirements as appropriate. The reset level on the TEST pin must be tied in a way that is compatible with the configured serial interface of the sensor, for instance, TEST = 1 for MIPI.

Typical configurations are shown in Figure 3 on page 8 These operating modes are described in "Control of the Signal Interface" on page 21.

For low-noise operation, the AR0543 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled from the ground using capacitors as close as possible to the die.

Caution **ON Semiconductor does not recommend the use of inductance filters on the power supplies or output signals.**

Figure 3: Typical Configuration: Serial Dual-Lane MIPI Pixel Data Interface



Notes:
1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.

3. VDD_IO can be either 1.8V(nominal) or 2.8V(nominal). If VDD_IO is 1.8V, VDD_IO can be tied to Digital 1.8V Power.
4. VAA and VAA_PIX must be tied together.
5. VDD and VDD_PLL must be tied together
6. ON Semiconductor recommends having 0.1µF and 1.0µF decoupling capacitors for analog power supply and 0.1µF decoupling capacitor for other power supplies. Actual values and results may vary depending on layout and design considerations.
7. TEST must be tied to VDD_IO for MIPI configuration (Device ID address = 0x6C).
8. VDD _TX and REG_IN must be tied together.
9. Refer to the power-up sequence for XSHUTDOWN and RESET_BAR control.
10. The frequency range for EXTCLK must be 6-27MHz.
11. The GPI[3:0] pins, which can be either statically pulled HIGH/LOW to be used as module IDs, or they can be programmed to perform special functions (TRIGGER, OE_BAR, SADDR, STANDBY) to be dynamically controlled, are not shown in Figure 3.
12. The FLASH, which can be used for flash control, is not shown in Figure 3.

Signal Descriptions

Table 1 provides signal descriptions for AR0543 die. For pad location and aperture information, refer to the AR0543 die data sheet. The CSP package only supports MIPI signals.

Table 1: Signal Descriptions

Pad Name	Pad Type	Description
EXTCLK	Input	Master clock input, 6–27 MHz.
RESET_BAR	Input	Asynchronous active LOW reset. When asserted, data output stops and all internal registers are restored to their factory default settings.
XSHUTDOWN	Input	Asynchronous active LOW reset. When asserted, data output stops and all internal registers are restored to their factory default settings. This pin will turn off the digital power domain and is the lowest power state of the sensor.
SCLK	Input	Serial clock for access to control and status registers.
GPI[3:0]	Input	General purpose inputs. After reset, these pads are powered-down by default; this means that it is not necessary to bond to these pads. Any of these pads can be configured to provide hardware control of the standby, output enable, SADDR select, and shutter trigger functions. ON Semiconductor recommends that unused GPI pins be tied to DGND, but can also be left floating.
TEST	Input	Enable manufacturing test modes. Connect to VDD_IO power for the MIPI-configured sensor.
SDATA	I/O	Serial data from reads and writes to control and status registers.
REG_OUT	I/O	1.2V on-chip regulator output node.
REG_IN	I/O	On-chip regulator input node. It needs to be connected to external 1.8V.
REG_FB	I/O	This pad is receiving the 1.2V feedback from REG_OUT. It needs to be connected to REG_OUT.
LINE_VALID	Output	LINE_VALID (LV) output. Qualified by PIXCLK.
FRAME_VALID	Output	FRAME_VALID (FV) output. Qualified by PIXCLK.
DOUT[9:0]	Output	Parallel pixel data output. Qualified by PIXCLK.
PIXCLK	Output	Pixel clock. Used to qualify the LV, FV, and DOUT[9:0] outputs.
FLASH	Output	Flash output. Synchronization pulse for external light source. Can be left floating if not used.
VPP	Supply	Power supply used to program one-time programmable (OTP) memory.
VDD_TX	Supply	Digital PHY power supply. Digital power supply for the serial interface.
VAA	Supply	Analog power supply.
VAA_PIX	Supply	Analog power supply for the pixel array.
AGND	Supply	Analog ground.
VDD	Supply	Digital core power supply.
VDD_IO	Supply	I/O power supply.
DGND	Supply	Common ground for digital and I/O.
VDD_PLL	Supply	PLL power supply.

Table 2: CSP (MIPI) Package Pinout

	1	2	3	4	5	6	7	8
A	DGND	DATA1_P	DATA0_P	CLK_P	DGND	RESET_BAR	GPI2	DGND
B	DGND	DATA1_N	DATA0_N	CLK_N	EXTCLK	VDD	DGND	VDD
C	VDD	VDD_TX					DGND	VDD_IO
D	REG_OUT	REG_IN0					NC	AGND
E	DGND	VDD				NC	GPI1	VAA
F	SCLK	DGND	SDATA	VDD_IO	TEST	AGND	GPI0	VAA
G	REG_IN1	REG_IN1	XSHUTDOWN	VPP	VAA_PIX	AGND	AGND	VAA

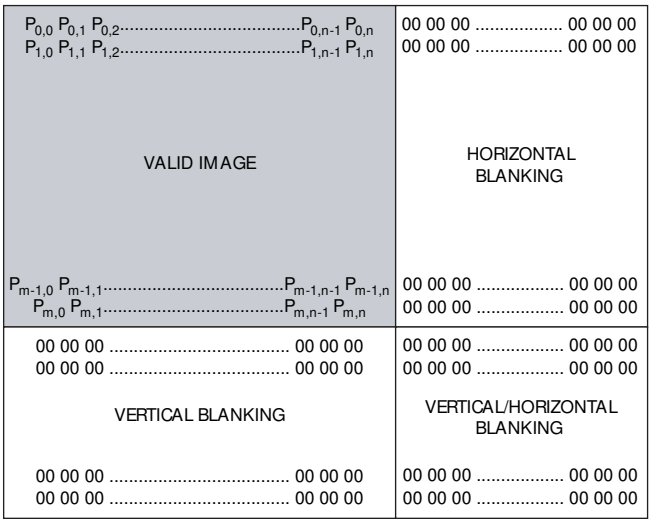
NC = Do not connect. For manufacturing test purpose only.

Output Data Format

Pixel Data Interface

AR0543 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 4. The amount of horizontal blanking and vertical blanking is programmable.

Figure 4: Spatial Illustration of Image Readout



Two-Wire Serial Register Interface

The two-wire serial interface bus enables read/write access to control and status registers within the AR0543.The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off-chip by a 1.5kΩ resistor. Either the slave or master device can drive SDATA LOW—the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two-wire serial interface specification allow the slave device to drive SCLK LOW; the AR0543 uses SCLK as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements:

1. a (repeated) start condition
2. a slave address/data direction byte
3. an (a no) acknowledge bit
4. a message byte
5. a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a WRITE, and a “1” indicates a READ. The default slave addresses used by the AR0543 for the MIPI configured sensor are 0x6C (write address) and 0x6D (read address) in accordance with the MIPI specification. Alternate slave addresses of 0x6E(write address) and 0x6F(read address) can be selected by enabling and asserting the SADDR signal through the GPI pad.

An alternate slave address can also be programmed through R0x31FC.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No-Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a “0” indicates a write and a “1” indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

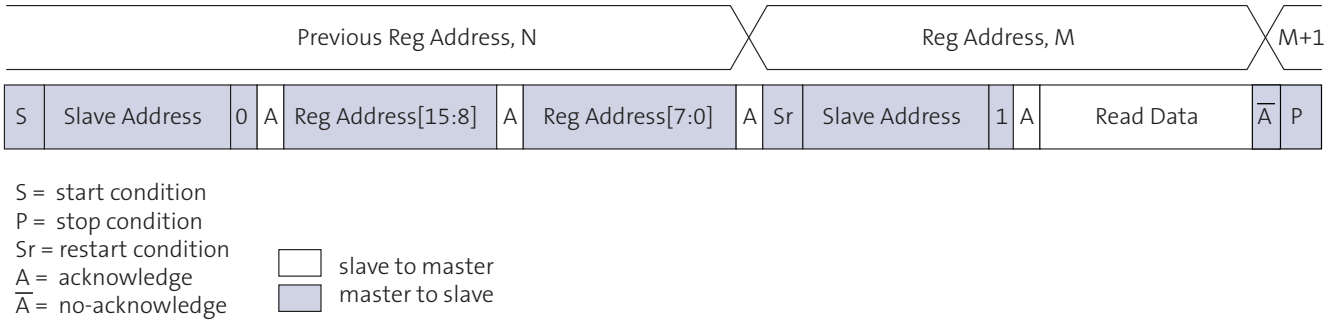
If the request was a WRITE, the master then transfers the 16-bit register address to which the WRITE should take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8-bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The slave’s internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Single READ from Random Location

This sequence (Figure 5 on page 15) starts with a dummy WRITE to the 16-bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8-bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. Figure 5 shows how the internal register address maintained by the AR0543 is loaded and incremented as the sequence proceeds.

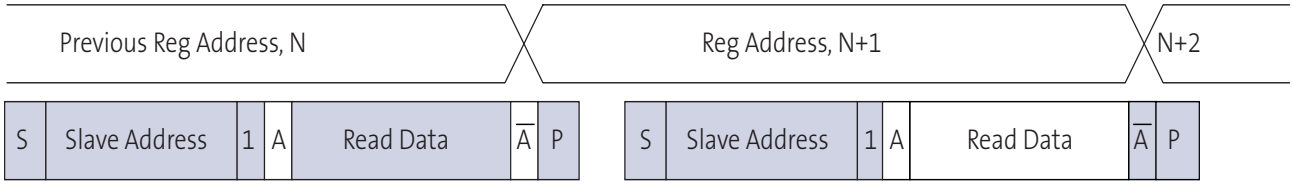
Figure 5: Single READ from Random Location



Single READ from Current Location

This sequence (Figure 6) performs a read using the current value of the AR0543 internal register address. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

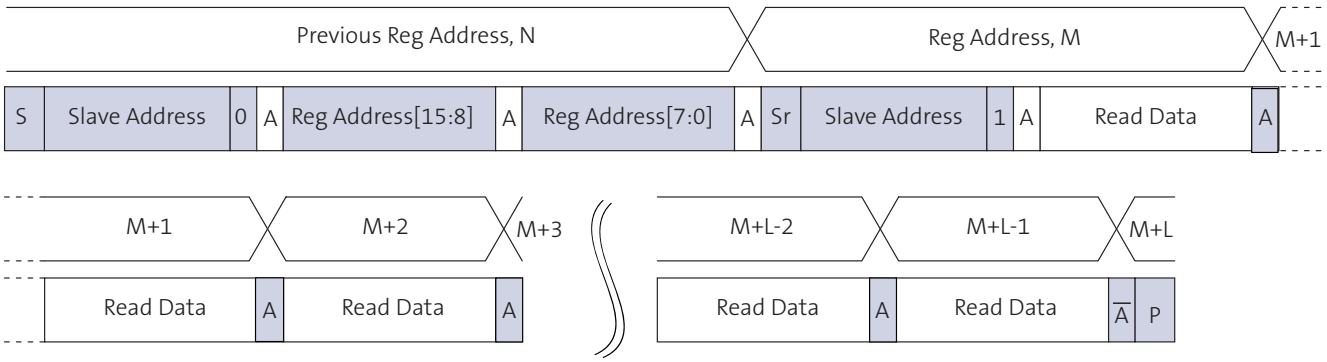
Figure 6: Single READ from Current Location



Sequential READ, Start from Random Location

This sequence (Figure 7) starts in the same way as the single READ from random location (Figure 5). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

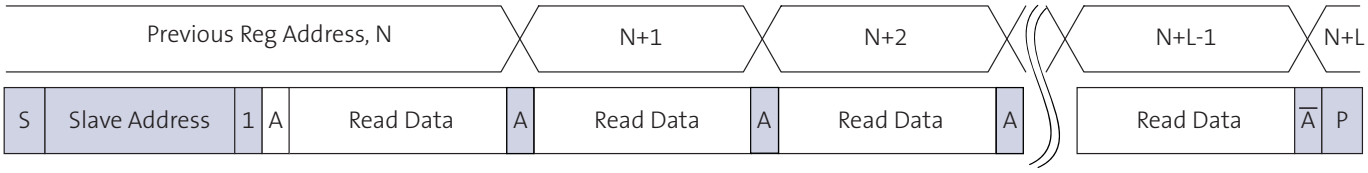
Figure 7: Sequential READ, Start from Random Location



Sequential READ, Start from Current Location

This sequence (Figure 8) starts in the same way as the single READ from current location (Figure 6 on page 15). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

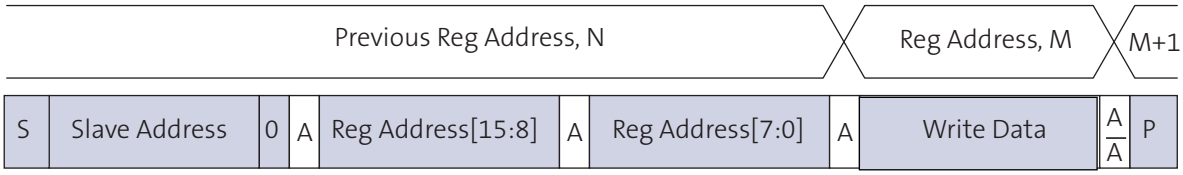
Figure 8: Sequential READ, Start from Current Location



Single WRITE to Random Location

This sequence (Figure 9) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

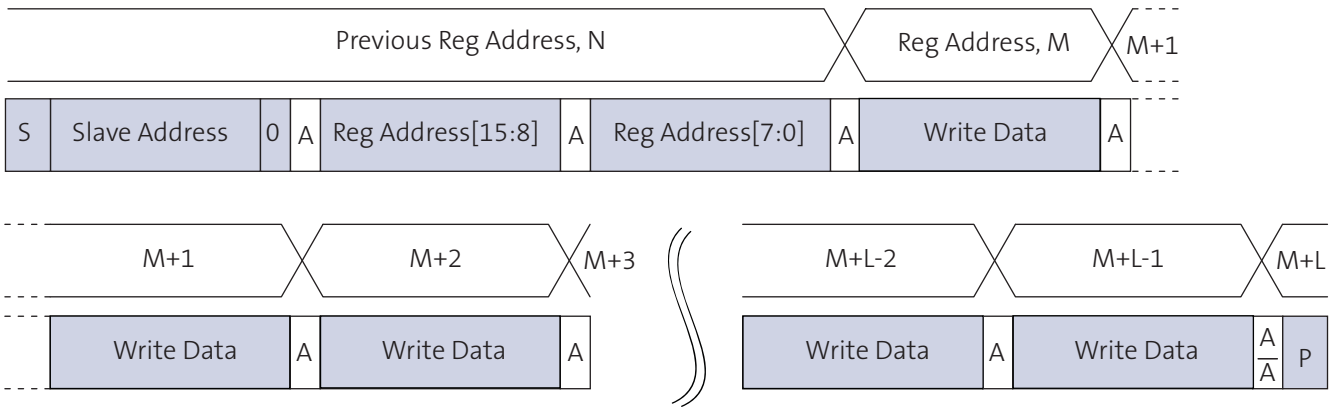
Figure 9: Single WRITE to Random Location



Sequential WRITE, Start at Random Location

This sequence (Figure 10) starts in the same way as the single WRITE to random location (Figure 9). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

Figure 10: Sequential WRITE, Start at Random Location



Registers

The AR0543 provides a 16-bit register address space accessed through a serial interface (“Two-Wire Serial Register Interface” on page 13). See the AR0543 Register Reference for details.

Programming Restrictions

Table 6 shows a list of programming rules that must be adhered to for correct operation of the AR0543. It is recommended that these rules are encoded into the device driver stack—either implicitly or explicitly.

Table 1: Definitions for Programming Rules

Name	Definition
xskip	xskip = 1 if x_odd_inc = 1; xskip = 2 if x_odd_inc = 3; xskip = 4 if x_odd_inc = 7
yskip	yskip = 1 if y_odd_inc = 1; yskip = 2 if y_odd_inc = 3; yskip = 4 if y_odd_inc = 7

Table 2: Programming Rules

Parameter	Minimum Value	Maximum Value
coarse_integration_time	8	frame_length_lines - coarse_integration_time_max_margin
fine_integration_time	fine_integration_time_min	line_length_pck - fine_integration_time_max_margin
digital_gain_* digital_gain_* is an integer multiple of digital_gain_step_size	digital_gain_min	digital_gain_max
frame_length_lines	min_frame_length_lines	max_frame_length_lines
line_length_pck	min_line_length_pck	max_line_length_pck
	((x_addr_end - x_addr_start + x_odd_inc)/xskip) + min_line_blanking_pck	
frame_length_lines	((y_addr_end - y_addr_start + y_odd_inc)/yskip) + min_frame_blanking_lines	
x_addr_start (must be an even number)	x_addr_min	x_addr_max
x_addr_end (must be an odd number)	x_addr_start	x_addr_max
(x_addr_end – x_addr_start + x_odd_inc)	must be positive	must be positive
y_addr_start (must be an even number)	y_addr_min	y_addr_max
y_addr_end (must be an odd number)	y_addr_start	y_addr_max
(y_addr_end – y_addr_start + y_odd_inc)	must be positive	must be positive
x_even_inc (must be an even number)	min_even_inc	max_even_inc
y_even_inc (must be an even number)	min_even_inc	max_even_inc
x_odd_inc (must be an odd number)	min_odd_inc	max_odd_inc
y_odd_inc (must be an odd number)	min_odd_inc	max_odd_inc
scale_m	scaler_m_min	scaler_m_max
scale_n	scaler_n_min	scaler_n_max

Table 2: Programming Rules (continued)

Parameter	Minimum Value	Maximum Value
x_output_size (must be even number – this is enforced in hardware)	256	2608
y_output_size (must be even number – this is enforced in hardware)	2	frame_length_lines
With subsampling, start and end pixels must be addressed (impact on x/y start/end addresses, function of image orientation bits)		

Output Size Restrictions

When the serial pixel data path is in use, there is an additional restriction that x_output_size must be small enough such that the output row time (set by x_output_size, the framing and CRC overhead of 12 bytes and the output clock rate) must be less than the row time of the video array (set by line_length_pck and the video timing clock rate).

Effect of Scaler on Legal Range of Output Sizes

When the scaler is enabled, it is necessary to adjust the values of x_output_size and y_output_size to match the image size generated by the scaler. The AR0543 will operate incorrectly if the x_output_size and y_output_size are significantly larger than the output image.

To understand the reason for this, consider the situation where the sensor is operating at full resolution and the scaler is enabled with a scaling factor of 32 (half the number of pixels in each direction).

Output Data Timing

The output FIFO acts as a boundary between two clock domains. Data is written to the FIFO in the VT (video timing) clock domain. Data is read out of the FIFO in the OP (output) clock domain.

When the scaler is disabled, the data rate in the VT clock domain is constant and uniform during the active period of each pixel array row readout. When the scaler is enabled, the data rate in the VT clock domain becomes intermittent, corresponding to the data reduction performed by the scaler.

A key constraint when configuring the clock for the output FIFO is that the frame rate out of the FIFO must exactly match the frame rate into the FIFO. When the scaler is disabled, this constraint can be met by imposing the rule that the row time on the serial data stream must be greater than or equal to the row time at the pixel array. The row time on the serial data stream is calculated from the x_output_size and the data_format (8 or 10 bits per pixel), and must include the time taken in the serial data stream for start of frame/row, end of row/frame and checksum symbols.

Caution **If this constraint is not met, the FIFO will either underrun or overrun. FIFO underrun or overrun is a fatal error condition that is signaled through the data path_status register (R0x306A).**

Changing Registers while Streaming

The following registers should only be reprogrammed while the sensor is in software standby:

- ccp_channel_identifier
- ccp_data_format
- ccp_signaling_mode
- vt_pix_clk_div
- vt_sys_clk_div
- pre_pll_clk_div
- pll_multiplier
- op_pix_clk_div
- op_sys_clk_div
- scale_m

Programming Restrictions when Using Global Reset

Interactions between the registers that control the global reset imposes some programming restrictions on the way in which they are used; these are discussed in "Analog Gain" on page 34.

Control of the Signal Interface

This section describes the operation of the signal interface in all functional modes.

Serial Register Interface

The serial register interface uses these signals:

- SCLK
- SDATA
- SADDR (through the GPI pad)

SCLK is an input-only signal and must always be driven to a valid logic level for correct operation; if the driving device can place this signal in High-Z, an external pull-up resistor should be connected on this signal.

SDATA is a bidirectional signal. An external pull-up resistor should be connected on this signal.

SADDR is a signal, which can be optionally enabled and controlled by a GPI pad, to select an alternate slave address. These slave addresses can also be programmed through R0x31FC.

This interface is described in detail in "Two-Wire Serial Register Interface" on page 51.

The AR0543 sensor can provide the MIPI serial interface.

At power-up and after a hard or soft reset, the reset state of the sensor is to enable serial interface when available.

The serial pixel data interface uses the following output-only signal pairs:

- DATA0_P
- DATA0_N
- CLK_P
- CLK_N

The signal pairs are driven differentially using sub-LVDS switching levels. The serial pixel data interface is enabled by default at power up and after reset.

The DATA0_P, DATA0_N, CLK_P, and CLK_N pads are turned off if the SMIA serial disable bit is asserted (R0x301A-B[12]=1) or when the sensor is in the soft standby state.

MIPI Serial Pixel Data Interface

The serial pixel data interface uses the following output-only signal pairs:

- DATA0_P
- DATA0_N
- DATA1_P
- DATA1_N
- CLK_P
- CLK_N

The signal pairs use both single-ended and differential signaling, in accordance with the MIPI specification. The serial pixel data interface is enabled by default at power up and after reset.

The DATA0_P, DATA0_N, DATA1_P, DATA1_N, CLK_P and CLK_N pads are set to the Ultra Low Power State (ULPS) if the SMIA serial disable bit is asserted (R0x301A-B[12]=1) or when the sensor is in the hardware standby or soft standby system states.

The ccp_data_format (R0x0112-3) register can be programmed to any of the following data format settings that are supported:

- 0x0A0A – Sensor supports RAW10 uncompressed data format. This mode is supported by discarding all but the upper 10 bits of a pixel value.
- 0x0808 – Sensor supports RAW8 uncompressed data format. This mode is supported by discarding all but the upper 8 bits of a pixel value.
- 0x0A08 – Sensor supports RAW8 data format in which an adaptive compression algorithm is used to perform 10-bit to 8-bit compression on the upper 10 bits of each pixel value

The serial_format register (R0x31AE) register controls which serial interface is in use when the serial interface is enabled (reset_register[12] = 0). The following serial formats are supported:

- 0x0201 – Sensor supports single-lane MIPI operation
- 0x0202 – Sensor supports dual-lane MIPI operation

Configuration of the Pixel Data Interface

Fields in R0x301A are used to configure the operation of the pixel data interface. The supported combinations are shown in Table 7.

Table 3: Configuration of the Pixel Data Interface

Serializer Disable R0x301 A–B[12]	Parallel Enable R0x301A–B[7]	Standby End-of-Frame R0x301A–B[4]	Description
0	0	1	Power up default. Serial pixel data interface and its clocks are enabled. Transitions to soft standby are synchronized to the end of frames on the serial pixel data interface.

System States

The system states of the AR0543 are represented as a state diagram in Figure 11 and described in subsequent sections. The effect of RESET_BAR on the system state and the configuration of the PLL in the different states are shown in Table 8 on page 12.

The sensor's operation is broken down into three separate states: hardware standby, software standby, and streaming. The transition between these states might take a certain amount of clock cycles as outlined in Table 8 on page 12.

Figure 1: AR0543 System States

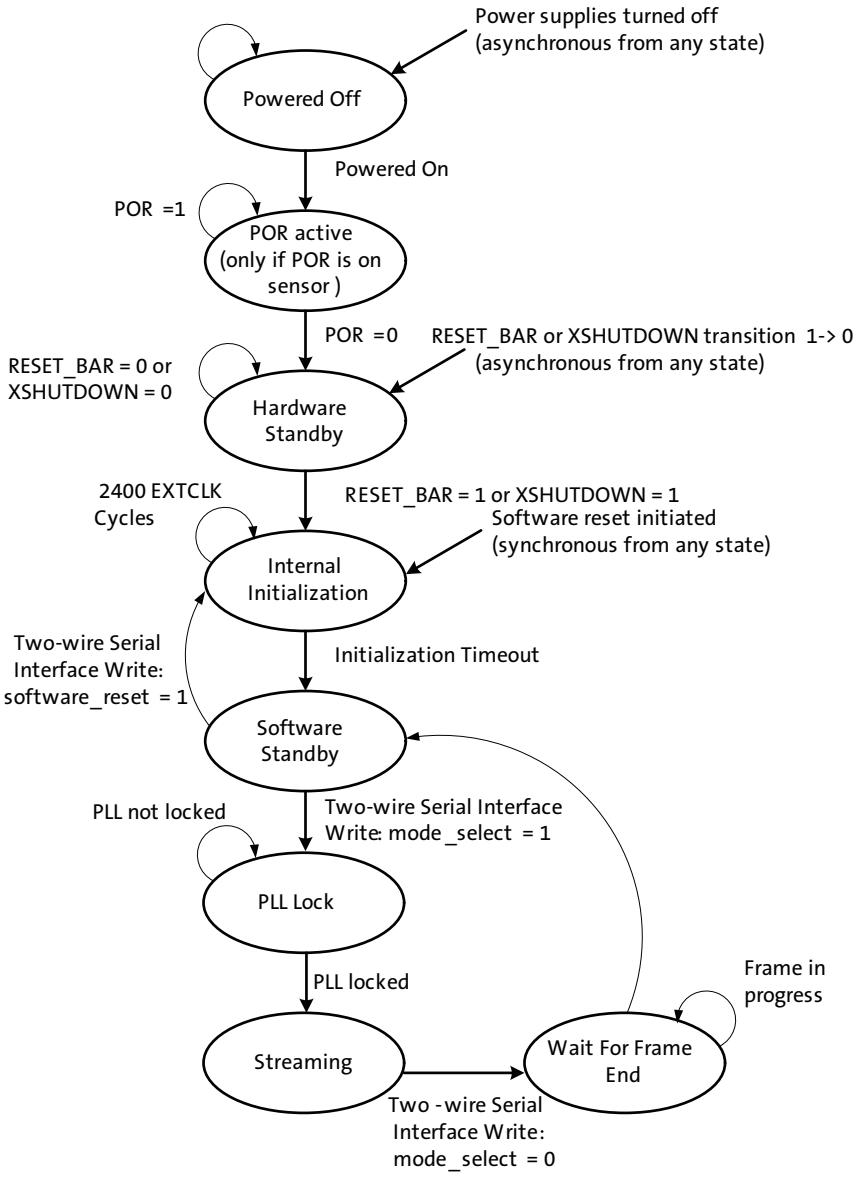


Table 4: XSHUTDOWN and PLL in System States

State	XSHUTDOWN	PLL
Powered off	x	VCO powered down
POR active	x	
Hardware standby	0	
Internal initialization	1	
Software standby		
PLL Lock		VCO powering up and locking, PLL output bypassed
Streaming		VCO running, PLL output active
Wait for frame end		

Power-On Reset Sequence

When power is applied to the AR0543, it enters a low-power hardware standby state. Exit from this state is controlled by the later of two events:

- The negation of the XSHUTDOWN input.
- A timeout of the internal power-on reset circuit.

When XSHUTDOWN is asserted it asynchronously resets the sensor, truncating any frame that is in progress.

s

When the sensor leaves the hardware standby state it performs an internal initialization sequence that takes 2400 EXTCLK cycles. After this, it enters a low-power software standby state. While the initialization sequence is in progress, the AR0543 will not respond to read transactions on its two-wire serial interface. Therefore, a method to determine when the initialization sequence has completed is to poll a sensor register; for example, R0x0000. While the initialization sequence is in progress, the sensor will not respond to its device address and reads from the sensor will result in a NACK on the two-wire serial interface bus. When the sequence has completed, reads will return the operational value for the register (0x4800 if R0x0000 is read).

When the sensor leaves software standby mode and enables the VCO, an internal delay will keep the PLL disconnected for up to 1ms so that the PLL can lock. The VCO lock time is 200µs (typical), 1ms (maximum).

Soft Reset Sequence

The AR0543 can be reset under software control by writing “1” to software_reset (R0x0103). A software reset asynchronously resets the sensor, truncating any frame that is in progress. The sensor starts the internal initialization sequence, while the PLL and analog blocks are turned off. At this point, the behavior is exactly the same as for the power-on reset sequence.

Signal State During Reset

Table 9 shows the state of the signal interface during hardware standby (RESET_BAR asserted) and the default state during software standby (after exit from hardware standby and before any registers within the sensor have been changed from their default power-up values).