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AR8031 Integrated 10/100/1000 Mbps Ethernet Transceiver

General Description

The AR8031 is part of the Arctic family of devices — which includes the AR8031, AR8033, and AR8035. The AR8031 is Atheros' 4th generation, single port, 10/100/1000 Mbps, Tri-speed Ethernet PHY. It supports both RGMII and SGMII interfaces to the MAC.

The AR8031 provides a low power, low BOM (Bill of Materials) cost solution for comprehensive applications including enterprise, carrier and home networks such as CPE, home gateway, enterprise switch, carrier switch/router, mobile base station and base station controller, optical module and media converter, industry automation and measurement.

The AR8031 integrates Atheros Green ETHOS® power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE. SmartEEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system. Further, the AR8031 supports Wake-on-LAN (WoL) feature to be able to help manage and regulate total system power requirements.

The AR8031 embeds CDT (Cable Diagnostics Test) technology on-chip which allows customers to measure cable length, detect the cable status, and identify remote and local PHY malfunctions, bad or marginal patch cord segments or connectors. Some of the possible problems that can be detected include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and a bad transformer.

The AR8031 requires only a single, 3.3V power supply. On-chip regulators provide all the other required voltages. It integrates the termination R/C circuitry on both the MAC interfaces (RGMII/SGMII) and the serial resistors for the line side.

The AR8031 device also incorporates a 1.25 GHz SerDes. This interface can be connected directly to a fiber-optic transceiver for 1000 BASE-X /100 BASE-FX mode or to MAC device for SGMII interface.

The AR8031 supports both 1588v2 and synchronous Ethernet to offer a complete time synchronization solution to meet the next generation network requirements. The key new features supported by the device are:

- Clock synchronization between slave and grandmaster by the exchange of PTP packets. Supports IEEE 1588v2 by offering a 1588 paket parser, accurate time-stamping and insertion to support both one-step and two-step clock modes
- Supports both IEEE 1588v2 and Synchronous Ethernet by offering recovered clock output from data on the network-line side.

The AR8031 supports IEEE 802.3az Energy Efficient Ethernet (EEE) standard. The key features supported by the device are:

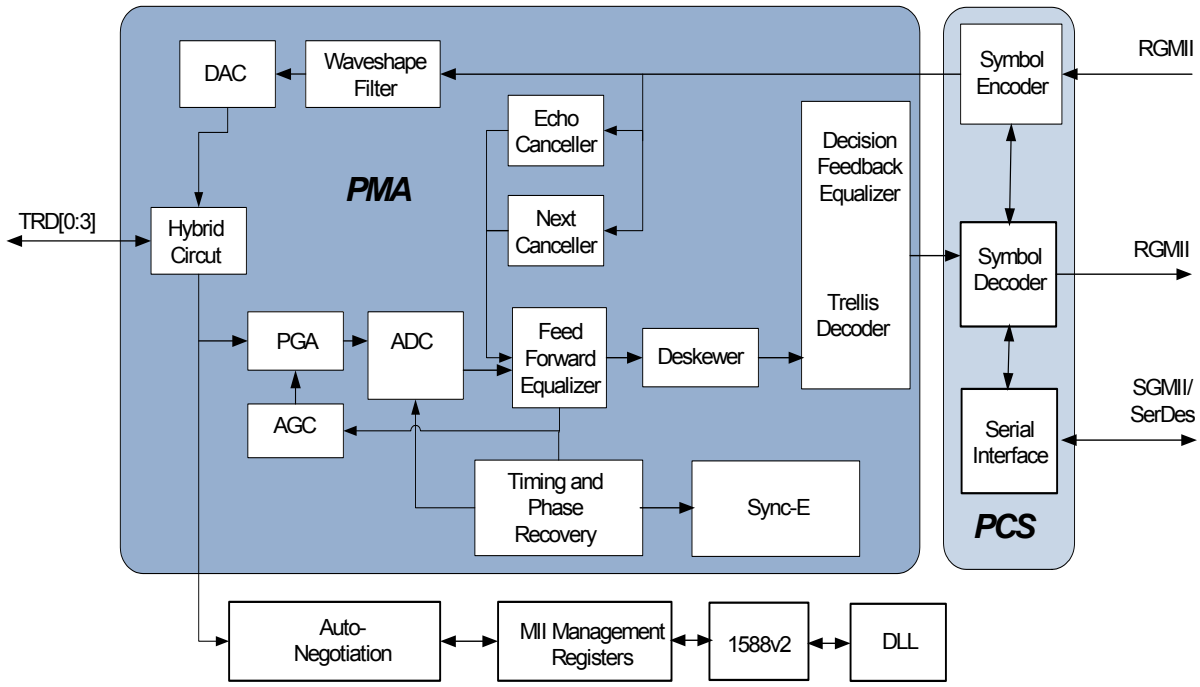
- 10 BASE-Te PHY uses reduced transmit amplitude.
- 100 BASE-TX and 1000 BASE-T use Low Power Idle (LPI) mode to turn off unused analog and digital blocks to save power while data traffic is idle.

Features

- 10/100/1000 BASE-T IEEE 802.3 compliant
- Supports 1000 BASE-T PCS and auto-negotiation with next page support
- Supports RGMII and/or SGMII interfaces to MAC devices
- Supports Fiber and Copper combo mode when MAC interface works in RGMII mode
- Supports additional IEEE 1000 BASE-X and 100 BASE-FX with Integrated SerDes
- RGMII timing modes support internal delay and external delay on Rx path

- Supports Atheros Green ETHOS® power saving modes with internal automatic DSP power saving scheme
- Supports IEEE 802.3az (Energy Efficient Ethernet)
- Supports SmartEEE which allows MAC/SoC devices withoug 802.3az support to function as the complete 802.3az system
- Supports Wake-on-LAN (WoL) to detect magic packet and notify the sleeping system to wake up
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Supports Synchronous Ethernet with selectable recovered clock output
- Robust Cable Discharge Event (CDE) protection of ±6 kV
- Error-free operation over up to 140 meters of CAT5 cable
- Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Jumbo Frame support up to 10KB (full duplex)
- Multiple loopback modes for diagnostics
- Robust Surge Protection with ±750 V/differential mode and ±4 kV/common mode
- Cable Diagnostic Test (CDT)
- Single power supply: 3.3V, optional for external regulator for core voltage
- 6mm x 6mm, 48-pin QFN package
- Industry temperature (I-temp) option available.

AR8031 Functional Block Diagram



Revision History

Date	Revsion Details	Revision
2010/11/15	First draft	0.1
2011/4/14	General Description ■ Overall update for revision from MPW to mass production ■ Block diagram: add SYNC-E and 1588v2 block Pin Descriptions ■ RXD [3:0], RX_DV pin damping resistor 22ohm requirement is deleted. ■ RST pin type change from "IH" to "I," mass production chip does not have internal weak PU ■ INT, WOL_INT from "I/O active high" change to "D active low" need an external PU ■ Power on strapping LED_ACT from "1.1V/1.2V selection" to "PHY ADDRESS [2]". ■ LED_ACT/LED_LINK1000/LED_LINK10_100 from internal weak "PD" change to internal weak "PU". Functional Descriptions ■ 2.2.4 Mode definition adds work mode"1011" combo mode. Electrical Characteristics ■ 3.1 Absolute Maximum Rating: update CDM max ■ 3.2 Recommeded Operating Condition: update Tj max ■ 3.7 Clock Characteristics: update values in Table 3-13 Recommended Crystal Parameters ■ Update Table 3-11 MDIO AC Characteristic to add tmdelay row Register ■ 4.2.29LED Control (0x18): update register bit definitions ■ 4.2.30 Manual LED Override (0x19): new register Topside Marking ■ Add topside marking illustration	1.0
2011/8/29	Electrical Characteristics ■ 3.2 Recommended Operation Conditions: delete DVDDL/AVDDL, Ψ_{JA}; add VDDH_REG, Ψ_{JT}, AVDDL/DVDDL (industrial and commercial); add thermal conditions ■ 3.6 change title from MDIO DC Charateristics to MDIO/MDC DC...; change V_{IH} min value and V_{IL} max value ■ 3.7 table 3-14: change $Jitter_{pk-pk}$ max value to 100 ■ 3.11 Digital pin design guide (new) Registers ■ 4.2.3 Status Register – Copper page, change bit[8] reset value to always 1 ■ 4.3.4 Hib control and auto-neg test register: change bit[12], [6:5] to reserved ■ 4.3.5 External loopback selection, change bit[0] to R/W ■ 4.3.7 Power saving control (new) ■ 4.4.75 SGMII Control register 2 (new) ■ 4.4.76 SGMII Control register 3(new) ■ 4.4.78 1588 RTC clock select register (new)	1.1

Table of Contents

1. Pin Descriptions

This section contains a package pinout for the AR8031 QFN 48 pin and a listing of the signal descriptions (see Figure 1-1).

The following nomenclature is used for signal names:

NC	No connection to the internal die is made from this pin
n	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types described in Table 1-1:

D	Open drain
IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal
PD	Internal pull-down for input
PU	Internal pull-up for input

Figure 1-1 shows the pinout diagram for AR8031.

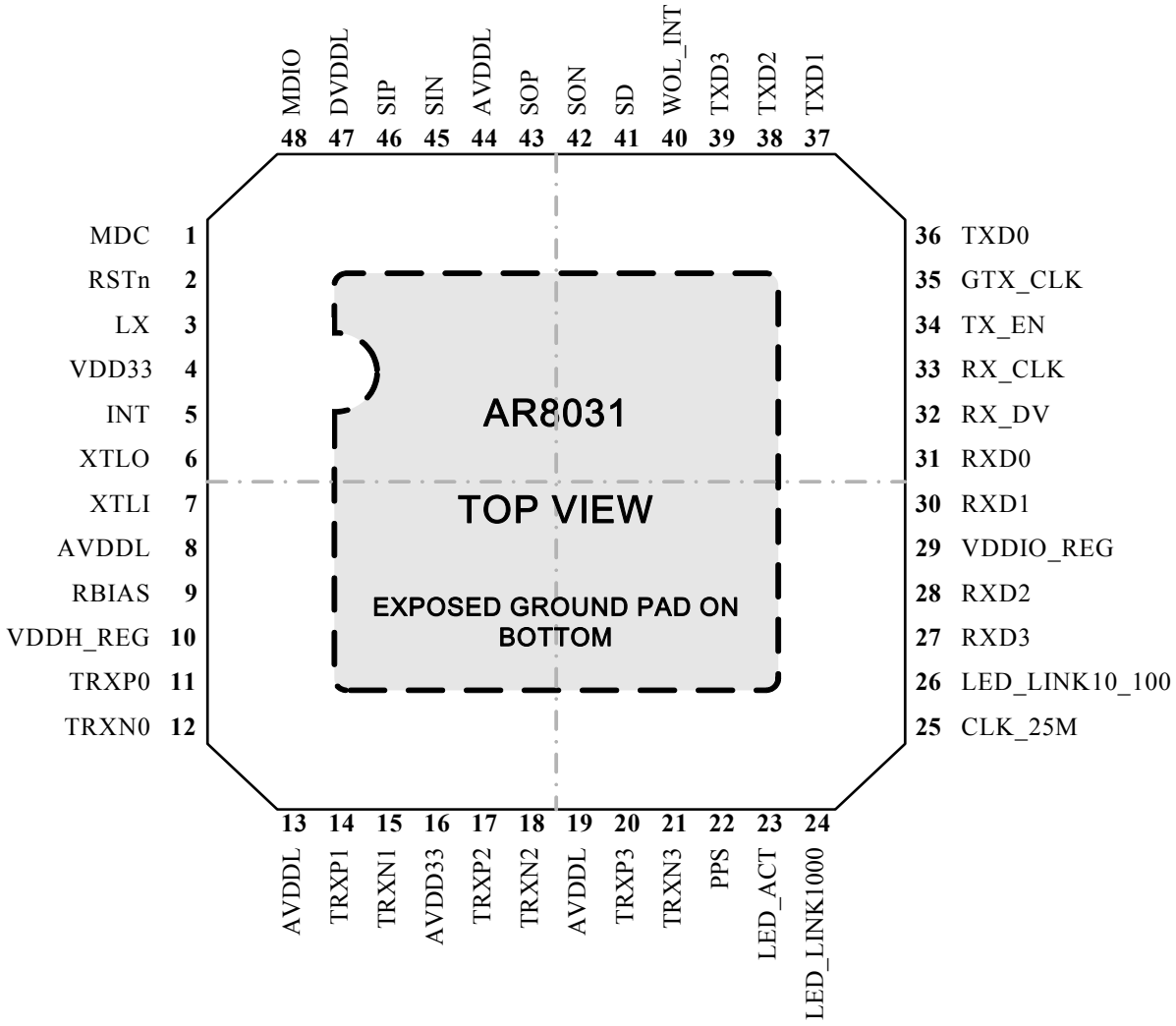


Figure 1-1. **AR8031 48-pin QFN Pinout Diagram (Top View)**

NOTE: There is an exposed ground pad on the back side of the package.

Table 1-1. **Signal to Pin Relationships and Descriptions**

Symbol	Pin	Type	Description
MDI			
TRXP0, TRXN0	11, 12	IA, OA	Media-dependent interface 0, differential 100 Ω transmission line
TRXP1, TRXN1	14, 15	IA, OA	Media-dependent interface 1, differential 100 Ω transmission line
TRXP2, TRXN2	17, 18	IA, OA	Media-dependent interface 2, differential 100 Ω transmission line
TRXP3, TRXN3	20, 21	IA, OA	Media-dependent interface 3, differential 100 Ω transmission line
RGMII			
GTX_CLK	35	I, PD	RGMII transmit clock, 125 MHz at 1000 Mbps, 25 MHz at 100 Mbps, and 2.5 MHz at 10 Mbps digital clock input
RX_CLK	33	I/O, PD	RGMII receive clock, 125 MHz at 1000 Mbps, 25 MHz at 100 Mbps, and 2.5 MHz at 10 Mbps digital clock output
RX_DV	32	I/O, PD	RGMII receive data valid
RXD0	31	I/O, PD	RGMII receive data 0
RXD1	30	I/O, PD	RGMII receive data 1
RXD2	28	I/O, PD	RGMII receive data 2
RXD3	27	I/O, PD	RGMII receive data 3
TX_EN	34	I, PD	RGMII transmit enable
TXD0	36	I, PD	RGMII transmit data 0
TXD1	37	I, PD	RGMII transmit data 1
TXD2	38	I, PD	RGMII transmit data 2
TXD3	39	I, PD	RGMII transmit data 3
SGMII/1000FX			
SIP/SIN	46, 45	IA	1.25 Gbps transmit differential inputs When this interface is used as a MAC interface, the MAC transmitter's positive output connects to SIP and the MAC transmitter's negative output connects to the SIN. When this interface is used as a fiber interface, the fiber-optic transceiver's positive output connects to the SIP and the fiber-optic transceiver's negative output connects to the SIN.
SOP/SON	43, 42	OA	1.25 Gbps receive differential outputs When this interface is used as a MAC interface, the MAC receiver's positive input connects to SOP and the MAC receiver's negative input connects to the SON. When this interface is used as a fiber interface, the fiber-optic transceiver's positive input connects to the SOP and the fiber-optic transceiver's negative input connects to the SON.
SD	41	IA	Signal Detect. 1.2 V voltage level. Input signals must not exceed 1.4V.
Management Interface and Interrupt			

Table 1-1. **Signal to Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description	
MDC	1	I, PU	Management data clock reference	
MDIO	48	I/O, D, PU	Management data, 1.5 kΩ pull-up resistor to 3.3 V/ 2.5 V	
LED				
LED_ACT	23	I/O, PU	Parallel LED output for 10/100/1000 BASE-T activity; active blinking LED active based upon power-on strapping. If pulled up, active low; If pulled-down, active high	
LED_LINK1000	24	I/O, PU	Parallel LED output for 1000 BASE-T link; LED active based upon power-on strapping. If pulled up, active low; If pulled-down, active high	
LED_LINK10_100	26	I/O, PU	Parallel LED output for 10/100 BASE-T link. LED active based upon power-on strapping of LED_LINK1000. If LED_LINK1000 is pulled up, this pin is active low; if LED_LINK1000 is pulled-down, this pin is active high.	
			High, external PU	10 Mbps
			Low, external PU	100 Mbps
System Signal Group/Reference				
CLK_25M	25	I/O	Synchronous Ethernet recovered clock (25MHz, 50MHz, 62.5MHzor 125MHz) output, register configurable, or IEEE 1588v2 reference 50 MHz- 125 MHz clock input.	
RSTn	2	I	System reset, active low. This pin requires an external pull-up resistor.	
XTLI	7	IA	Crystal oscillator input; 27 pF capacitor to GND. Support external 25 MHz 1.2 V swing clock input through this pin.	
XTLO	6	OA	Crystal oscillator output; 27 pF capacitor to GND	
RBIAS	9	OA	External 2.37 kΩ 1% resistor to GND to set bias current	
INT	5	D, PD	System Interrupt Output. This pin is OD-gate by default and requires external 10 kΩ pull-up resistor, active low.	
WOL_INT	40	D, PD	Wake-on-LAN interrupt output. This pin is OD-gate by default and requires external 10 kΩ resistor pull-up, active with a low pulse of 32 link speed clock cycles. See "Wake On LAN (WoL)" on page 32 for details.	
Power				
LX	3	OA	Power inductor pin. Add an external 4.7 µH/500 mA power inductor to this pin directly.	
VDDH_REG	10	OA	2.5V regulator output.	
VDDIO_REG	29	OA	Regulator output for the RGMII I/O voltage. It can be either 1.5V (default) or 1.8V. If 2.5V is intended for the RGMII I/O, simply connect this pin with the 2.5V regulator output at pin 10.	
AVDDL	8, 13, 19, 44	P	1.1V analog input. Connect to Pin 47 through a bead	

Table 1-1. **Signal to Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
DVDDL	47	P	1.1V digital core power input. Connect to power inductor directly and 10uF+0.1uF ceramic capacitors to GND
VDD33	4	P	3.3V input for switching regulator
AVDD33	16	P	3.3V input for PHY, from VDD33 through a bead
1588v2 Pins			
PPS	22	O	IEEEv2 Pulse Per Second output. 1 Hz clock which is synchronous with internal RTC.

1.1 Power-on Strapping Pins

Table 1-2 shows the pin-to-PHY core Power-on strapping relationship

Table 1-2. **Power-on Strapping Pins**

PHY Pin	PHY Core Config Signal	Description	Default Internal Weak Pull-up/down
RXD0	PHYADDRESS0	LED_ACT and RXD1-0 set the lower three bits of the physical address. The upper two bits of the physical address are set to the default, “00”.	0
RXD1	PHYADDRESS1		0
LED_ACT	PHYADDRESS2		1
RX_DV	MODE[0]	Mode select bit 0	0
RXD2	MODE[1]	Mode select bit 1	0
RX_CLK	MODE[2]	Mode select bit 2	0
RXD3	MODE[3]	Mode select bit 3	0
LED_LINK1000	INT SELECT	An external 10 kΩ pull-down resistor is required	1

NOTE: 0 = Pull-down, 1 = Pull-up.

NOTE: Power-on strapping pins are latched during power-up reset or warm hardware reset.

NOTE: Since the MAC device input pins may be driven high or low during power-up or reset, PHY power-on strapping status may be affected by the MAC side. In this case an external 10 k pull-down or pull-up resistor is required to ensure stable status.

1.1.1 Mode Definition

Table 1-3 shows the Mode and its Description.

Table 1-3. **Mode Definition**

Mode [3:0]	Description
0000	1000 BASE-T, RGMII
0001	1000 BASE-T, SGMII
0010	1000 BASE-X, RGMII, 50Ω
0011	1000 BASE-X, SGMII, 75Ω
0100	Converter mode between 1000 BASE-X and 1000 BASE-T media, 50Ω
0101	Converter mode between 1000 BASE-X and 1000 BASE-T media, 75Ω
0110	100 BASE-FX, RGMII, 50Ω
0111	Converter mode between 100 BASE-FX and 100 BASE-TX media, 50Ω
1011	RGMII, copper fiber auto-detection
1110	100 BASE-FX, RGMII mode, 75Ω
1111	Converter mode between 100 BASE-FX and 100 BASE-TX media, 75 Ω
Others	Reserved

NOTE: The 50 or 75 Ω is the single end output impedance.

2. Functional Description

The AR8031 is Atheros's low cost GbE PHY. It is a highly integrated Analog Front End (AFE) and digital signal transceiver, providing high performance combined with substantial cost reduction. The AR8031 provides physical layer functions for half/full-duplex 10 BASE-Te, 100 BASE-TX and 1000 BASE-T Ethernet to transmit and receive high-speed data over standard Category 5 (CAT5) un-shielded twisted pair cable.

The AR8031 10/100/1000 PHY is fully 802.3ab compliant, and supports Reduced Gigabit Media-Independent Interface (RGMII) to connect to a Gigabit-capable MAC.

The AR8031 transceiver combines echo canceller, Near End Cross Talk (NEXT) canceller, feed-forward equalizer, joint Viterbi, feedback equalizer, and timing recovery, to enhance signal performance in noisy environments.

See "AR8031 Functional Block Diagram" on page 2.

Table 2-1 shows a feature comparison across the AR8031, AR8033, and AR8035 family.

Table 2-1. **AR8031, AR8033, and AR8035 Comparison**

Feature	AR8031	AR8033	AR8035
RGMII	yes	yes	yes
SGMII	yes	yes	
Cu Ethernet**	yes	yes	yes
EEE (802.3az)	yes	yes	yes
Wake-on-LAN	yes	yes	yes
SERDES/Fiber***	yes	yes	
1588v2	yes		
Sync-E	yes	yes	
Packaging	48-pin	48-pin	40-pin

NOTE: AR8031, AR8033 are pin-to-pin compatible.

** 10 BASE-Te, 100 BASE-TX, 1000 BASE-T are supported

*** 100BASE-FX, and 1000BASE-X are supported

2.2 Modes of Operation

2.2.1 Operation Mode, Copper

The AR8031 operates in the following modes, as illustrated below:

Figure 2-1 shows the copper operating mode for AR8031.

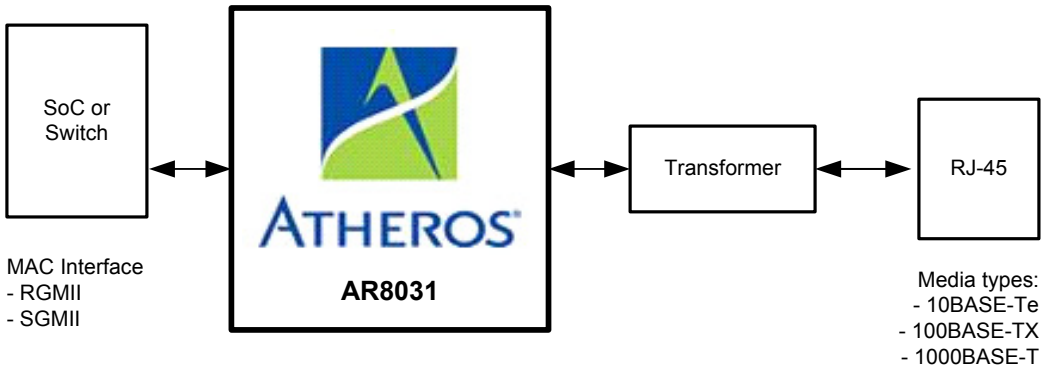


Figure 2-1. **Operating Modes — Copper**

SGMII is serial GMII interface which uses only 4 lines to connect with MAC/SOC. When copper-side link is established, SGMII will pass the copper-side link status (link, speed, duplex) to MAC side for building the link. SGMII interface shares the same SerDes with fiber port.

2.2.2 Operation Mode, Fiber

Figure 2-2 shows the fiber operating mode for AR8031.

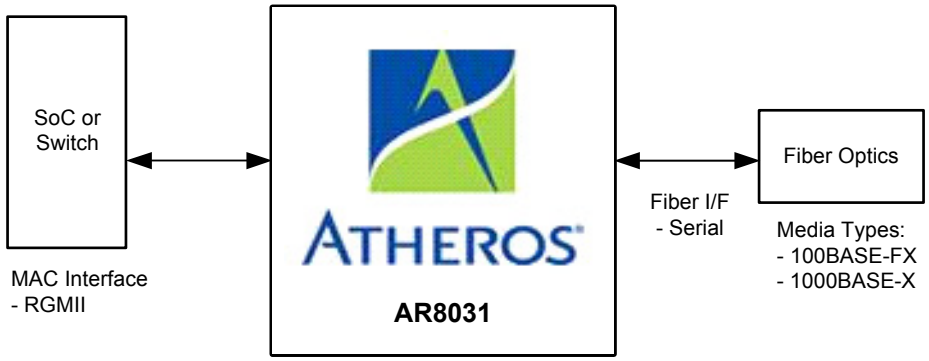


Figure 2-2. **Operating Modes — Fiber**

AR8031 supports both 1000 BASE-X and 100 BASE-FX modes which are configured by power-on strapping pins (see "Power-on Strapping Pins" on page 13) and by register 0x1F [3:0]. In fiber mode, the MDI+/-[3:0] can be left floating.

2.2.3 Operation Mode, Media Converter

Figure 2-3 shows the operating mode Media Converter for AR8031.

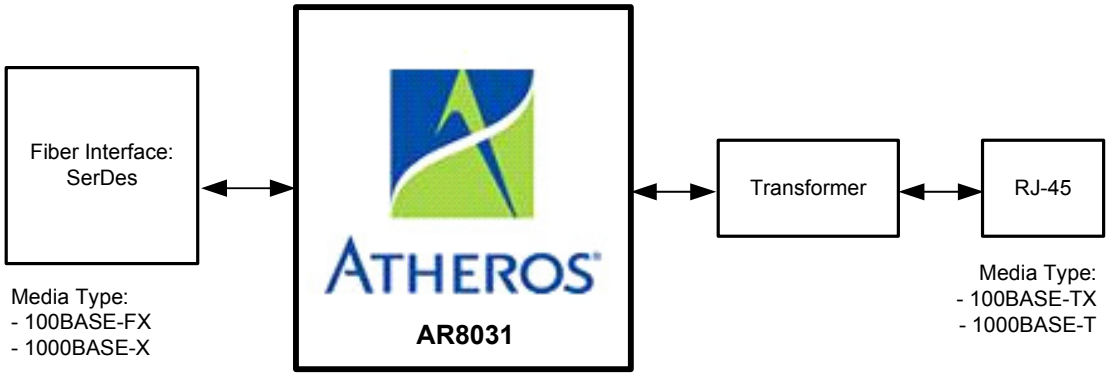


Figure 2-3. **Operating Modes — Media Converter**

AR8031 supports the following converter modes:

- 100 BASE-FX fiber to 100 BASE-TX copper
- 1000 BASE-X fiber to 1000 BASE-T copper

Converter mode can be configured by power-on strapping (see "Power-on Strapping Pins" on page 13). It can also be configured by register 0x1F [3:0]. The register configuration takes effect immediately. Three LEDs are used to indicate fiber interface status.

In converter mode, auto-negotiation is running independently on fiber and copper interfaces. Link status can be checked from copper page and fiber page respectively. Set 0x1F [15] to 1 to select copper page, set 0x1F [15] to0 to select fiber page. Offset address 0x0, 0x1, 0x4, 0x5, 0x6, 0x7, 0x8 and 0x11 refers to two register pages respectively. See "Register Descriptions" chapter for details.

When the fiber and copper interfaces link up to the same speed, packets can go through the PHY. When 1000M converter mode (BX1000_CONV) is enabled, the copper port can still link to 100M with a 100M link partner. But packets can not go through the PHY.

NOTE: Since the two interfaces implement auto-negotiation individually, controller is required to ensure the duplex and pause of two remote link partners are matched.

In converter mode, the RGMII interface signal can be left floating.

2.2.4 Operation Mode, Auto-Media Detect (Combo)

AR8031 supports auto-media detect feature which allows MAC to detect active link partners and process data from copper or fiber interface according to the priority setting. The copper and fiber work modes can be enabled simultaneously by setting the mode bit to 1011 by power-on strapping pin or register 0x1F [3:0].

- No fiber or cable connection: Both interfaces in power saving mode.
- Fiber connected: RGMII fiber mode. The PHY uses external fiber signal detection from the fiber module along with the synchronization state machine to recognize a valid connection.
- Copper connected: RGMII copper mode. The PHY recognizes copper connection by power transmitted over the copper line.
- Combo mode: When active link partners over both fiber and copper are detected, the PHY operation mode is defined by priority setting. Priority is configured at register 0x1F [10] (0 = copper; 1 = fiber).

In auto media detect mode, fiber port can be configured to 1000 BASE-X or 100 BASE-FX by register 0x1F[8] (1 = 1000 BASE-X, default setting; 0 = 100 BASE-FX).

2.3 Transmit Functions

Table 2-2 describes the transmit function encoder modes.

Table 2-2. **Transmit Function Encoder Modes**

Encoder Mode	Description
1000 BASE-T	In 1000 BASE-T mode, the AR8031 scrambles transmit data bytes from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT5 cable.
100 BASE-TX	In 100 BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.
10 BASE-Te	In 10 BASE-Te mode, the AR8031 transmits and receives Manchester-encoded data.

2.4 Receive Functions

2.4.1 Decoder Modes

Table 2-3 describes the receive function decoder modes.

Table 2-3. **Receive Function Decoder Modes**

Decoder Mode	Description
1000 BASE-T	In 1000 BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately and data is output to the MAC interfaces.
100 BASE-TX	In 100 BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to the MII receive data pins after data stream delimiters have been translated.
10 BASE-Te	In 10 BASE-Te mode, the recovered 10 BASE-Te signal is decoded from Manchester then aligned.

2.4.2 Analog to Digital Converter

The AR8031 device employs an advanced high speed ADC on each receive channel with high resolution, which results in better SNR and lower error rates.

2.4.3 Echo Canceller

A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects back as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, also result in drastic SNR degradation on the receive signal. The AR8031 device implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

2.4.4 NEXT Canceller

The 1000 BASE-T physical layer uses all four pairs of wires to transmit data. Because the four twisted pairs are bundled together, significant high frequency crosstalk occurs between adjacent pairs in the bundle. The AR8031 device uses three parallel NEXT cancellers on each receive channel to cancel high frequency crosstalk. The AR8031 cancels NEXT by subtracting an estimate of these signals from the equalizer output.

2.4.5 Baseline Wander Canceller

Baseline wander results from Ethernet links that AC-couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. Baseline wander is more problematic in the 1000 BASE-T environment than in 100 BASE-TX due to the DC baseline shift in the transmit and receive signals. The AR8031 device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

2.4.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision

feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

2.4.7 Auto-Negotiation

The AR8031 device supports 10/100/1000 BASE-T Copper auto-negotiation in accordance with IEEE 802.3 clauses 28 and 40. Auto-negotiation provides a mechanism for transferring information between a pair of link partners to choose the best possible mode of operation in terms of speed, duplex modes, and master/slave preference. Auto-negotiation is initiated upon any of the following scenarios:

- Power-up reset
- Hardware reset
- Software reset
- Auto-negotiation restart
- Transition from power-down to power-up
- The link goes down

If auto-negotiation is disabled, a 10 BASE-Te or 100 BASE-TX can be manually selected using the IEEE MII registers.

NOTE: Smartspeed enable bit requires a software reset to take effect after writing (write register 0x0[15]).

2.4.8 Smartspeed Function

The Atheros Smartspeed function is an enhanced feature of auto-negotiation that allows the AR8031 device to fall back in speed based on cabling conditions as well as operate over CAT3 cabling (in 10 BASE-T mode) or two-pair CAT5 cabling (in 100 BASE-TX mode).

By default, the Smartspeed feature is enabled. Refer to the register "Smart Speed Register" on page 75, which describes how to set the parameters. Set these register bits to control the Smartspeed feature:

- Bit [5]: 1 = Enables Smartspeed (default)
- Bits [4:2]: Sets the number of link attempts before adjusting
- Bit [1]: Timer to determine the stable link condition

NOTE: Smartspeed enable bit needs a software reset (write register 0x0[15] = 1'b1 to take effect after writing.

2.4.9 Automatic MDI/MDIX Crossover

During auto-negotiation, the AR8031 device automatically determines and sets the required MDI configuration, eliminating the need for external crossover cable. If the remote device also implements automatic MDI crossover, the crossover algorithm as described in IEEE 802.3 clause 40.4.4 ensures that only one device performs the required crossover.

2.4.10 Polarity Correction

If cabling has been incorrectly wired, the AR8031 automatically corrects polarity errors on the receive pairs in 1000 BASE-T, 1000BASE-TX, and 10 BASE-Te modes.

2.5 Loopback Modes

2.5.1 Digital Loopback

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the AR8031 device. Figure 2-4 shows a block diagram of digital loopback.

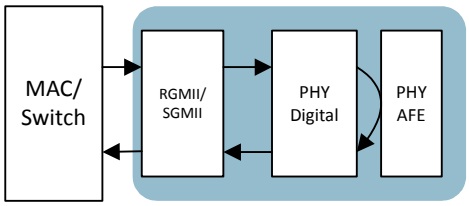


Figure 2-4. **Digital Loopback**

Followings are the register settings for loopback mode selection:

- 1000M loopback: register 0x0 = 0x4140
- 100M loopback: register 0x0 = 0x6100
- 10M loopback: register 0x0 = 0x4100

2.5.2 External Cable Loopback

External cable loopback loops RGMII/SGMII Tx to RGMII/SGMII Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. Figure 2-5 shows a block diagram of external cable loopback.

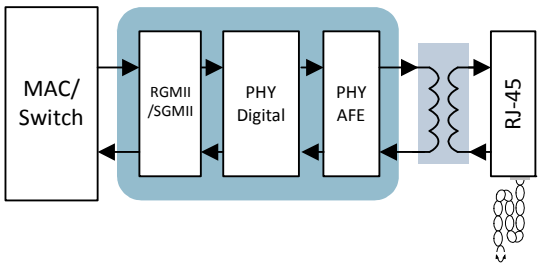


Figure 2-5. **External Cable Loopback**

To configure external loopback:

1. Plug in an external loopback cable (1-3/2-6/4-7/5-8).
2. Set debug register bit 0xB[15] to 0 to disable hibernate (power saving) mode.
3. Set debug register bit 0x11[0] to 1 to enable external loopback.
4. Set register 0x0 to select loopback modes:
   - 1000M loopback: register 0x0 = 0x8140
   - 100M loopback: register 0x0 = 0xA100
   - 10M loopback: register 0x0 = 0x8100

NOTE: When cable is removed and then reconnected to 1000M mode, the register 0x0 must be configured again to 0x8140 to establish PHY link.

2.5.3 Remote PHY Loopback

Remote PHY loopback connects the MDI receive path to the MDI transmit path, thus the remote link partner can detect the connectivity in the resulting loop.

Figure 2-6 shows a block diagram of external cable loopback.

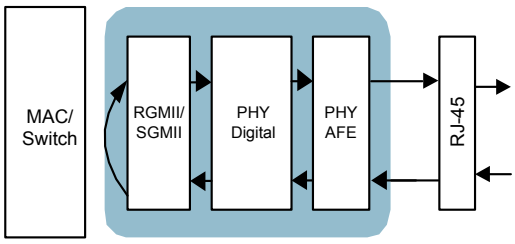


Figure 2-6. **Remote PHY Loopback**

To enable remote PHY loopback, set MMD3 register bit 0x805A[0] to 1.

NOTE: When remote loopback is enabled, packets from link partner will still appear at RGMII interface. Remote loopback is independent of PHY auto-negotiation.

2.6 Cable Diagnostic Test

The Cable Diagnostic Test (CDT) feature in the AR8031 device uses Time Domain Reflectometry (TDR) to identify remote and local PHY malfunctions, bad/marginal cable or patch cord segments, or connectors. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics. The CDT can be performed when there is no link partner or when the link partner is auto-negotiating.

To perform the cable diagnostic test:

1. Set register bits 0x16[9:8] to select the MDI pair to be tested
2. Set register bit 0x16 to 1 to enable CDT
3. Check register bits 0x1C[9:8] for cable failure status.
4. Check register bits 0x1C[7:0] for delta time. The distance between the falure point and PHY is [delta time] * 0.824.

2.7 Fiber Mode Support

Besides standard 10/100/1000 BASE-T copper port support, Both AR8031 and AR8031 provide additional IEEE 1000 BASE-X and 100 BASE-FX support in fiber applications through integrated SERDES. Both the AR8031 and the AR8033 can work in RGMII mode to fiber or 10/100/1000 BASE-T to fiber.

Besides 1000 BASE-X and 100 BASE-FX support, Both devices will support IEEE 802.3 remote Fault Indication and fault propagation in fiber application.

2.7.1 IEEE 802.3 Remote Fault Indication Support

Remote Fault allows stations on a fiber optic link to know when there is a problem on the link. Without Remote Fault, a station can not detect a problem that affects only one fiber (Transmit, for example).

With Remote Fault, the loss of a Receive signal (Link) causes the Transmitter to send a special pattern of data indicating that a fault has occurred. 84 '1's followed by a single '0' is sent three times, in-band, and is readily detectable by the remote station, but is constructed so as to not satisfy the 100BASE-X carrier sense criterion, so the message will not be interpreted as normal traffic. If the remote station has Remote Fault, the link is dropped. If the remote station does not have Remote Fault, the special data pattern is ignored.

The AR8031 indicates whether or not a Remote Fault pattern has been received from the remote station using the "Remote Fault Status Bit". This "Remote Fault Status Bit" can be "Propagated" (see below) to the copper links on both ends of a fiber link. In the event of a

detected fault, both ends of the link can be notified of the failure in this way. This is particularly useful given the distances fiber links are generally used over.

2.7.2 Fault Propagation

The AR8031 supports Fault Propagation - this allows the fiber link fault to be propagated to the Twisted-pair copper connections where the "link down" status can be easily and quickly detected.

The following steps describe Fault Propagation (for both 100 BASE-FX and 1000 BASE-X):

The AR8031 supports Fault Propagation - this allows the fiber link fault to be propagated to the Twisted-pair copper connections where the "link down" status can be easily and quickly detected.

The following steps describe Fault Propagation (for both 100 BASE-FX and 1000 BASE-X):

- The Twisted-pair transmit path will be OFF when the Receive path of the Fiber link has no signal detected or is link down. The two Fiber media types are then handled as described below:
- The Media Converter (in 100 BASE-FX mode) will transmit Far-End Fault message, on the TX pair, when the Receive path of Fiber has no signal detected or is link down. This alerts the Media Converter on the remote end of the link.
- The Transmit Twisted-pair will then be switched OFF on the remote end of the link.
- The Media Converter (in 1000 BASE-X mode) will restart auto-negotiation when the Receive path of the Fiber detects no signal or is link down.
- Auto-negotiation will carry remote fault indications from the Transmit fiber and the local station will restart auto-negotiation when its' Receive path has no detected signal or is link down.
- The Twisted-pair transmit path will be OFF when the Receive path of a 1000 BASE-X learns of the fault from an AN message.

Figure 2-7 shows the Fiber Fault mechanism.

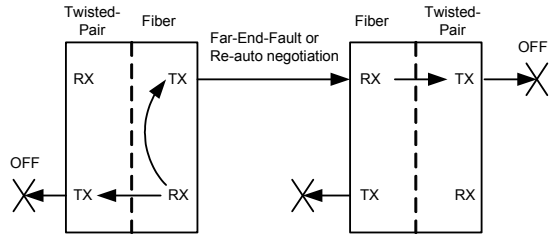


Figure 2-7. **Fiber Fault Propagation or Re-Auto-negotiation**

2.8 LED Interface

The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. The LEDs have three status to indicate operation speed, traffic mode, and link status. The LEDs can be programmed to different status functions from their default value.

Figure 2-8 and Figure 2-9 shows the references designs for the LED interface.

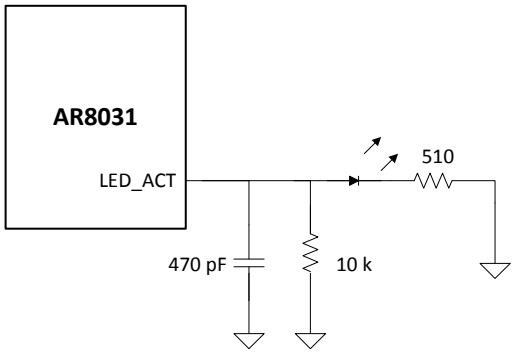


Figure 2-8. **Reference Design for LED, Active High**

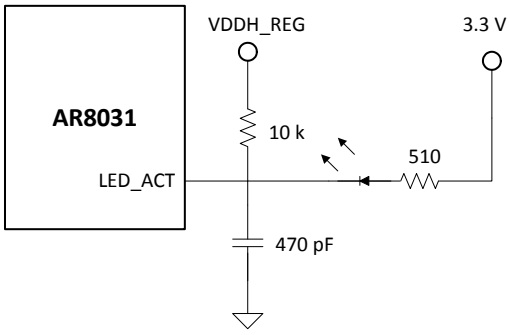


Figure 2-9. **Reference Design for LED, Active Low**

The active status of LED_ACT and LED_LINK1000 depends on power-on strapping mode. When the interface is strapped high, the LED interface are active low; when strapped low, active high. The active status of LED_LINK10_100 depends on LED_LINK1000 power-on strapping mode and thus LED_LINK10_100 and LED_LINK1000 use the same LED reference design.

Table 2-4. **LED Status**

Symbol	10M Link	10M Active	100M Link	100M Active	1000M Link	1000M Active
LED_LINK10_100	OFF	OFF	ON	ON	OFF	OFF
LED_LINK1000	OFF	OFF	OFF	OFF	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK

NOTE: ON = active; OFF = inactive

2.9 Power Supplies

The AR8031 device requires only one 3.3 V external power supply. Internal power rails are 3.3 V, 2.5V, 1.1V and 1.8V/1.5V.

AR8031 integrates a switch regulator to convert 3.3V to 1.1V with high efficiency for core power rail, thus external regulator is optional.

Two on-chip LDOs are integrated to support 2.5V/1.5V/1.8V RGMII I/O voltages. AR8031 can also work at 2.5 V RGMII I/O voltage and 3.3 V MAC RGMII interface. Since the input can bear 3.3V logic signal, and the output logic VoH and VoL can satisfy the 3.3V LVCMOS/LVTTL requirement. Refer to "Electrical Characteristics" for parameter details.

Figure 2-10 shows the reference design for 2.5V/3.3V RGMII voltage level:

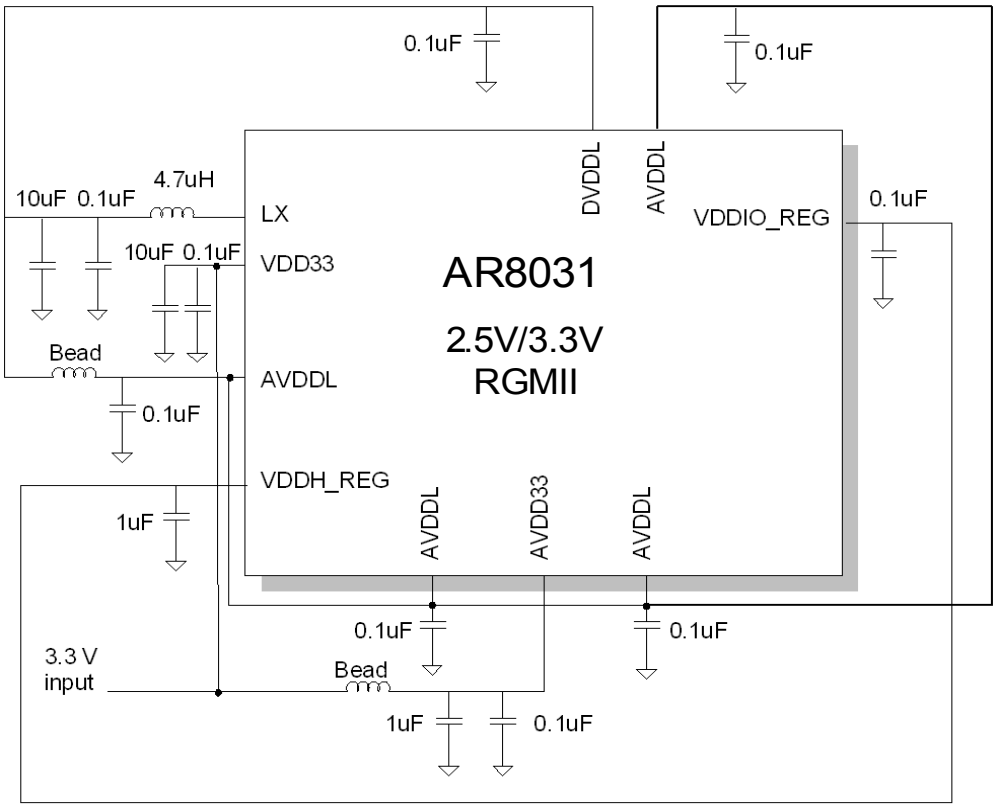


Figure 2-10. **Reference Design, 2.5 V/ 3.3 V RGMII I/O**

Figure 2-11 shows the reference design for 1.5/1.8 V RGMII voltage level.

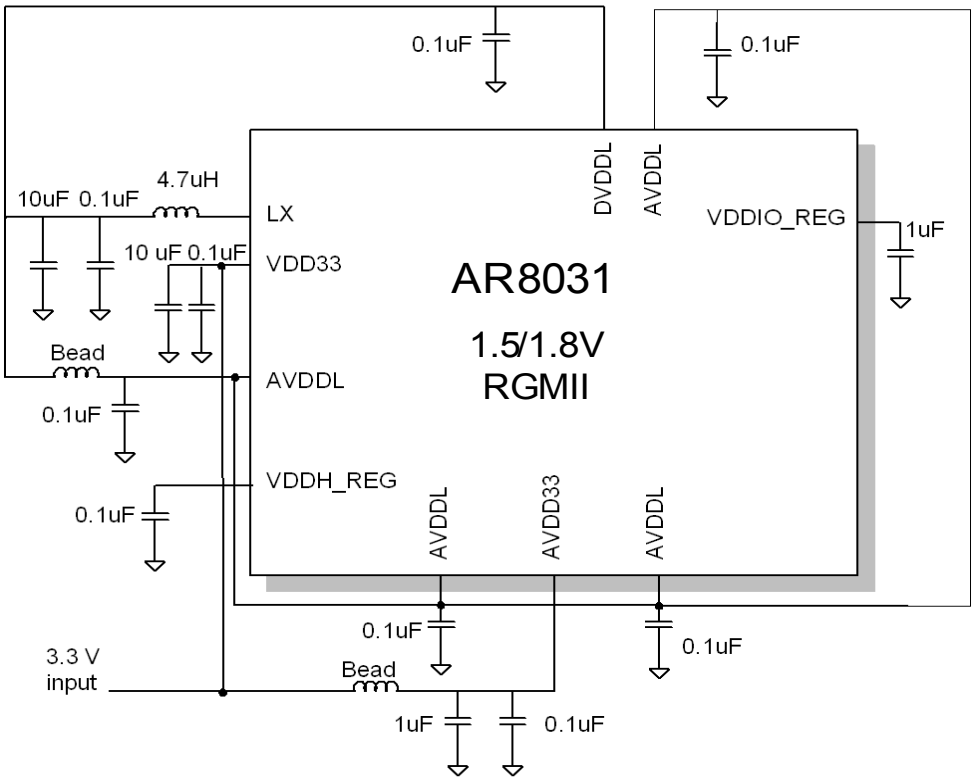


Figure 2-11. **Reference Design, 1.5/1.8 V RGMII I/O**

2.10 Management Interface

AR8031 integrates an MDC/MDIO management interface in compliance with IEEE802.3u clause 22.

MDC is input clock reference provided by the MAC. MDIO is the management data input/output bi-directional signal that runs synchronously to MDC.

MDIO is an OD-gate and requires an external 1.5k pull-up resistor.

Table 2-5 shows the structure of the management frame.

Table 2-5. **Management Frame Fields**

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Table 2-6. **Management Interface Field Definitions**

Field	Definition
PRE	A sequence of 32 contiguous single logic bits on MDIO with corresponding cycles on MDC to provide PHY with a pattern to for synchronization.
ST	Start of frame
OP	Operation code. 10 = read transaction, 01 = write transaction
PHYAD	PHY address. The 5-bit PHY address is configured by power-on strapping. Three address bits can be configured in AR8031, thus eight PHYs can be connected to a single management interface. The PHYs connected to the same bus has unique PHY addresses. The first PHY address bit transmitted and received is the MSB of the address.
REGAD	Register address. The 5-bit register address allows 32 registers to be addressed at each PHY. The first register address bit transmitted and received is the MSB of the address.
TA	2-bit field to avoid contention during a read operation. In read operation, both MAC and PHY are at high-impedance state for the first bit time. The PHY drives a zero during the second bit time of the turnaround. In write operation, the MAC must drive 10.
DATA	16-bit data from accessed register. MSN is transmitted first.
IDLE	High-impedance without driving state of the MDIO. At least one clocked idle state is required between frames.