Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

March 2011

# AR8035 Integrated 10/100/1000 Gigabit Ethernet Transceiver

## General Description

The AR8035 is part of the Arctic family of devices - which includes the AR8031, AR8033, and the AR8035. It is Atheros' 4th generation, single port 10/100/1000 Mbps Tri-speed Ethernet PHY. It supports RGMII interface to the MAC.™

The AR8035 provides a low power, low BOM (Bill of Materials) cost solution for comprehensive applications including consumer, enterprise, carrier and home networks such as PC, HDTV, Gaming machines, Blue-ray players, IPTV STB, Mdia Players, IP Cameras, NAS, Printers, Digital Photo Frames, MoCA/Homeplug (Powerline)/EoC/ adapters and Home Router & Gateways, etc.

The AR8035 integrates Atheros latest Green Ethos® power saving technologies and significantly saves power not only during work time, but also during overtime. Atheros Green Ethos® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. Furthermore, the AR8035 supports Wake-on-LAN (WoL) feature to be able to help manage and regulate total system power requirements.

The AR8035 embeds CDT (Cable Diagnostics Test) technology on-chip which allows customers to measure cable length, detect the cable status, and identify remote and local PHY malfunctions, bad or marginal patch cord segments or connectors. Some of the possible problems that can be detected include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and a bad transformer.

The AR8035 also integrates a voltage regulator on chip. It reduces the termination R/C circuitry on both the MAC interface (RGMII) and line side.

The AR8035 supports IEEE 802.3az Energy Efficient Ethernet (EEE) standard and Atheros proprietary SmartEEE, which allows legacy MAC/SoC devices without 802.3az support to function as the complete 802.3az system. The key features supported by the device are:

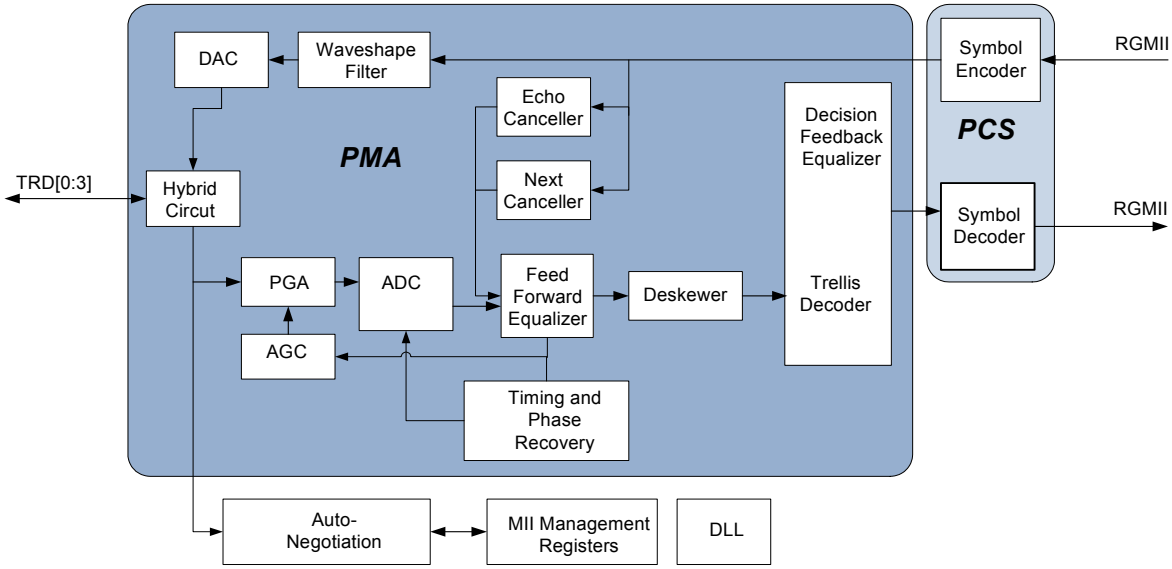
- 10BASE-Te PHY supports reduced transmit amplitude.
- 100BASE-Tx and 1000BASE-T use Low Power Idle (LPI) mode to turn off unused analog and digital blocks to save power while data traffic is in idle.

## Features

- 10BASE-Te/100BASE-Tx/1000 BASE-T IEEE 802.3 compliant
- Supports 1000 BASE-T PCS and auto-negotiation with next page support
- Supports RGMII interface to MAC devices with a broad I/O voltage level options including 2.5V, 1.8V and 1.5V, and is compatible with 3.3V I/O
- RGMII timing modes support internal delay and external delay on Rx path
- Error-free operation up to 140 meters of CAT5 cable
- Supports Atheros latest Green Ethos® power saving modes with internal automatic DSP power saving scheme
- Supports 802.3az (Energy Efficient Ethernet)
- Fully integrated digital adaptive equalizers, echo cancellers, and near end crosstalk (NEXT) cancellers
- Supports Wake-on-LAN (WoL) to detect magic packet and notify the sleeping system to wake up
- A robust Cable Discharge Event (CDE) tolerence of ± 6kV
- A robust surge protection with ±750V/ differential mode and ±4KV/common mode
- Jumbo Frame support up to 10KB (full duplex)
- All digital baseline wander correction
- Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Software programmable LED modes
- Multiple Loopback modes for diagnostics

- Cable Diagnostic Test (CDT)
- Single power supply: 3.3V
- 5mm x 5mm. 40-pin QFN package

## AR8035 Functional Block Diagram



## Table of Contents

# 1. Pin Descriptions

This section contains a package pinout for the AR8035 QFN 40 pin and a listing of the signal descriptions (see Figure 1-1).

The following nomenclature is used for signal names:

| | |
|---|---|
| NC | No connection to the internal die is made from this pin |
| n | At the end of the signal name, indicates active low signals |
| P | At the end of the signal name, indicates the positive side of a differential signal |
| N | At the end of the signal name indicates he negative side of a differential signal |

The following nomenclature is used for signal types described in Table 1-1:

| | |
|---|---|
| D | Open drain |
| IA | Analog input signal |
| I | Digital input signal |
| IH | Input signals with weak internal pull-up, to prevent signals from floating when left open |
| IL | Input signals with weak internal pull-down, to prevent signals from floating when left open |
| I/O | A digital bidirectional signal |
| OA | An analog output signal |
| O | A digital output signal |
| P | A power or ground signal |
| PD | Internal pull-down for input |
| PU | Internal pull-up for input |

Figure 1-1 shows the pinout diagram for the AR8035.

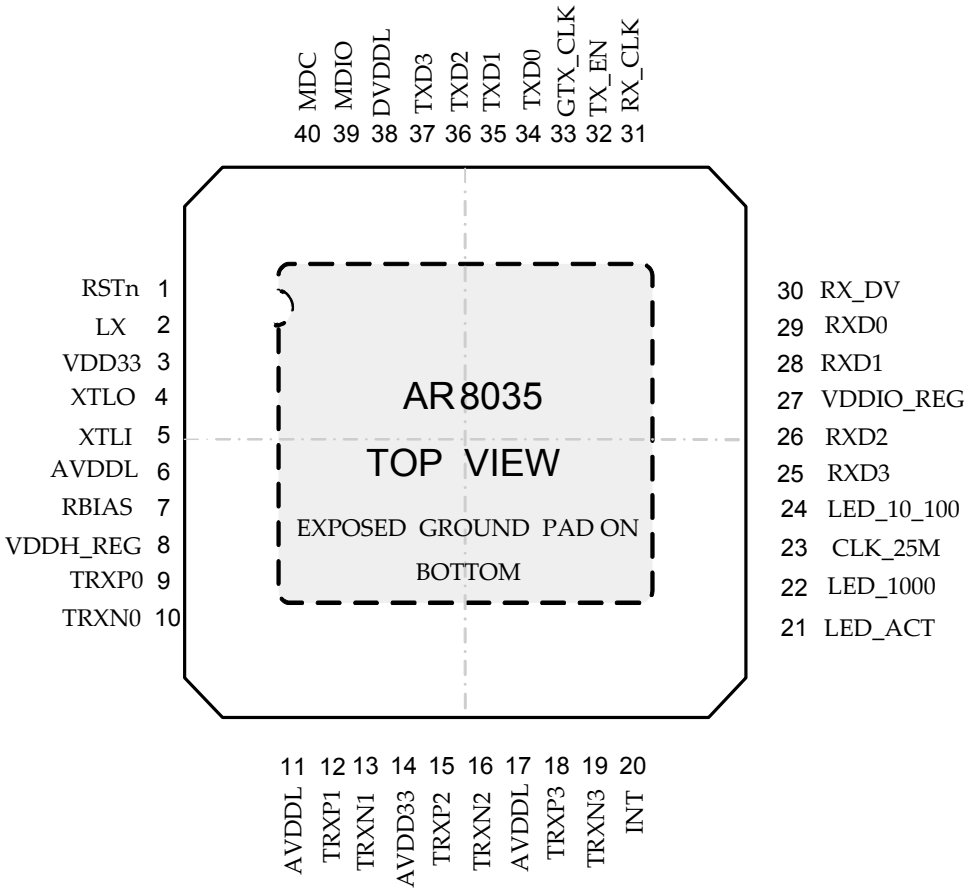



*Figure 1-1*. **Pinout Diagram**

**NOTE:** There is an exposed ground pad on the back side of the package.

| Symbol | Pin | Type | Description |
|---|---|---|---|
| **MDI** | | | |
| TRXP0, TRXN0 | 9, 10 | IA, OA | Media-dependent interface 0, 100 Ω transmission line |
| TRXP1, TRXN1 | 12, 13 | IA, OA | Media-dependent interface 1, 100 Ω transmission line |
| TRXP2, TRXN2 | 15, 16 | IA, OA | Media-dependent interface 2, 100 Ω transmission line |
| TRXP3, TRXN3 | 18, 19 | IA, OA | Media-dependent interface 3, 100 Ω transmission line |
| **RGMII** | | | |
| GTX_CLK | 33 | I, PD | RGMII transmit clock, 125 MHz digital. Adding a 22Ω damping resistor is recommended for EMI design near MAC side. |
| RX_CLK | 31 | I/O, PD | 125MHz digital, adding a 22Ω damping resistor is recommended for EMI design near PHY side. |
| RX_DV | 30 | I/O, PD | RGMII receive data valid |
| RXD0 | 29 | I/O, PD | RGMII received data 0 |
| RXD1 | 28 | I/O, PD | RGMII received data 1 |
| RXD2 | 26 | I/O, PD | RGMII received data 2 |
| RXD3 | 25 | I/O, PD | RGMII received data 3 |
| TX_EN | 32 | I, PD | RGMII transmit enable |
| TXD0 | 34 | I, PD | RGMII transmit data 0 |
| TXD1 | 35 | I, PD | RGMII transmit data 1 |
| TXD2 | 36 | I, PD | RGMII transmit data 2 |
| TXD3 | 37 | I, PD | RGMII transmit data 3 |
| **Management Interface and Interrupt** | | | |
| MDC | 40 | I, PU | Management data clock reference |
| MDIO | 39 | I/O, D, PU | Management data, 1.5KΩ pull-up to 3.3V/2.5V |
| INT | 20 | I/O, D, PD | Interrupt Signal to System; default OD-gate, needs an external 10KΩ pull-up, active low; can be configured to I/O by register, active high. |
| **LED** | | | |
| LED_ACT | 21 | I/O, PU | Parallel LED output for 10/100/1000 BASE-T activity, active blinking. LED active based upon power-on strapping. If pulled up — active low, if pulled down — active high |
| LED_1000 | 22 | I/O, PU | Parallel LED output for 1000 BASE-T link, LED active based upon power-on strapping. If pulled up — active low, if pulled down — active high |

| Symbol | Pin | Type | Description | |
|---|---|---|---|---|
| LED_10_100 | 24 | I/O, PU | Parallel LED output for 10/100 BASE-T link.<br>LED active based upon power-on strapping of LED_1000. If LED_1000 is pulled up,this pin is active low; If LED_1000 is pulled-down, active high. | |
| | | | High, external PU | 10 Mbps |
| | | | Low, external PU | 100 Mbps |
| **System Signal Group/Reference** | | | | |
| CLK_25M | 23 | O, PD | 25 MHz clock output (default). It can be 125, 62.5 or 50 MHz clock output | |
| RSTn | 1 | I | System reset, active low. Requires an external pull-up resistor | |
| XTLI | 5 | IA | Crystal oscillator input. Requries a 27 pF capacitor to GND. Support external 25 MHz, 1.2V swing clock input through this pin. | |
| XTLO | 4 | OA | Crystal oscillator output; 27 pF to GND | |
| RBIAS | 7 | OA | External 2.37 kΩ 1% to GND to set bias current | |
| **Power** | | | | |
| LX | 2 | OA | Power inductor pin. Add an external 4.7 uH power inductor between this pin and pin 38. | |
| VDDH_REG | 8 | OA | 2.5 V regulator output. A 1uF capacitor connected to this pin | |
| VDDIO_REG | 27 | OA | 1.5V/1.8V regulator output.If RGMII interface voltage level is 2.5V, connect this pin to pin 8 directly. | |
| AVDDL | 6, 11, 17 | P | 1.1 V analog power input. Connect to Pin 38 through a bead | |
| DVDDL | 38 | P | 1.1 V digital core power input. Connect to power inductor and 10uF+0.1uF ceramic capacitors to GND | |
| VDD33 | 3 | P | 3.3 V power for switching regulator | |
| AVDD33 | 14 | P | Analog 3.3 V power input for PHY, from VDD33 through a bead | |
| - | - | | Exposed ground pad on back of the chip, tie to ground | |

| PHY Pin | PHY Core Config Signal | Description | Default Internal Weak Pull-up/Pull-down |
|---|---|---|---|
| RXD0 | PHYADDRESS0 | LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, “00” | 0 |
| RXD1 | PHYADDRESS1 | | 0 |
| LED_ACT | PHYADDRESS2 | | 1 |
| RX_DV | MODE0 | mode select bit 0 | 0 |
| RXD2 | MODE1 | mode select bit 1 | 0 |
| LED_1000 | MODE2 | mode select bit 2 | 1 |
| RXD3 | MODE3 | mode select bit 3 | 0 |
| RX_CLK | 1.8V/1.5V | Select the RGMII/RMII I/O voltage level<br>1: 1.8V I/O<br>0: 1.5V I/O | 0 |

**NOTE:** 0=Pull-down, 1=Pull-up

**NOTE:** Power on strapping pins are latched during power-up reset or warm hardware reset.

**NOTE:** Some MAC devices input pins may drive high/low during power-up or reset. So PHY power on strapping status may be affected by the MAC side. In this case an external 10kΩ pull-down or pull-high resistor is needed to ensure a stable expected status.

**NOTE:** When using 2.5V RGMII I/O voltage level, RX_CLK can be pull-up or pull-down.

| MODE[3:0] | Description |
|---|---|
| 1100 | RGMII, PLLOFF, INT; |
| 1110 | RGMII, PLLON, INT; |
| Others | Reserved |

**NOTE:** PLLOFF means AR8035 can shut down internal PLL in power saving mode; In PLLOFF mode, when the AR8035 enters power saving mode (hibernation), CLK_25m output drops periodically, which saves more power. In PLLON mode, CLK_25M outputs continuously.

# 2. Functional Description

The AR8035 is Atheros's low cost GbE PHY. It is a highly integrated analog front end (AFE) and digital signal transceiver, providing high performance combined with substantial cost reduction. The AR8035 provides physical layer functions for half/full -duplex 10 BASE-Te, 100 BASE-Tx and 1000 BASE-T Ethernet to transmit and receive high-speed data over standard category 5 (CAT5) unshielded twisted pair cable.

The AR8035 10/100/1000 PHY is fully 802.3ab compliant, and supports the reduced Gigabit Media-Independent Interface (RGMII) to connect to a Gigabit-capable MAC.

The AR8035 transceiver combines echo canceller, near end cross talk (NEXT) canceller, feed-forward equalizer, joint Viterbi, feedback equalizer, and timing recovery, to enhance signal performance in noisy environments.

The AR8035 is a part of the Arctic family of devices — which includes the AR8031, the AR8033, and the AR8035. A comparison of these is shown below.

Table 2-1 shows a feature comparison across the AR8031, AR8033, and AR8035 family.

*Table 2-1.* **AR8031, AR8033, AR8035 Comparison**

| Feature | AR8031 | AR8033 | AR8035 |
|---|---|---|---|
| RGMII | yes | yes | yes |
| SGMII | yes | yes | |
| Cu Ethernet** | yes | yes | yes |
| EEE (802.3az) | yes | yes | yes |
| Wake-on-LAN | yes | yes | yes |
| SERDES/Fiber | yes*** | yes*** | |
| 1588v2 | yes | | |
| Sync-E | yes | yes | |
| Packaging | 48-pin | 48-pin | 40-pin |

**NOTE:** AR8031, AR8033 is pin-to-pin compatible

**NOTE:** ** 10BASE-Te, 100BASE-TX, 1000BASE-T will be supported

**NOTE:** *** 100BASE-FX, and 1000BASE-X will be supported

## 2.1 Transmit Functions

Table 2-2 describes the transmit function encoder modes.

*Table 2-2.* **Transmit Encoder Modes**

| Encoder Mode | Description |
|---|---|
| 1000 BASE-T | In 1000 BASE-T mode, the AR8035 scrambles transmit data bytes from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT5 cable. |
| 100 BASE-TX | In 100 BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA. |
| 10 BASE-Te | In 10 BASE-Te mode, the AR8035 transmits and receives Manchester-encoded data. |

## 2.2 Receive Functions

### 2.2.1 Decoder Modes

Table 2-3 describes the receive function decoder modes.

*Table 2-3.* **Receive Decoder Modes**

| Decoder Mode | Description |
|---|---|
| 1000 BASE-T | In 1000 BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately and data is output to the MAC interfaces. |
| 100 BASE-TX | In 100 BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to the MII receive data pins after data stream delimiters have been translated. |
| 10 BASE-Te | In 10 BASE-Te mode, the recovered 10 BASE-Te signal is decoded from Manchester then aligned. |

### 2.2.2 Analog to Digital Converter

The AR8035 device employs an advanced high speed ADC on each receive channel with high resolution, which results in better SNR and lower error rates.

### 2.2.3 Echo Canceller

A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects back as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, also result in drastic SNR degradation on the receive signal. The AR8035 device implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

### 2.2.4 NEXT Canceller

The 1000 BASE-T physical layer uses all four pairs of wires to transmit data. Because the four twisted pairs are bundled together, significant high frequency crosstalk occurs between adjacent pairs in the bundle. The AR8035 device uses three parallel NEXT cancellers on each receive channel to cancel high frequency crosstalk. The AR8035 cancels NEXT by subtracting an estimate of these signals from the equalizer output.

### 2.2.5 Baseline Wander Canceller

Baseline wander results from Ethernet links that AC-couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. Baseline wander is more problematic in the 1000 BASE-T environment than in 100 BASE-TX due to the DC baseline shift in the transmit and receive signals. The AR8035 device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

### 2.2.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision

feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

### 2.2.7 Auto-Negotiation

The AR8035 device supports 10/100/1000 BASE-T Copper auto-negotiation in accordance with IEEE 802.3 clauses 28 and 40. Auto-negotiation provides a mechanism for transferring information between a pair of link partners to choose the best possible mode of operation in terms of speed, duplex modes, and master/slave preference. Auto-negotiation is initiated upon any of the following scenarios:

- Power-up reset
- Hardware reset
- Software reset
- Auto-negotiation restart
- Transition from power-down to power-up
- The link goes down

If auto-negotiation is disabled, a 10 BASE-Te or 100 BASE-TX can be manually selected using the IEEE MII registers.

### 2.2.8 Smartspeed Function

The Atheros Smartspeed function is an enhanced feature of auto-negotiation that allows the AR8035 device to fall back in speed based on cabling conditions as well as operate over CAT3 cabling (in 10 BASE-T mode) or two-pair CAT5 cabling (in 100 BASE-TX mode).

By default, the Smartspeed feature is enabled. Refer to the register "Smart Speed" on page 43, which describes how to set the parameters. Set these register bits to control the Smartspeed feature:

- Bit [5]: 1 = Enables Smartspeed (default)
- Bits [4:2]: Sets the number of link attempts before adjusting
- Bit [1]: Timer to determine the stable link condition

### 2.2.9 Automatic MDI/MDIX Crossover

During auto-negotiation, the AR8035 device automatically determines and sets the required MDI configuration, eliminating the need for external crossover cable. If the remote device also implements automatic MDI crossover, the crossover algorithm as described in IEEE 802.3 clause 40.4.4 ensures that only one device performs the required crossover.

### 2.2.10 Polarity Correction

If cabling has been incorrectly wired, the AR8035 automatically corrects polarity errors on the receive pairs in 1000 BASE-T, 100 BASE-TX and 10 BASE-Te modes.

## 2.3 Loopback Modes

### 2.3.1 Digital Loopback

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the AR8035 device. Figure 2-1 shows a block diagram of a digital loopback.

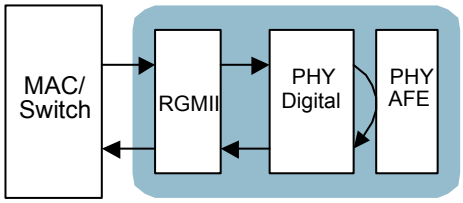



*Figure 2-1.* **Digital Loopback**

- 1000M loopback: write register 0x0 = 0x4140 to enable 1000M digital loopback.
- 100M loopback: write register 0x0 = 0x6100 to enable 100M digital loopback.
- 10M loopback: write register 0x0 = 0x4100 to enable 10M digital loopback.

### 2.3.2 External Cable Loopback

External cable loopback loops Tx to Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. Figure 2-2 shows a block diagram of external cable loopback.

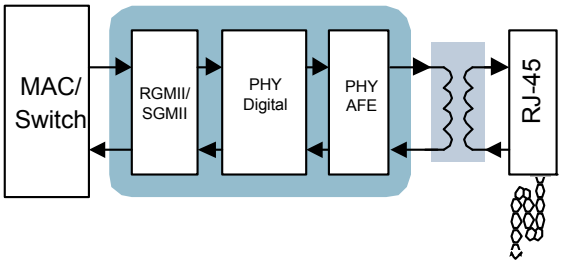



*Figure 2-2.* **External Cable Loopback**

1. Plug in an external loopback cable (1-3/2-6/4-7/5-8)
2. Write debug register 0xB[15] = 0 to disable hibernate (power-saving mode)
3. Write debug register 0x11[0] = 1 to enable external loopback
4. Select wire speed, as follows:

- 1000M loopback: write register 0x0 = 0x8140 to set 1000M external loopback
- 100M loopback: write register 0x0 = 0xA100 to set 100M external loopback
- 10M loopback: write register 0x0 = 0x0x8100 to set 10M external loopback

5. When the cable in 1000M mode is re-plugged, need to write 0x0 = 0x8140 again to make the PHY link.

### 2.3.3 Remote PHY Loopback

The Remote loopback connects the MDI receive path to the MDI transmit path, near the RGMII interface, thus the remote link partner can detect the connectivity in the resulting loop. Figure 2-3, below, shows the path of the remote loopback.

Figure 2-3 shows a block diagram of external cable loopback.

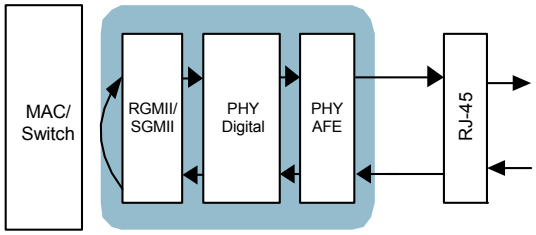



*Figure 2-3.* **Remote PHY Loopback**

- Write MMD3 register 0x805A[0]= 1 to enable remote PHY loopback.

**Please note**: The packets from link partner will still appear at RGMII interface when remote loopback is enabled.

Also, remote loopback is independant of PHY auto-negotiation.

## 2.4 Cable Diagnostic Test

The Cable Diagnostic Test (CDT) feature in the AR8035 device uses Time Domain Reflectometry (TDR) to identify remote and local PHY malfunctions, bad/marginal cable or patch cord segments, or connectors. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics. The CDT can be performed when there is no link partner or when the link partner is auto-negotiating.

1. Set register 0x16[9:8] to select MDI pair under test
2. Write register 0x16[0]=1 to enable CDT
3. Check register 0x1C[9:8] for fail status
4. Check register 0x1C[7:0] to get delta time. The distance between the fail point and PHY is delta time *0.842

## 2.5 LED Interface

The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. Three status LEDs are available. These can be used to indicate operation speed, duplex mode, and link status. The LEDs can be programmed to different status functions from their default value. They can also be controlled directly from the MII register interface.

The reference design schematics for the AR8035's LEDs are shown

Figure 2-4 Reference Design Schematic — Active Low

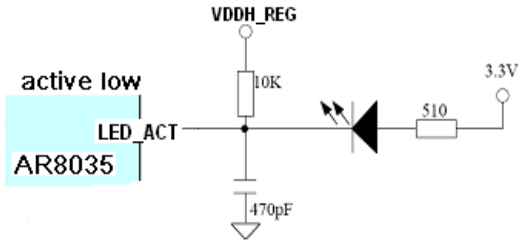



*Figure 2-4.* **Reference Design Schematic — Active Low**

Figure 2-5 Reference Design Schematic — Active High

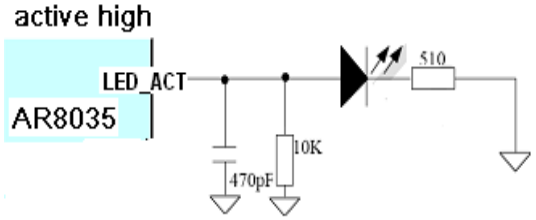



*Figure 2-5.* **Reference Design Schematic — Active High**

LED_ACT/LED_1000 active states depend on power on strapping mode.

When strapped high, active low. When strapped low, active high.

LED_10_100 depends on LED_1000 power on strapping mode.

So LED_10_100 and LED_1000 should have the same LED design.

| Symbol | 10M link | 10M active | 100M link | 100M active | 1000M link | 1000M active |
|---|---|---|---|---|---|---|
| LED_10_100 | off | off | on | on | off | off |
| LED_1000 | off | off | off | off | on | on |
| LED_ACT | on | blink | on | blink | on | blink |

**NOTE:** Notes: on=active off=inactive

## 2.6 Power Supplies

The AR8035 device requires only one external power supply: 3.3 V.

Inside the chip there is a 3.3V rail, 2.5V rail, 1.1V rail and a 1.8V/1.5V rail.

AR8035 integrates a switch regulator which converts 3.3V to 1.1V at a high-efficiency for core power rail. (It is optional for an external regulator to provide this core voltage).

The AR8035 integrates two on chip LDOs which can support 2.5V; 1.5V/1.8V RGMII I/O voltage. Also with 2.5V RGMII I/O voltage configuration AR8035 can work with a 3.3V MAC RGMII interface — because the input can bear 3.3V logic signal, and the output logic VoH and VoL can satisfy the 3.3V LVCMOS/LVTTL requirement. The parameter details are in the Electrical Characteristics chapter.

Reference design for 2.5V RGMII voltage level is shown below:

Figure 2-6 shows the AR8035 reference design for a 2.5V RGMII voltage level.

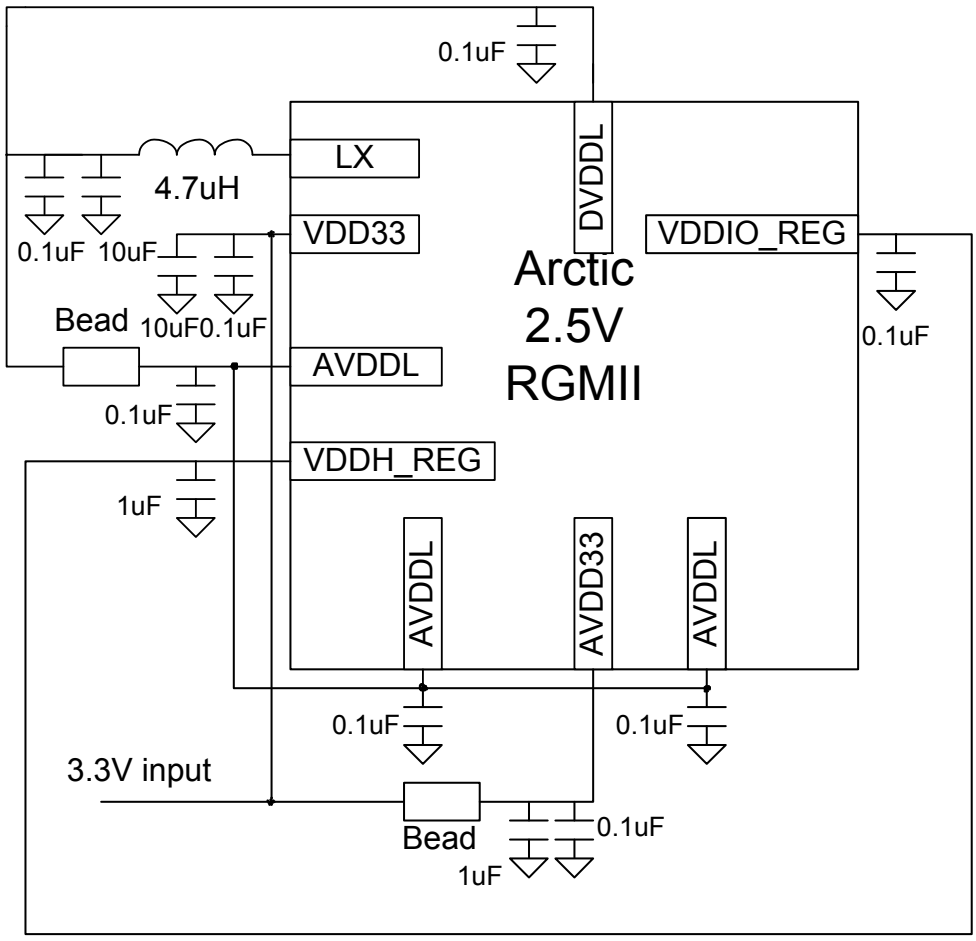



*Figure 2-6.* **AR8035 reference design for a 2.5V RGMII voltage level**

Reference design for 1.5/1.8V RGMII voltage level is shown below:

Figure 2-7 shows the AR8035 reference design for a 1.5/1.8V RGMII voltage level.

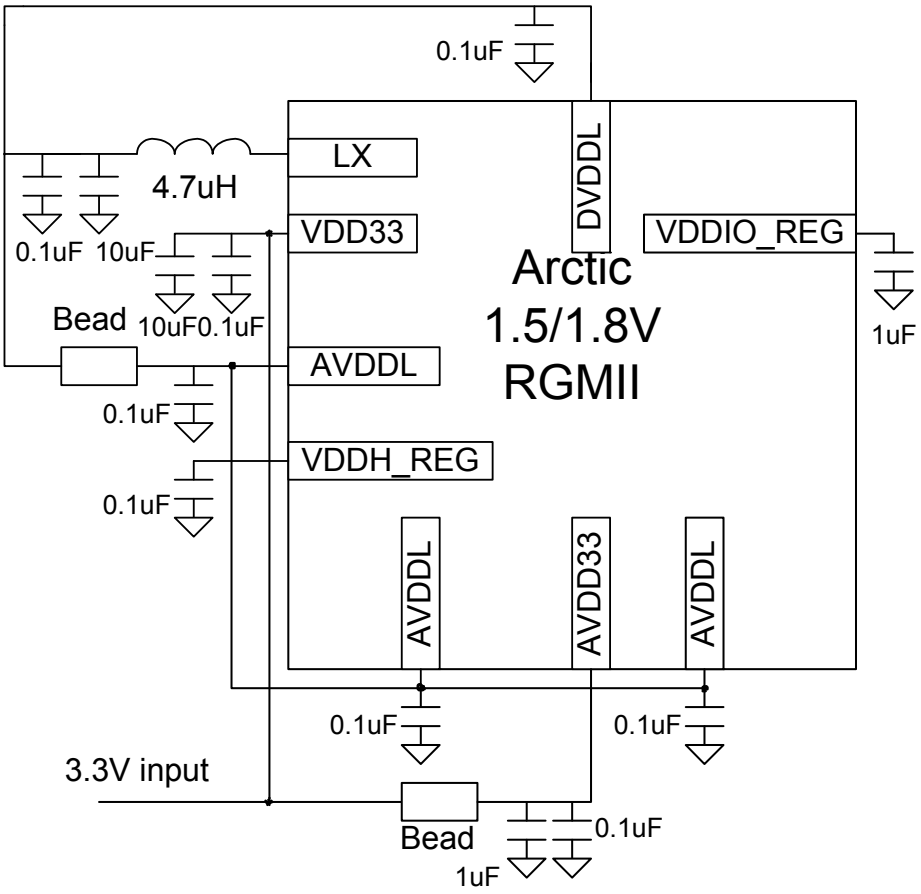



*Figure 2-7.* **AR8035 reference design for a 1.5/1.8V RGMII voltage level**

## *2.7 Management Interface*

The AR8035 integrates an MDC/MDIO management interface which is compliant with IEEE802.3u clause 22.

MDC is an input clock reference provided by the MAC.

MDIO is the management data input/output bi-directional signal that runs synchronously to MDC.

MDIO is an OD-gate, needs an external 1.5k pull-up resistor.

Definition of the management frame is shown below.

Figure 2-8 shows the AR8035 Management frame fields.

| | Management frame fields | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | PRE | ST | OP | PHYAD | REGAD | TA | DATA | IDLE |
| READ | 1...1 | 01 | 10 | AAAAA | RRRRR | Z0 | DDDDDDDDDDDDDDDD | Z |
| WRITE | 1...1 | 01 | 01 | AAAAA | RRRRR | 10 | DDDDDDDDDDDDDDDD | Z |

*Figure 2-8.* **AR8035 Management Frame Fields**

1. PRE is a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can use to establish synchronization.
2. ST is start of frame
3. OP is the operation code. The operation code for a read transaction is <10>, while the operation code for a write transaction is <01>.
4. PHYAD is 5 bits PHY address. PHY address of AR8035 is configured by power on strapping. There are three address bits can be configured in AR8035 which means 8 PHYs can be connected to the same management interface. Each PHY connected to the same bus line should have a unique PHY address. The first PHY address bit transmitted and received is the MSB of the address.
5. The Register Address is five bits, allowing 32 individual registers to be addressed within each PHY. The first Register Address bit transmitted and received is the MSB of the address.
6. TA is 2 bits to avoid contention during a read operation. For a read operation, both the MAC and PHY shall remain in a high-impedance state for the first bit time. The PHY shall drive a zero during the second bit time of the turnaround. During a write transaction, the MAC must drive 10.
7. Data is the 16 bits data from accessed register. MSB is transmitted first.
8. Idle is a high-impedance without driving state of the MDIO. At least one clocked idle state is required between frames.

There are three kinds of registers in AR8035. All can be accessed using the management frames.

1. IEEE defined 32 MII registers.
2. Atheros defined Debug registers.
3. IEEE defined MDIO Manageable Device (MMD) register

MII register can be access directly through the frame defined above.

Debug register access:

1. Write the debug offset address to 0x1D
2. Read/ Write the data from/to 0x1E

MMD register access:

See detail in register description

example: Write 0x8000 to Register 0 of MMD3

1. Write 0x3 to register 0xD: 0xD=0x0003;(function= address; set the device address)
2. Write 0x0 to register 0xE: 0xE=0x0; (set the register offset address)
3. Write 0x4003 to register 0xD:0xD=0x4003;(function=data; keep the device address)
4. Read register 0xE:0xE==(data from register 0x0 of MMD3)
5. Write 0x8000 to register 0xE :0xE=0x8000(write 0x8000 to register 0x0 of MMD3)

**Please Note:** Read operation please refers to process 1 ~ 4

## 2.8 Atheros Green Ethos®

### 2.8.1 Low Power Modes

The AR8035 device supports the software power-down low power mode. The standard IEEE power-down mode is entered by setting the POWER_DOWN bit (bit [11]) of the register "Control" equal to one. In this mode, the AR8035 ignores all MAC interface signals except the MDC/MDIO. It does not respond to any activity on the CAT 5 cable. The AR8035 cannot wake up on its own. It can only wake up by setting the POWER_DOWN bit of the "Control" register to 0, or a Hardware Reset See Table 4.1.15 on page 39.

### 2.8.2 Shorter Cable Power Mode

With Atheros latest propriatary Green Ethos® power saving technology, the AR8035 can attain an additional 25% power savings when a cable length is detected that is < 30M vs. stantard power consumption for a 100M Cat5 cable. The equals and additional 100mW power savings and less than 350mW total power for 1000BASE-T mode in a typical home application.

### 2.8.3 Hibernation Mode

The AR8035 supports hibernation mode. When the cable is unplugged, the AR8035 will enter hibernation mode after about 10 seconds. The

power consumption in this mode can go as low as 10mW only when compared to the normal mode of aperation. When the cable is re-connected, the AR8035 wakes up and normal functioning is restored.

## 2.9 IEEE 802.3az and Energy Efficient Ethernet

IEEE 802.3az provides a mechanism to greatly save the power consumption between data packets bursts. The link partners enter Low Power Idle state by sending short refresh signals to maintain the link.

There are two operating states, Active state for normal data transfer, and Low-power state between the data packet bursts.

In the low-power state, PHY shuts off most of the analog and digital blocks to reserve energy. Due to the bursty traffic nature of Ethernet, system will stay in low-power mode in the most of time, thus the power saving can be more than 90%.

At the link start up, both link partners exchange information via auto neg to determine if both parties are capable of entering LPI mode.

Legacy Ethernet products are supported, and this is made transparent to the user.

### 2.9.1 IEEE 802.3az LPI Mode

AR8035 works in the following modes when 802.3 az feature is turned on:

- Active: the regular mode to transfer data
- Sleep: send special signal to inform remote link of entry into low-power state
- Quiet: No signal transmitted on media, most of the analog and digital blocks are turned off to reduce energy.
- Refresh: send periodically special training signal to maintain timing recovery and equalizer coefficients
- Wake: send special wakup signal to remote link to inform of the entry back into Active.

Figure 2-9 shows the 802.3az operating states for the AR8035.

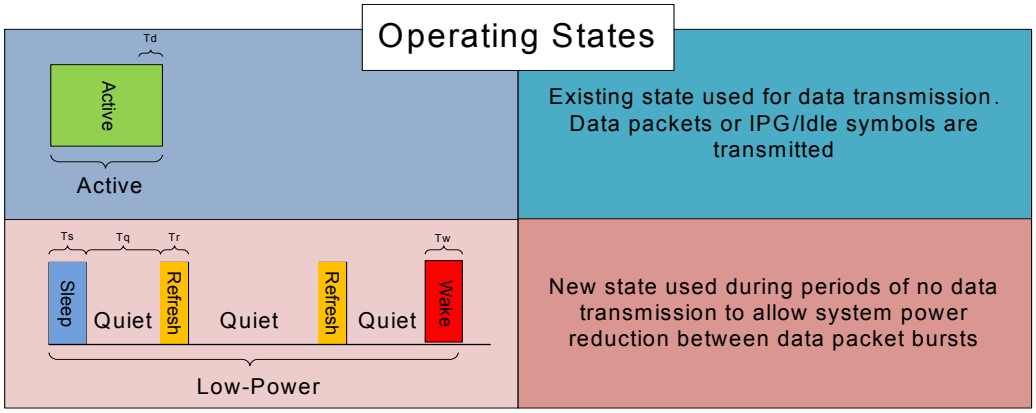



*Figure 2-9.* **Operating States — 802.3az LPI Mode**

Figure 2-10 shows the 802.3az operating power modes — 802.3az for the AR8035.

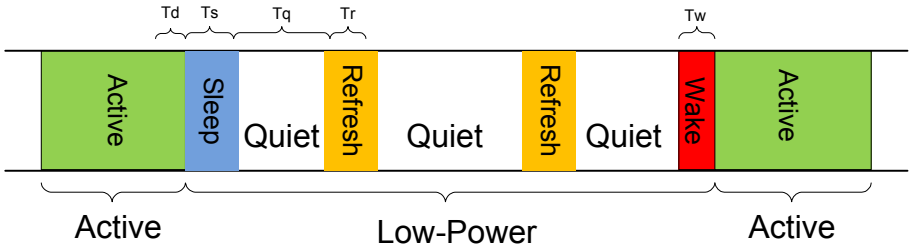



*Figure 2-10.* **Operating Power Modes — 802.3az LPI Mode**

The AR8035 supports both 100BASE-TX EEE and 1000BASE-T EEE.

100BASE-TX EEE allows asymmetrical operation, which allows each link partner to enter the LPI mode independent of the other partner.

1000BASE-T EEE requires symmetrical operation, which means that both link partners must enter the LPI mode simultaneously.

## 2.10 Atheros SmartEEE

AR8035 SmartEEE is compatible with normal 802.3az standard. It helps legacy MAC without EEE ability to work as a complete EEE power saving system.

AR8035 SmartEEE will detect egress data flow, if there are no packets to transfer after a defined time which are cofigurable based on system design, it will enter EEE mode. If there are packets need to transfer, AR8035 will wait typically 16.5us to wake up as 802.3az defined and send out datas after the timer configuration in register. It provides a 2048*20bit buffer for egress data before waking up to ensure no packet loss.

AR8035 default mode enables smart EEE after power on or hardware reset.

Working in smartEEE, AR8035 RX side will not generate MDI LPI pattern. So only normal packets and idle packets will appear on the RGMII inteface. There is no TX LPI pattern at all if MAC has no EEE capability. LPI is generated inside PHY according to smartEEE mechanism.

If the MAC has EEE capability, can write SmartEEE control register to bypass SmartEEE function.

**Please Note**:

1. Wait time before entering EEE mode is in register MMD3 0x805c,0x805d[7:0];
2. Adjustable wait time before sending out data is in register MMD3 0x805b, To cooperate with link partner for special requirement.

## 2.11 Wake On LAN (WoL)

Originally Wake-on-LAN (WoL) was an Ethernet networking standard that allowed a computer to be turned on (or woken up) by a network message for Adminstrator attention, etc. However as part of the latest industry trend towards energy savings, WoL gets wide interest to be adopted across networking systems as a mechanism to help to manage and regulate the total power consumed by the network. The AR8035 supports Wake-on-LAN (WoL):

- Able to enter the sleep/isolate state (PHY's all TX bus (including clock) are in High-Z state, but PHY can still receive packets) by ISOLATE bit in MII register configuration
- Consumes less than 50mW when in sleep/isolate mode
- Supports automatic detection of magic packets (a specific frame containing anywhere within its payload: 6 bytes of ones (resulting in hexadecimal FF FF FF FF FF FF), followed by sixteen repetitions of the target computer's MAC address) and notification via hardware interrupt.
- Supports exit from the sleep state, by register configuration

# 3. Electrical Characteristics

## 3.1 Absolute Maximum Ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the AR8035. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

*Table 3-1.* **Absolute Maximum Ratings**

| Symbol | Parameter | Max Rating | Unit |
|---|---|---|---|
| $V_{DD33}$ | 3.3V analog supply voltage | 3.8 | V |
| $A_{VDD}$ | 1.1V analog supply voltage | 1.6 | V |
| $D_{VDD}$ | 1.1V digital core supply voltage | 1.6 | V |
| $T_{store}$ | Storage temperature | –65 to 150 | °C |
| HBM | Electrostatic discharge tolerance - Human Body Model | ±2kV | V |
| MM | Machine Model | ±200V | V |
| CDM | Charge Device Model | ±500V | V |

## 3.2 Recommended Operating Conditions

*Table 3-2.* **Recommended Operating Conditions**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VDD33/AVDD33 | 3.3V supply voltage | 3.14 | 3.3 | 3.47 | V |
| AVDDL/DVDDL | 1.1V digital core supply voltage | 1.04 | 1.1 | 1.17 | V |
| $T_A$ | Ambient temperature for normal opteraiton - Commercial chip version | 0 | — | 70 | °C |
| $T_A$ | Ambient temperature for normal opteraiton - Industrial chip version | -40 | — | 85 | °C |
| $T_J$ | Junction temperature | -40 | — | 125 | °C |
| $\Psi_{JT}$ | Thermal Dissipation Coefficient | — | 4 | — | °C/W |

**NOTE:** The following condition must be satisfied:

$$T_{Jmax} > T_{Cmax} + \Psi_{JT} \times P_{Typical}$$

Where:

$T_{Jmax}$ = maximum allowable temperature of the Junction

$T_{Cmax}$ = Maximum allowable case temperature

$\Psi_{JT}$ = Thermal Dissipation Coefficient

$P_{Typical}$ = Typical power dissapation

## 3.3 RGMII Characteristics

Table 3-3 shows the RGMII DC characteristics with 2.5/3.3V I/O supply.

*Table 3-3.* **RGMII DC Characteristics — 2.5/3.3V I/O Supply**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $I_{IH}$ | Input high current | — | 15 | µA |
| $I_{IL}$ | Input low current | –15 | — | µA |
| $V_{IH}$ | Input high voltage | 1.7 | 3.5 | V |
| $V_{IL}$ | Input low voltage | — | 0.7 | V |
| $V_{OH}$ | Output high voltage | 2.4 | 2.8 | V |
| $V_{OL}$ | Output low voltage | GND – 0.3 | 0.4 | V |

Table 3-4 shows the RGMII DC characteristics with 1.8V I/O supply.

*Table 3-4.* **RGMII DC Characteristics — 1.8V I/O Supply**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 1.4 | — | V |
| $V_{IL}$ | Input low voltage | — | 0.4 | V |
| $V_{OH}$ | Output high voltage | 1.5 | — | V |
| $V_{OL}$ | Output low voltage | — | 0.3 | V |

Table 3-5 shows the RGMII DC characteristics with 1.5V I/O supply.

*Table 3-5.* **RGMII DC Characteristics — 1.5 I/O Supply**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 1.2 | — | V |
| $V_{IL}$ | Input low voltage | — | 0.3 | V |
| $V_{OH}$ | Output high voltage | 1.3 | — | V |
| $V_{OL}$ | Output low voltage | — | 0.2 | V |

Figure 3-1 shows the RGMII AC timing diagram — no internal delay.

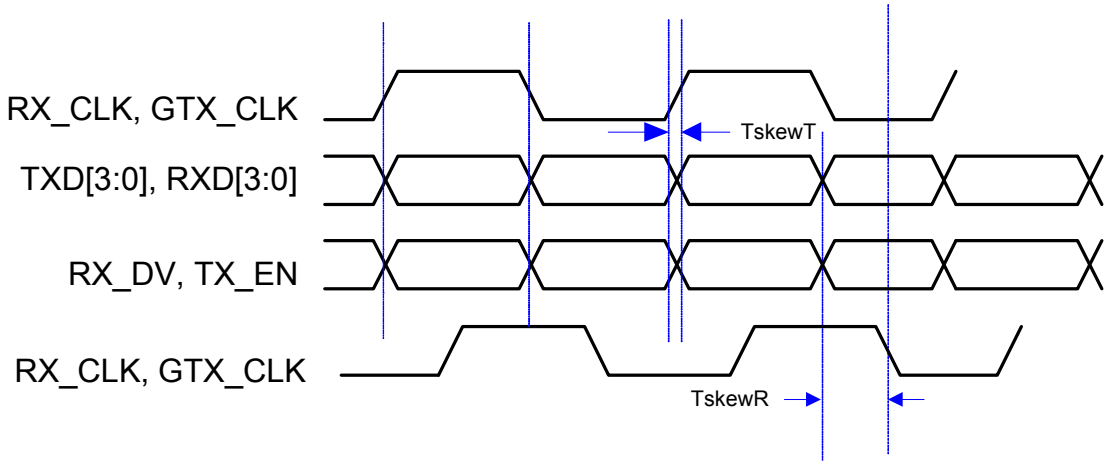



*Figure 3-1*. **RGMII AC Timing Diagram — no Internal Delay**

Table 3-6 shows the RGMII AC characteristics.

*Table 3-6*. **RGMII AC Characteristics — no Internal Delay**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{skewT}$ | Data to clock output skew (at Transmitter) | -500 | 0 | 500 | ps |
| $T_{skewR}$ | Data to clock output skew (at Receiver) | 1 | — | — | ns |
| $T_{cyc}$ | Clock cycle duration | 7.2 | 8.0 | 8.8 | ns |
| Duty_G | Duty cycle for Gigabit | 45 | 50 | 55 | % |
| Duty_T | Duty cycle for 10/100T | 40 | 50 | 60 | % |
| $T_r/T_f$ | Rise/Fall time (20 - 80%) | — | — | 0.75 | ns |

Figure 3-2 shows the RGMII AC timing diagram with internal delay added (default RGMII timing).

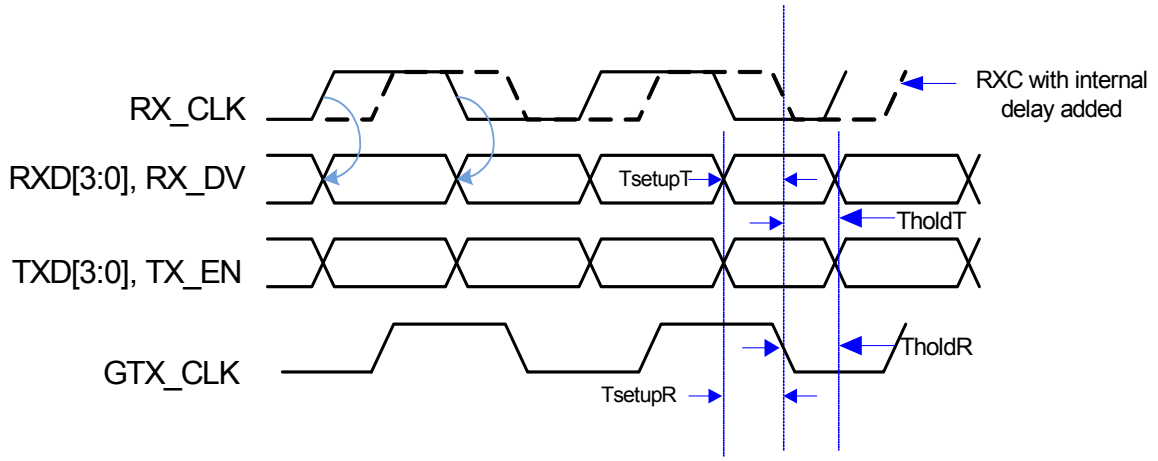



*Figure 3-2.* **RGMII AC Timing Diagram — With Internal Delay Added (Default)**

Table 3-7 shows the RGMII AC characteristics with delay added.

*Table 3-7.* **RGMII AC Characteristics — with internal delay added (Default)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TsetupT | Data to Clock output Setup (at Transmitter — integrated delay) | 1.65 | 2.0 | 2.2 | ns |
| TholdT | Clock to Data output Hold (at Transmitter — integrated delay) | 1.65 | 2.0 | 2.2 | ns |
| TsetupR | Data to Clock input setup Setup (at Receiver — integrated delay) | 1.0 | 2.0 | | ns |
| TholdR | Data to Clock output setup Setup (at Reciever — integrated delay) | 1.0 | 2.0 | | ns |

## 3.4 MDIO Characteristics

MDIO is OD-gate, and can be pulled-up to 2.5/3.3V.

Table 3-8 shows the MDIO DC characteristics.

*Table 3-8.* **MDIO DC Characteristics**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $I_{IH}$ | Input high current | — | 0.4 | mA |
| $I_{IL}$ | Input low current | 0.4 | — | mA |
| $V_{OH}$ | Output high voltage | 2.4 | — | V |
| $V_{OL}$ | Output low voltage | — | 0.4 | V |
| $V_{IH}$ | Input high voltage | 2.0 | — | V |
| $V_{IL}$ | Input low voltage | — | 0.8 | V |

Table 3-9 shows the MDIO AC Characteristics.

*Table 3-9.* **MDIO AC Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| tmdc | MDC Period | 40 | | | ns |
| tmdcl | MDC Low Period | 16 | | | ns |
| tmdch | MDC High Period | 16 | | | ns |
| tmdsu | MDIO to MDC rising setup time | 10 | | | ns |
| tmdhold | MDIO to MDC rising hold time | 10 | | | ns |
| tmdelay | MDC to MDIO output delay | 10 | | 30 | ns |

## *3.5 XTAL/OSC characteristic table*

*Table 3-10.* **XTAL/OSC Characteristic**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| T_XI_PER | XI/OSCI Clock Period | 40.0 - 50ppm | 40.0 | 40.0 + 50ppm | ns |
| T_XI_HI | XI/OSCI Clock High | 14 | 20.0 | | ns |
| T_XI_LO | XI/OSCI Clock Low | 14 | 20.0 | | ns |
| T_XI_RISE | XI/OSCI Clock Rise Time, VIL (max) to VIH (min) | | | 4 | ns |
| T_XI_FALL | XI/OSCI Clock Fall time, VIL (max) TO VIH (min) | | | 4 | ns |
| V_IH_XI | The XI input high level | 0.8 | 1.2 | 1.5 | V |
| V_IL_XI | The XI input low level voltage | - 0.3 | 0 | 0.15 | V |
| Cin | Load capacitance | | 1 | 2 | pF |
| Jitter_rms | Period broadband rms jitter | | | 15 | ps |
| Jitter_pk-pk | Period broadband PK-PK jitter | | | 200 | ps |

*Table 3-11.* **CLK_25M Output Characteristics**

| Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Frequency | -50ppm | 20, 50, 62.5, 125 | +50ppm | MHz |
| Output high voltage | 2.3 | 2.62 | 2.8 | V |
| Output low voltage | GND-0.3 | 0 | 0.4 | V |
| JitterRMS | | | 15 | ps |
| JitterPK-PK | | | 125 | ps |