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ARG82801

Fully Integrated PMIC for Safety-Related Systems with Buck or Buck-Boost Pre-Regulator, 4× Linear Regulators, 4× Gate Drivers, and SPI

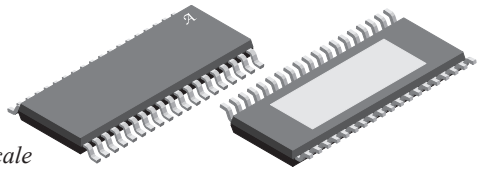
FEATURES AND BENEFITS

- A²-SIL™ product—device features for safety-critical systems
- Automotive AEC-Q100 qualified
- Wide input voltage range, 3.8 to 36 V_{IN} operating range, 40 V_{IN} maximum
- 2.2 MHz buck or buck/boost pre-regulator (VREG: 5.35 V)
- Four internal linear regulators with foldback short-circuit protection
  - □ VUC: selectable output (3.3 V / 5.0 V) regulator for microcontroller
  - □ V5C: 5 V general purpose LDO regulator
  - □ V5P1 and V5P2: two LDO regulators (track VUC voltage) with short-to-battery protection for remote sensors
- Q&A Watchdog and Window Watchdog timer
- Floating gate drivers with charge pump for external isolator NFET control
- Control and diagnostic reporting through a serial peripheral interface (SPI)
- Logic enable input (ENB) for microprocessor control
- Ignition enable input (ENBAT)
- Frequency dithering and controlled slew rate help reduce EMI/EMC
- Undervoltage protection for all output rails
- Thermal shutdown protection
- –40°C to 150°C junction temperature range

APPLICATIONS

- Provides system power for (microcontroller/DSP, CAN, sensors, etc.) and high current isolation FET gate driver in automotive control modules, such as:
  - □ Electronic power steering (EPS)
  - □ Advanced braking systems (ABS)
  - □ Other automotive applications

PACKAGE: 38-Pin eTSSOP (suffix LV)



Not to scale

DESCRIPTION

The ARG82801 is a power management IC that integrates a buck or buck/boost pre-regulator, four LDOs, and four floating gate drivers. The pre-regulator uses a buck or buck/boost topology to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage complete with control, diagnostics, and protections.

The output of the pre-regulator supplies a 3.3 V or 5.0 V selectable 350 mA linear regulator, a 5 V / 115 mA linear regulator, and two 120 mA protected linear regulators which track VUC output. Designed to supply power for microprocessors, sensors, and CAN transceivers, the ARG82801 is ideal for underhood applications.

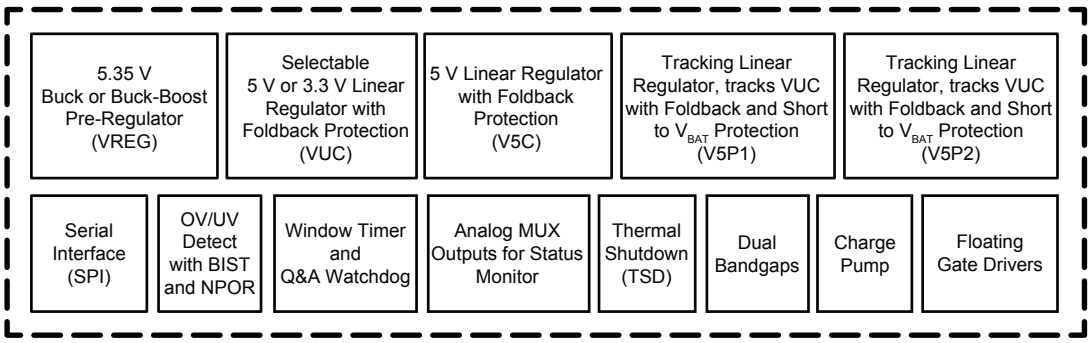
The independent floating gate drivers have the capability of controlling N-channel MOSFETs through SPI. These MOSFETs can be configured as phase or battery isolation devices in high current motor applications. An integrated charge pump allows the driver outputs to maintain the power MOSFETs in the on state over the full supply range with high phase-voltage slew rates.

Enable inputs to the ARG82801 include a logic level (ENB) and a high voltage (ENBAT). The ARG82801 also provides flexibility with disable function of the individual output rails through a serial peripheral interface (SPI).

Diagnostic outputs from the ARG82801 include a power-on-reset output (NPOR) and a fault flag output (FFn) to alert the microprocessor that a fault has occurred. The microprocessor can read fault status through SPI. Dual bandgaps, one for regulation and one for fault checking, improve safety coverage and fault detection of the ARG82801.

The ARG82801 contains two types of watchdog functions: Q&A and Window Watchdog timer. The watchdog timer is activated once it receives a valid SPI command from a processor. The watchdog can be put into flash mode or be reset via secure SPI commands.

The ARG82801 is supplied in a low-profile (1.2 mm maximum height) 38-lead eTSSOP package (suffix "LV") with exposed power pad.



ARG82801 Simplified Block Diagram

SELECTION GUIDE

Part Number	Package	Packing [1]	Lead Frame
ARG82801KLVATR	38-pin eTSSOP with thermal pad	4000 pieces per 7-inch reel	100% matte tin

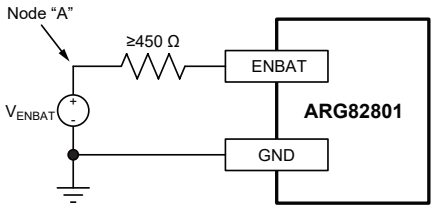
[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
VIN	V_{VIN}		−0.3 to 40	V
ENBAT	V_{ENBAT}	With current limiting resistor [3]	−13 to 40	V
			−0.3 to 8	V
	I_{ENBAT}		±75	mA
LX	V_{LX}		-0.3 to $V_{VIN} + 0.3$	V
		t < 250 ns	−1.5	V
		t < 50 ns	$V_{VIN} + 3$	V
GU, GV, GW, GVBB	V_{GU}, V_{GV}, V_{GW}, V_{GVBB}		$V_{SX} - 0.3$ to $V_{SX} + 12$	V
SU, SV, SW, SVBB	V_{SU}, V_{SV}, V_{SW}, V_{SVBB}		-6 to $V_{VIN} + 5$	V
		Transient	-18 to $V_{VIN} + 5$	V
VCP1	V_{VCP1}		$V_{VIN} - 0.3$ to $V_{VIN} + 8$	V
VCP2	V_{VCP2}		$V_{VIN} - 0.3$ to $V_{VIN} + 12$	V
CP1C1	V_{CP1C1}	$V_{VIN} \geq 12V$	$V_{VIN} - 12$ to $V_{VIN} + 0.3$	V
		$V_{VIN} < 12V$	-0.3 to $V_{VIN} + 0.3$	V
CP2C1	V_{CP2C1}		$V_{VIN} - 0.3$ to $V_{VCP1} + 0.3$	V
CP1C2	V_{CP1C2}		$V_{VIN} - 0.3$ to $V_{VCP1} + 0.3$	V
CP2C2	V_{CP2C2}		$V_{CP1C2} - 0.3$ to $V_{VCP2} + 0.3$	V
V5P1, V5P2	V_{V5P1}, V_{V5P2}	Independent of V_{VIN}	−1.0 to 40	V
All other pins			−0.3 to 7	V
Junction Temperature	T_J		−40 to 150	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[3] The higher ENBAT ratings (–13 V and 40 V) are measured at node “A” in the following circuit configuration:



THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [4]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	eTSSOP-38 (LV) package	30	°C/W

[4] Additional thermal information available on the Allegro website.

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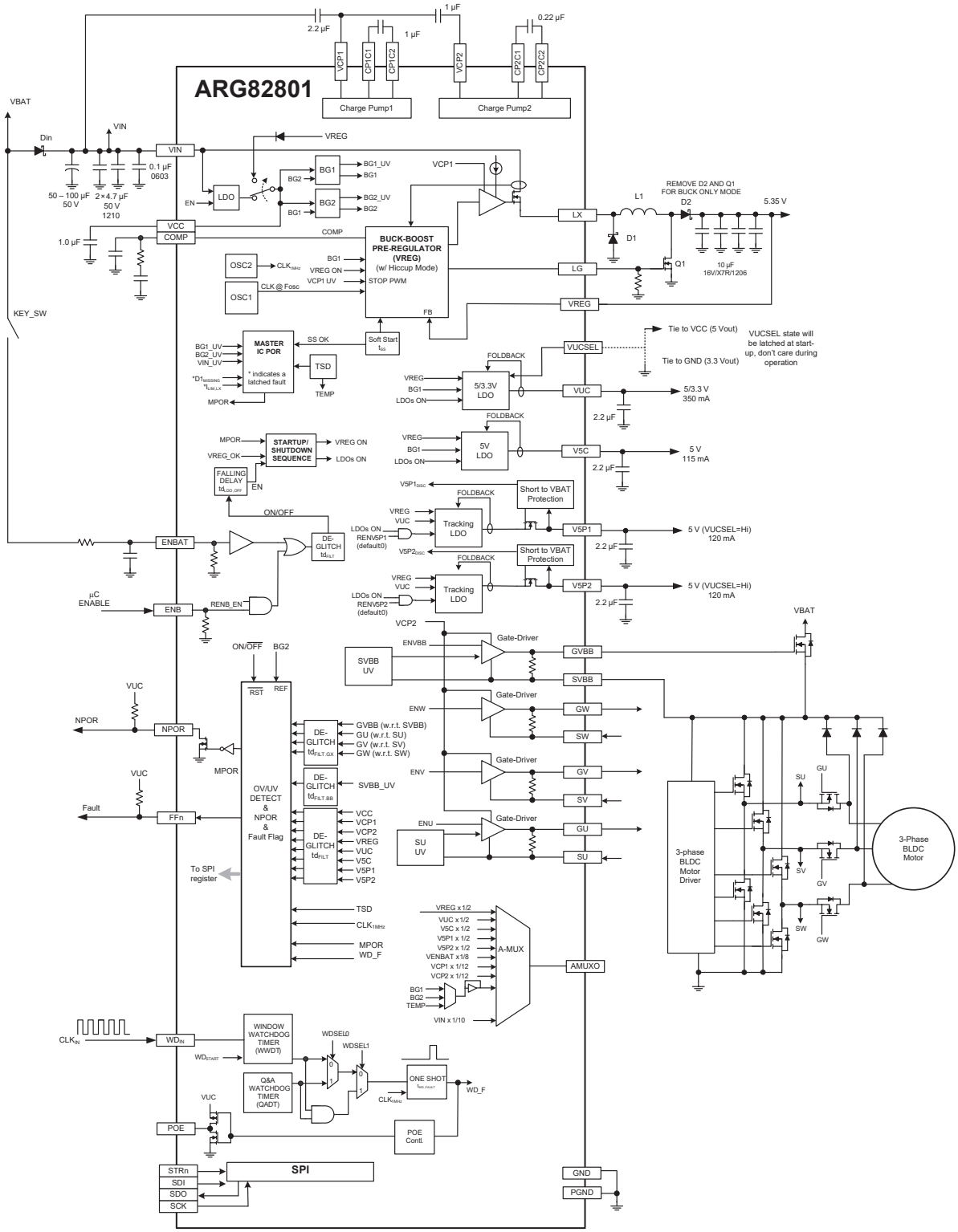
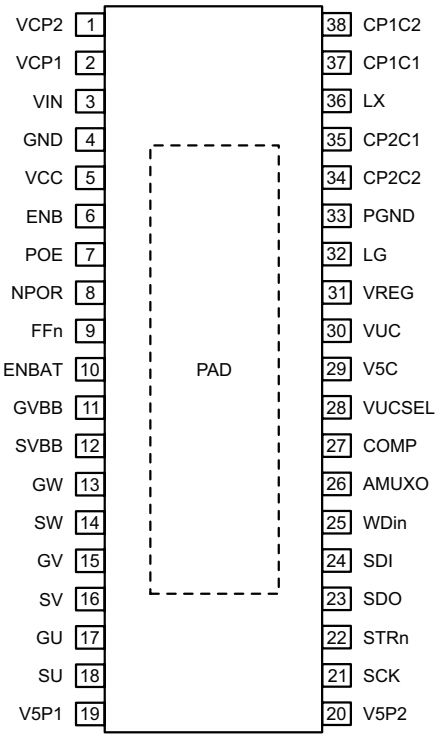
FUNCTIONAL BLOCK DIAGRAM





Package LV, 38-Pin eTSSOP Pinout Diagram

Terminal List Table

Number	Name	Function
1	VCP2	Charge pump 2 reservoir capacitor connection
2	VCP1	Charge pump 1 reservoir capacitor connection
3	VIN	Input voltage pin
4	GND	Ground
5	VCC	Internal voltage regulator bypass capacitor pin
6	ENB	Logic enable input from a microcontroller or DSP
7	POE	Gate drive enable signal, goes low if a watchdog fault is detected
8	NPOR	Active low, open-drain regulator fault detection output
9	FFn	Fault Flag to microcontroller
10	ENBAT	Ignition enable input from the key/switch via a series resistor
11	GVBB	Battery line MOSFET gate drive
12	SVBB	Battery line MOSFET source reference
13	GW	W phase MOSFET gate drive
14	SW	W phase MOSFET source reference
15	GV	V phase MOSFET gate drive
16	SV	V phase MOSFET source reference
17	GU	U phase MOSFET gate drive
18	SU	U phase MOSFET source reference
19	V5P1	5 V protected regulator output which tracks VUC
20	V5P2	5 V protected regulator output which tracks VUC
21	SCK	SPI clock input from the microcontroller
22	STRn	SPI chip select input from the microcontroller
23	SDO	SPI data output to the microcontroller
24	SDI	SPI data input from the microcontroller
25	WDin	Watchdog refresh input from a microcontroller or DSP
26	AMUXO	Analog Multiplexer output
27	COMP	Error amplifier compensation network pin for the buck/boost pre-regulator
28	VUCSEL	VUC output voltage selection pin: 1 (High: should be tied to VCC), V_{VUC} = 5 V 0 (Low: tied to GND), V_{VUC} = 3.3 V
29	V5C	5 V regulator output
30	VUC	Selectable V_{OUT} (5 V or 3.3 V by VUCSEL) regulator output
31	VREG	Voltage feedback input of the pre-regulator and supply input of the linear regulators
32	LG	Boost gate drive output for the buck/boost pre-regulator
33	PGND	Power ground
34	CP2C2	Charge pump 2 capacitor connection
35	CP2C1	Charge pump 2 capacitor connection
36	LX	Switching node for the buck/boost pre-regulator
37	CP1C1	Charge pump 1 capacitor connection
38	CP1C2	Charge pump 1 capacitor connection
–	PAD	Exposed thermal pad

ELECTRICAL CHARACTERISTICS [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Operating Input Voltage [2]	V_{VIN}	After V_{VIN} > $V_{VIN(START)}$ and VREG in regulating, Buck-Boost Mode	3.8	13.5	36	V
		After V_{VIN} > $V_{VIN(START)}$ and VREG in regulating, Buck Mode	5.5	13.5	36	V
VIN UVLO Start Voltage	$V_{VIN(START)}$	V_{VIN} rising	4.55	4.8	5.05	V
VIN UVLO Stop Voltage	$V_{VIN(STOP)}$	V_{VIN} falling	3.25	3.5	3.75	V
VIN UVLO Hysteresis	$V_{VIN(HYS)}$	$V_{VIN(START)}$ – $V_{VIN(STOP)}$	–	1.3	–	V
VIN Supply Quiescent Current [1]	I_Q	V_{VIN} = 13.5 V, V_{VREG} = 5.6 V (no PWM)	–	13	–	mA
	$I_{Q(SLEEP)}$	V_{VIN} = 13.5 V, V_{ENBAT} = Low and V_{ENB} = Low, T_J = 25°C	–	–	13	µA
PWM SWITCHING FREQUENCY AND DITHERING						
Switching Frequency	f_{OSC}	Dithering off	2.0	2.2	2.4	MHz
Frequency Dithering	Δf_{OSC}	As a percent of f_{OSC}	–	±10	–	%
VIN Dithering Start Threshold [2]	$V_{VIN(DITHER,ON)}$	V_{VIN} rising	8.5	9.0	9.5	V
		V_{VIN} falling	–	17	–	V
VIN Dithering Stop Threshold [2]	$V_{VIN(DITHER,OFF)}$	V_{VIN} falling	7.8	8.3	8.8	V
		V_{VIN} rising	–	18	–	V
CHARGE PUMP (VCP1 AND VCP2)						
VCP1 Output Voltage	V_{VCP1}	V_{VCP1} – V_{VIN}, V_{VIN} ≥ 9 V, I_{VCP1} > –5 mA, Buck Mode	4.1	6.6	–	V
		V_{VCP1} – V_{VIN}, 5.5 V < V_{VIN} ≤ 9 V, I_{VCP1} > –5 mA, Buck Mode	3.6	4.4	–	V
		V_{VCP1} – V_{VIN}, 3.8 V < V_{VIN} ≤ 5.5 V, V_{REG} = 5.35 V, I_{VCP1} > –5 mA, Buck-Boost Mode	3.0	3.8	–	V
VCP2 Output Voltage	V_{VCP2}	V_{VCP2} – V_{VIN}, V_{VIN} > 9 V, I_{VCP2} > –1 mA, Buck Mode	9	10	–	V
		V_{VCP2} – V_{VIN}, 5.5 V < V_{VIN} ≤ 9 V, I_{VCP2} > –1 mA, Buck Mode	8	10	–	V
		V_{VCP2} – V_{VIN}, 3.8 V < V_{VIN} ≤ 5.5 V, V_{VREG} = 5.35 V, I_{VCP2} > –1 mA, Buck-Boost Mode	6.6	9.5	–	V
Switching Frequency	$f_{SW(CP)}$		–	65	–	kHz
VCC PIN VOLTAGE						
Output Voltage	V_{VCC}	V_{VREG} = 5.35 V	–	4.4	–	V
THERMAL PROTECTION						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	165	–	–	°C
Thermal Shutdown Hysteresis [2]	T_{HYS}		–	15	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{VCP(UV,H)}$ and V_{VREG} in regulating are satisfied before V_{VIN} is reduced.

ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE SPECIFICATIONS						
Pre-Regulator Output Voltage [2]	V_{VREG}	V_{VIN} = 13.5 V, 0.1 A < I_{VREG} < 1.2 A	5.25	5.35	5.45	V
PULSE-WIDTH MODULATION (PWM)						
PWM Ramp Offset	$V_{PWM(OFFS)}$	V_{COMP} for 0% duty cycle	–	480	–	mV
LX Rising Slew Rate [2]	SR_{LXRISE}	V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A	–	1.4	–	V/ns
LX Falling Slew Rate [2]	SR_{LXFALL}	V_{VIN} = 13.5 V, 90% to 10%, I_{VREG} = 1 A	–	1.5	–	V/ns
Buck Minimum On-Time	$t_{ON(BUCK,MIN)}$		–	85	160	ns
Buck Maximum Duty Cycle	$D_{BUCK(MAX)}$	V_{VIN} < 7.8 V	–	–	100	%
Boost Maximum Duty Cycle	$D_{BST(MAX)}$	After V_{VIN} > $V_{VIN(START)}$, and VREG in regulating, V_{VIN} = 3.8 V	–	65	–	%
COMP to LX Current Gain	gm_{POWER}		–	4.57	–	A/V
Slope Compensation [2]	S_E		1.1	1.62	2.15	A/µs
INTERNAL MOSFET						
MOSFET On Resistance	$R_{DS(on)}$	V_{VIN} = 13.5 V, T_J = –40°C [2], I_{DS} = 0.1 A	–	60	90	mΩ
		V_{VIN} = 13.5 V, T_J = 25°C [3], I_{DS} = 0.1 A	–	95	115	mΩ
		V_{VIN} = 13.5 V, T_J = 150°C, I_{DS} = 0.1 A	–	160	190	mΩ
MOSFET Leakage Current	$I_{FET(LKG)}$	V_{ENBAT} ≤ 2.2 V, V_{ENB} = Low, V_{LX} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 85°C [3]	–	–	10	µA
		V_{ENBAT} ≤ 2.2 V, V_{ENB} ≤ Low, V_{LX} = 0 V, V_{VIN} = 16 V, −40°C < T_J < 150°C	–	50	150	µA
ERROR AMPLIFIER						
Open Loop Voltage Gain	A_{VOL}		–	60	–	dB
Transconductance	gm_{EA}	V_{SS} (internal signal) = 750 mV	520	720	920	µA/V
		V_{SS} (internal signal) = 500 mV	260	360	460	µA/V
Output Current	$I_{O(EA)}$		–	±75	–	µA
Maximum Output Voltage	$V_{O(EA,MAX)}$	V_{VIN} < 8.5 V	1.2	1.52	2.1	V
		V_{VIN} > 9.5 V	0.9	1.22	1.7	V
Minimum Output Voltage	$V_{O(EA,MIN)}$		–	–	300	mV
COMP Pull-Down Resistance	R_{COMP}	HICCUP = 1 or FAULT = 1 or V_{ENBAT} = Low and V_{ENB} = Low	–	1	–	kΩ

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
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[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{VCP(UV,H)}$ and V_{VREG} in regulating are satisfied before V_{VIN} is reduced.

ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
BOOST MOSFET (LG) GATE DRIVER						
LG High Output Voltage	$V_{LG(ON)}$	V_{VIN} = 6 V, V_{VREG} = 5.35 V	4.6	–	5.35	V
LG Low Output Voltage	$V_{LG(OFF)}$	V_{VIN} = 13.5 V, V_{VREG} = 5.35 V	–	0.2	0.4	V
LG Source Current [1]	$I_{LG(ON)}$	V_{VIN} = 6 V, V_{VREG} = 5.35 V, V_{LG} = 1 V	–	−300	–	mA
LG Sink Current [1]	$I_{LG(OFF)}$	V_{VIN} =13.5 V, V_{VREG} = 5.35 V, V_{LG} = 1 V	–	150	–	mA
SOFT-START						
SS Ramp Time [2]	t_{SS}		–	900	–	µs
SS PWM Frequency Foldback	$f_{SW(SS)}$	0 V ≤ V_{VREG} < 0.67 V typical	–	f_{OSC}/8	–	–
		0.67 V ≤ V_{VREG} < 1.34 V typical	–	f_{OSC}/4	–	–
		1.34 V ≤ V_{VREG} < 2.68 V typical	–	f_{OSC}/2	–	–
		V_{VREG} ≥ 2.68 V typical	–	f_{OSC}	–	–
HICCUP MODE						
Hiccup Enable Delay Time [2]	$t_{HIC(EN)}$		–	230	–	µs
Hiccup Recovery Time [2]	$t_{HIC(REC)}$		–	930	–	µs
Hiccup OCP PWM Counts	$t_{HIC(OCP)}$	V_{VREG} < 1.3 V_{TYP}, V_{COMP} = $V_{O(EA,MAX)}$	–	32	–	PWM cycles
		V_{VREG} > 1.3 V_{TYP}, V_{COMP} = $V_{O(EA,MAX)}$	–	120	–	PWM cycles
CURRENT PROTECTIONS						
Pulse-by-Pulse Current Limit	$I_{LIM(ton,min)}$	V_{VIN} < 8.5 V	3.83	4.2	4.77	A
		V_{VIN} > 9.5 V	2.49	2.8	3.11	A
LX Short-Circuit Current Limit	$I_{LIM(LX)}$	Latched fault after 2nd detection	5.3	7.1	–	A

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
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[3] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.
[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{VCP(UV,H)}$ and V_{VREG} in regulating are satisfied before V_{VIN} is reduced.

ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
MISSING ASYNCHRONOUS DIODE (D1) PROTECTION						
Detection Level	$V_{D(OPEN)}$		−1.9	−1.4	−1.0	V
Time Filtering [2]	$t_{D(OPEN)}$		50	–	250	ns
VUC, V5C, V5P1, V5P2 LINEAR REGULATORS						
VUC Accuracy and Load Regulation (5 V_{OUT})	V_{VUC5}	10 mA < I_{VUC} < 350 mA, V_{VREG} = 5.25 V, VUCSEL = 1	4.9	5.0	5.1	V
VUC Accuracy and Load Regulation (3.3 V_{OUT})	V_{VUC33}	10 mA < I_{VUC} < 350 mA, V_{VREG} = 5.25 V, VUCSEL = 0	3.23	3.30	3.37	V
VUC Output Capacitance Range [2]	$C_{OUT(VUC)}$		1.0	–	15	µF
V5C Accuracy and Load Regulation	V_{V5C}	5 mA < I_{V5C} < 115 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
V5C Output Capacitance Range [2]	$C_{OUT(V5C)}$		1.0	–	15	µF
V5P1 Accuracy and Load Regulation (5 V_{OUT})	V_{V5P1}	5 mA < I_{V5P1} < 120 mA, V_{VREG} = 5.25 V, VUCSEL = 1	4.9	5.0	5.1	V
V5P1 Output Capacitance Range [2]	$C_{OUT(V5P1)}$		1.0	–	15	µF
V5P2 Accuracy and Load Regulation (5 V_{OUT})	V_{V5P2}	5 mA < I_{V5P2} < 120 mA, V_{VREG} = 5.25 V, VUCSEL = 1	4.9	5.0	5.1	V
V5P2 Output Capacitance Range [2]	$C_{OUT(V5P2)}$		1.0	–	15	µF
V5Px/VUC Tracking Ratio	$TRACK_{V5Px/VUC}$	V_{VUC} = 3.3 V, V_{V5Px} / V_{3V3}, VUCSEL = 0	1.500	1.515	1.530	V/V
V5Px Tracking Accuracy, V_{VUC} = 3.3 V	$TRACK_{33}$	I_{V5Px} = I_{VUC} = 60 mA, VUCSEL = 0	–0.66	–	0.66	%
V5Px Tracking Accuracy, V_{VUC} = 5 V	$V_{TRACK(5V)}$	I_{V5Px} = I_{VUC} = 60 mA, VUCSEL = 1	–25	–	25	mV
VUC OVERCURRENT PROTECTION						
VUC Current Limit [1]	$I_{VUC(LIM)}$		–385	–570	–800	mA
VUC Foldback Current [1]	$I_{VUC(FBK)}$	V_{VUC} = 0 V	–60	–170	–250	mA
V5C OVERCURRENT PROTECTION						
V5C Current Limit [1]	$I_{V5C(LIM)}$		–120	–180	–250	mA
V5C Foldback Current [1]	$I_{V5C(FBK)}$	V_{V5C} = 0 V	–15	–60	–125	mA
V5P1 OVERCURRENT PROTECTION						
V5P1 Current Limit [1]	$I_{V5P1(LIM)}$		–135	–230	–350	mA
V5P1 Foldback Current [1]	$I_{V5P1(FBK)}$	V_{V5P1} = 0 V	–20	–60	–125	mA
V5P2 OVERCURRENT PROTECTION						
V5P2 Current Limit [1]	$I_{V5P2(LIM)}$		–135	–230	–350	mA
V5P2 Foldback Current [1]	$I_{V5P2(FBK)}$	V_{V5P2} = 0 V	–20	–60	–125	mA

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[4] The lowest operating voltage is only valid if the conditions V_{VIN} > $V_{VIN(START)}$ and V_{VCP} – V_{VIN} > $V_{VCP(UV,H)}$ and V_{VREG} in regulating are satisfied before V_{VIN} is reduced.

ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VUC, V5C, V5P1, AND V5P2 STARTUP TIMING						
VUC Startup Time (5 V_{OUT}) [2]	$t_{VUC5(START)}$	C_{VUC} ≤ 2.9 µF, Load = 33 Ω ±5% (152 mA), VUCSEL = 1	–	–	1.0	ms
VUC Startup Time (3.3 V_{OUT}) [2]	$t_{VUC33(START)}$	C_{VUC} ≤ 2.9 µF, Load = 33 Ω ±5% (100 mA), VUCSEL = 0	–	–	1.0	ms
V5C Startup Time [2]	$t_{V5C(START)}$	C_{V5C} ≤ 2.9 µF, Load = 100 Ω ±5% (50 mA)	–	–	1.0	ms
V5P1 Startup Time [2]	$t_{V5P1(START)}$	C_{V5P1} ≤ 2.9 µF, Load = 100 Ω ±5%	–	–	1.0	ms
V5P2 Startup Time [2]	$t_{VP2(START)}$	C_{V5P2} ≤ 2.9 µF, Load = 100 Ω ±5%	–	–	1.0	ms
IGNITION ENABLE (ENBAT) INPUT						
ENBAT Thresholds	$V_{ENBAT(H)}$	V_{ENBAT} rising	2.9	3.1	3.5	V
	$V_{ENBAT(L)}$	V_{ENBAT} falling	2.2	2.6	2.9	V
ENBAT Hysteresis	$V_{ENBAT(HYS)}$	$V_{ENBAT(H)} – V_{ENBAT(L)}$	–	500	–	mV
ENBAT Bias Current [1]	$I_{ENBAT(BIAS)}$	V_{ENBAT} = 0.8 V via a 1 kΩ series resistor	–	–	5	µA
		V_{ENBAT} = 5.5 V via a 1 kΩ series resistor	–	50	100	µA
		V_{ENBAT} = 20 V via a 1 kΩ series resistor	–	–	2	mA
ENBAT Pulldown Resistance	R_{ENBAT}	V_{ENBAT} < 1.2 V	–	600	–	kΩ
LOGIC ENABLE (ENB) INPUT						
ENB Thresholds	$V_{ENB(H)}$	V_{ENB} rising	–	–	2.0	V
	$V_{ENB(L)}$	V_{ENB} falling	0.8	–	–	V
ENB Bias Current [1]	$I_{ENB(IN)}$	V_{ENB} = 3.3 V	–	–	175	µA
ENB Resistance	R_{ENB}		–	60	–	kΩ
ENB/ENBAT FILTER/DEGLITCH						
Enable Filter/Deglitch Time	$t_{d(EN)}$		10	15	20	µs
VUC, V5C, V5P1, AND V5P2 UNDERVOLTAGE PROTECTION THRESHOLDS						
VUC (5 V_{OUT}), V5C, V5P1, and V5P2 Undervoltage Thresholds	$V_{V5(UV,H)}$	V_{V5} rising, VUCSEL = 1	–	4.68	–	V
	$V_{V5(UV,L)}$	V_{V5} falling, VUCSEL = 1	4.50	4.65	4.80	V
VUC (3.3 V_{OUT}) Undervoltage Thresholds	$V_{V33(UV,H)}$	V_{V33} rising, VUCSEL = 0	–	3.12	–	V
	$V_{V33(UV,L)}$	V_{V33} falling, VUCSEL = 0	2.8	3.1	3.19	V
VUC (5 V_{OUT}), V5C, V5P1, and V5P2 Undervoltage Hysteresis	$V_{V5(UV,HYS)}$	$V_{V5(UV,H)} – V_{V5(UV,L)}$	–	30	–	mV
VUC (3.3 V_{OUT}) Undervoltage Hysteresis	$V_{V33(UV,HYS)}$	$V_{V33(UV,H)} – V_{V33(UV,L)}$	–	20	–	mV

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VUC, V5C, V5P1, AND V5P2 OVERVOLTAGE PROTECTION THRESHOLDS						
VUC (5 V_{OUT}), V5C, V5P1, and V5P2 Overvoltage Thresholds	$V_{V5(OV,H)}$	V_{V5} rising, VUCSEL = 1	5.15	5.33	5.5	V
	$V_{V5(OV,L)}$	V_{V5} falling, VUCSEL = 1	–	5.30	–	V
VUC (3.3 V_{OUT}) Overvoltage Thresholds	$V_{V33(OV,H)}$	V_{V33} rising, VUCSEL = 0	3.41	3.51	3.62	V
	$V_{V33(OV,L)}$	V_{V33} falling, VUCSEL = 0	–	3.49	–	V
VUC (5 V_{OUT}), V5C, V5P1, and V5P2 Overvoltage Hysteresis	$V_{V5(OV,HYS)}$	$V_{V5(OV,H)} – V_{V5(OV,L)}$	–	30	–	mV
VUC (3.3 V_{OUT}) Overvoltage Hysteresis	$V_{V33(OV,HYS)}$	$V_{V33(OV,H)} – V_{V33(OV,L)}$	–	20	–	mV
V5Px Output Disconnect Threshold	$V_{V5PX(DISC)}$	V_{V5PX} rising	–	7.2	–	V
VREG, VCPX, AND BG THRESHOLDS						
VREG Non-Latching Overvoltage Threshold	$V_{VREG(OV,H)}$	V_{VREG} rising, LX PWM disabled	5.70	5.95	6.20	V
	$V_{VREG(OV,L)}$	V_{VREG} falling, LX PWM enabled	–	5.85	–	V
VREG Non-Latching Overvoltage Hysteresis	$V_{VREG(OV,HYS)}$	$V_{VREG(OV,H)} – V_{VREG(OV,L)}$	–	100	–	mV
VREG Undervoltage Thresholds	$V_{VREG(UV,H)}$	V_{VREG} rising, triggers rise of VUC linear regulator	4.14	4.38	4.62	V
	$V_{VREG(UV,L)}$	V_{VREG} falling	–	4.28	–	V
VREG Undervoltage Hysteresis	$V_{VREG(UV,HYS)}$	$V_{VREG(UV,H)} – V_{VREG(UV,L)}$	–	100	–	mV
VCP1 Overvoltage Thresholds [2]	$V_{VCP1(OV,H)}$	V_{VCP1} rising (w.r.t. V_{VIN})	11.0	12.5	14.0	V
VCP1 Undervoltage Thresholds	$V_{VCP1(UV,H)}$	V_{VCP1} rising, PWM enabled (w.r.t. V_{VIN})	2.9	3.1	3.35	V
	$V_{VCP1(UV,L)}$	V_{VCP1} falling, PWM disabled (w.r.t. V_{VIN})	–	2.8	–	V
VCP1 Undervoltage Hysteresis	$V_{VCP1(UV,HYS)}$	$V_{VCP1(UV,H)} – V_{VCP1(UV,L)}$	–	400	–	mV
VCP2 Undervoltage Thresholds	$V_{VCP2(UV,H)}$	V_{VCP2} rising, PWM enabled (w.r.t. V_{VIN})	5.95	6.3	6.65	V
	$V_{VCP2(UV,L)}$	V_{VCP2} falling, PWM disabled (w.r.t. V_{VIN})	–	5.1	–	V
VCP2 Undervoltage Hysteresis	$V_{VCP2(UV,HYS)}$	$V_{VCP2(UV,H)} – V_{VCP2(UV,L)}$	–	1.2	–	V
BG1 and BG2 Undervoltage Thresholds [2]	$V_{BGx(UV)}$	V_{BG1} or V_{BG2} falling	1.00	1.05	1.10	V
OVERVOLTAGE FILTERING/DEGLITCH TIME						
Overvoltage Detection Delay [2]	$t_{d(OV)}$	Overvoltage detection delay time	5	–	25	µs
UNDERVOLTAGE FILTERING/DEGLITCH TIME						
Undervoltage Filter/Deglitch Times [2]	$t_{d(UV)}$	Undervoltage detection delay time	5	–	25	µs

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NPOR TURN-ON AND TURN-OFF DELAYS						
NPOR Turn-on Delay	$t_{d(NPOR,ON)}$	Time from when VUC and V5C are all in regulation to NPOR being asserted high	15	20	25	ms
NPOR OUTPUT VOLTAGES						
NPOR Output Low Voltage	$V_{NPOR(L)}$	V_{VIN} ≥ 2.5 V, I_{NPOR} = 2 mA	–	150	400	mV
NPOR Leakage Current [1]	$I_{NPOR(LKG)}$	V_{NPOR} = 3.3 V	–	–	2	µA
NPOR ONE-SHOT TIME						
NPOR One-Shot “Low” Time After Watchdog Fault	$t_{WD(FAULT)}$		1.6	2	2.4	ms
FAULT FLAG OUTPUT VOLTAGES (FFn)						
FFn Output Voltage	$V_{FF(L)}$	FFn is tripped, V_{VIN} ≥ 2.5 V, I_{FF} = 2 mA	–	150	400	mV
FFn Leakage Current	$I_{FF(LKG)}$	V_{FF} = 3.3 V	–	–	2	µA
WD_{IN} VOLTAGE THRESHOLDS AND CURRENT						
WD_{IN} Input Voltage Thresholds	$V_{WDIN(LO)}$	V_{WDIN} falling	0.8	–	–	V
	$V_{WDIN(HI)}$	V_{WDIN} rising	–	–	2.0	V
WD_{IN} Pull-Down Resistance [2]	R_{WDIN}		–	50	–	kΩ
WD_{IN} TIMING SPECIFICATIONS						
WD_{IN} Duty Cycle [2]	D_{WDIN}		–	50	–	%
Watchdog Activation Delay	$t_{d(WD)}$		–	30	–	ms
GATE DRIVE ENABLE (POE)						
POE Output Voltage	$V_{POE(L)}$	I_{POE} = 4 mA	–	150	400	mV
	$V_{POE(H)}$	I_{POE} = –1.5 mA	0.8 × V_{VUC}	–	–	V
VUCSEL LOGIC INPUT						
VUCSEL Thresholds	$V_{VUCSEL(H)}$	V_{VUCSEL} rising	–	–	2.0	V
	$V_{VUCSEL(L)}$	V_{VUCSEL} falling	0.8	–	–	V

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SERIAL INTERFACE (STRn, SDI, SDO, SCK)						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}	All logic inputs	2.0	–	–	V
Input Hysteresis	V_{Ihys}	All logic inputs	250	550	–	mV
Input Pull-Down SDI, SCK	R_{PDS}	0 V < V_{VIN} < 5 V	–	50	–	kΩ
Input Pull-Up To VCC	I_{PU}	STRn	–	50	–	kΩ
Output Low Voltage	V_{OL}	I_{OL} = 1 mA [1]	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OL} = –1 mA [1]	0.8 × V_{VUC}	–	–	V
Clock High Time	t_{SCKH}	A in Figure 1	50	–	–	ns
Clock Low Time	t_{SCKL}	B in Figure 1	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in Figure 1	30	–	–	ns
Strobe Lag Time	t_{STLG}	D in Figure 1	30	–	–	ns
Strobe High Time	t_{STRH}	E in Figure 1	300	–	–	ns
Data Out Enable Time	t_{SDOE}	F in Figure 1	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G in Figure 1	–	–	30	ns
Data Out Valid Time From Clock Falling	t_{SDOV}	H in Figure 1	–	–	40	ns
Data Out Hold Time From Clock Falling	t_{SDOH}	J in Figure 1	5	–	–	ns
Data In Setup Time To Clock Rising	t_{SDIS}	K in Figure 1	15	–	–	ns
Data In Hold Time From Clock Rising	t_{SDIH}	L in Figure 1	10	–	–	ns
Wake Up From Sleep	t_{EN}		–	–	2	ms

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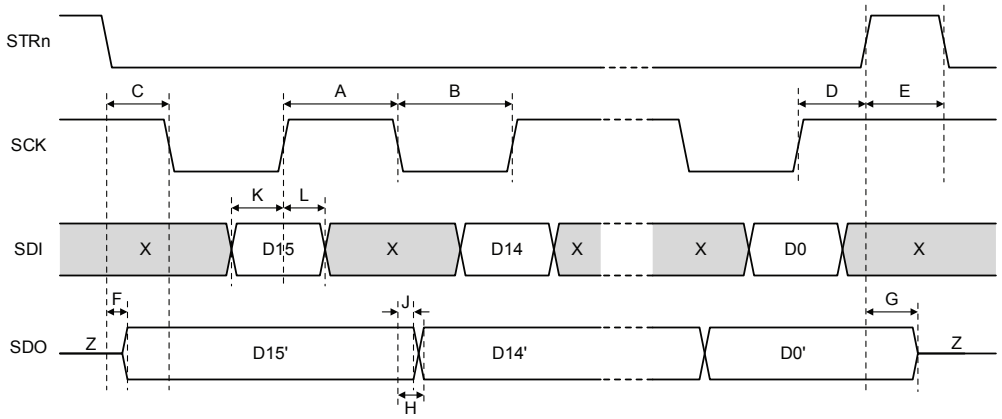

Figure 1: Serial Interface Timing
X = do not exceed Watchdog Config timeout; Z = high-impedance (tri-state)

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Gate Output Drive						
Turn-On Time	t_r	C_{LOAD} = 10 nF, 20% to 80%	–	5	–	µs
Turn-Off Time	t_f	C_{LOAD} = 10 nF, 80% to 20%	–	0.5	–	µs
Turn-On Pulse Current	I_{GXP}		8.5	10	12	mA
Turn-On Pulse Time	t_{GXP}		22	–	42	µs
On Hold Current	I_{GXH}		–	400	–	µA
Pull-Down On Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{Gx} = 10 mA	–	5	–	Ω
		T_J = 150°C, I_{Gx} = 10 mA	–	10	–	Ω
Gx Output High Voltage	V_{GH}	V_{VIN} > 5.5 V (w.r.t. Sx, or VIN if V_{Sx} > V_{VIN})	8	9	12	V
		5.0 V < V_{VIN} ≤ 5.5 V (w.r.t. Sx, or VIN if V_{Sx} > V_{VIN}), Buck-boost mode	7.2	9	–	V
		V_{VIN} = 4.5 V, V_{SX} = 5.5 V (w.r.t. Sx), Buck-boost mode	6.2	6.9	–	V
Gate Drive Static Load Resistance [2]	R_{GS}	Between Gx and Sx (using ±1% tolerance resistor)	100	–	–	kΩ
Gx Output Voltage Low	V_{GL}	–10 µA < I_{Gx} < 10 µA	–	–	V_{Sx} + 0.3	V
Gx Passive Pull-Down	R_{GPD}	V_{Gx} – V_{Sx} < 0.3 V	–	950	–	kΩ
SVBB Undervoltage Threshold Falling	$V_{SVBB(UV,L)}$	V_{SVBB} falling (w.r.t. GND)	–	–	3	V
SVBB Undervoltage Filter/Deglitch Times	$t_{d(UV,FILT,BB)}$	Undervoltage detection delay time, slow; GD_UV_FLT = 0	–	0.8	1.0	ms
		Undervoltage detection delay time, fast; GD_UV_FLT = 1	3.7	–	18	µs
SU Undervoltage Threshold Falling	$V_{SUUV(L)}$	V_{SU} falling (w.r.t. GND); GD_U_SEL = 1	–	–	3	V
SU Undervoltage Filter/Deglitch Times	$t_{d(UV,FILT,SU)}$	Undervoltage detection delay time, slow; GD_UV_FLT = 0, GD_U_SEL = 1	–	0.8	1.0	ms
		Undervoltage detection delay time, fast; GD_UV_FLT = 1	3.7	–	18	µs
GSx Undervoltage Threshold Rising [2]	$V_{GSx(UV,H)}$	V_{Gx} rising (w.r.t. Sx, x = VBB, U, V, W)	6.0	–	7.0	V
GSx Undervoltage Threshold Hysteresis [2]	$V_{GSx(UV,HYS)}$	x = VBB, U, V, W	–	250	–	mV
GSx Undervoltage Filter/Deglitch Time	$t_{d(UV,FILT,GSx)}$	Undervoltage detection delay time, x = VBB, U, V, W	–	1.4	–	ms

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.8 V [4] ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENB} = High or V_{ENBAT} = High, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE (continued)						
ENVBB Enable/Disable Delay Time	$t_{d(EN,BB)}$	From “SPI command is written” to GVBB 20% (enable), to GVBB 80% (disable); GD_EN_DLY = 0	–	1.5	–	ms
ENU Enable/Disable Delay Time	$t_{d(EN,U)}$	From “SPI command is written” to GU 20% (enable), to GU 80% (disable); GD_U_SEL = 1; GD_EN_DLY = 0	–	1.5	–	ms
		From “SPI command is written” to GU 20% (enable), to GU 80% (disable); GD_U_SEL = 0; GD_EN_DLY = 0	–	10	–	ms
ENV and ENW Enable/Disable Delay Time	$t_{d(EN,X)}$	From “SPI command is written” to Gx 20% (enable), to Gx 80% (disable); GD_EN_DLY = 0	–	10	–	ms
ENVBB, ENU, ENV, and ENW Enable Delay Time, Fast	$t_{d(EN,X)}$	From “SPI command is written” to Gx 20%; GD_EN_DLY = 1	–	–	3	µs
ENVBB, ENU, ENV, and ENW Disable Delay Time, Fast	$t_{d(EN,X)}$	From “SPI command is written” to Gx 80%; GD_EN_DLY = 1	–	–	2.25	µs

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Table 1: Startup and Shutdown Logic (signal names consistent with Block Diagram)

ARG82801 MODE	Regulator/Isolator Control Bits (0 = OFF, 1 = ON, R = Ready)					ARG82801 Status Signals						
	VREG ON	VUC ON	V5C ON	V5P1 and V5P2 ON	Isolator Drivers	EN	MPOR	VREG UV	VUC UV	V5C UV	V5P1 and V5P2 UV	NPOR
RESET	0	0	0	0	0	0	1	0	0	0	0	0
OFF	0	0	0	0	0	0	0	1	1	1	1	0
STARTUP	1	0	0	0	0	1	0	1	1	1	1	0
↓	1	1	0	0	R	1	0	0	1	1	1	0
↓	1	1	1	0	R	1	0	0	0	1	1	1
↓	1	1	1	R	R	1	0	0	0	0	1	1
RUN	1	1	1	R	R	1	0	0	0	0	0	1
15 µs DEGLITCH	1	1	1	R	R	0	0	0	0	0	0	0
SHUTTING DOWN	1	1	0	0	R	0	0	0	0	0	0	0
↓	1	0	0	0	0	0	0	0	0	1	1	0
↓	0	0	0	0	0	0	0	0	1	1	1	0
OFF	0	0	0	0	0	0	0	1	1	1	1	0

TIME

X = DON'T CARE
EN = ENBAT + ENB
MPOR = VCC_UV + VCPx_UV + BG1_UV + BG2_UV + TSD + $D1_{MISSING}$ (latched) + $I_{LIM(LX)}$ (latched)

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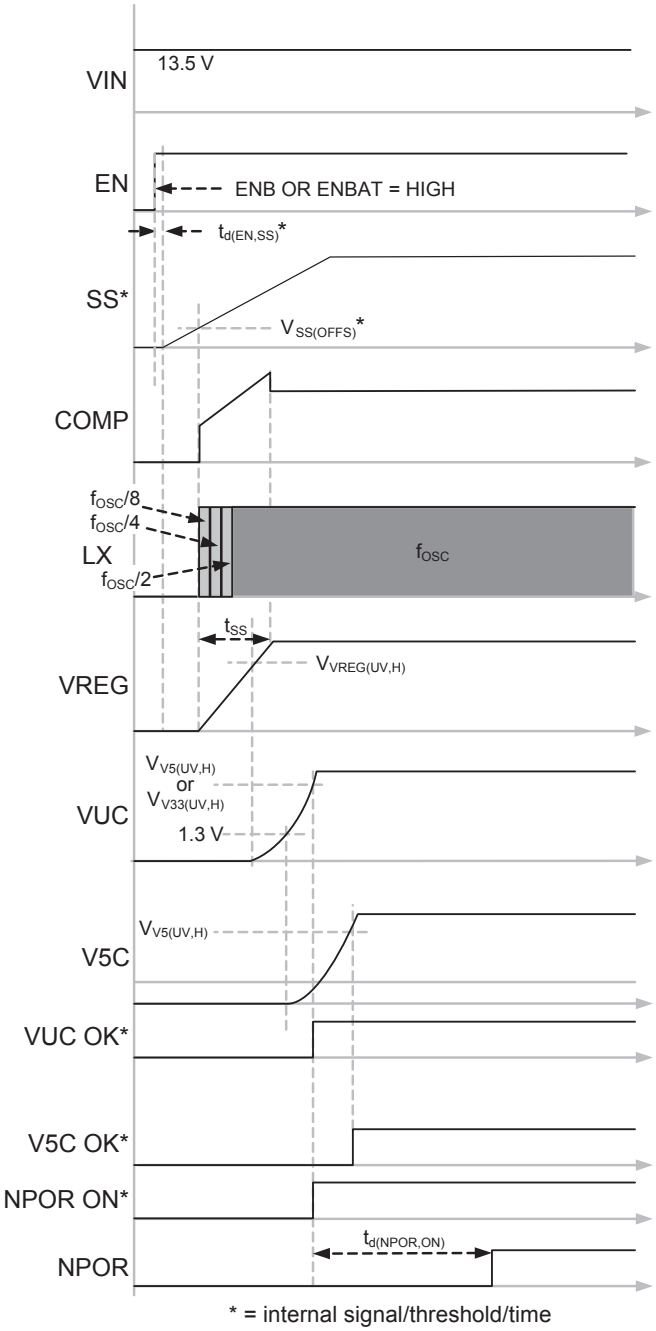
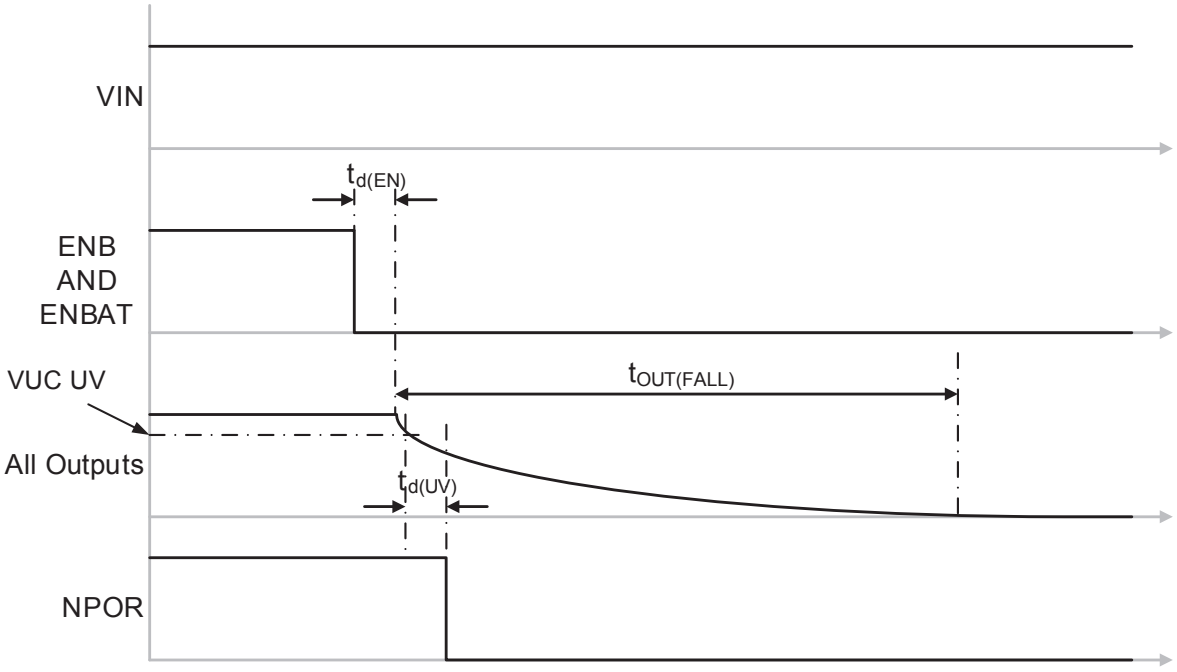


Figure 2: Startup Timing Diagram



All outputs start to decay $t_{d(EN)}$ seconds after ENB and ENBAT are low.
Time for outputs to drop to zero, $t_{OUT(FALL)}$, various for each output and depends on load current and capacitance.
NPOR falls when VUC reaches its UV point.

Figure 3: Shutdown Timing Diagram

TIMING DIAGRAMS (not to scale)

* = internal signal/threshold, + is for “or”

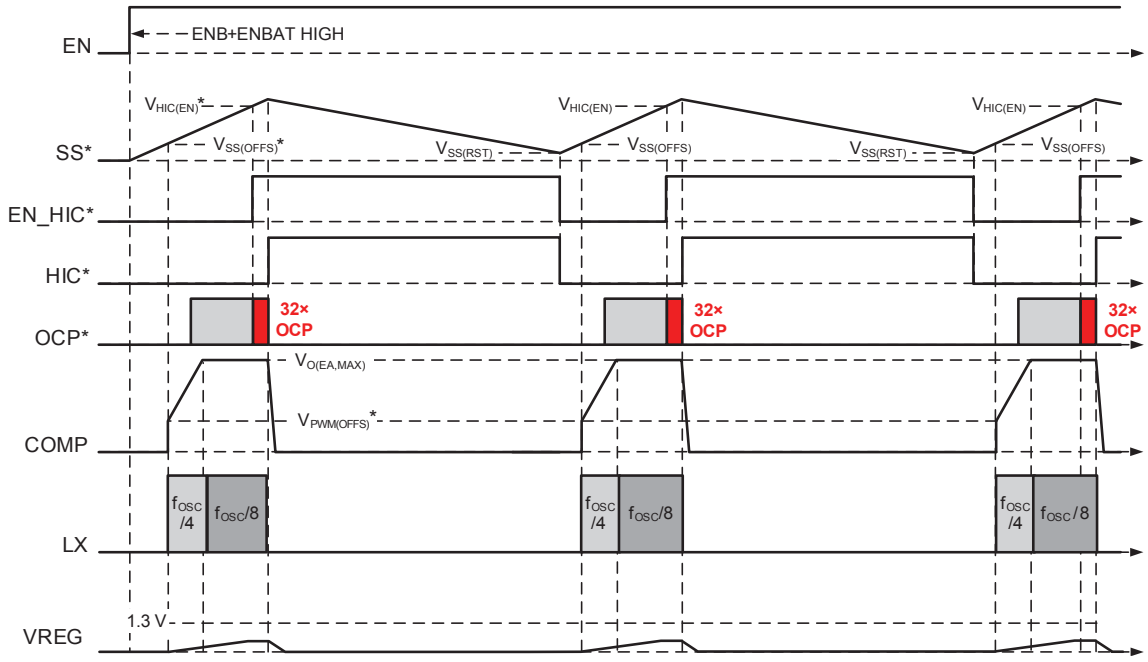


Figure 4: Hiccup Mode Operation with VREG Shorted to GND (R_{LOAD} < 50 mΩ)

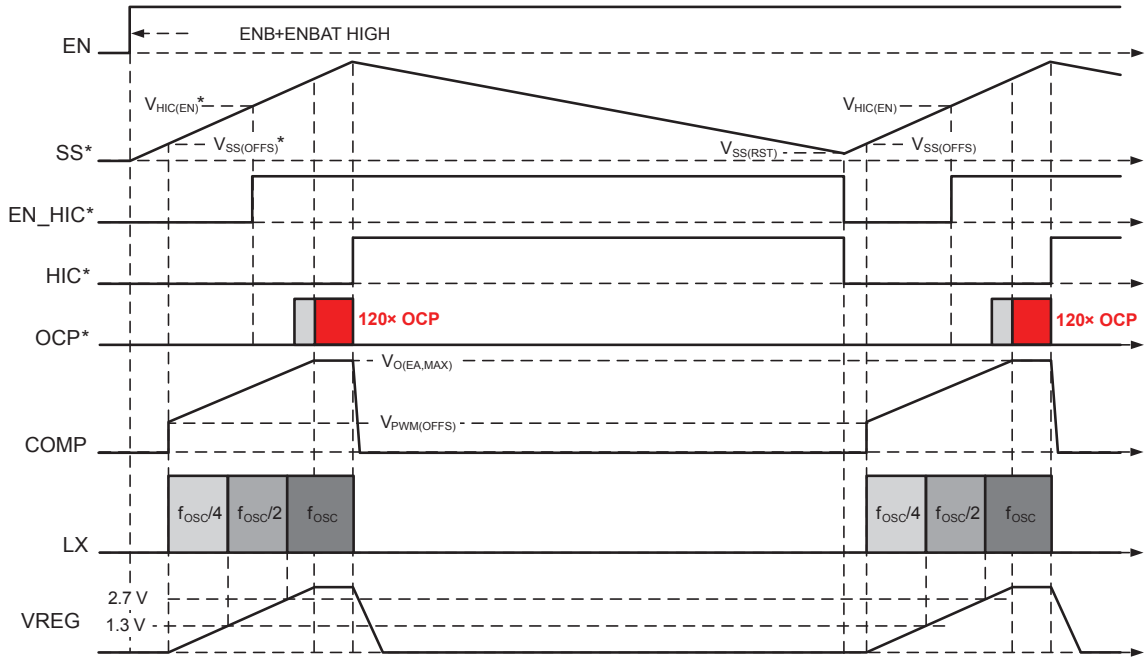


Figure 5: Hiccup Mode Operation with VREG Overloaded (R_{LOAD} ≈ 0.5 Ω)

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Table 2: Summary of Fault Mode Operation

FAULT TYPE and CONDITION	ARG82801 RESPONSE TO FAULT	LATCHED FAULT?	VCC	VCP1	VCP2	VREG	VUC	V5C	V5P1	V5P2	Isolator Drivers	NPOR	FFn	POE	SPI	WD	RESET METHOD
VREG asynchronous diode (D1) missing	Results in an MPOR after 1 detection, so all regulators are shut off	Yes	No effect	No effect	No effect	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Place D1 then cycle EN or VIN
Asynchronous diode (D1) short-circuited or LX shorted to ground	Results in an MPOR after the high-side MOSFET current exceeds $I_{LIM(LX)}$ so all regulators are shut off	Yes	No effect	No effect	No effect	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Remove the short then cycle EN or VIN
VCP1 OV	If OV condition persists for more than $t_{d(OV)}$, then set FFn Low	No	No effect	> $V_{VCP1(OV,H)}$	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	On	On	Check for short circuits on VCP1
VIN UVLO	ARG82801 is in reset state	No	Ramping	VIN	VIN	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Increase VIN
BG1 UVLO	ARG82801 is in reset state	No	Ramping	VIN	VIN	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Replace ARG82801
BG2 UVLO	ARG82801 is in reset state	No	Ramping	VIN	VIN	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Replace ARG82801
VCC UVLO	ARG82801 is in reset state	No	UVLO	VIN	VIN	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Remove the short circuit
VCC short limit	ARG82801 is in reset state	No	UVLO	VIN	VIN	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Remove the short circuit
VCP1 UVLO	ARG82801 is in reset state	No	ON	UVLO	No effect	Off	Off	Off	Off	Off	Off	Low	Low	Low	Off	Off	Remove the short circuit
VCP2 UVLO	Terminate isolator portion	No	ON	No effect	UVLO	No effect	No effect	No effect	No effect	No effect	Off	No effect	Low	Low	No effect	No effect	Remove the short circuit
VREG overvoltage $V_{VREG(OV,H)} < V_{VREG}$	Stop PWM switching of LX	No	No effect	No effect	No effect	> $V_{VREG(OV,H)}$	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on VREG
VREG pin open circuit	VREG will decay to 0 V, LX will switch at maximum duty cycle so the voltage on the output capacitors will be very close to VBAT	No	No effect	No effect	No effect	Decay to 0 V	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Low if VUC < $V_{VXX(UV,L)}$	Low	Off if V_{VREG} < UVLO	No effect	No effect	Connect the VREG pin
VREG shorted to ground V_{VREG} < 1.95 V, $V_{COMP} \neq V_{O(EA,MAX)}$	Continue to PWM but turn off LX when the high side MOSFET current exceeds $I_{LIM(LX)}$	No	No effect	No effect	No effect	Shorted	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Low if VUC < $V_{VXX(UV,L)}$	Low	Off if V_{VREG} < UVLO	No effect	No effect	Remove the short circuit
VREG overcurrent V_{VREG} < 1.95 V, $V_{COMP} = V_{O(EA,MAX)}$	Enters hiccup mode after 30 OCP faults	No	No effect	No effect	No effect	Over-current	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Low if VUC < $V_{VXX(UV,L)}$	Low	Off if V_{VREG} < UVLO	No effect	No effect	Decrease the load
VREG overcurrent V_{VREG} > 1.95 V, $V_{COMP} = V_{O(EA,MAX)}$	Enters hiccup mode after 120 OCP faults	No	No effect	No effect	No effect	Over-current	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Off if V_{VREG} < UVLO	Low if VUC < $V_{VXX(UV,L)}$	Low	Low if VUC < $V_{VXX(UV,L)}$	No effect	No effect	Decrease the load
VUC undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback or pulse-by-pulse current limit	No	No effect	No effect	No effect	No effect	V_{VUC} < $V_{VXX(UV,L)}$	No effect	No effect (Track to VUC)	No effect (Track to VUC)	Off	Low	Low	Low	No effect	No effect	Decrease the load
VUC overvoltage	If OV condition persists for more than $t_{d(OV)}$ then set NPOR Low	No	No effect	No effect	No effect	No effect	V_{VUC} > $V_{VXX(OV,H)}$	No effect	No effect (Track to VUC)	No effect (Track to VUC)	Off	Low	Low	Low	No effect	No effect	Check for short circuits
VUC overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	Falling	No effect	No effect (Track to VUC)	No effect (Track to VUC)	Low if VUC < $V_{VXX(UV,L)}$	Low if VUC < $V_{VXX(UV,L)}$	Low if VUC < $V_{VXX(UV,L)}$	Low if VUC < $V_{VXX(UV,L)}$	No effect	No effect	Decrease the load
V5P1 undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	No effect	No effect	V_{V5P1} < $V_{V5(UV,L)}$	No effect	No effect	No effect	Low	No effect	No effect	No effect	Decrease the load
V5P1 overvoltage or shorted to VBAT	If OV condition persists for more than td (OV) then set FFn Low	No	No effect	No effect	No effect	No effect	No effect	No effect	Off	No effect	No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on V5P1

Continued on next page...

Table 2: Summary of Fault Mode Operation (continued)

FAULT TYPE and CONDITION	ARG82801 RESPONSE TO FAULT	LATCHED FAULT?	VCC	VCP1	VCP2	VREG	VUC	V5C	V5P1	V5P2	Isolator Drivers	NPOR	FFn	POE	SPI	WD	RESET METHOD
V5P1 overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	No effect	No effect	Falling	No effect	No effect	No effect	Low	No effect	No effect	No effect	Decrease the load
V5P2 undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	$V_{V5P2} < V_{V5(UV,L)}$	No effect	No effect	Low	No effect	No effect	No effect	Decrease the load
V5P2 overvoltage or shorted to VBAT	If OV condition persists for more than $t_{d(OV)}$ then set FFn Low	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Off	No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on V5P2
V5P2 overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Falling	No effect	No effect	Low	No effect	No effect	No effect	Decrease the load
V5C overvoltage	If OV condition persists for more than $t_{d(OV)}$ then set FFn Low	No	No effect	No effect	No effect	No effect	No effect	$V_{V5C} > V_{V5(OV,H)}$	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on V5C
V5C undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	No effect	$V_{V5C} < V_{V5(UV,L)}$	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Decrease the load
V5C overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	No effect	Falling	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Decrease the load
Thermal shutdown	Results in an MPOR, so all regulators are shut off	No	No effect	No effect	No effect	Off	Off	Off	Off	Off	Off	Low	Low	Low	No effect	No effect	Let the ARG82801 cool
Window WD error	Put the system into a safe state	No	No effect	No effect	No effect	No effect	No effect	No effect	Off	Off	Off	Low (One shot)	Low	Low	No effect	–	Get proper signal from microcontroller
Q&A watchdog error	Put the system into a safe state	No	No effect	No effect	No effect	No effect	No effect	No effect	Off	Off	Off	Low (One shot)	Low	Low	No effect	–	Get proper signal from microcontroller
BIST error	Fault flag	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Off	No effect	Low	Low	No effect	No effect	Write 1 to reset
SVBB_UV	Corresponding (GVBB) Isolator off	Yes	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	GVBB: off GU, GV, GW: No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on SVBB, Toggle ENVBB
SU_UV (see 0x09 [D7])	Corresponding (GU) Isolator off	Yes	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	GU: off GVBB, GV, GW: No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on SU, Toggle ENU and Write 1 to reset
GSx_UV	Fault flag	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on Gx
LG operation failure	Fault flag	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Check for short circuits on LG
VDD_UV	Fault flag	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	May lose contents	May have effect	Restart the device
DBE Fault	Fault flag	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Restart the device
SE Fault	Fault flag	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Check SPI signal

FUNCTIONAL DESCRIPTION

Overview

The ARG82801 is a power management IC designed for safety-critical applications. It contains one switching and four linear regulators to create the voltages necessary for typical automotive applications such as electrical power steering.

The ARG82801 pre-regulator can be configured as a buck converter or buck boost. Buck boost is suitable for when applications must work with extremely low battery voltages. This pre-regulator generates a fixed 5.35 V to power the internal or external post-regulators. These post-regulators generate the various voltage levels for the end system.

Pre-Regulator

The pre-regulator incorporates an internal high-side buck switch and a boost switch gate driver. An external freewheeling diode and LC filter are required to complete the buck converter. By adding a MOSFET and boost diode, the pre-regulator can now maintain all outputs with input voltages down to 3.8 V.

The pre-regulator provides many protection and diagnostic functions:

1. Pulse-by-pulse and hiccup mode current limit
2. Undervoltage detection and reporting
3. Shorted switch node to ground
4. Open freewheeling diode protection
5. High voltage rating for load dump

Bias Supply

The bias supply (V_{CC}) is generated by an internal linear regulator. This supply is the first rail to start up. Most of the internal control circuitry is powered by this supply. The bias supply includes some unique features to ensure safe operation of the ARG82801. These features include:

1. Input voltage undervoltage lockout
2. Output undervoltage detection and reporting
3. Overcurrent and short-circuit limit
4. Dual input, VIN and VREG, for low battery voltage operation

Charge Pump

Charge pump circuits provide the voltage necessary to drive high-side N-channel MOSFETs in the pre-regulator, linear regulators, and floating gate drivers. Four external capacitors are required for charge pump operation. During the first cycle of the charge pump action, the flying capacitor between pins CP1C1 and CP1C2 is charged either from VIN or VREG, whichever is highest. During the second cycle, the voltage on the flying capacitor charges the VCP1 capacitor and the flying capacitor, between pins CP2C1 and CP2C2. During the next cycle, the voltage on the flying capacitor charges the VCP2 capacitor. The charge pump incorporates some safety features:

1. Undervoltage and overvoltage detection and reporting
2. Overcurrent safe mode protection

Bandgap

Dual bandgaps are implemented within the ARG82801. One bandgap is dedicated to the voltage regulation loops within each of the regulators, VCC, VCPx, VREG, and the four post-regulators. The second is dedicated to the monitoring function of all the regulators undervoltage and overvoltage. This improves safety coverage and fault reporting from the ARG82801.

Should the regulation bandgap fail, then the outputs will be out of specification and the monitoring bandgap will report the fault.

If the monitoring bandgap fails, the outputs will remain in regulation, but the monitoring circuits will report the outputs as out of specification and trip the fault flag.

The bandgap circuits include two other bandgaps that are used to monitor the undervoltage state of the main bandgaps.

Enable

Two Enable pins are available on the ARG82801. A high signal on either of these pins enables the regulated outputs of the ARG82801. One Enable (ENB) is logic-level compatible. The second enable (ENBAT), is battery-level rated and can be connected to the ignition switch.

Linear Regulators

The ARG82801 has four linear regulators: one 5 V regulator, one 5 V or 3.3 V selectable regulator, and two protected regulators which track VUC (5 V or 3.3 V).

All linear regulators provide the following protection features:

1. Current limit with foldback
2. Undervoltage and overvoltage detection and reporting

The protected regulators (V5P1 and V5P2) include protection against connection to the battery voltage. This makes these outputs suitable for powering remote sensors or circuitry where short to battery is possible.

The pre-regulator powers these linear regulators which reduces power dissipation and temperature.

	VUCSEL	$V_{OUT(TYP)}$	Startup	Tracking
VUC	1	5 V	When $V_{VREG} > V_{VREG(UV,H)}$	n/a
	0	3.3 V		
V5C	Don't Care	5 V	When $V_{VUC} > V_{V5} / V_{V33(UV,H)}$	n/a
V5Px	Don't Care	5 V	Enabled via SPI	VUC (DC level) During start-up it does not track VUC since default SPI bit is "disabled"

Fault Detection and Reporting

There is extensive fault detection within the ARG82801; most have been discussed previously. There are two fault reporting mechanisms used by the ARG82801: one through hardwired pins and the other through a serial communications interface (SPI).

Two hardwired pins on the ARG82801 are used for fault reporting. The first pin, NPOR, reports on the status of the VUC output. This signal goes low if this output is out of regulation. The second pin, FFn (active low fault flag), reports on all other faults. FFn goes low if a fault within the ARG82801 exists. The FFn pin can be used by the processor as an alert to check the status of the ARG82801 via SPI and see where the fault occurred.

Startup Self-Test

The ARG82801 includes self-test which is performed during the startup sequence. This self-test verifies the operation of the undervoltage and overvoltage detection circuits for the main outputs.

In the event the self-test fails, the ARG82801 will report the failure through SPI.

Undervoltage Detect Self-Test

The undervoltage (UV) detectors are verified during startup of the ARG82801. A voltage that is higher than the undervoltage threshold is applied to each UV comparator; this should cause the relative undervoltage fault bit in the diagnostic registers to change state. If the diagnostic UV register bits change state, the corresponding verify register bits will latch high. When the test of all UV detectors is complete, the verify register bits will remain high if the test passed. If any UV bits in the verify registers, after test, are not set high, then the verification has failed. The following UV detectors are tested: VREG, VUC, V5C, V5P1, and V5P2.

Overvoltage Detect Self-Test

The overvoltage (OV) detectors are verified during startup of the ARG82801. A voltage is applied to each OV comparator that is higher than the overvoltage threshold; this should cause the relative overvoltage fault bit in the diagnostic registers to change state. If the diagnostic OV register bits change state, the corresponding verify register bits will latch high. When the test of all OV detectors is complete, the verify register bits will remain high if the test passed. If any OV bits in the verify registers after test are not set high, then the verification has failed. The following OV detectors are tested: VREG, VUC, V5C, V5P1, and V5P2.

Overtemperature Shutdown Self-Test

The overtemperature shutdown (TSD) detector is verified on startup of the ARG82801. A voltage is applied to the comparator that is lower than the overtemperature threshold and should cause the general fault flag to be active and an overtemperature fault bit, TSD, to be latched in the Verify Result register 0. When the test is complete, the general fault flag will be cleared and the overtemperature fault will remain in the Verify Result register 0 until reset. If the TSD bit is not set, then the verification has failed.

Power-On Enable Self-Test

The ARG82801 also incorporates continuous self-testing of the power-on enable (POE) output. It compares the status of the POE pin with the internal demanded status. If they differ for any reason, an FFn is set and the POE_OK in SPI diagnostic register goes low.

Watchdog Timer

The ARG82801 has two watchdog functions: window watchdog timer and Q&A watchdog timer. When the regulators (VUC and V5C) have been above their undervoltage thresholds for watchdog activation delay ($t_{d(WD)}$), WD is activated, WD state will be in the configuration state ("Config"), and the user can set the configuration within 220 ms (min, $t_{WDTO(CONFIG)}$). If no configuration input until $t_{WDTO(CONFIG)}$ is expired, WD moves into "RESET". Moving back to "Config" mode requires secure SPI command (0x0B).

WINDOW WATCHDOG

The ARG82801 window watchdog circuit monitors an external clock applied to the WDIN pin. This clock should be generated by the microcontroller or DSP. The time between rising edges of the clock must fall within a SPI-programmed "window" or a watchdog fault will be generated. A watchdog fault will set NPOR and POE "low".

After startup, if no clock edges are detected at WDIN for watchdog activation delay $t_{d(WD)}$ + max timeout (written in 0x09), the ARG82801 will generate watchdog fault and reset its counters. This process will repeat until the system recovers and clock edges are applied to WDIN.

Q&A WATCHDOG

The Q&A watchdog circuit monitors an answer code from the microcontroller. The Q&A watchdog procedure is as follows:

1. Write 0x08 to set open window period and acceptable number of mis-refresh in “Config” mode.
2. Write 0x0B for watchdog restart. Then ARG82801 enters into “Normal” mode and generates 6-bit random code.
3. Microcontroller reads 0x0A to get 6-bit random code via SDO.
4. Write 0x0A with 6-bit inverted random code within open window period. In case the ARG82801 can’t get the right inverted code, then the watchdog timer is refreshed and generates new 6-bit random code. ARG82801 can accept mis-refresh.
5. Repeat #2 to #4 within the programmed window.

Analog Multiplexer Output

The AMUXO terminal is an analog multiplexer output to monitor the voltage of the nodes detailed in Table 3. The output is selected through the serial interface (0x0C). The driving capability of this output is 1 mA and maximum voltage is 3.8 V. Reference response time from SPI register write to AMUX output change is ~20 µs.

Table 3: Analog Multiplexer Output

Node	Signal Divide Ratio	Tolerance (reference)
VREG	1/2	±6%
VUC	1/2	±6%
V5C	1/2	±6%
V5P1	1/2	±6%
V5P2	1/2	±6%
VENBAT	1/8	±6%
VCP1	1/12	±6%
VCP2	1/12	±6%
BG1	1/1	±6%
BG2	1/1	±6%
VIN	1/10	±6%
TEMP	–	Output (mV) = 1440 mV – 3.92 mV/°C × T_J (°C)

Floating MOSFET Gate Drivers

The ARG82801 has four independent floating gate drive outputs to drive external, low on-resistance, power N-channel MOSFETs connected as a 3-phase solid state relay in phase-isolation applications and an input battery line isolator.

A charge pump regulator provides the above-battery supply voltage necessary to maintain the power MOSFETs in the on state continuously when the phase voltage is equal to the battery voltage.

An internal resistor, R_{GPD}, between the Gx and Sx pins plus an integrated hold-off circuit, will ensure that the gate-source voltage of the MOSFET is held close to 0 V even with the power disconnected. This can remove the need for additional gate-source resistors on the isolation MOSFETs. In any case, if gate-source resistors are mandatory for the application, then the pump regulator can provide sufficient current to maintain the MOSFET in the on state with a gate-source resistor as low as 100 kΩ.

The four gate drives can be controlled independently through the serial interface by setting the appropriate bit in the control register.

The floating gate-drive outputs for external N-channel MOSFETs are provided on pins GVBB, GU, GV, and GW. Gx=1 (or “high”) means that the upper half of the driver is turned on and current will be sourced to the gate of the MOSFET in the phase isolation circuit, turning it on. Gx=0 (or “low”) means that the lower half of the driver is turned on and will sink current from the external MOSFET’s gate to the respective Sx terminal, turning it off.

The reference points for the floating drives are the load phase connections, SVBB, SU, SV, and SW. The discharge current from the floating MOSFET gate capacitance flows through these connections.

In some applications, it may be necessary to provide a current recirculation path when the motor load is isolated. This will be necessary in situations where the motor driver does not reduce the load current to zero before the isolation MOSFETs are turned off.

The recirculation path can be provided by connecting a suitably rated power diode to the “motor” side of the isolation MOSFETs and GND. See the Functional Block Diagram for more details.

Table 4: Floating MOSFET Driver

Name	GD_U_SEL (0x09 [D5])	Purpose	Enable/Disable			Gate to Source UV	Source to GND UV		UV Filter		
			Register Bit	GD_EN_DLY	Delay	State Register bit	Function	State Register bit	GD_UV_FLT	GSx UV Filter	SVBB/SU UV Filter
GVBB / SVBB	X (don't care)	VBAT disconnect	ENVBB (0x07 [D3])	0	1.5 ms	GSVBB_UV (0x02 [D7])	Yes	SVBB_UV (0x02 [D3])	0	1.4 ms	0.8 ms
				1	EN < 3 µs DIS < 2.25 µs				1	11 µs	11 µs
GU / SU	0	Phase disconnect	ENU (0x07 [D2])	0	10 ms	GSU_UV (0x02 [D6])	No (Disabled)	SU_UV (0x02 [D2]) Always=0	0	1.4 ms	–
				1	EN < 3 µs DIS < 2.25 µs				1	11 µs	–
	1	VBAT disconnect		0	1.5 ms		Yes	SU_UV (0x02 [D2])	0	1.4 ms	0.8 ms
				1	EN < 3 µs DIS < 2.25 µs				1	11 µs	11 µs
GV / SV	X	Phase disconnect	ENV (0x07 [D1])	0	10 ms	GSV_UV (0x02 [D5])	No	–	0	1.4 ms	–
				1	EN < 3 µs DIS < 2.25 µs				1	11 µs	–
GW / SW	X	Phase disconnect	ENW (0x07 [D0])	0	10 ms	GSW_UV (0x02 [D4])	No	–	0	1.4 ms	–
				1	EN < 3 µs DIS < 2.25 µs				1	11 µs	–