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AS1119

144-LED Cross-Plexing Driver with 320mA Charge-Pump

General Description

The AS1119 is a compact LED driver for 144 (90) single LEDs. The devices can be programmed via an I²C compatible interface.

The AS1119 offers two blocks driving each 72 LEDs (3 blocks each 30LEDs) with 1/9 (1/6) cycle rate. The required lines to drive all 144 (90) LEDs are reduced to 18 by using the cross-plexing feature optimizing space on the PCB. Every block driving 72(30) LEDs can be analog dimmed from 1 to 30mA in 256 steps (8 bit).

Additionally each of the 144 (90) LEDs can be dimmed individually with 8-bit allowing 256 steps of linear dimming. To reduce CPU usage up to 6 frames can be stored with individual time delays between frames to play small animations automatically.

The AS1119 operates from 2.7V to 5.5V and includes a 320mA charge-pump to drive also white LEDs. The charge-pump operates in 2:3 and 1:2 mode.

The AS1119 features very low shutdown and operational current. The device is available in a ultrasmall 36-pin WL-CSP.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of the AS1119, 144-LED Cross-Plexing Driver with 320mA Charge-Pump are listed below:

Figure 1:
Added Value of Using AS1119

Benefits	Features
• Excellent PCB real estate vs LED count	• Up to 144LEDs as 2x 8x9 or 3x 5x6
• 16.7M full color matrix with white balance	• 8bit PWM per LED and current control per matrix
• Reduces MCU load and increases battery lifetime	• 6 frames of memory
• Extends battery lifetime while reducing BOM and increasing ease of use	• Internal automatic charge pump

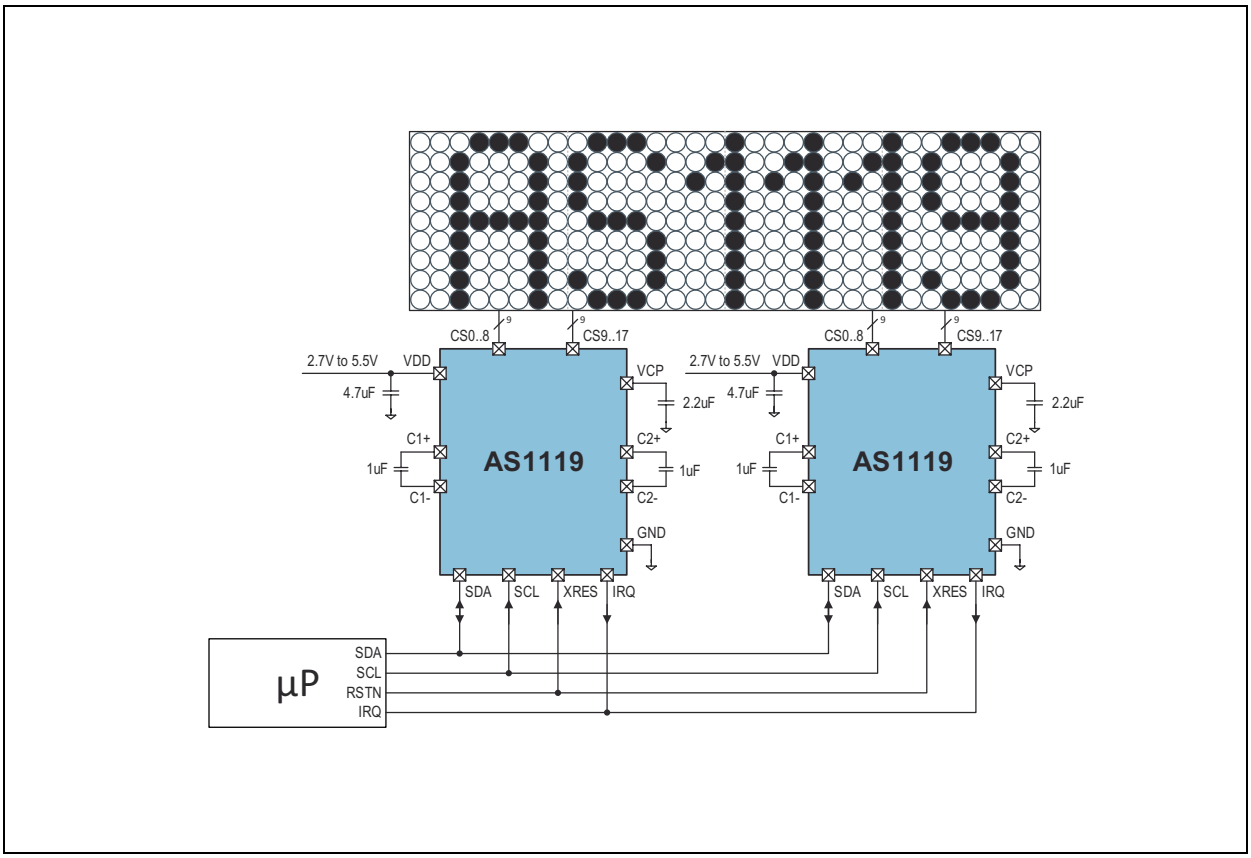
- 1MHz I²C-compatible interface
- Open and shorted LED error detection
- 144 LEDs in dot matrix
- Low-power shutdown current

- Individual 8-bit LED PWM control
- 8-bit analog brightness control
- (1:1), 2:3, 1:2 320mA charge pump
- 6 frames memory for animations
- System-clk synchronisation for multiple devices
- Supply voltage range: 2.7V to 5.5V
- Minimum PCB space required
- 36-pin WL-CSP package

Applications

The AS1119 is ideal for dot matrix displays in mobile phones, personal electronics and toys.

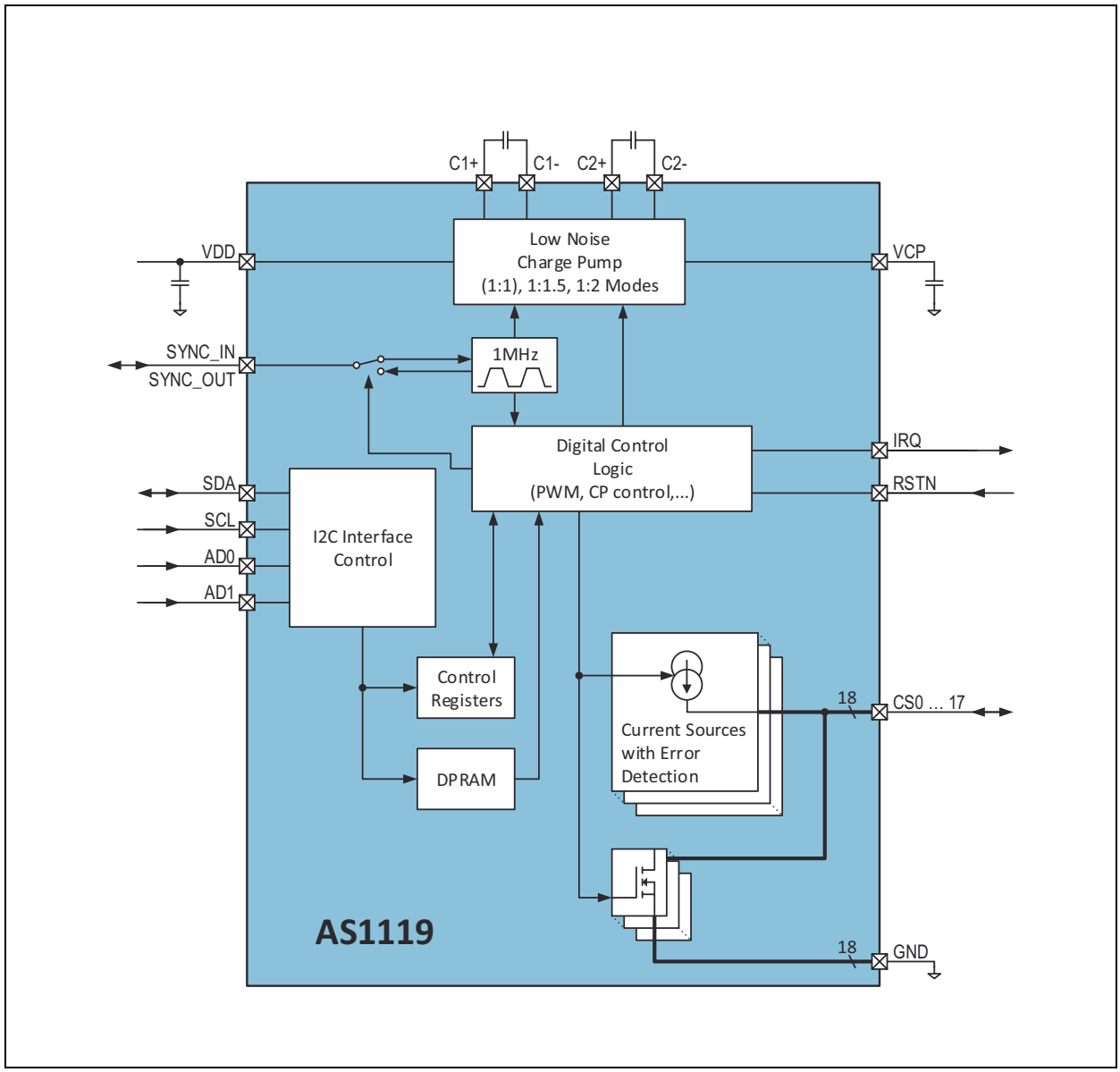
Figure 2:
Typical Application Diagram



Block Diagram

The functional blocks of this device are shown below:

Figure 3:
AS1119 Block Diagram



Pin Assignments

The AS1119 pin assignments are described below:

Figure 4:
Pin Diagram (Top View)

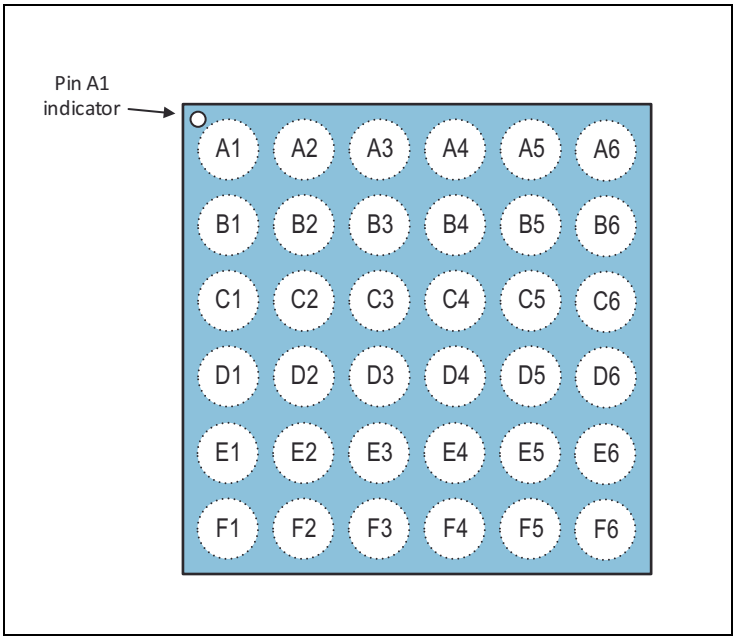


Figure 5:
Pin Description

Pin Name	Pin Number	Description
V_{DD1}, V_{DD2}, V_{DD3}	A6, E5, E1	**Positive Supply Voltage**. Connect to a +2.7V to +5.5V supply. Bypass this pin with 10µF capacitance to GND1, GND2, GND3.
VCP	F1	**Charge-Pump Output Voltage**. Connect a 2.2µF capacitor to GND3.
C1-, C1+	B1, C1	**Flying Cap 1**. Connect a 1µF capacitor.
C2-, C2+	A1, D1	**Flying Cap 2**. Connect a 1µF capacitor.
GND1	B5	**Ground for VDD1**. Used for CS0-CS8
GND2	F5	**Ground for VDD2**. Used for CS9-CS17
GND3	A2	**Ground for VDD3**. Used for Charge-Pump.
SDA	C6	**Serial-Data I/O**. Open drain digital I/O I^2C data pin.
SCL	D6	**Serial-Clock Input**.
AD0	C5	**I^2C Address for bit 0**. Put to GND or VDD to set I^2C addresses.
AD1	D5	**I^2C Address for bit 1**. Put to GND or VDD to set I^2C addresses.

Pin Name	Pin Number	Description	
RSTN	F6	**Reset Input**. Pull this pin to logic low to reset all control registers (set to default values) and to put the device into power-down. For normal operation pull this pin to VDD.	
SYNC_IN, SYNC_OUT	B6	**Synchronization Clock Input or Output**	
IRQ	E6	**Interrupt Request**. Open drain digital Output.	
CS0 - CS8	A5-A3, B4-B2, C4-C2	2 Matrices	**Sinks and Sources** for 72 LEDs each matrix.
CS9 - CS17	D4-D2, E4-E2, F4-F2		
CS0 - CS5	A5-A3, B4-B2	3 Matrices	**Sinks and Sources** for 30 LEDs each matrix.
CS6 - CS11	C4-C2, D4-D2		
CS12 - CS17	E4-E2, F4-F2		

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Parameter	Min	Max	Unit	Comments
Electrical Parameters				
V_{DD} to GND	-0.3	7	V	
All other pins to GND	-0.3	7 or V_{DD} + 0.3	V	
Sink current		500	mA	
Segment current		100	mA	
Input current (latch-up immunity)	-100	100	mA	JEDEC 78
Electrostatic Discharge				
Electrostatic discharge HBM	±1.5		kV	MIL 883 E method 3015
Temperature Ranges and Storage Conditions				
Junction temperature		125	°C	
Storage temperature range	-55	125	°C	
Package body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/ JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".*
Relative humidity (non-condensing)	5	85	%	
Moisture sensitivity level	1			Represents a max. floor life time of unlimited

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

V_{DD} = 2.7V to 5.5V, T_{AMB} = -40°C to 85°C, typ. values are at T_{AMB} = 25°C (unless otherwise specified).

Figure 7:
Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{AMB}	Operating temperature range			-40		85	°C
V_{DD}	Operating supply voltage			2.7		5.5	V
I_{DDSD}	Software shutdown supply current	All digital inputs at V_{DD} or GND, VDD = 5.5V, T_{AMB} = 25°C			7		µA
I_{DDFSD}	Full shutdown supply current	Pin RSTN = 0V, T_{AMB} = 25°C			0.1	1	µA
I_{DD}	Operating supply current (all current sources turned off)	CP disabled @ V_{DD} = 5.5V			1.4		mA
		With CP in 2:3 mode @ V_{DD} = 2.7V			3		
		With CP in 1:2 mode @ V_{DD} = 2.7V			4		
I_{START}	Max. peak inrush current				1.5		A
	Max. DC current				700		mA
I_{DIGIT}	Digit drive sink current (drive capability of all sources of one digit[1], [2])	CP disabled				500	mA
		CP enabled	V_{DD} < 3.3V			160	
			V_{DD} ≥ 3.3V			320	
I_{SEG}	Segment drive source current LED	V_{OUT} = 1.8V to V_{DD} - 400mV		28	30	32	mA
ΔI_{SEG}	Segment drive current matching LED [3]				2		%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DSSAT}	Saturation voltage	Current = 30mA, V_{DD} = 5V		100		mV
$R_{DSON(N)}$	Resistance for NMOS			0.5	1	Ω
f_{OSC}	Oscillator frequency		0.9	1	1.1	MHz
$f_{REFRESH}$	Display scan rate	2 time 9 × 8 matrixes	0.39	0.43	0.48	kHz

Note(s):

1. Not all sources are allowed to be fully ON at the same time.
2. guaranteed by design
3. $I_{SEG} = \frac{I_{max} - I_{min}}{I_{max} + I_{min}} \times 100$

Figure 8:
Logic Inputs/Outputs Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}, I_{IL}	Logic input current	V_{IN} = 0V or V_{DD}	-1		1	µA
V_{IH}	Logic high input voltage		1.6			V
V_{IL}	Logic low input voltage				0.6	V
ΔV_I	Hysteresis voltage			0.1		V
$V_{OL(SDA)}$	SDA output low voltage	I_{SINK} = 3mA			0.4	V
$V_{OL(IRQ)}$	IRQ output low voltage	I_{SINK} = 3mA			0.4	V
$V_{OL(SYNC\_OUT)}$	Sync clock output low voltage	I_{SINK} = 1mA			0.4	V
$V_{OH(SYNC\_OUT)}$	Sync clock output high voltage	I_{SOURCE} = 1mA			V_{DD} - 0.4	V
	Open detection level threshold		V_{DD} - 0.4	V_{DD}-0.1		V
	Short detection level threshold			0.9	1.2	V
	Capacitive load for each bus line	SCL frequency = 400kHz			400	pF
		SCL frequency = 1000kHz			100	

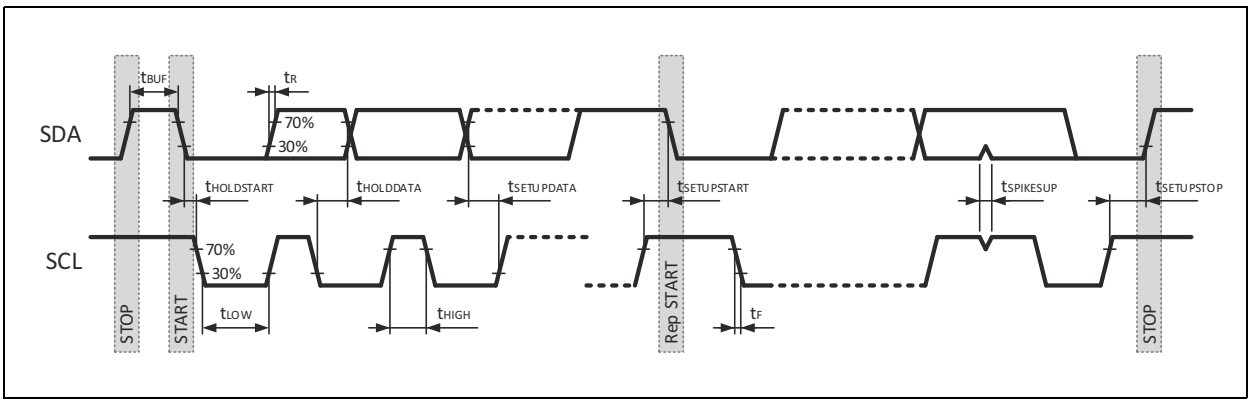
Figure 9:
I²C Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL frequency		100		1000	kHz
t_{BUF}	Bus free time between STOP and START conditions		1.3			µs
$t_{HOLDSTART}$	Hold time for repeated START condition		160			ns
t_{LOW}	SCL low period		50		75	ns
t_{HIGH}	SCL high period		50		75	ns
$t_{SETUPSTART}$	Setup time for repeated START condition		100			ns
$t_{SETUPDATA}$	Data setup time		10			ns
$t_{HOLDDATA}$	Data hold time				70	ns
$t_{RISE(SCL)}$	SCL rise time		10		40	ns
$t_{RISE(SCL1)}$	SCL rise time after repeated START condition and after an ACK bit		10		80	ns
$t_{FALL(SCL)}$	SCL fall time		10		40	ns
$t_{RISE(SDA)}$	SDA rise time		20		80	ns
$t_{FALL(SDA)}$	SDA fall time		20		80	ns
$t_{SETUPSTOP}$	STOP condition setup time		160			ns
$t_{SPIKESUP}$	Pulse width of spike suppressed			50		ns

Note(s):

1. The Min / Max values of the Timing Characteristics are guaranteed by design.

Figure 10:
Timing Diagram



Typical Operating Characteristics

Figure 11:
Segment Drive Current vs. Supply Voltage

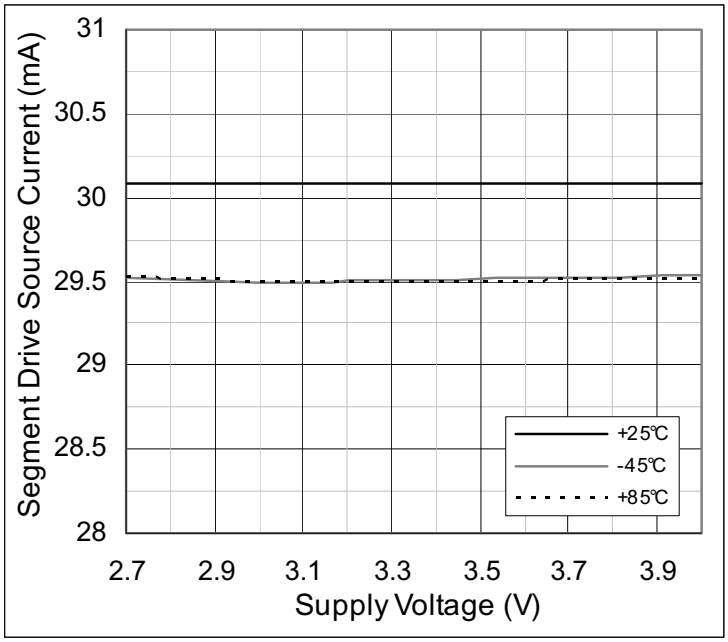


Figure 12:
Segment Drive Current vs. Temperature

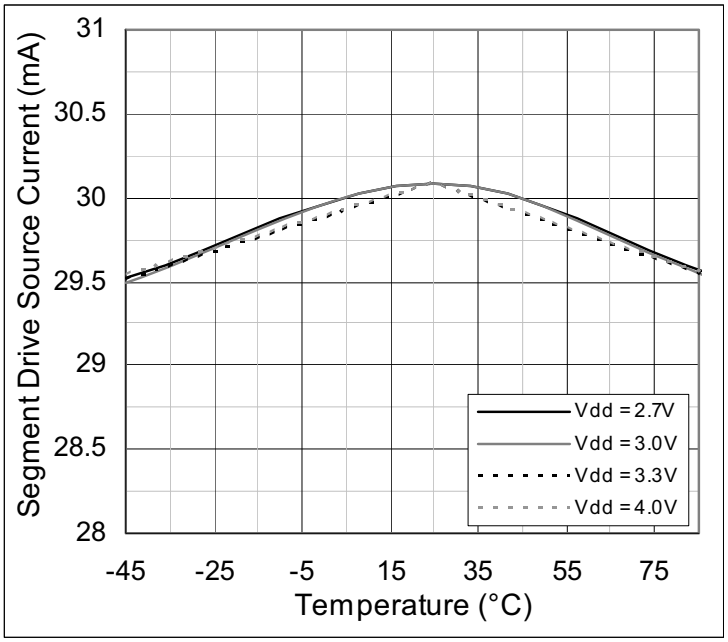


Figure 13:
Segment Drive Current vs. Output Voltage

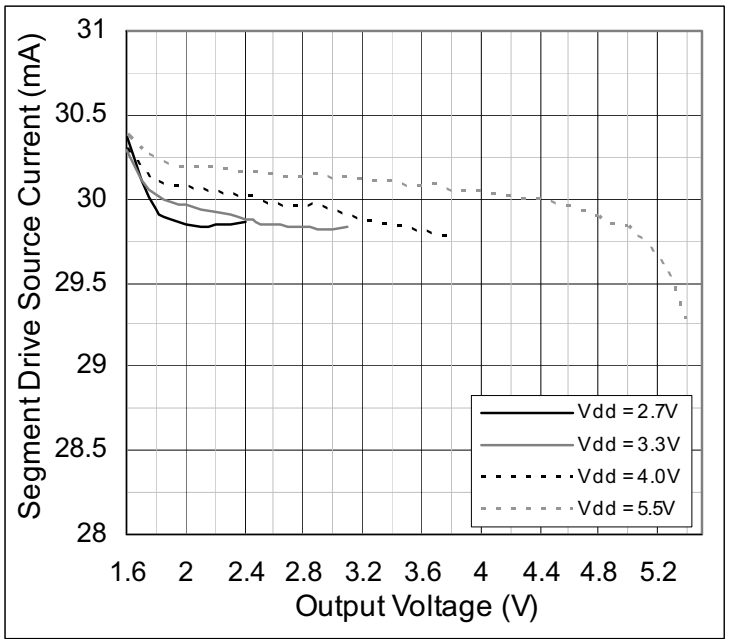


Figure 14:
R_{ONNMOS} vs. Supply Voltage

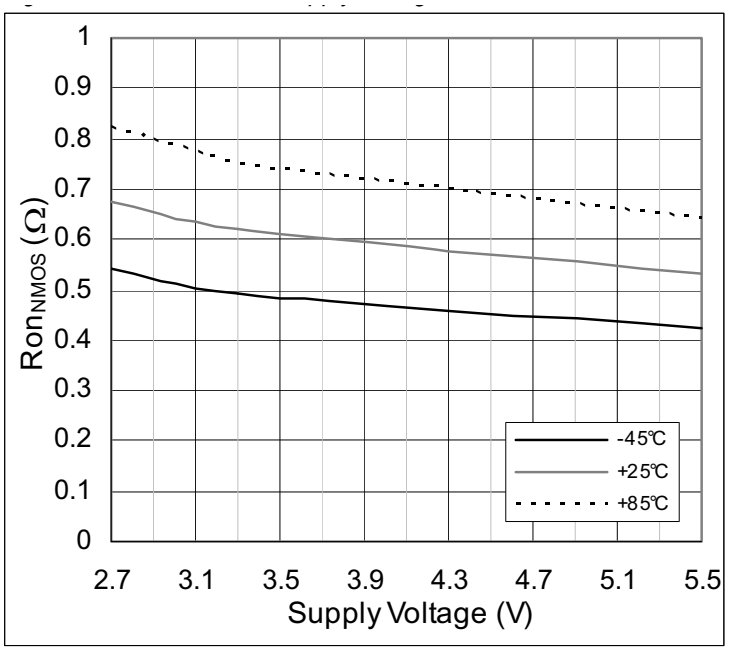


Figure 15:
Open Detection Level vs. Supply Voltage

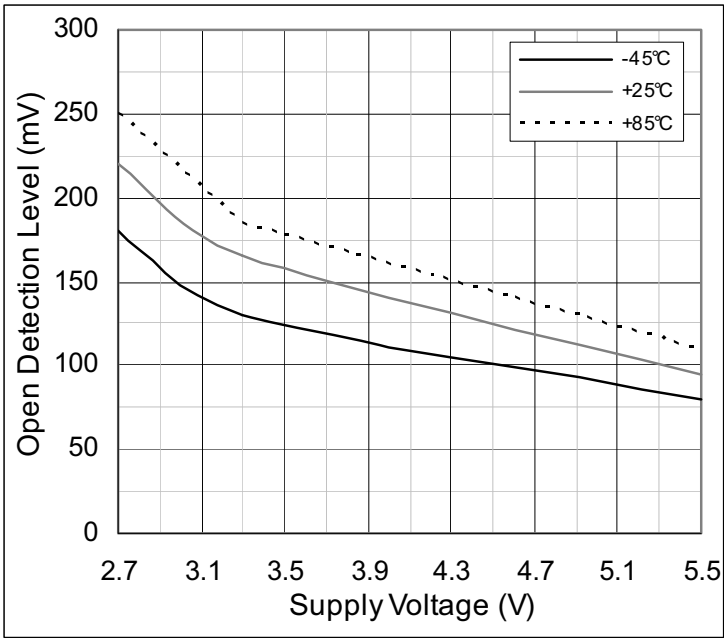


Figure 16:
Short Detection Level vs. Supply Voltage

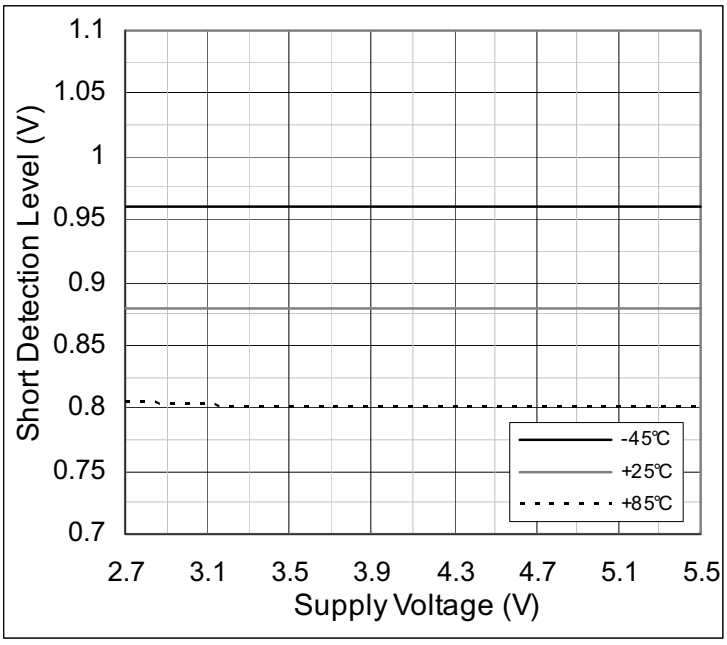


Figure 17:
Efficiency vs. Supply Voltage

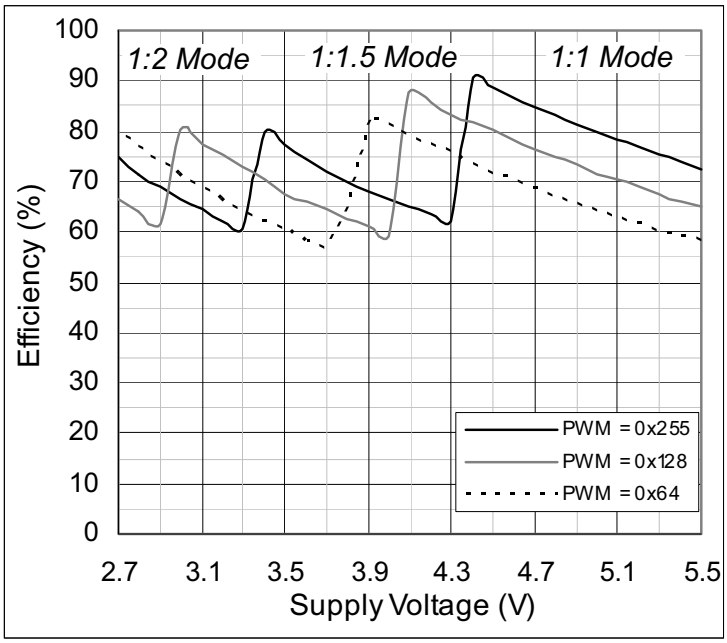


Figure 18:
Logic Input Voltage Levels

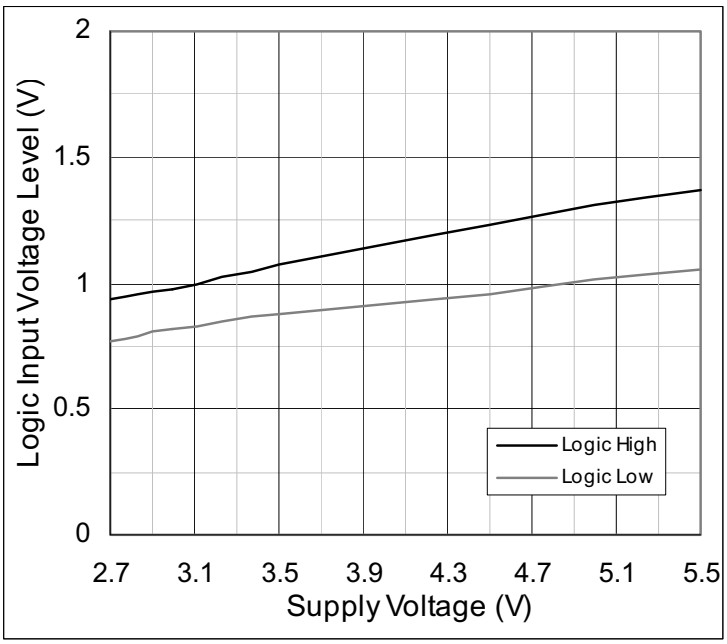
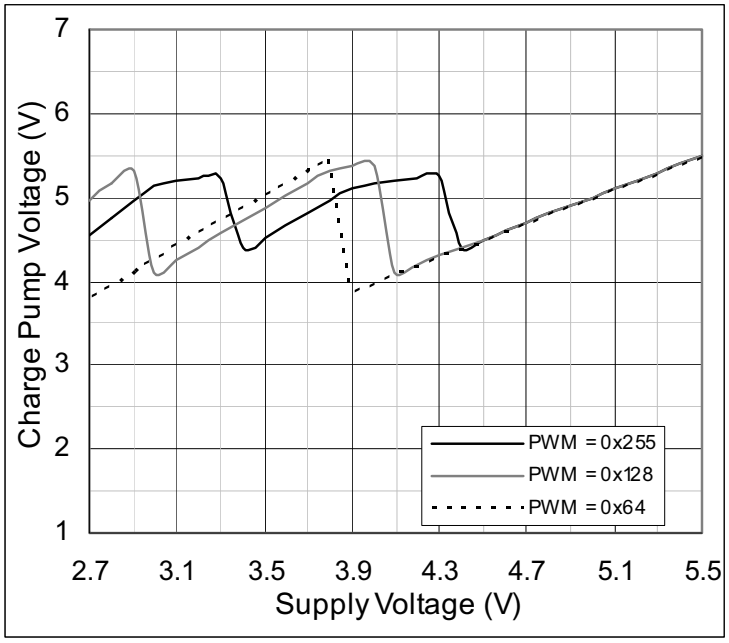


Figure 19:
Charge Pump Voltage vs. Supply Voltage



Detailed Description

I²C Interface

The AS1119 supports the I²C serial bus and data transmission protocol in fast mode at 1MHz. The AS1119 operates as a slave on the I²C bus. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. Connections to the bus are made via the open-drain I/O pins SCL and SDA.

Figure 20:
I²C Interface Initialization

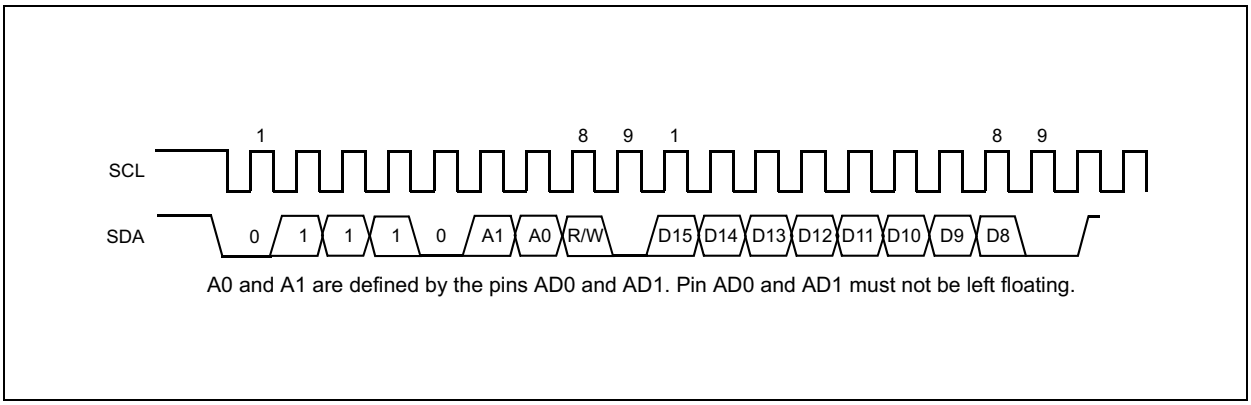
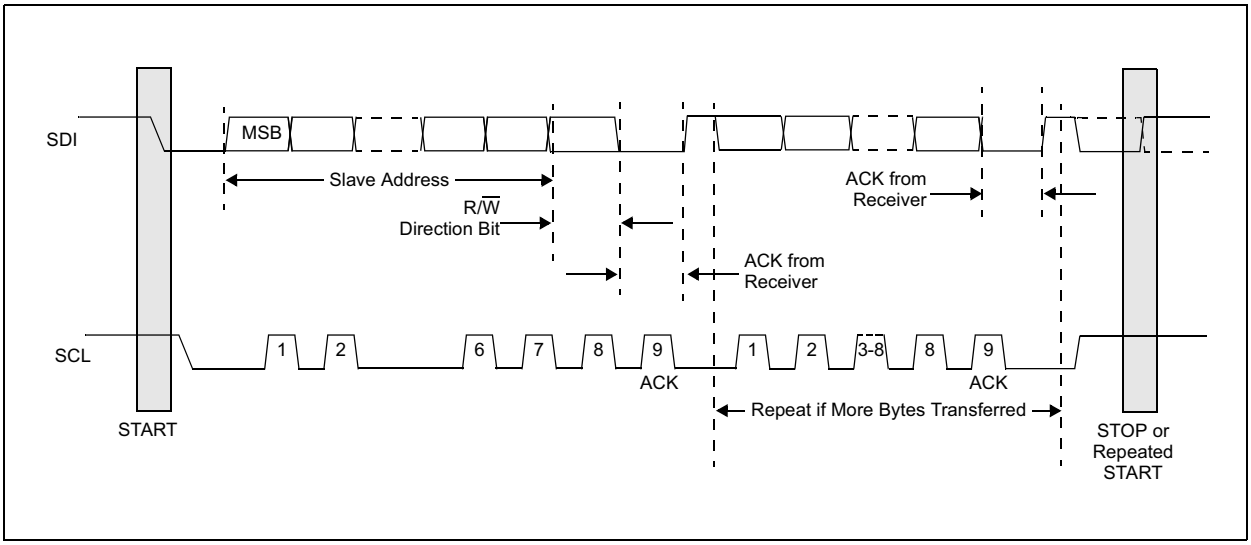


Figure 21:
Bus Protocol



The bus protocol (as shown in Figure 21) is defined as:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The bus conditions are defined as:

- **Bus Not Busy**. Data and clock lines remain HIGH.
- **Start Data Transfer**. A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.
- **Stop Data Transfer**. A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.
- **Data Valid**. The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit. Within the I^2C bus specifications a high-speed mode (3.4MHz clock rate) is defined.
- **Acknowledge**. Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Ofcourse, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.
- Figure 21 details how data transfer is accomplished on the I^2C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:
- **Master Transmitter to Slave Receiver**. The first byte transmitted by the master is the slave address, followed by a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
- **Slave Transmitter to Master Receiver**. The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

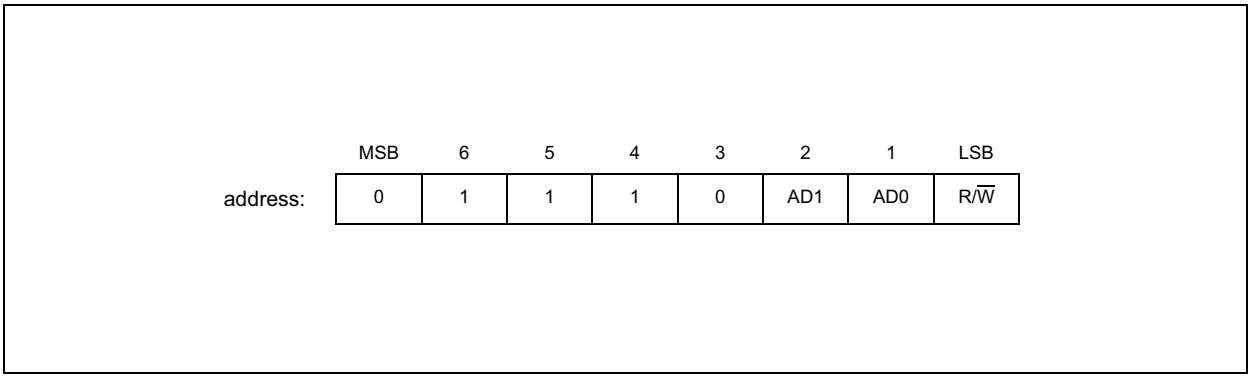
The AS1119 can operate in the following slave modes:

- **Slave Receiver Mode**. Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- **Slave Transmitter Mode**. The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the AS1119 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

I²C Device Address Byte

The address byte (see Figure 22) is the first byte received following the START condition from the master device.

Figure 22:
I²C Device Address Byte



- The bit 1 and bit 2 of the address byte are the device select pins AD0 and AD1, which must be set to V_{DD} or to GND. A maximum of four devices with the same pre-set code can therefore be connected on the same bus at one time.
- The last bit of the address byte (R/$\overline{W}$) define the operation to be performed. When set to a 1 a read operation is selected; when set to a 0 a write operation is selected.

Following the START condition, the AS1119 monitors the I²C bus, checking the device type identifier being transmitted. Upon receiving the address code, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Command Byte

The AS1119 operation, (see Figure 21) is determined by a command byte (see Figure 23).

Figure 23:
Command Byte

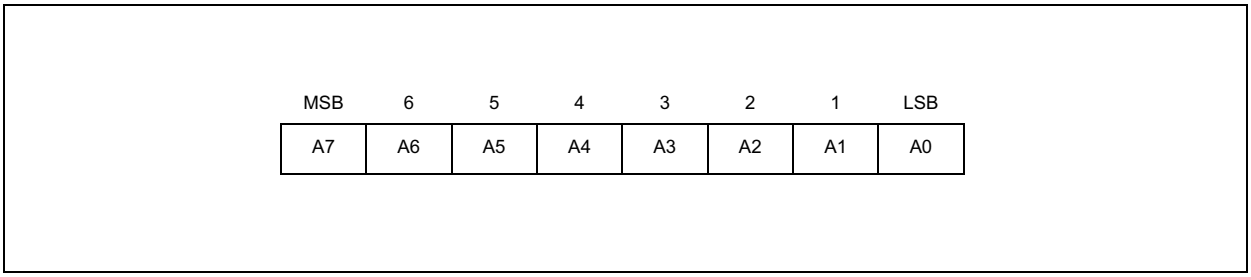


Figure 24:
Command and Single Data Byte Received by AS1119

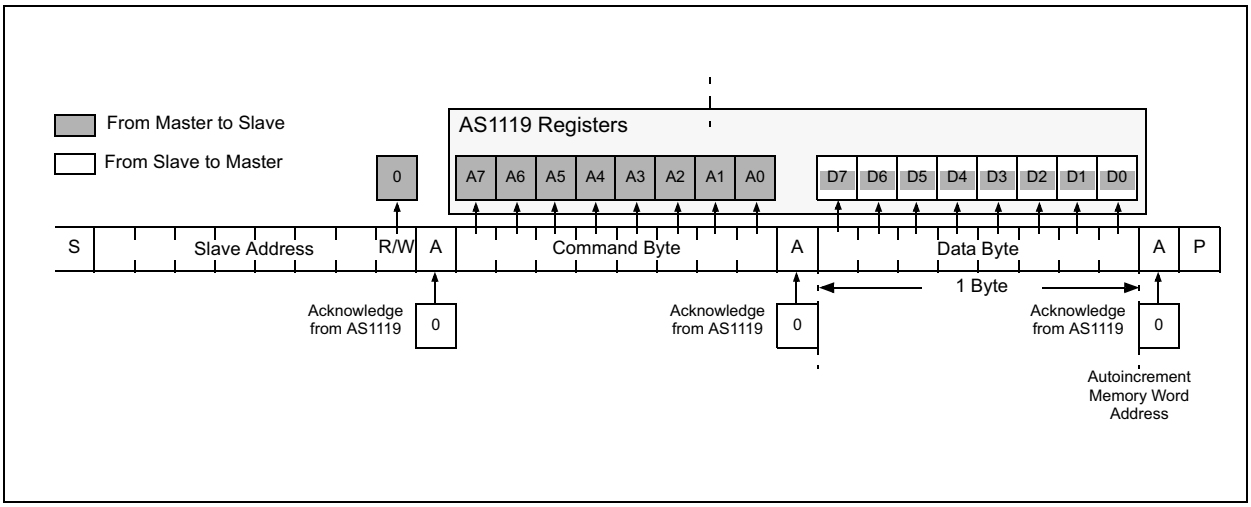


Figure 25:
Setting the Pointer to a Address Register to Select a Data Register for a Read Operation

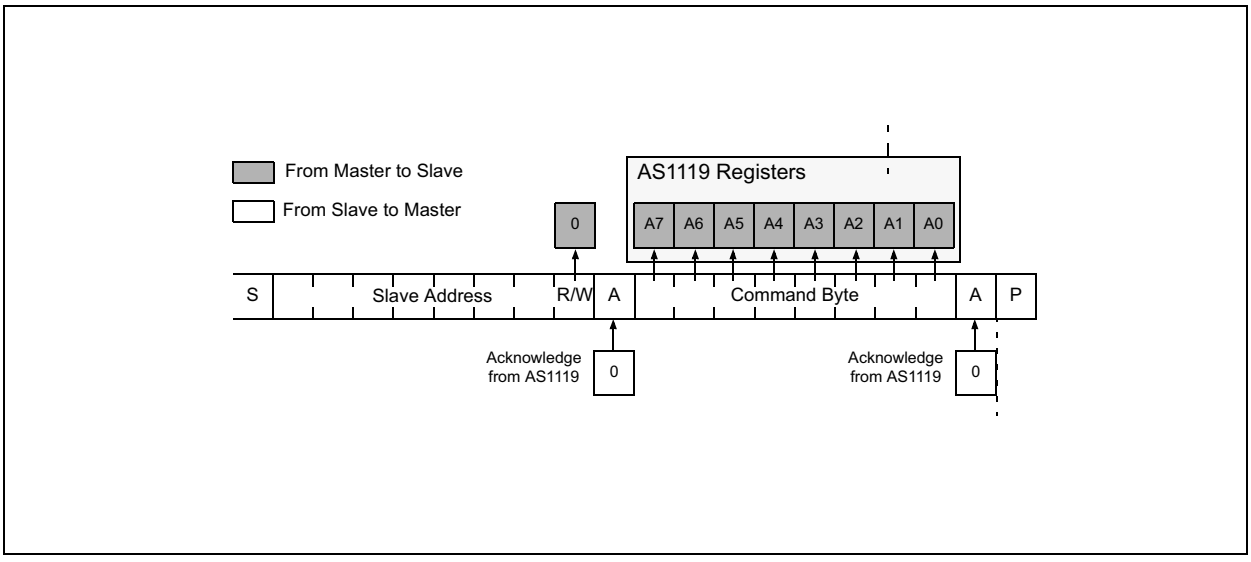
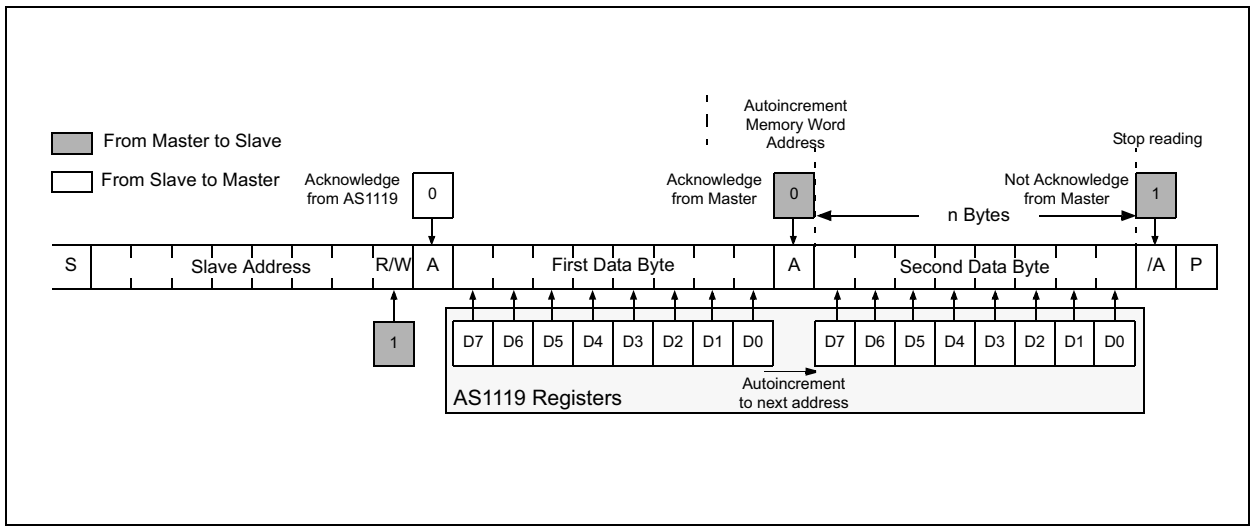


Figure 26:
Reading n Bytes from AS1119



Initial Power-Up

On initial power-up, the AS1119 registers are reset to their default values, the display is blanked, and the device goes into shutdown mode. At this time, all registers should be programmed for normal operation.

Note(s): The default settings enable only scanning of one digit; the internal decoder is disabled and the Intensity Control Register (see Figure 32) and (see Figure 37) is set to the minimum values.

Shutdown Mode

The AS1119 device features two different shutdown modes. A software shutdown via shutdown register (see Shutdown Register (0x0A)) and a hardware shutdown via the RSTN pin.

The software shutdown disables all LEDs and stops the internal operation of the logic. A shutdown mode via the RSTN pin additionally powers down the power-on-reset (PO) of the device. In this shutdown mode the AS1119 consumes only 100nA (typ.).

Register Description

Register Selection

Within this register the access to one of the RAM sections or to the Control register is selected. After one section is selected this section is valid as long as an other section is selected.

Figure 27:
Register Selection Address Map

Register Section	Address									Data									Description
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	HEX	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	253	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	No operation
Data Frame 0										1	0	0	0	0	0	0	0	1	Selection of RAM section for frame
Data Frame 1										2	0	0	0	0	0	0	1	0	
Data Frame 2										3	0	0	0	0	0	0	1	1	
Data Frame 3										4	0	0	0	0	0	1	0	0	
Data Frame 4										5	0	0	0	0	0	1	0	1	
Data Frame 5										6	0	0	0	0	0	1	1	0	
Control Register										11	0	0	0	0	1	0	1	1	Selection of Control Register

Data Definition of Single Frames

One frame consists of 2 blocks (a 8 × 9 LED-matrix) or 3 blocks (a 5 × 6 LED-matrix). This configuration is set in the AS1119 config register (see Figure 43).

In the internal DPRAM of the device 6 frames can be stored. For each frame the following parameters have to be stored.

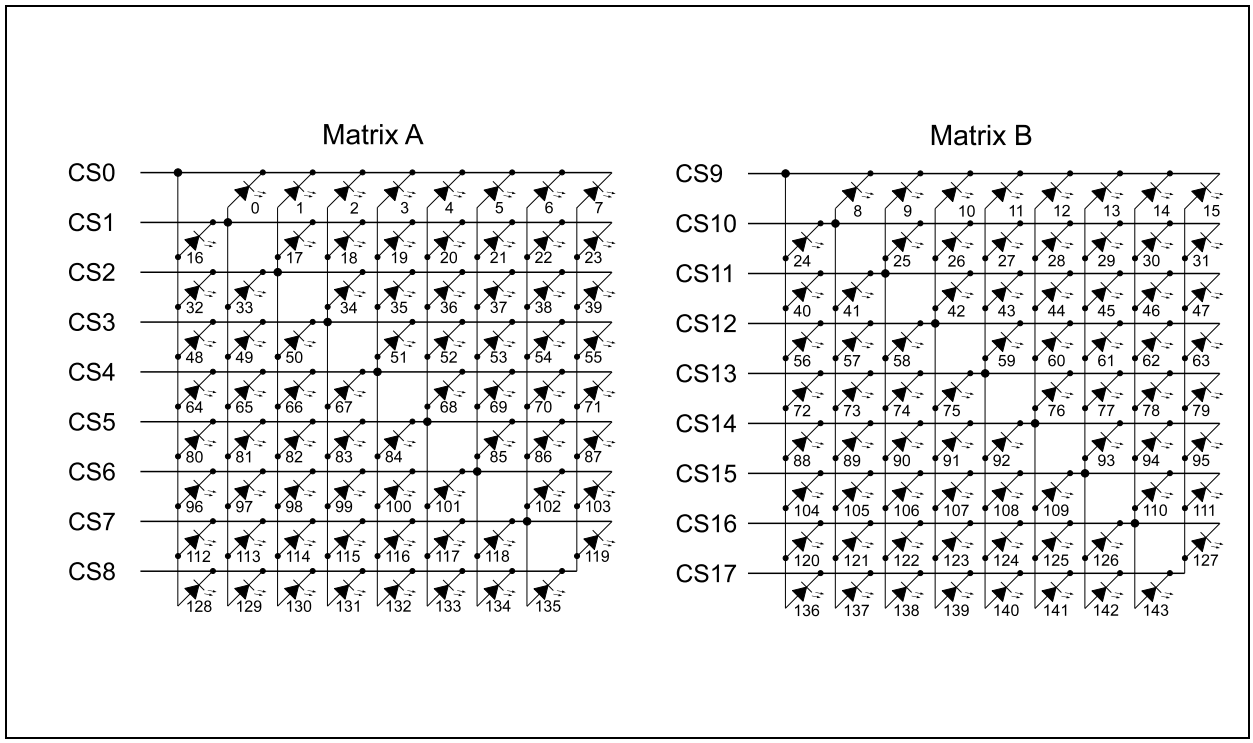
- LED is ON or OFF.
- LED is steady ON or blinking.
- The intensity of every single LED can be set via a 8 bits PWM.

Note(s): After power-up the data in the DPRAM is undefined (either '0' or '1').

2 Blocks with 8x9 LED Matrix

The AS1119 can be configured to control two separated blocks of LEDs matrixes. This must be set via the bit D0 in the AS1119 config register (see Figure 43).

Figure 28:
8x9 LED Matrix with Two Blocks



The address structure (as shown in Figure 29) within on frame is always the same independent which frame was selected via the register selection (Register Selection Address Map).

Figure 29:
Dataframe Address Structure for 2 Matrixes

		Addresses Within Frame (HEX code)					
Current Source		On / Off		Blink		Intensity	
Matrix A	Matrix B	Matrix A	Matrix B	Matrix A	Matrix B	Matrix A	Matrix B
CS0	CS9	0x00	0x01	0x12	0x13	0x24-0x2B	0x2C-0x33
CS1	CS10	0x02	0x03	0x14	0x15	0x34-0x3B	0x3C-0x43
CS2	CS11	0x04	0x05	0x16	0x17	0x44-0x4B	0x4C-0x53
CS3	CS12	0x06	0x07	0x18	0x19	0x54-0x5B	0x5C-0x63
CS4	CS13	0x08	0x09	0x1A	0x1B	0x64-0x6B	0x6C-0x73
CS5	CS14	0x0A	0x0B	0x1C	0x1D	0x74-0x7B	0x7C-0x83
CS6	CS15	0x0C	0x0D	0x1E	0x1F	0x84-0x8B	0x8C-0x93
CS7	CS16	0x0E	0x0F	0x20	0x21	0x94-0x9B	0x9C-0xA3
CS8	CS17	0x10	0x11	0x22	0x23	0xA4-0xAB	0xAC-0xB3

In Figure 30 it's described which databit represents which LED in the matrix. Per default all databits are '0', meaning no LED is On. A '1' puts the LED On.

Figure 30:
LEDs ON/OFF Register Format for 2 Matrices Setup

Matrix	Current Source	Address									Data							
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
A	CS0	0x00	0	0	0	0	0	0	0	0	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
B	CS9	0x01	0	0	0	0	0	0	0	1	LED15	LED14	LED13	LED12	LED11	LED10	LED9	LED8
A	CS1	0x02	0	0	0	0	0	0	1	0	LED23	LED22	LED21	LED20	LED19	LED18	LED17	LED16
B	CS10	0x03	0	0	0	0	0	0	1	1	LED31	LED30	LED29	LED28	LED27	LED26	LED25	LED24
A	CS2	0x04	0	0	0	0	0	1	0	0	LED39	LED38	LED37	LED36	LED35	LED34	LED33	LED32
B	CS11	0x05	0	0	0	0	0	1	0	1	LED47	LED46	LED45	LED44	LED43	LED42	LED41	LED40
A	CS3	0x06	0	0	0	0	0	1	1	0	LED55	LED54	LED53	LED52	LED51	LED50	LED49	LED48
B	CS12	0x07	0	0	0	0	0	1	1	1	LED63	LED62	LED61	LED60	LED59	LED58	LED57	LED56
A	CS4	0x08	0	0	0	0	1	0	0	0	LED71	LED70	LED69	LED68	LED67	LED66	LED65	LED64
B	CS13	0x09	0	0	0	0	1	0	0	1	LED79	LED78	LED77	LED76	LED75	LED74	LED73	LED72
A	CS5	0x0A	0	0	0	0	1	0	1	0	LED87	LED86	LED85	LED84	LED83	LED82	LED81	LED80
B	CS14	0x0B	0	0	0	0	1	0	1	1	LED95	LED94	LED93	LED92	LED91	LED90	LED89	LED88
A	CS6	0x0C	0	0	0	0	1	1	0	0	LED103	LED102	LED101	LED100	LED99	LED98	LED97	LED96
B	CS15	0x0D	0	0	0	0	1	1	0	1	LED111	LED110	LED109	LED108	LED107	LED106	LED105	LED104
A	CS7	0x0E	0	0	0	0	1	1	1	0	LED119	LED118	LED117	LED116	LED115	LED114	LED113	LED112

Matrix	Current Source	Address								Data							
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
B	CS16	0x0F	0	0	0	0	1	1	1	1	LED127	LED126	LED125	LED124	LED123	LED122	LED121	LED120
A	CS8	0x10	0	0	0	1	0	0	0	0	LED135	LED134	LED133	LED132	LED131	LED130	LED129	LED128
B	CS17	0x11	0	0	0	1	0	0	0	1	LED143	LED142	LED141	LED140	LED139	LED138	LED137	LED136

In the blink register (see Figure 31) every single LED can be set to blink. The blink period is set in the display option register (see Display Option Register (0x03)).

Figure 31:
LEDs Blink Register Format for 2 Matrixes Setup

Matrix	Current Source	Address								Data							
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
A	CS0	0x12	0	0	0	1	0	0	1	0	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
B	CS9	0x13	0	0	0	1	0	0	1	1	LED15	LED14	LED13	LED12	LED11	LED10	LED9	LED8
A	CS1	0x14	0	0	0	1	0	1	0	0	LED23	LED22	LED21	LED20	LED19	LED18	LED17	LED16
B	CS10	0x15	0	0	0	1	0	1	0	1	LED31	LED30	LED29	LED28	LED27	LED26	LED25	LED24
A	CS2	0x16	0	0	0	1	0	1	1	0	LED39	LED38	LED37	LED36	LED35	LED34	LED33	LED32
B	CS11	0x17	0	0	0	1	0	1	1	1	LED47	LED46	LED45	LED44	LED43	LED42	LED41	LED40
A	CS3	0x18	0	0	0	1	1	0	0	0	LED55	LED54	LED53	LED52	LED51	LED50	LED49	LED48
B	CS12	0x19	0	0	0	1	1	0	0	1	LED63	LED62	LED61	LED60	LED59	LED58	LED57	LED56
A	CS4	0x1A	0	0	0	1	1	0	1	0	LED71	LED70	LED69	LED68	LED67	LED66	LED65	LED64

Matrix	Current Source	Address									Data							
		HEX	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
B	CS13	0x1B	0	0	0	1	1	0	1	1	LED79	LED78	LED77	LED76	LED75	LED74	LED73	LED72
A	CS5	0x1C	0	0	0	1	1	1	0	0	LED87	LED86	LED85	LED84	LED83	LED82	LED81	LED80
B	CS14	0x1D	0	0	0	1	1	1	0	1	LED95	LED94	LED93	LED92	LED91	LED90	LED89	LED88
A	CS6	0x1E	0	0	0	1	1	1	1	0	LED103	LED102	LED101	LED100	LED99	LED98	LED97	LED96
B	CS15	0x1F	0	0	1	1	1	1	1	1	LED111	LED110	LED109	LED108	LED107	LED106	LED105	LED104
A	CS7	0x20	0	0	1	0	0	0	0	0	LED119	LED118	LED117	LED116	LED115	LED114	LED113	LED112
B	CS16	0x21	0	0	1	0	0	0	0	1	LED127	LED126	LED125	LED124	LED123	LED122	LED121	LED120
A	CS8	0x22	0	0	1	0	0	0	1	0	LED135	LED134	LED133	LED132	LED131	LED130	LED129	LED128
B	CS17	0x23	0	0	1	0	0	0	1	1	LED143	LED142	LED141	LED140	LED139	LED138	LED137	LED136

In the intensity register (see Figure 32) the brightness of every single LED can be set via a 8bit PWM (255 steps).