



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# AS1120

## 46-Segment LCD Driver

### 1 General Description

The AS1120 is an LCD direct-driver capable of driving up to 46 LCD segments with one non-multiplexed backplane.

The device contains an integrated serial-to-parallel interface and generates the necessary signals to drive LCD panels.

Internal synchronous backplane signal regeneration allows the device to mix different drivers with different LCDs for superior brightness stability over a wide temperature range. The device also supports external backplane signals.

The AS1120 was specifically designed to easily interface with a variety of microprocessors and a wide range of LCD panel types.

The AS1120 is available in a 64-pin LQFP package.

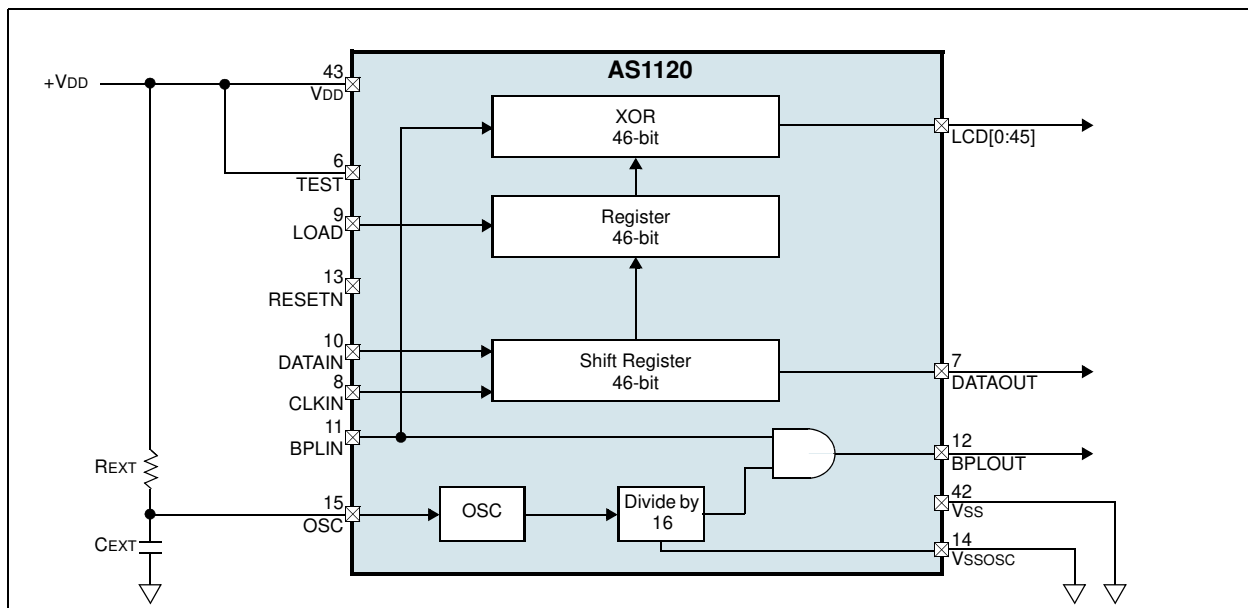
### 2 Key Features

- 46-Segment LCD Driver
- Serial-to-Parallel Interface
- Integrated Oscillator w/ External R/C and Backplane Input
- Supports Alphanumeric and Bar-Graph Devices
- Two Data Transfer Configurations:
  - Cascade
  - Parallel
- Non-Multiplexed Backplane
- Very-Low Current Consumption
- Power Supply Range: -0.3 to +7.0V
- Operating Temperature Range: -40 to +85°C
- 64-pin LQFP Package

### 3 Applications

The device is ideal for industrial LCD systems, portable-system displays, panel meters with wide temperature ranges, high-performance optical displays, or for any other space-limited A/D application with low power-consumption and single-supply requirements.

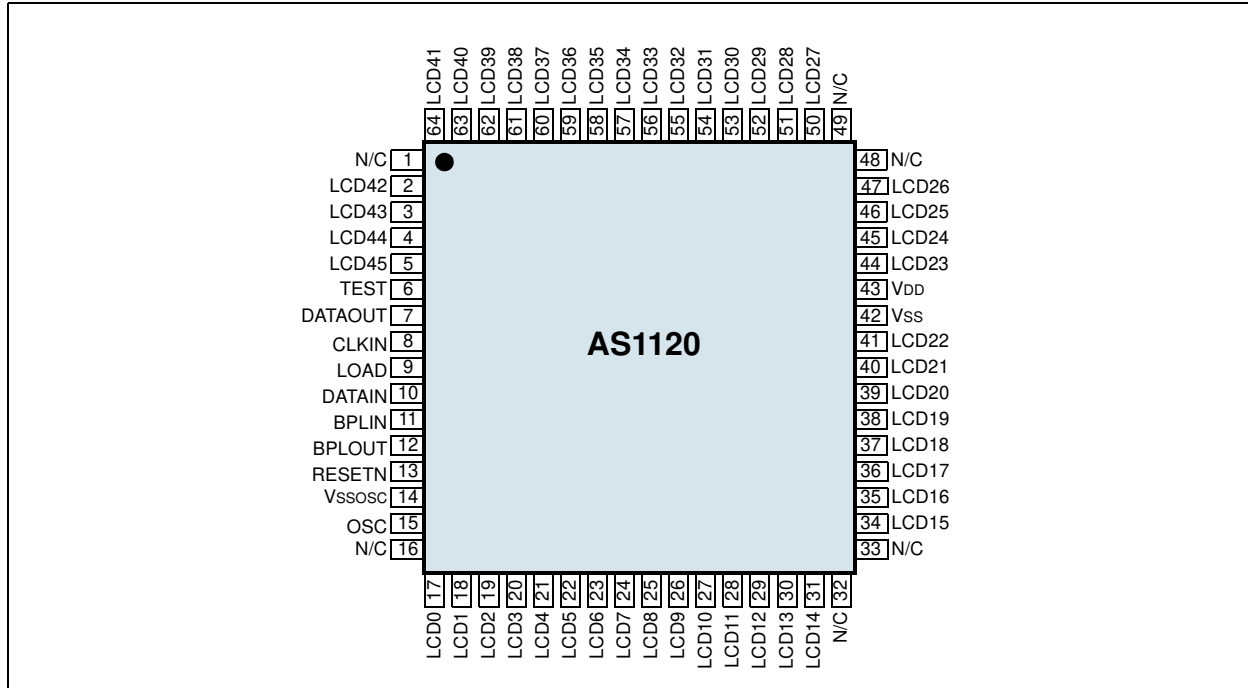
Figure 1. AS1120 - Application Diagram



## 4 Pinout and Packaging

### Pin Assignments and Markings

Figure 2. Pin Assignments (Top View) and Markings



### Pin Descriptions

Table 1. Pin Descriptions

| Pin Number            | Pin Name    | Description   |
|-----------------------|-------------|---|
| 1, 16, 32, 33, 48, 49 | N/C         | Not Connected   |
| 2:5                   | LCD42:LCD45 | LCD Output Segments 42:45   |
| 6                     | TEST        | Test pin. This pin must be tied to pin VDD.   |
| 7                     | DATAOUT     | Serial Data Output  |
| 8                     | CLKIN       | Shift Register Clock  |
| 9                     | LOAD        | Load Strobe from Shift Register to Latch  |
| 10                    | DATAIN      | Serial Data Input   |
| 11                    | BPLIN       | Backplane Input   |
| 12                    | BPLOUT      | Backplane Output  |
| 13                    | RESETN      | Active-Low Asynchronous Reset   |
| 14                    | Vssosc      | Internal Oscillator Power Ground  |
| 15                    | OSC         | Oscillator Pad.<br>a). Internal clock (see page 8)<br>b) External clock; tied to VSSOSC |
| 17:31                 | LCD0:LCD14  | LCD Output Segments 0:14  |
| 34:41                 | LCD15:LCD22 | LCD Output Segments 15:22   |
| 42                    | Vss         | Power Ground  |
| 43                    | VDD         | Positive Power Supply   |
| 44:47                 | LCD23:LCD26 | LCD Output Segments 23:26   |
| 50:64                 | LCD27:LCD41 | LCD Output Segments 27:41   |

## 5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

| Symbol                             | Parameter  | Min  | Max             | Unit | Comments  |
|------------------------------------|--|------|-----------------|------|---|
| V <sub>DD</sub>                    | Positive Supply Voltage to Ground  | -0.3 | +7.0            | V    |   |
| V <sub>IN</sub> , V <sub>OUT</sub> | Digital Input and Output Voltage to Ground   | 0    | V <sub>DD</sub> | V    |   |
| I <sub>SCR</sub>                   | Input Current (Latchup Immunity)   | -200 | +200            | mA   | Norm: JEDEC 17  |
| T <sub>JMAX</sub>                  | Maximum Junction Temperature   |      | +150            | °C   |   |
| T <sub>STRG</sub>                  | Storage Temperature  | -65  | +150            | °C   |   |
| P <sub>t</sub>                     | Package Power Dissipation<br>(T <sub>JMAX</sub> - T <sub>AMB</sub> )/R <sub>TH</sub> |      | 760             | mW   | Package related   |
| ESD                                | Electrostatic Discharge  |      | 1000            | V    | HBM Mil-Std883E 3015.7 methods  |
|                                    | Humidity (Non-Condensing)  | 5    | 85              | %    |   |
|                                    | Package Body Temperature   |      | +260            | °C   | The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices" |



## 6 Electrical Characteristics

Table 3. Electrical Characteristics

| Symbol   | Parameter                                 | Conditions   | Min                   | Max                   | Unit |
|--|---|--|-----------------------|-----------------------|------|
| V <sub>DD</sub>  | Positive Supply Voltage                   |  | +3.0                  | +5.5                  | V    |
| T <sub>AMB</sub>   | Ambient Temperature                       | Verify that the LCD is compatible with the desired temperature range   | -40                   | 85                    | °C   |
| I <sub>DD</sub>  | Supply Current                            | f <sub>BPL</sub> = 50Hz, output not connected, T <sub>AMB</sub> = 25°C | 5                     |                       | μA   |
| f <sub>OSC</sub>   | Oscillator Frequency                      | Bpfreq = f <sub>osc</sub> /16  | 0.5                   | 100                   | kHz  |
| C <sub>SEG</sub>   | Segment Capacitance                       |  |                       | 300                   | pF   |
| C <sub>BP</sub>  | Backplane Capacitance                     |  |                       | 50                    | nF   |
| <b>CMOS Input Pin: TEST</b> (V <sub>DD</sub> = 5V, T <sub>AMB</sub> = -40 to +85 °C unless otherwise noted).   |   |  |                       |                       |      |
| V <sub>IH</sub>  | High Level Input Voltage                  |  | 0.7 x V <sub>DD</sub> |                       | V    |
| V <sub>IL</sub>  | Low Level Input Voltage                   |  |                       | 0.2 x V <sub>DD</sub> | V    |
| I <sub>LEAK</sub>  | Input Leakage Current                     |  |                       | ±1                    | μA   |
| t <sub>T</sub>   | Input Transition Time                     |  |                       | 10                    | ns   |
| <b>CMOS Input with Schmitt Trigger, Pin: CLKIN, LOAD, DATAIN, BPLIN, RESETN</b> (V <sub>DD</sub> = 5V, T <sub>AMB</sub> = -40 to +85 °C unless otherwise noted). |   |  |                       |                       |      |
| V <sub>TH+</sub>   | Positive-Going Threshold                  | V <sub>DD</sub> = 4.5V   | 2.8                   | 3.2                   | V    |
|  |   | V <sub>DD</sub> = 5.5V   | 3.4                   | 3.9                   |      |
| V <sub>TL-</sub>   | Negative-Going Threshold                  | V <sub>DD</sub> = 4.5V   | 1.1                   | 1.6                   | V    |
|  |   | V <sub>DD</sub> = 5.5V   | 1.4                   | 1.9                   |      |
| I <sub>LEAK</sub>  | Input Leakage Current                     |  |                       | ±1                    | μA   |
| <b>CMOS Output Pins: BPLOUT, DATAOUT</b> (V <sub>DD</sub> = 5V, T <sub>AMB</sub> = -40 to +85 °C unless otherwise noted).  |   |  |                       |                       |      |
| V <sub>OH</sub>  | High Level Input Voltage                  | V <sub>DD</sub> = 5V, I <sub>OH</sub> = -4mA                           | 4.0                   |                       | V    |
|  |   | V <sub>DD</sub> = 3.3V, I <sub>OH</sub> = -2.8mA                       | 2.5                   |                       |      |
| V <sub>OL</sub>  | Low Level Input Voltage                   | V <sub>DD</sub> = 5V, I <sub>OL</sub> = 4mA                            |                       | 0.4                   | V    |
|  |   | V <sub>DD</sub> = 3.3V, I <sub>OL</sub> = 3.2mA                        |                       | 0.4                   |      |
| <b>CMOS Output Pin: LCDxx</b> (V <sub>DD</sub> = 5V, T <sub>AMB</sub> = -40 to +85 °C unless otherwise noted).   |   |  |                       |                       |      |
| V <sub>OH</sub>  | High Level Input Voltage                  | V <sub>DD</sub> = 5V, I <sub>OH</sub> = -25μA                          | 4.0                   |                       | V    |
|  |   | V <sub>DD</sub> = 3.3V, I <sub>OH</sub> = -16μA                        | 2.5                   |                       |      |
| V <sub>OL</sub>  | Low Level Input Voltage                   | V <sub>DD</sub> = 5V, I <sub>OL</sub> = 22μA                           |                       | 0.4                   | V    |
|  |   | V <sub>DD</sub> = 3.3V, I <sub>OL</sub> = 17μA                         |                       | 0.4                   |      |
| <b>Oscillator Pin: OSC</b> (V <sub>DD</sub> = 5V, T <sub>AMB</sub> = -40 to +85 °C unless otherwise noted).  |   |  |                       |                       |      |
| V <sub>OL</sub>  | Low Level Output Voltage (open collector) | V <sub>DD</sub> = 5V, I <sub>OL</sub> = 4mA                            |                       | 0.4                   | V    |
| R <sub>EXT</sub>   | External Resistance                       |  | 47                    |                       | kΩ   |
| C <sub>EXT</sub>   | External Capacitance                      |  | 0.3                   | 1                     | nF   |
| f <sub>OSC</sub>   | Frequency                                 | 1/f <sub>OSC</sub> = 0.69 x R <sub>EXT</sub> x C <sub>EXT</sub>        | 0.5                   | 100                   | kHz  |

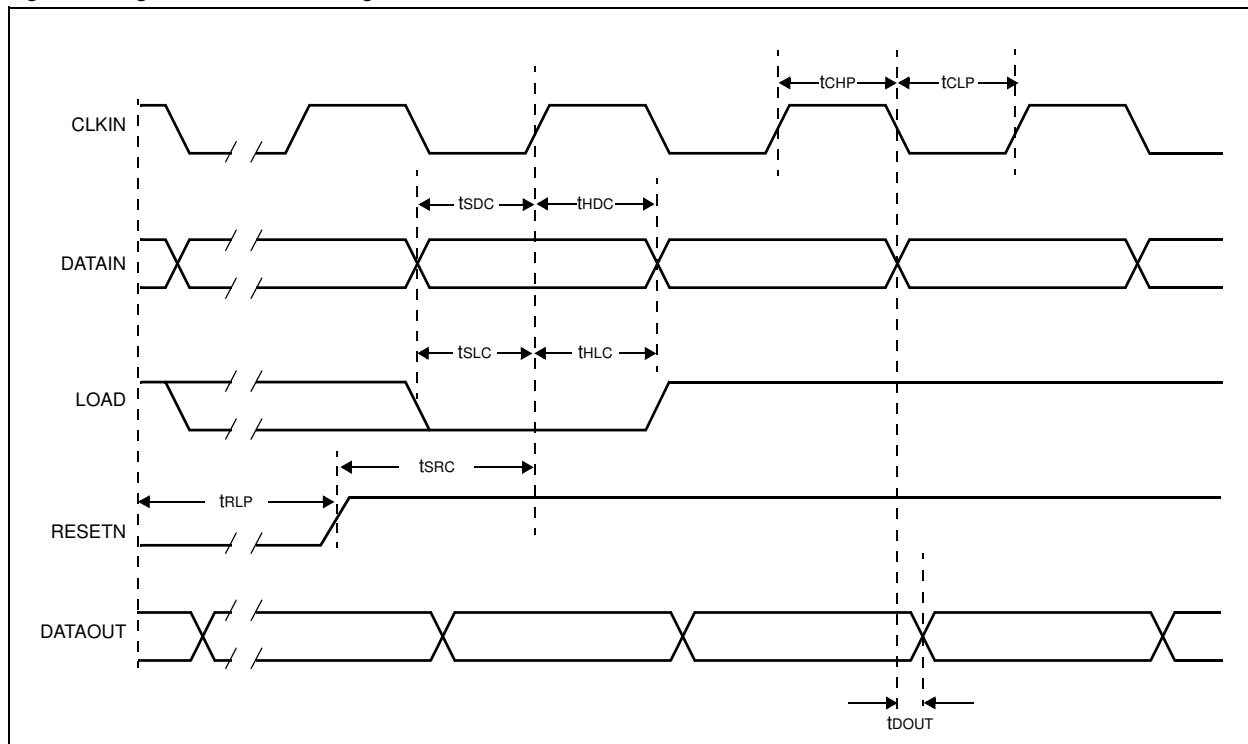
Table 4. Timing Characteristics

| Symbol | Parameter   | Min   | Max | Unit |
|--------|---|-------|-----|------|
| tCHP   | Time CLKIN high pulse   | 50    |     | ns   |
| tCLP   | Time CLKIN low pulse  | 50    |     | ns   |
| tSDC   | Time setup DATAIN to CLKIN rising edge                            | 30    |     | ns   |
| tHDC   | Time hold DATAIN from CLKIN rising edge                           | 30    |     | ns   |
| tSLC   | Time setup LOAD to CLKIN rising edge (active low) <sup>1, 2</sup> | 30    |     | ns   |
| tHLC   | Time hold LOAD to CLKIN rising edge (active low) <sup>1, 2</sup>  | 30    |     | ns   |
| trLP   | Time RESETN low pulse (active low)                                | 20000 |     | ns   |
| tsRC   | Time setup RESETN to CLKIN rising edge                            | 30    |     | ns   |
| tDOUT  | Time from CLKIN falling edge to DATAOUT                           |       | 10  | ns   |

1. LOAD must be high while RESETN is active (low).
2. LOAD can stay low for more than one CLKIN cycle.

**Note:** All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 3. Signal Waveform Timing



## 7 Detailed Description

The AS1120 can drive up to 46 LCD segments and multiple AS1120 devices can be cascaded (see Figure 8 on page 9) to increase the number of LCD segments.

**Note:** Due to the accurate delay balance between the backplane input, backplane output, and the LCD segments, it is possible to mix segments of different display crystal types.

### Shift Register

Data accesses are made serially via pins DATAIN and CLKIN. At each CLKIN rising edge the signal present at DATAIN pin is shifted in the first bit of the internal shift register and the other bits are shifted ahead of the first bit.

To cascade multiple AS1120 devices (see Figure 8 on page 9), the last bit of the internal shift register is presented at pin DATAOUT at the falling edge of the same CLKIN pulse. The LSB is entered first while MSB is the last bit to be shifted into the shift register.

**Note:** The shift register is cleared at when the AS1120 is reset.

### Latch Register and Error

When a signal is applied at pin LOAD, data present in the shift register is latched into the internal latch register and presented to the LCD output segments (LCD[0:45]), also passing through an XOR gate with the backplane signal (BPLIN). The XOR function is necessary to generate the appropriate signals to drive the LCD segments.

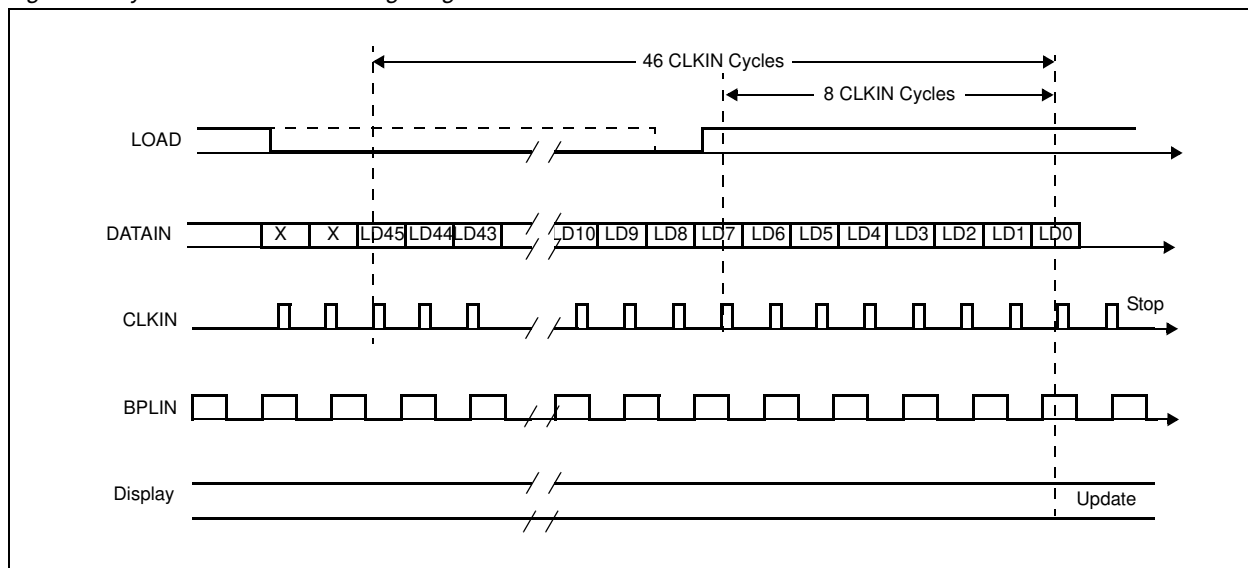
**Note:** At reset the latch register is cleared, thus no LCD segment will be active at power-on.

### Synchronous Mode

Data is shifted into the internal shift register at the rising edge of the CLKIN signal. To load the shift register all 46 data bits are clocked into the register at the rising edge of CLKIN (see Figure 4). The LOAD signal has to be set high for 8 CLKIN periods before the end of the 46 bits. The display will be updated at the 8th CLKIN rising edge after LOAD goes high as is shown in Figure 4.

**Note:** During synchronous mode, a clock on BPLIN must be applied to avoid the risk of damaging the LCD crystal.

Figure 4. Synchronous Mode Timing Diagram

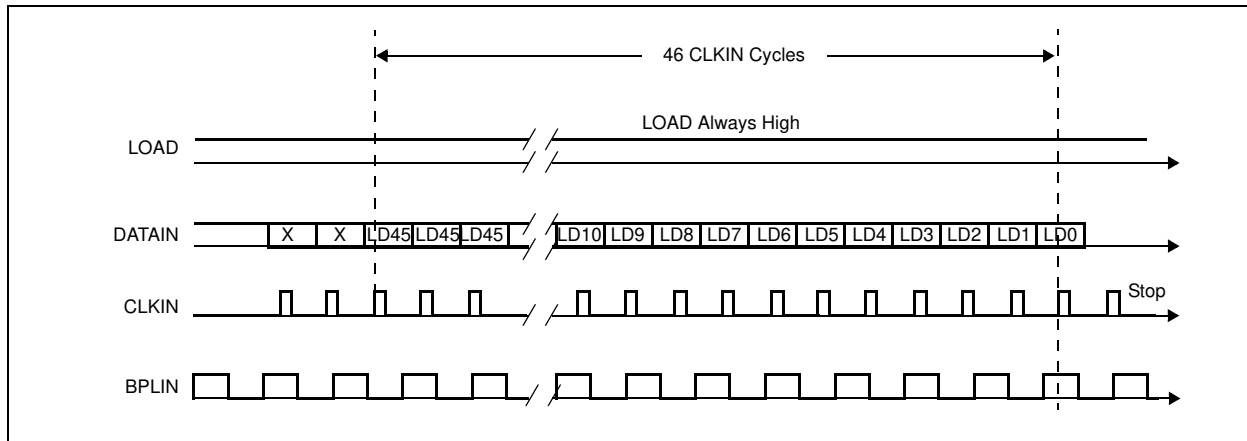


## Asynchronous Mode

Data can be preloaded into the AS1120 shift register and then activated via a LOAD pulse. To preload the shift register the LOAD signal must stay high as all 46 data bits are clocked into the internal shift register at the rising edge of CLKIN (see Figure 5).

**Note:** In asynchronous mode, a clock signal must be applied on pin BPLIN. Asynchronous mode does not support the use of the AS1120 internal clock.

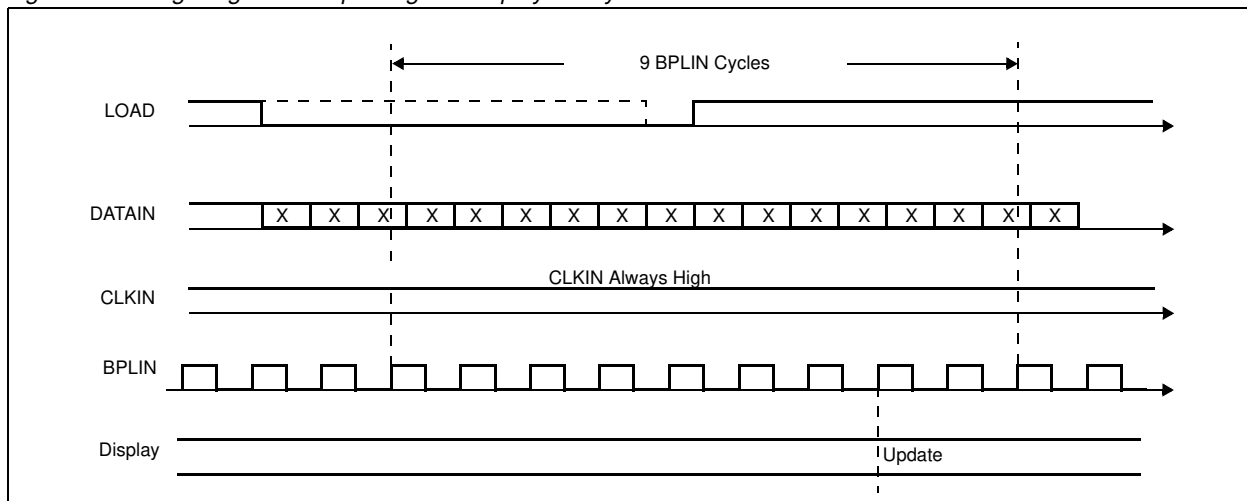
Figure 5. Timing Diagram for Preloading the Shift Register



To update the LCD display the LOAD signal must be held low for at least 8 periods of the clock applied at BPLIN, and CLKIN must be set to low. Note that since BPLIN is normally asynchronous in respect to LOAD, it is advisable to keep LOAD low for 8+1 BPLIN cycles. The display will be updated at the 8th BPLIN rising edge while LOAD is Low.

In case of internal BPLIN generation through the internal oscillator  $BPLIN = f_{osc}/16$ .

Figure 6. Timing Diagram for Updating the Display in Asynchronous Mode



## R/C Oscillator and Backplane Generation

The AS1120 can generate the backplane signal using an internal R/C oscillator, or an externally generated backplane signal can be supplied.

When cascading multiple AS1120 devices (see Figure 8 on page 9), only the first device should have the oscillator running; the other devices must use pin BPLIN to regenerate the backplane signal and to synchronize their LCD output segments with the common backplane.



The selection of internal or external backplane signal (see Table 5) is initiated after RESETN is disabled – the first rising edge at pin OSC after RESETN is disabled will force pin BPLOUT to deliver the internally generated backplane signal. If there is no rising edge at pin OSC, BPLOUT will simply buffer the signal at pin BPLIN.

Table 5. Backplane Source Generation Selection

| Mode     | OSC Pin  | BPLOUT  |
|----------|----------|---------|
| Internal | Running  | fosc/16 |
| External | Tied Low | BPLIN   |

**Note:** The LCD should never be supplied with static signals. Verify that signals at pins BPLIN and BPLOUT are always running while VDD is supplied; note that pin BPLOUT is stopped during a reset.

### Internal Mode – R/C Oscillator Running (Generating the Backplane)

Connect external R/C components to pin OSC as shown in Figure 1 on page 1. When an external REXT and CEXT are connected to pin OSC, a clock signal whose frequency is equal to fosc divided by 16 will be present at pin BPLOUT.

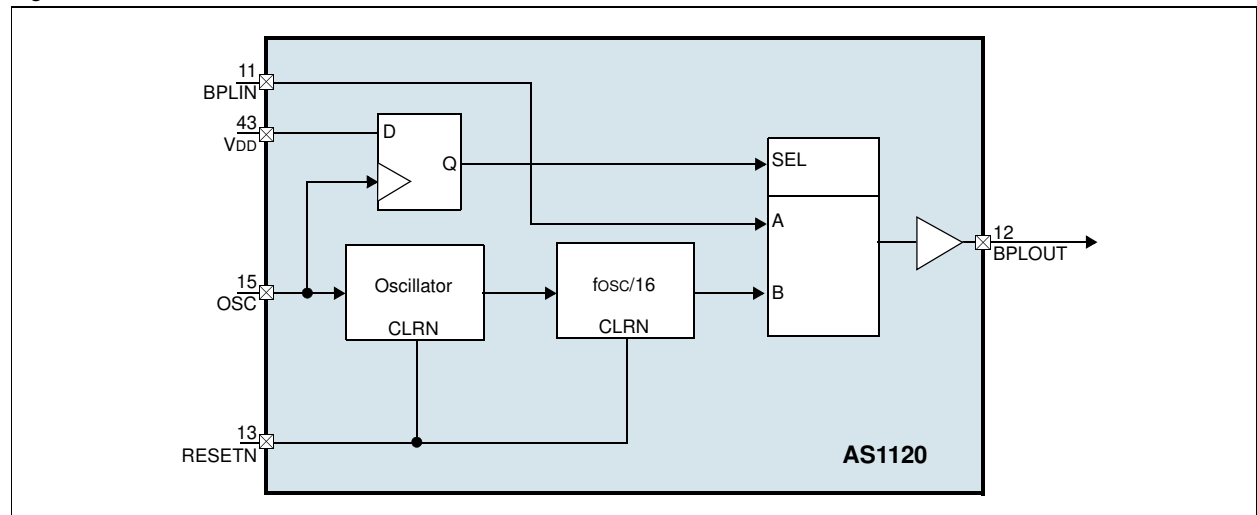
**Note:** Internal mode requires that pin BPLIN be connected to pin BPLOUT.

The oscillation period is approximately  $t_{OSC} = 1/f_{OSC} = 0.69 \times R_{EXT} \times C_{EXT}$ , and the error between the expected frequency and the generated frequency increases as indicated in Table 6.

Table 6. Oscillator Error Rate

| Expected Oscillator Frequency | Error |
|-------------------------------|-------|
| 1 kHz                         | 1%    |
| 10 kHz                        | 5%    |
| 50 kHz                        | 20%   |
| 100 kHz                       | 40%   |

Figure 7. AS1120 Clock Circuit



### External Mode: R/C Oscillator Stopped (External Backplane)

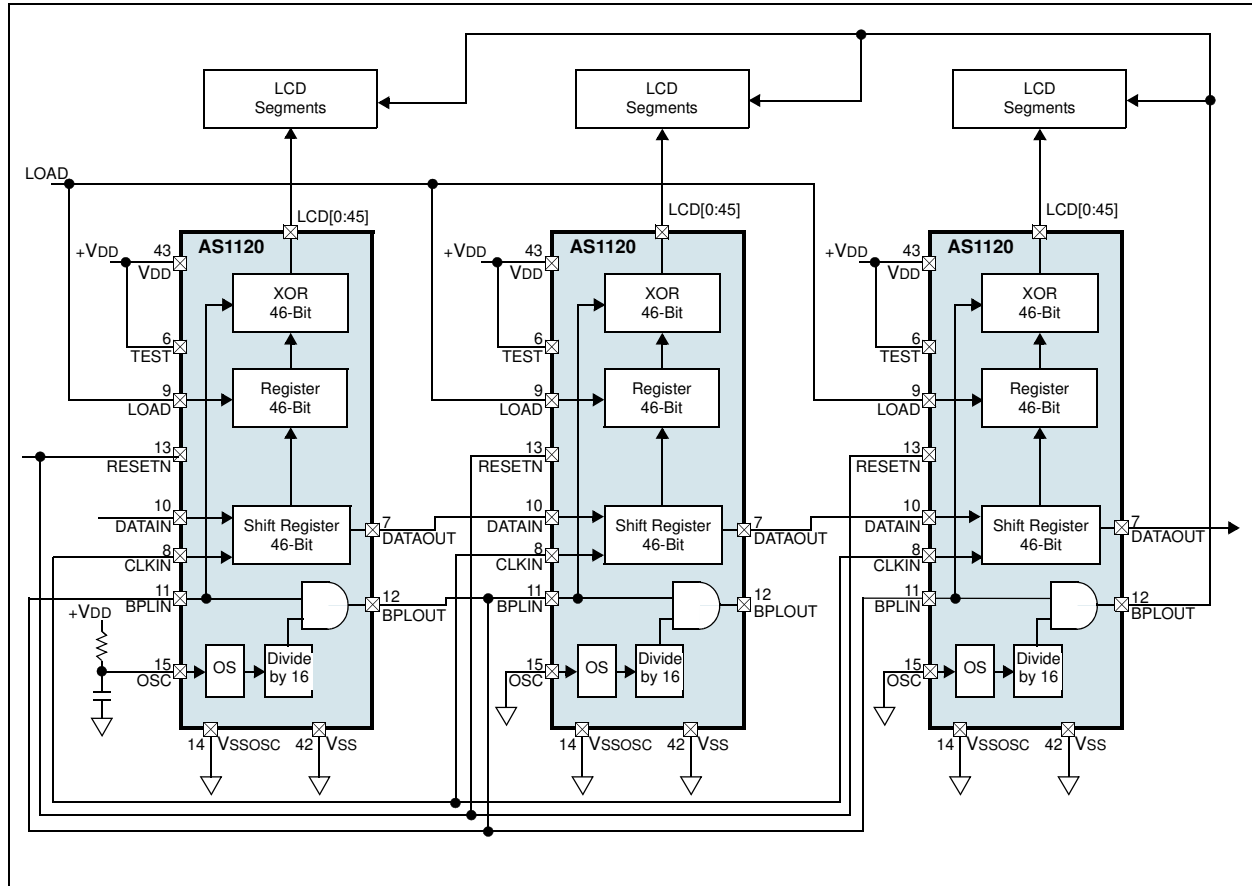
Connect pin OSC to Vss in order to block the internal oscillator. In this external mode, an external backplane signal should be presented at pin BPLIN, which will be regenerated and presented at pin BPLOUT.

## 8 Application Information

The AS1120 can support all types of static LCD displays.

**Note:** For proper display operation, ensure that the LCD can safely operate within the full temperature range of the AS1120 (see page 1).

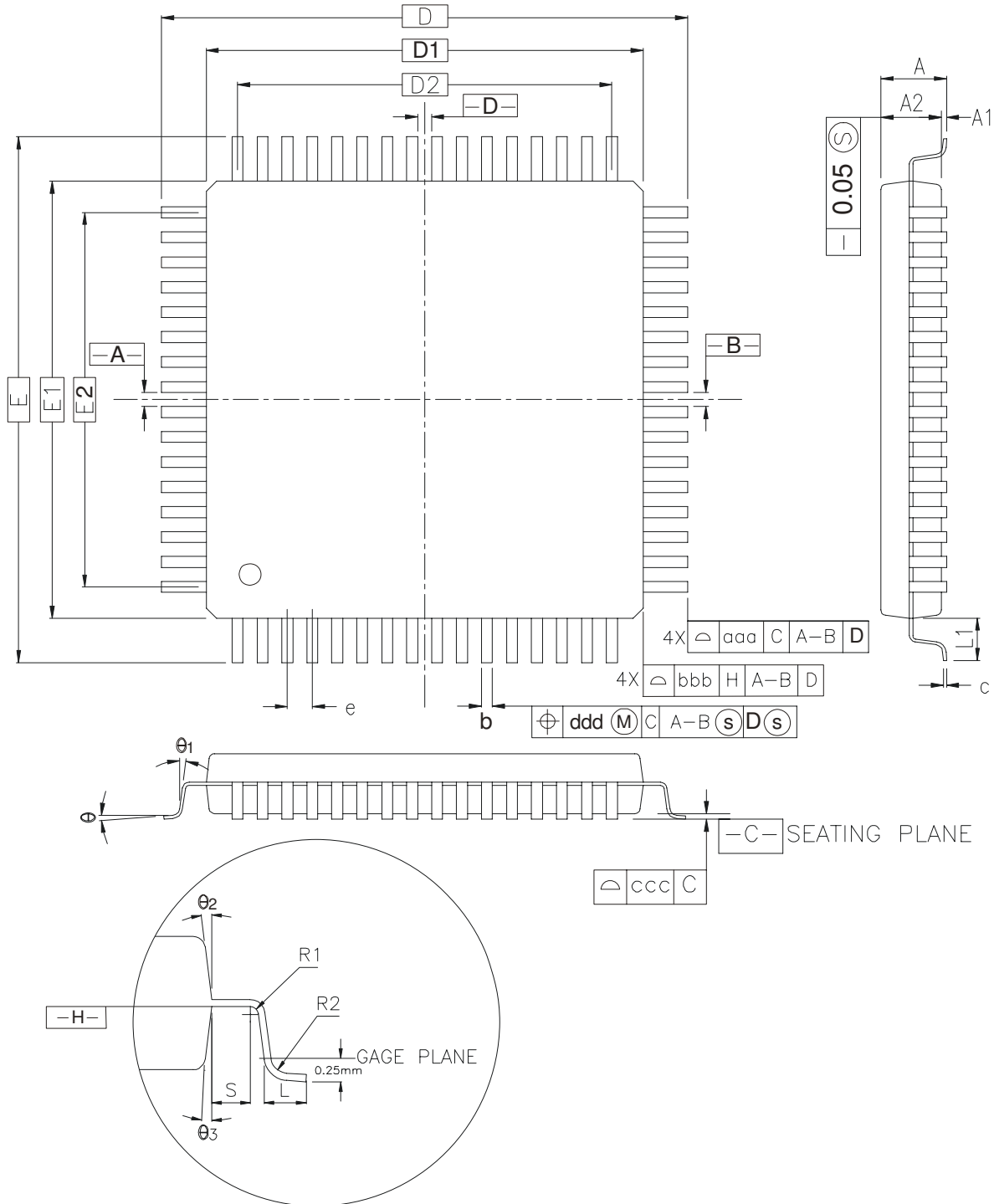
Figure 8. Cascaded Configuration



## Package Drawings and Markings

The devices are available in an 64-pin LQFP package.

Figure 9. 64-pin LQFP Package



## CONTROL DIMENSIONS ARE IN MILLIMETERS

| SYMBOL         | MILLIMETER |      |      |
|----------------|------------|------|------|
|                | MIN.       | NOM. | MAX. |
| A              | —          | —    | 1.60 |
| A1             | 0.05       | —    | 0.15 |
| A2             | 1.35       | 1.40 | 1.45 |
| D              | 16.00 BSC. |      |      |
| D1             | 14.00 BSC. |      |      |
| E              | 16.00 BSC. |      |      |
| E1             | 14.00 BSC. |      |      |
| R <sub>2</sub> | 0.08       | —    | 0.20 |
| R <sub>1</sub> | 0.08       | —    | —    |
| Θ              | 0°         | 3.5° | 7°   |
| Θ <sub>1</sub> | 0°         | —    | —    |
| Θ <sub>2</sub> | 11°        | 12°  | 13°  |
| Θ <sub>3</sub> | 11°        | 12°  | 13°  |
| c              | 0.09       | —    | 0.20 |
| L              | 0.45       | 0.60 | 0.75 |
| L <sub>1</sub> | 1.00 REF   |      |      |
| S              | 0.20       | —    | —    |

| SYMBOL | 64L        |      |      |
|--------|------------|------|------|
|        | MILLIMETER |      |      |
|        | MIN.       | NOM. | MAX. |
| b      | 0.30       | 0.35 | 0.45 |
| e      | 0.80 BSC.  |      |      |
| D2     | 12.00      |      |      |
| E2     | 12.00      |      |      |
| aaa    | 0.20       |      |      |
| bbb    | 0.20       |      |      |
| ccc    | 0.10       |      |      |
| ddd    | 0.20       |      |      |

**Notes:**

1. Top package may be smaller than bottom package by 0.15mm.
2. Datums A-B and -D- to be determined at datum plane -H-.
3. Dimensions D and E are to be determined at seating plane -C-.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.25mm per side. D1 and E1 are body size dimensions including mold mismatch.
5. Detail of pin1 identifier is optional but must be located within the zone indicated.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion is 0.08mm in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
7. Exact shape of each corner is optional.
8. These dimensions apply to the flat section of the lead between 0.10 and 0.25mm from the lead tip.
9. All dimensions are in millimeters.

## 9 Ordering Information

The device is available as the standard product shown in Table 7.

Table 7. Ordering Information

| Ordering Code | Marking | Description           | Delivery Form | Package     |
|---------------|---------|-----------------------|---------------|-------------|
| AS1120        | AS1120  | 46-Segment LCD Driver | Tape and Reel | 64-pin LQFP |

**Note:** All products are RoHS compliant and Pb-free.

Buy our products or get free samples online at ICdirect: <http://www.austriamicrosystems.com/ICdirect>

For further information and requests, please contact us <mailto:sales@austriamicrosystems.com>  
or find your local distributor at <http://www.austriamicrosystems.com/distributor>

## Copyrights

Copyright © 1997-2010, austriamicrosystems AG, Tobelbaderstrasse 30, 8141 Unterpremstaetten, Austria-Europe. Trademarks Registered ®. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

All products and companies mentioned are trademarks or registered trademarks of their respective companies.

## Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.



## Contact Information

Headquarters

austriamicrosystems AG  
Tobelbaderstrasse 30  
A-8141 Unterpremstaetten, Austria

Tel: +43 (0) 3136 500 0  
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

<http://www.austriamicrosystems.com/contact>