Chipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

AS1130

132-LED Cross-Plexing Driver with Scrolling Function

General Description

The AS1130 is a compact LED driver for 132 single LEDs. The devices can be programmed via an I²C compatible interface. The AS1130 offers a 12x11 LED-matrix with 1/12 cycle rate. The required lines to drive all 132 LEDs are reduced to 12 by using the cross-plexing feature optimizing space on the PCB. The whole LED-matrix driving 132 LEDs can be analog dimmed from 0mA to 30mA in 256 steps (8 bit).

Additionally each of the 132 LEDs can be dimmed individually with 8-bit allowing 256 steps of linear dimming. To reduce CPU usage up to 6 frames can be stored with individual time delays between frames to play small animations automatically.

The AS1130 operates from 2.7V to 5.5V and features a very low shutdown and operational current.

The device offers a programmable IRQ pin. Via a register it can be set on what event (CP_Request, Interface Timeout, Error-detection, POR, End of Frame or End of Movie) the IRQ is triggered.

Also hardware scroll function is implemented in the AS1130.

The device is available in an ultrasmall 20-Pin WL-CSP and an easy to solder 28-pin SSOP/TSSOP package.

Ordering Information and *Content Guide* appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS1130, 132-LED Cross-Plexing Driver with Scrolling Function are listed below:

Figure 1:
Added Value of Using AS1130

Benefits	Features
• Worlds lowest PCB real estate vs LED count	• Up to 132 LEDs in a 12x11 matrix
• 16.7M full color matrix with white balance	• 8-bit PWM per LED and current control per line
• Reduces MCU load and increases battery lifetime	• 36 frames of memory with scrolling option
• Identifies defect LEDs and "removes" them from the matrix	• Error detection and correction

Applications

The AS1130 is ideal for dot matrix displays in mobile phones, personal electronics and toys.
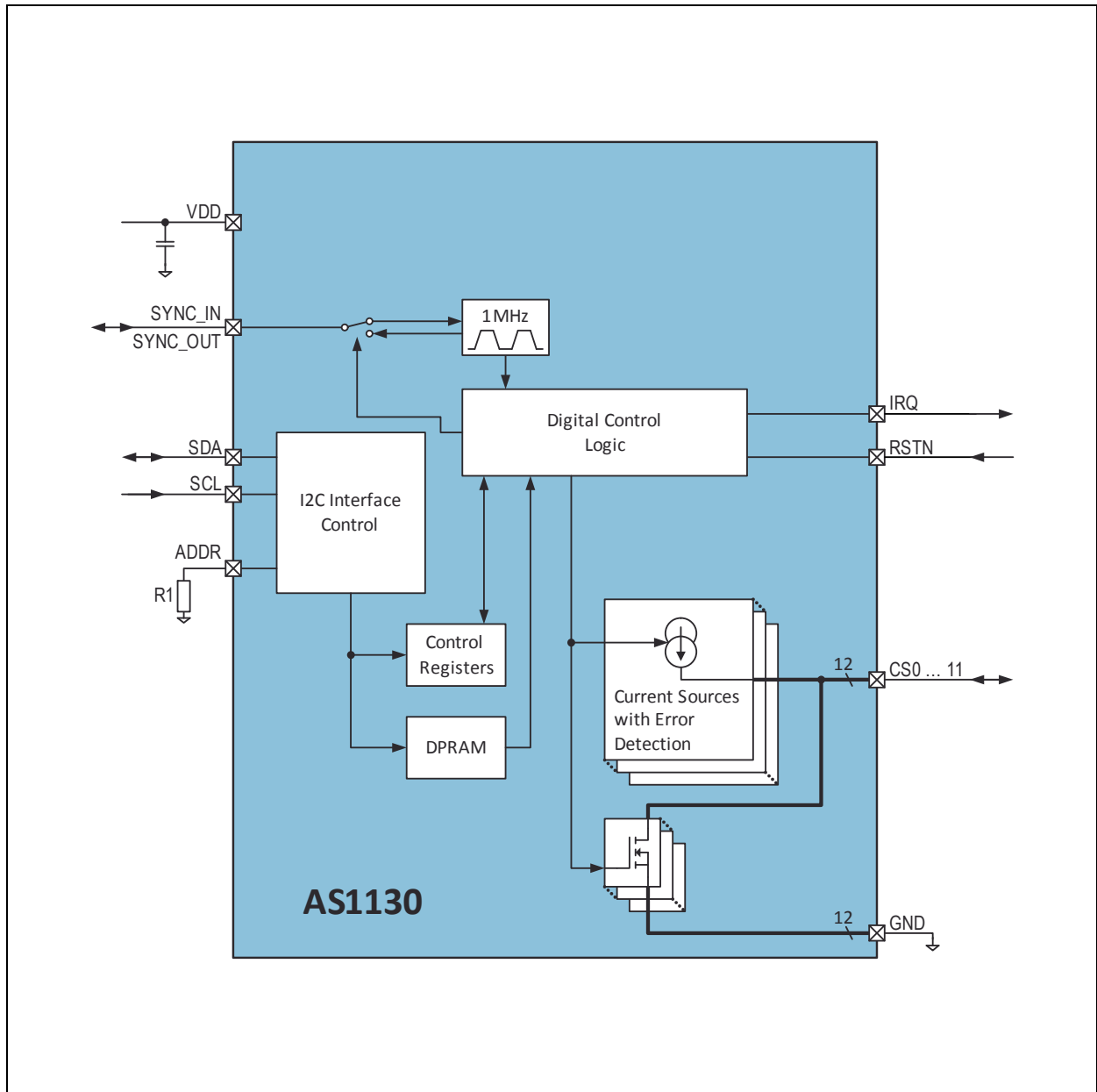
Figure 2:
AS1130- Typical Application Diagram
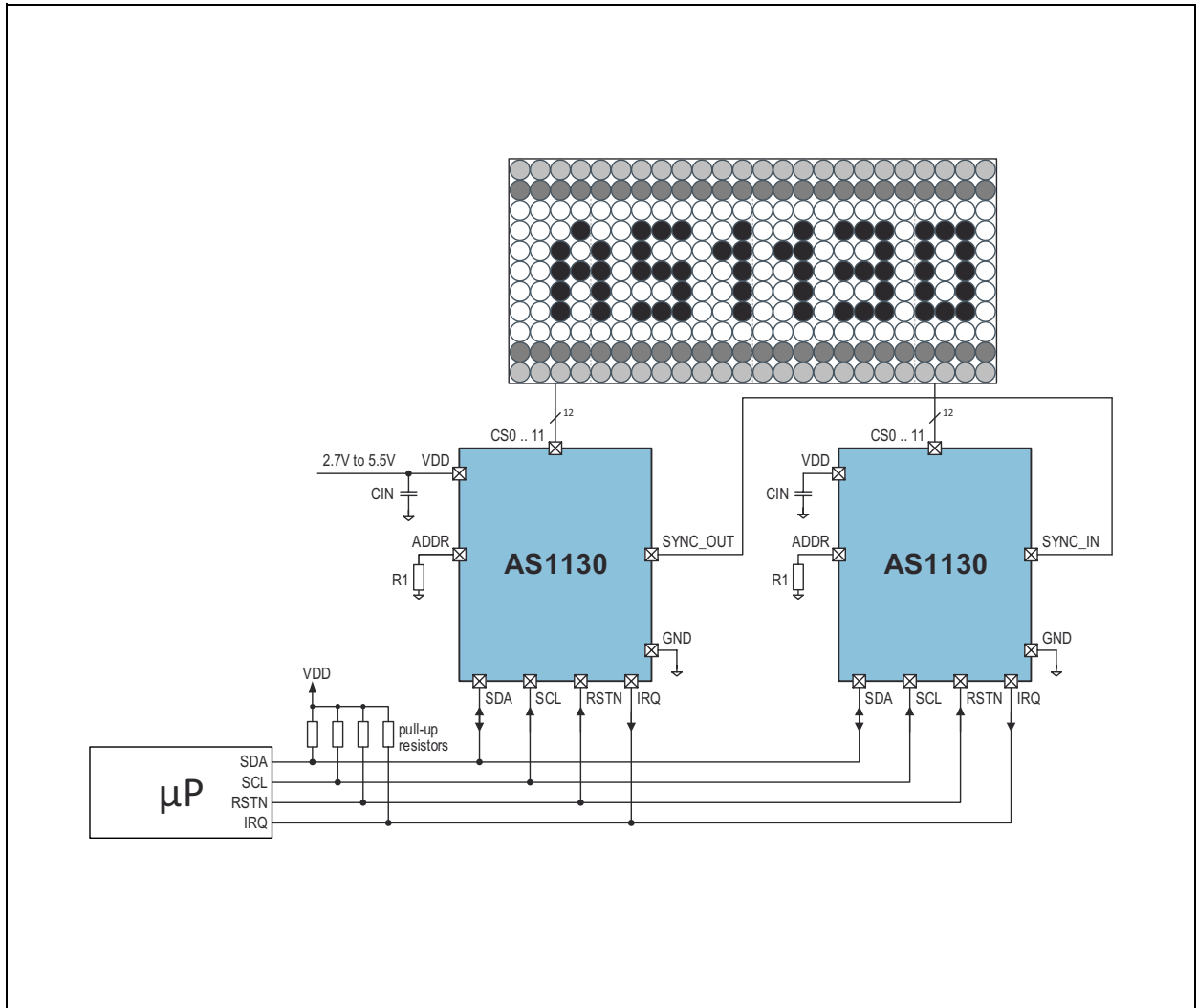
Block Diagram

The functional blocks of this device are shown below:

Figure 3:
AS1130 Block Diagram
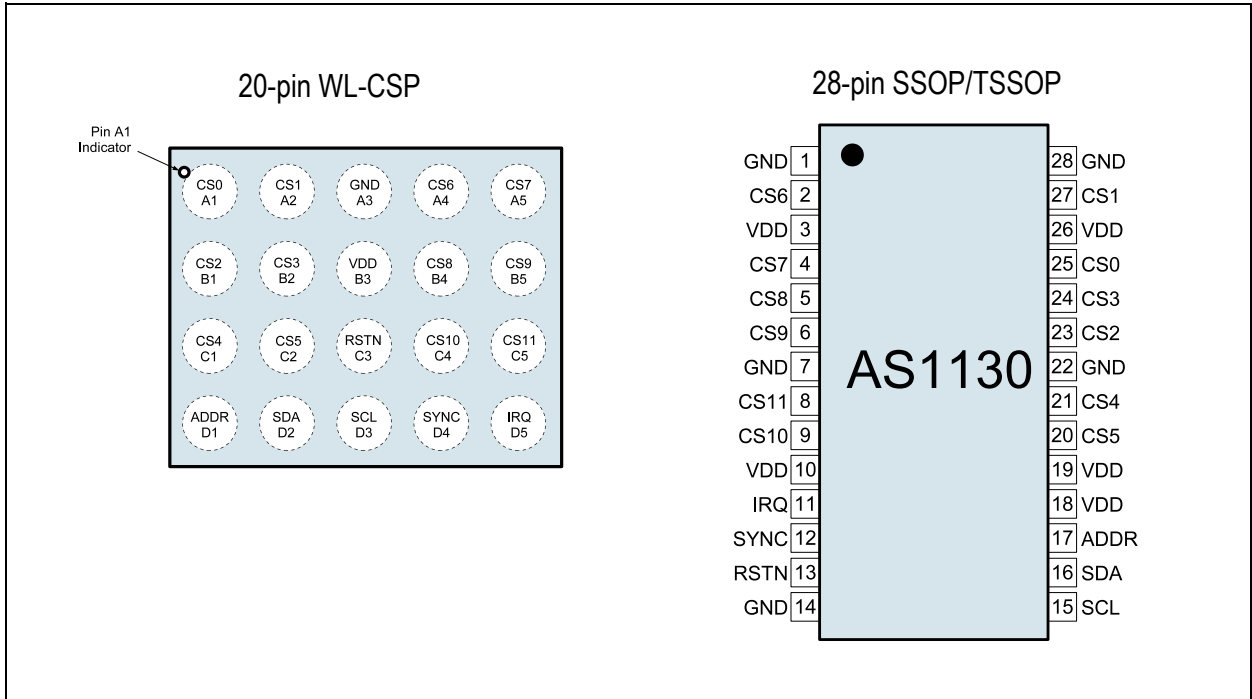
Pin Assignment

Figure 4:
Pin Diagram (Top View)

Figure 5:
Pin Description

Pin Number		Pin Name	Description
20-Pin WL-CSP	**28-Pin SSOP / TSSOP**		
A3	1, 7, 14, 22, 28	GND	**Ground**
C3	13	RSTN	**Reset Input**. Pull this pin to logic low to reset all control registers (set to default values). For normal operation pull this pin to VDD.
D1	17	ADDR	**I²C Address.** Connect to external resistor for I²C address selection. Up to 8 devices can be connected on one bus. See Figure 30
D2	16	SDA	**Serial-Data I/O**. Open drain digital I/O I²C data pin.
D3	15	SCL	**Serial-Clock Input**

Pin Number		Pin Name	Description
20-Pin WL-CSP	**28-Pin SSOP / TSSOP**		
B3	3, 10, 18, 19, 26	VDD	**Positive Supply Voltage**. Connect to a +2.7V to +5.5V supply. Bypass this pin with 10µF capacitance to GND.
D4	12	SYNC	**Synchronization Clock Input or Output.** The SYNC frequency for Input and Output is 1MHz. For SYNC_OUT the frequency can be reduced to 32kHz.
D5	11	IRQ	**Interrupt Request.** Programmable Open drain digital Output. It can be set via an register after which event (Interface Timeout, POR, CP_ Request, Error Detection, End of Frame or End of Movie) the pin triggers an Interrupt Request.
A1, A2, A4, A5, B1, B2, B4, B5, C1, C2, C4, C5	25, 27, 2, 4, 23, 24, 5, 6, 21, 20, 9, 8	CS0, CS1, CS6, CS7, CS2, CS3, CS8, CS9, CS4, CS5, CS10, CS11	**Sinks and Sources** for 132 LEDs.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments	
Electrical Parameters					
V_{DD} to GND	-0.3	7	V		
All other pins to GND	-0.3	7 or V_{DD} + 0.3	V		
Sink Current		500	mA		
Segment Current		100	mA		
Input Current (latch-up immunity)	-100	100	mA	JEDEC 78	
Electrostatic Discharge					
Electrostatic Discharge (human body model)		±2	kV	MIL 883 E method 3015	
Temperature Ranges and Storage Conditions					
Junction Temperature		150	ºC		
Storage Temperature Range	-55	125	ºC	For 20-Pin WL-CSP	
	-55	150	ºC	For 28-pin SSOP/TSSOP	
Package Body Temperature		260	ºC	28-pin SSOP/ TSSOP	IPC/JEDEC J-STD-020[1]The lead finish for Pb-free leaded packages is matte tin (100% Sn).
				20-Pin WL-CSP	IPC/JEDEC J-STD-020[1]
Relative Humidity (non-condensing)	5	85	%		
Moisture Sensitivity Level		1		20-Pin WL-CSP	Represents an unlimited floor life time
		3		28-pin SSOP/ TSSOP	Represents a max. floor life time of 168h

Note(s):

1. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices".

Electrical Characteristics

V_{DD} = 2.7V to 5.5V, typ. values are at T_{AMB} = 25ºC (unless otherwise specified). All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 7:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{AMB}	Operating Temperature Range		-40		85	°C
T_J	Operating Junction Temperature Range		-40		125	°C
V_{DD}	Operating Supply Voltage		2.7		5.5	V
I_{DD}	Operating Supply Current	All current sources turned ON, @ V_{DD} = 5.5V		340		mA
		All current sources turned OFF, @ V_{DD} = 5.5V		0.5		
I_{DDSSD}	Software Shutdown Supply Current	All digital inputs at V_{DD} or GND @ V_{DD} = 5.5V		7	15	µA
I_{DDFSD}	Full Shutdown Supply Current	Pin RSTN = 0V, T_{AMB} = 25ºC		0.1	1	µA
I_{DIGIT}	Digit Drive Sink Current (drive capability of all sources of one digit[1])				360	mA
I_{SEG}	Segment Drive Source Current LED[2]	V_{OUT} = 1.8V to V_{DD}-400mV	28	30	32	mA
ΔI_{SEG}	Segment Drive Current Matching LED			1		%
	Device to Device Current Matching LED	V_{OUT} = 1.8V, V_{DD} = 3.3V		1		%
I_{LEAK}	Leakage Output Current	All current sources OFF, V_{OUT} = 0V, V_{DD} = 5.5V, T_{AMB} = 25ºC		0.005	0.5	µA
ΔI_{LNR}	Line Regulation	V_{OUT} = 1.8V		0.25		%/V
ΔI_{LDR}	Load Regulation	V_{OUT} = 1.8V to V_{DD}-400mV		0.25		%/V
V_{DSSAT}	Saturation Voltage	Current = 30mA, V_{DD} = 3.3V		200		mV
$R_{DSON(N)}$	Resistance for NMOS			0.3	1	W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Open Detection Level Threshold		V_{DD}-0.4	V_{DD}-0.1		V
	Short Detection Level Threshold			770	900	mV
f_{OSC}	Oscillator Frequency		0.9	1	1.1	MHz
$f_{REFRESH}$	Display Scan Rate	12x11 matrix	0.29	0.33	0.36	kHz
t_{RSTN}	Reset Pulse Width Low		500			ns

Note(s):

1. Guaranteed by design.

2. $I_{SEG} = \dfrac{I_{max} - I_{min}}{I_{max} + I_{min}} \times 100$

Figure 8:
Logic Inputs/Outputs Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}, I_{IL}	Logic Input Current	V_{IN} = 0V or V_{DD}	-1		1	µA
V_{IH}	CMOS Logic High Input Voltage		0.7 x V_{DD}			V
V_{IL}	CMOS Logic Low Input Voltage				0.3 x V_{DD}	V
ΔV_I	CMOS Hysteresis Voltage			0.3		V
V_{IH}	Mobile Logic High Input Voltage [1]		1.6			V
V_{IL}	Mobile Logic Low Input Voltage [1]				0.6	V
ΔV_I	Hysteresis Voltage [1]			0.1		V
$V_{OL(SDA)}$	SDA Output Low Voltage	I_{SINK} = 3mA			0.4	V
$V_{OL(IRQ)}$	IRQ Output Low Voltage	I_{SINK} = 3mA			0.4	V
$V_{OL(SYNC\_OUT)}$	Sync Clock Output Low Voltage	I_{SINK} = 1mA			0.4	V
$V_{OH(SYNC\_OUT)}$	Sync Clock Output High Voltage	I_{SOURCE} = 1mA			V_{DD}-0.4	V
	Capacitive Load for Each Bus Line				400	pF

Note(s):

1. Available on request, see Ordering & Contact Information.

Figure 9:
I²C Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL Frequency		100		1000	kHz
t_{BUF}	Bus Free Time Between STOP and START Conditions		1.3			µs
$t_{HOLDSTART}$	Hold Time for Repeated START Condition		260			ns
t_{LOW}	SCL Low Period		500			ns
t_{HIGH}	SCL High Period		260			ns
$t_{SETUPSTART}$	Setup Time for Repeated START Condition		260			ns
$t_{SETUPDATA}$	Data Setup Time		100			ns
$t_{RISE(SCL)}$	SCL Rise Time				120	ns
$t_{RISE(SCL1)}$	SCL Rise Time after Repeated START Condition and After an ACK Bit				120	ns
$t_{FALL(SCL)}$	SCL Fall Time				120	ns
$t_{RISE(SDA)}$	SDA Rise Time				120	ns
$t_{FALL(SDA)}$	SDA Fall Time				120	ns
$t_{SETUPSTOP}$	STOP Condition Setup Time		260			ns
$t_{SPIKESUP}$	Pulse Width of Spike Suppressed				6	ns

Note(s):

1. The Min / Max values of the Timing Characteristics are guaranteed by design.

Figure 10:
Timing Diagram
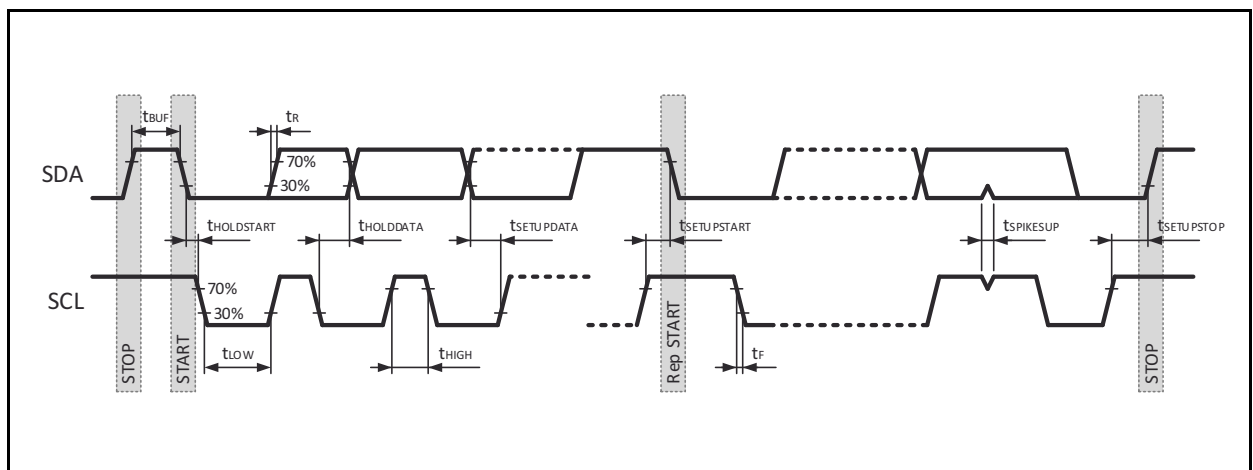
Typical Operating Characteristics
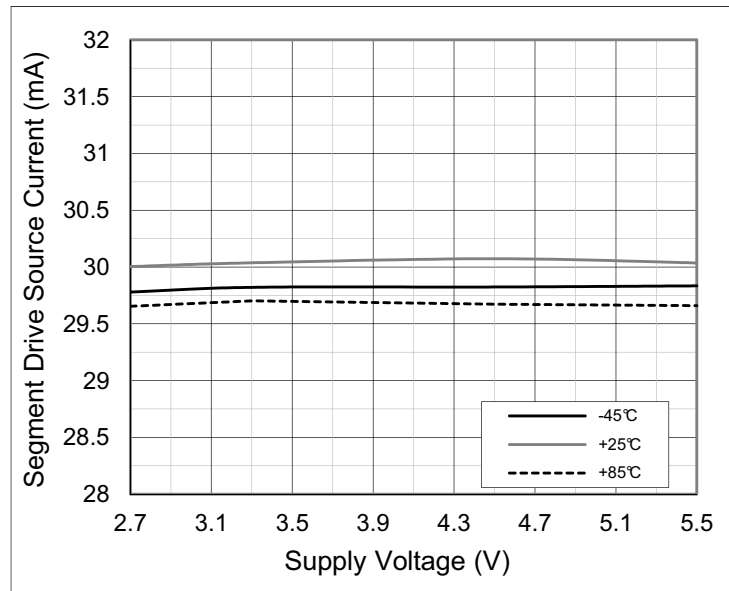
Figure 11:
Segment Drive Current vs. Supply Voltage

Figure 12:
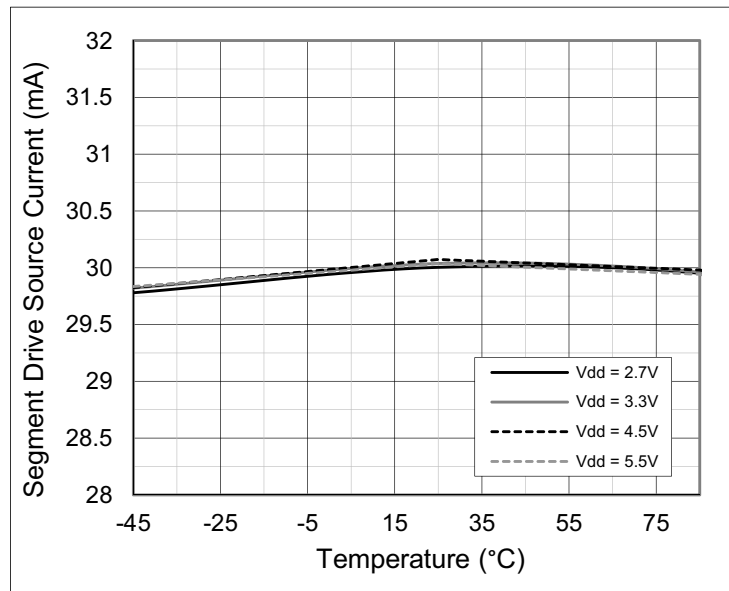**Segment Drive Current vs. Temperature**

Figure 13:
Segment Drive Current vs. Output Voltage

Figure 14:
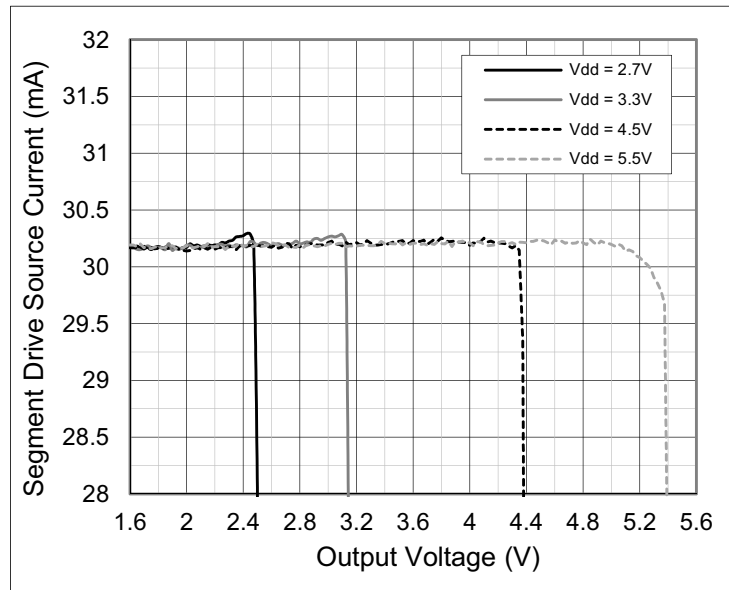**R_{ONNMOS} vs. Supply Voltage**

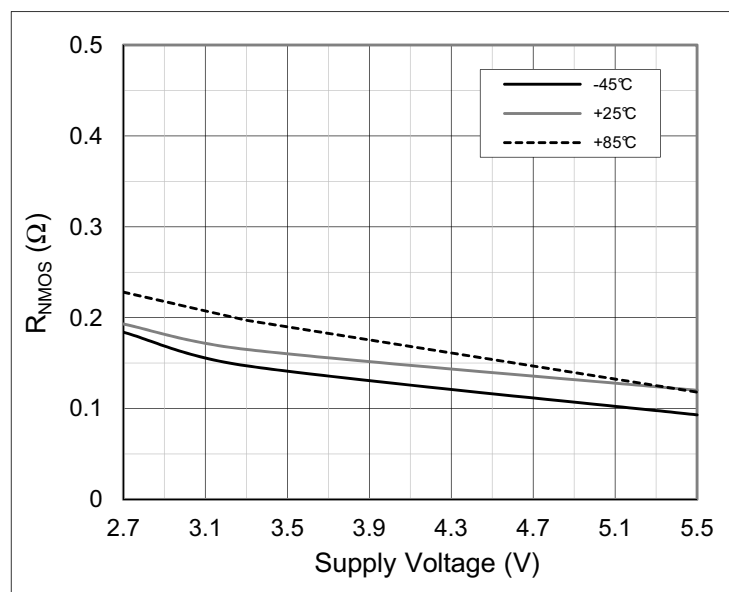R_{ONNMOS} vs. Supply Voltage

Figure 15:
Open Detection Level vs. Supply Voltage
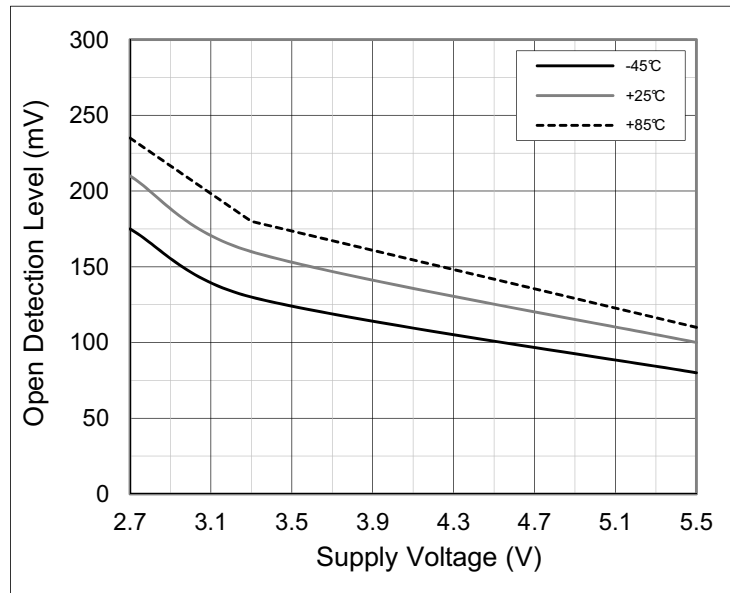

Figure 16:
Short Detection Level vs. Supply Voltage
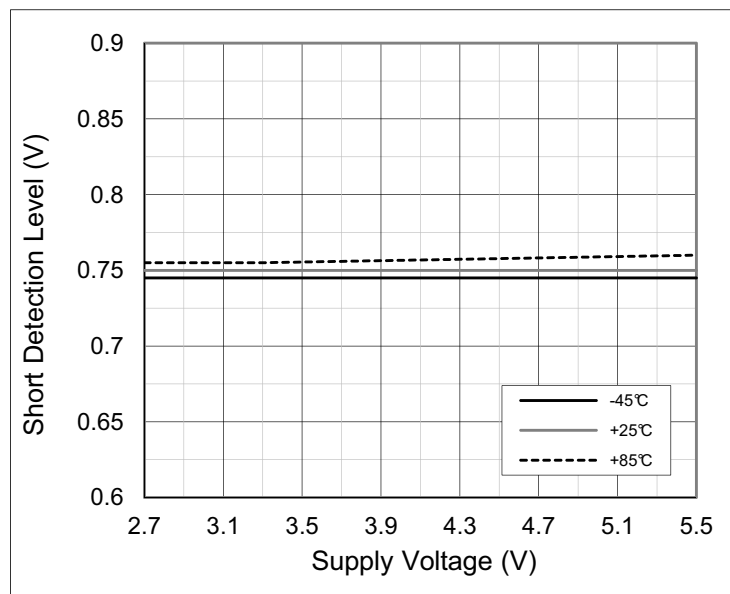
Figure 17:
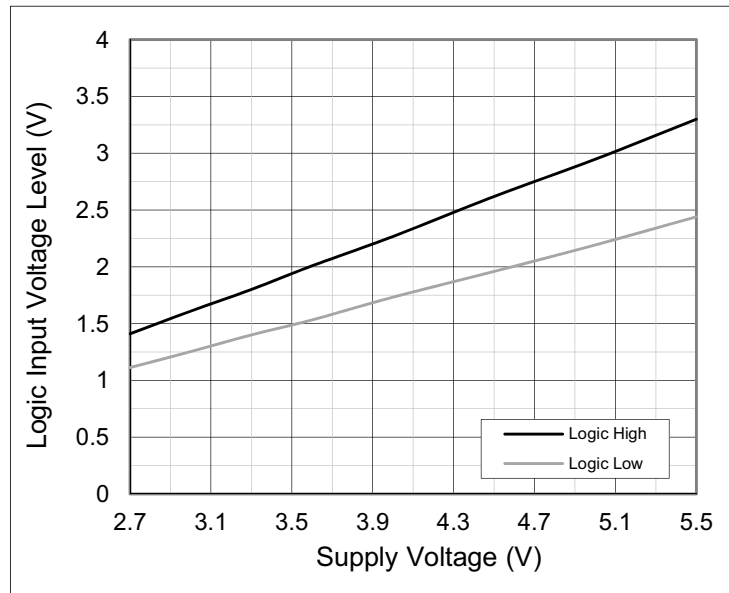**CMOS Logic Input Levels vs. Supply Voltage**

Figure 18:
CMOS Logic Input Levels vs. Temperature
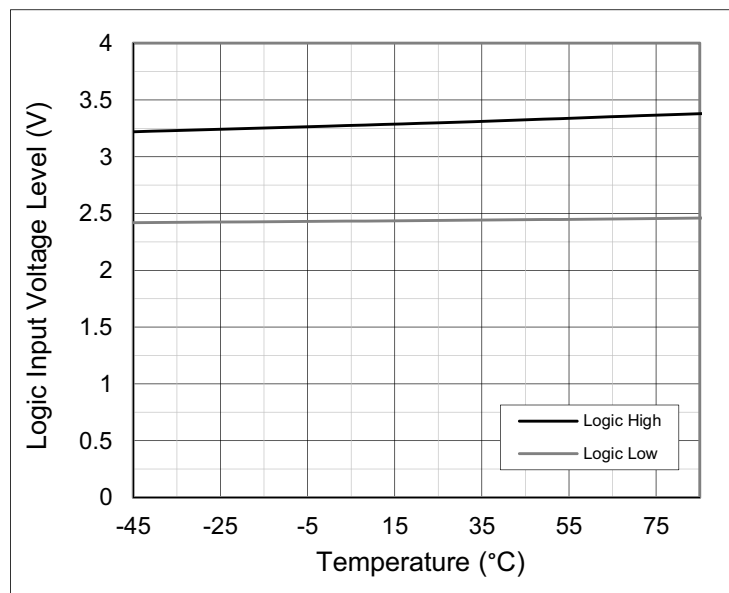
Figure 19:
MOBILE Logic Input Levels vs. Supply Voltage

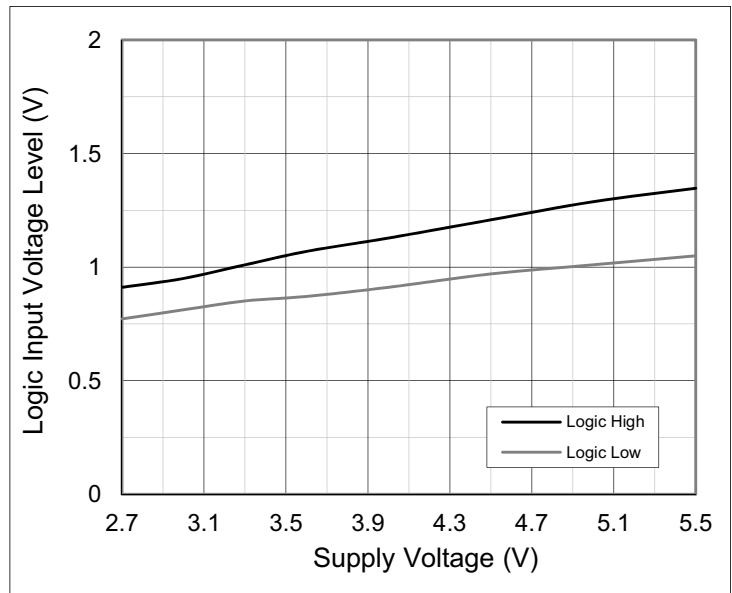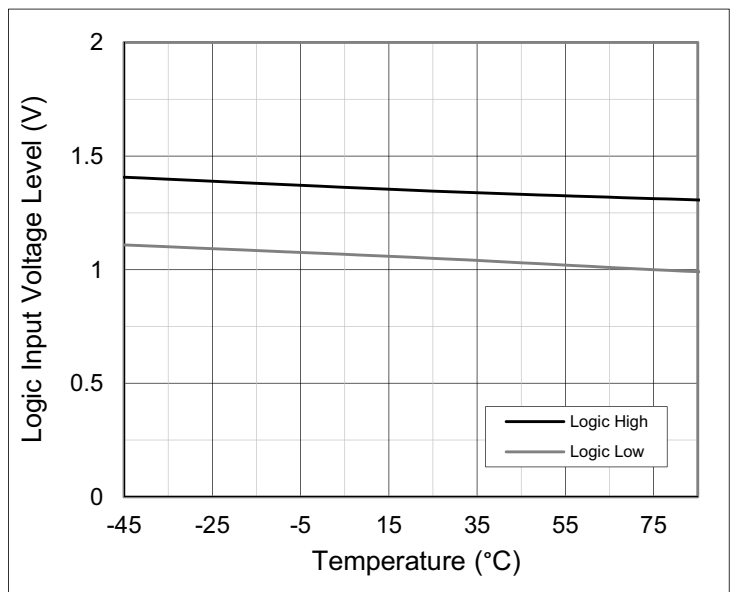

Figure 20:
MOBILE Logic Input Levels vs. Temperature

ams

Figure 21:
Oscillator Frequency vs. Supply Voltage

Figure 22:
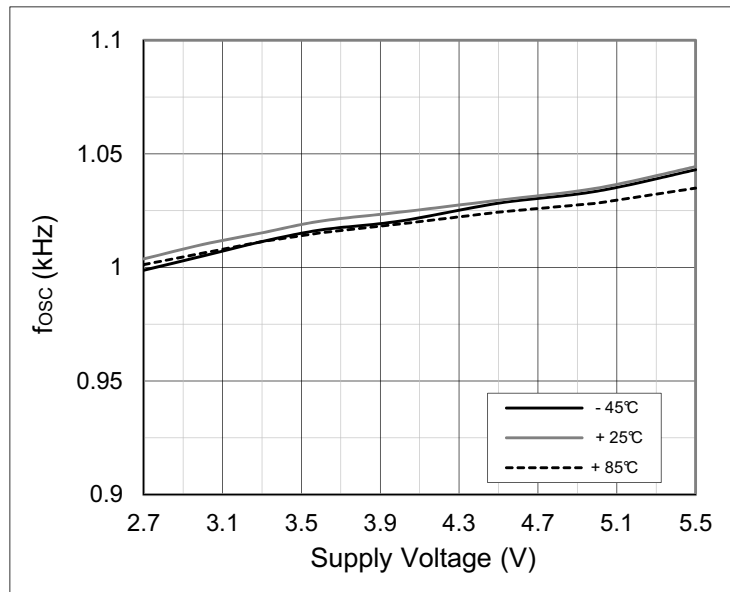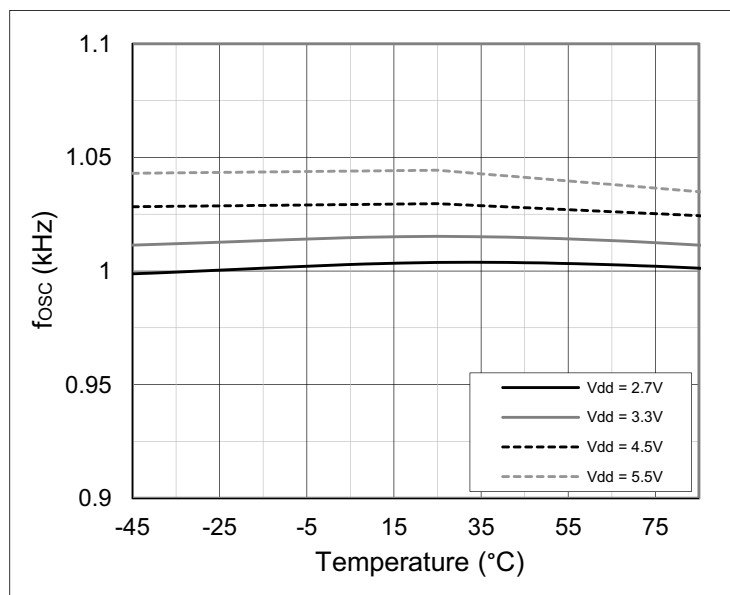**Oscillator Frequency vs. Temperature**

Figure 22:
Oscillator Frequency vs. Temperature

Detailed Description

Cross-Plexing Theorem

The cross-plexing theorem is using the fact that a LED has a forward and backward direction. A LED will only glow if there is a current flowing in forward direction. A parallel LED in backward direction will block the current flow. This effect is used in a cross-plexed matrix of LEDs.

Each CSx pin (CS0 to CS11) can be switched to VDD via the internal current source ("high"), to GND ("low") or not connected ("highZ").

The mode of operation which is controlled by an internal state machine looks like following. CS0 is switched to GND and all other CSx pins (CS1 to CS11) are controlled according to the settings in the On/Off Frame and Blink & PWM registers (see Figure 31).

Than CS1 is switched to GND and all other CSx pins (CS0 and CS2 to CS11) are controlled according to the settings in the On/Off Frame and Blink & PWM registers.

In this manner all LEDs in the matrix are scanned and turned on/off depending on the register settings.

I²C Interface

The AS1130 supports the I²C serial bus and data transmission protocol in fast mode at 1MHz. The AS1130 operates as a slave on the I²C bus. The bus must be controlled by a master device that generates the serial clock (SCLK), controls the bus access, and generates the START and STOP conditions. Connections to the bus are made via the open-drain I/O pins SCLK and SDA.

Figure 23:
I²C Interface Initialization

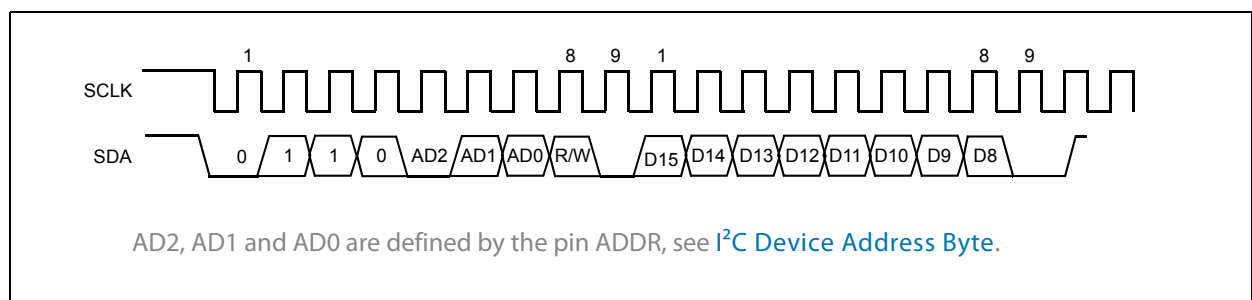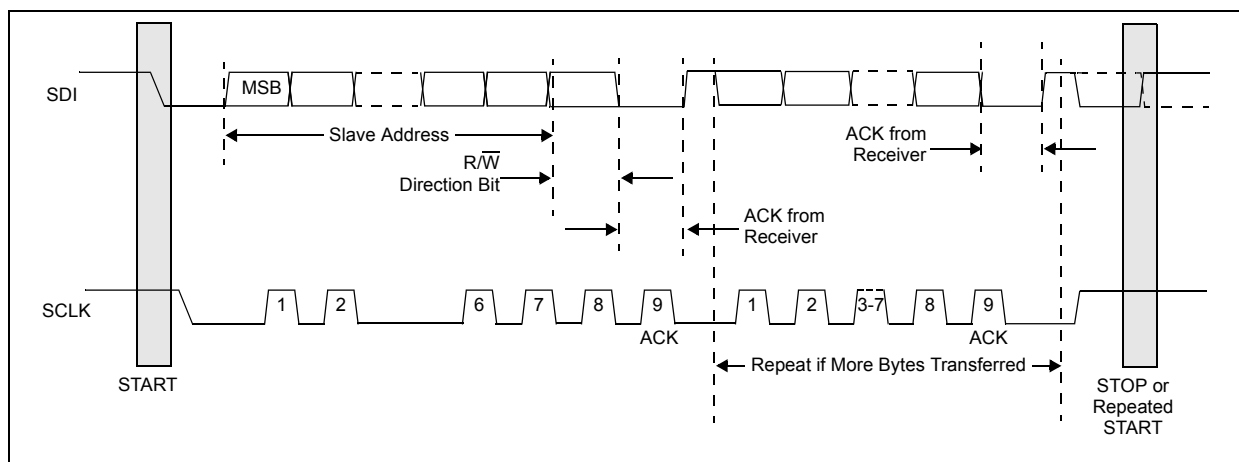AD2, AD1 and AD0 are defined by the pin ADDR, see I²C Device Address Byte.

Figure 24:
Bus Protocol

The bus protocol (as shown in Figure 24) is defined as:

- Data transfer may be initiated only when the bus is not busy.

- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The bus conditions are defined as:

- **Bus Not Busy**. Data and clock lines remain HIGH.

- **Start Data Transfer**. A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

- **Stop Data Transfe**r. A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

- **Data Valid**. The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit. Within the I^2C bus specifications a high-speed mode (3.4MHz clock rate) is defined.

- **Acknowledge**: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

- Figure 24 details how data transfer is accomplished on the I²C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

    - **Master Transmitter to Slave Receiver**. The first byte transmitted by the master is the slave address, followed by a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.

    - **Slave Transmitter to Master Receiver**. The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The AS1130 can operate in the following slave modes:

- **Slave Receiver Mode**. Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

- **Slave Transmitter Mode**. The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the AS1130 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Command Byte

The AS1130 operation (see Figure 38) is determined by a command byte (see Figure 25).

Figure 25:
Command Byte

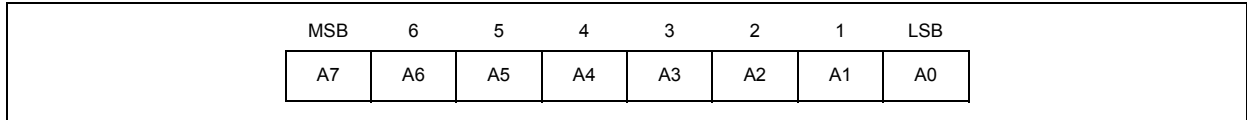|	MSB	6	5	4	3	2	1	LSB
	A7	A6	A5	A4	A3	A2	A1	A0

Figure 26:
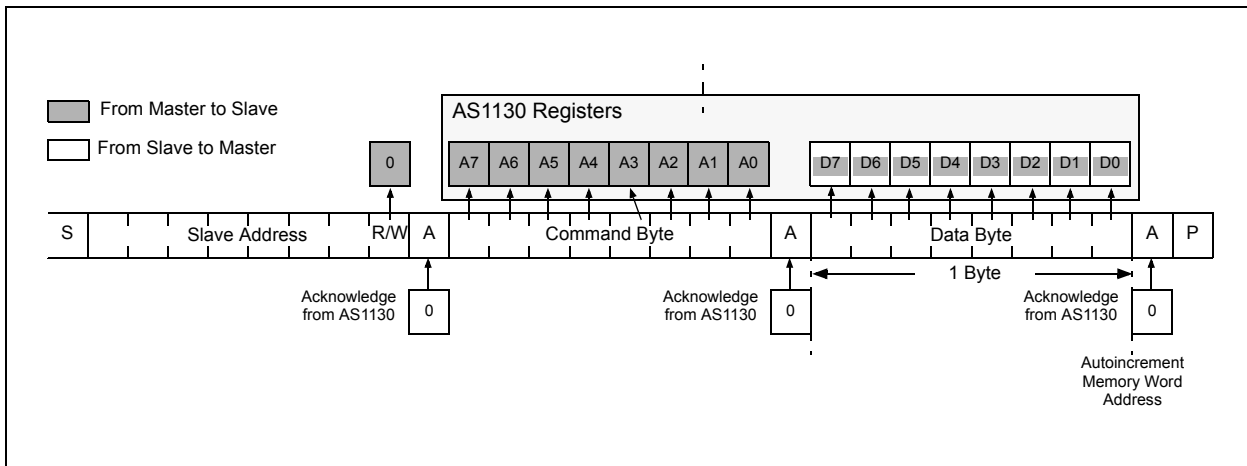**Command and Single Data Byte Received by AS1130**

Figure 27:
Setting the Pointer to a Address Register to Select a Data Register for a Read Operation
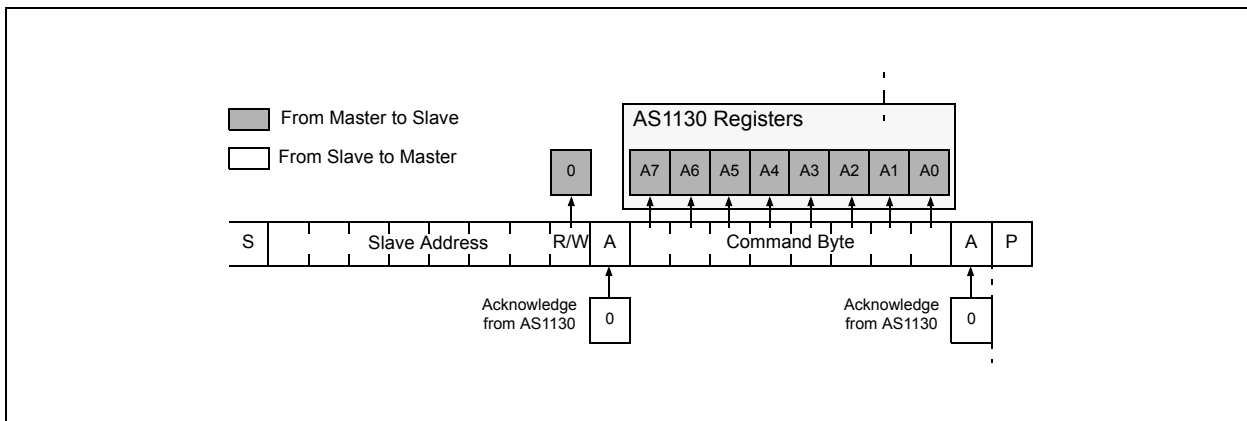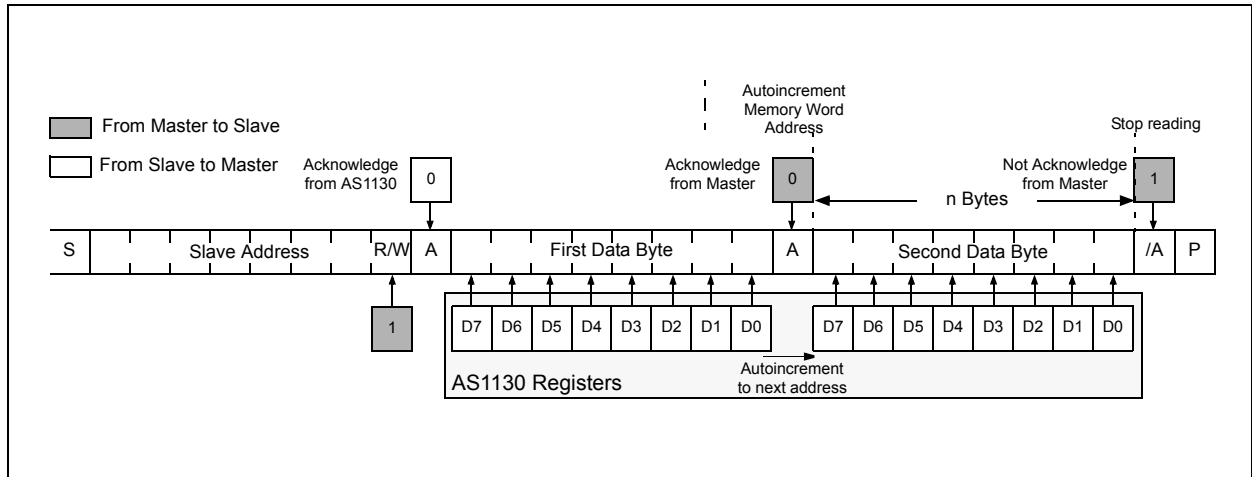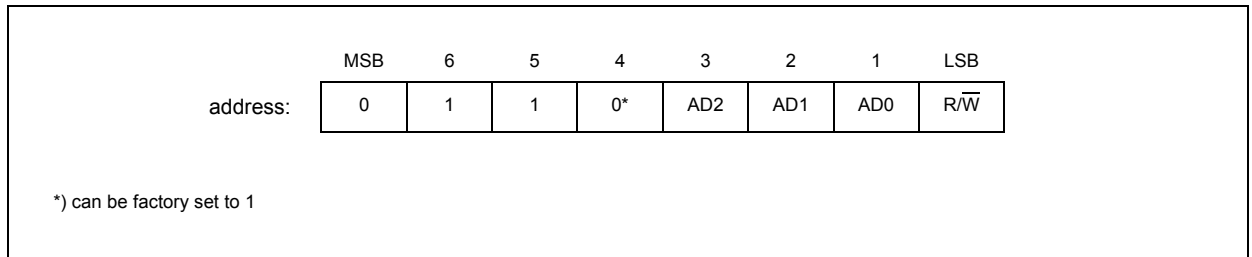
Figure 28:
Reading N Bytes from AS1130

I²C Device Address Byte

The address byte (see Figure 29) is the first byte received following the START condition from the master device.

Figure 29:
I²C Device Address Byte

	MSB	6	5	4	3	2	1	LSB
address:	0	1	1	0*	AD2	AD1	AD0	R/$\overline{W}$

*) can be factory set to 1

The bit 1, 2 and 3 of the address byte are defined through the resistor @ the device select pin ADDR (see Figure 30). A maximum of 8 devices with the same pre-set code can be connected on the same bus at one time.

- The last bit of the address byte (R/$\overline{W}$) define the operation to be performed. When set to a 1 a read operation is selected; when set to a 0 a write operation is selected.

- I²C Common address. All devices are responding on the address "0111111" if the function is enabled in the register AS1130 Config Register (0x06).

Following the START condition, the AS1130 monitors the I²C bus, checking the device type identifier being transmitted. Upon receiving the address code, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Figure 30:
Device Address

I2C Address				
Bit	**Bit Name**	**Default**	**Access**	**Description**
3:1	i2c_addr	000	R	Defines the I²C address of one device via an external resistor on pin ADDR **000:** 1MΩ or floating **001:** 470kΩ **010:** 220kΩ **011:** 100kΩ **100:** 47kΩ **101:** 22kΩ **110:** 10kΩ **111:** 4.7kΩ or GND

The pin ADDR is scanned after start up (POR) and defines the address for the device. The device reacts to this address until a hardware reset (low on pin RSTN) is performed or the power-on-reset (POR) triggers again.

Note(s): The internal address decoder needs 5ms to identify the address and to set up the device for this address.

Initial Power-Up

On initial power-up, the AS1130 registers are reset to their default values, the display is blanked, and the device goes into shutdown mode. At this time, all registers should be programmed for normal operation. To bring the device into normal operation the following sequence needs to be performed.

Start-Up Sequence

- Power-up the AS1130 (connect VDD to a source), the devices is in shutdown;

- After 5ms the address of the AS1130 is valid and the first I²C command can be send.

- Define RAM Configuration; bit mem_conf in the AS1130 Config Register (see Figure 45)
    - On/Off Frames
    - Blink & PWM Sets
    - Dot Correction, if specified

- Define Control Register (see Figure 38)
    - Current Source
    - Display options
    - Display picture / play movie

- To light up the LEDs set the shdn bit to '1' for normal operation mode (see Figure 48).

Shutdown Mode

The AS1130 device features two different shutdown modes. A software shutdown via shutdown register (see Shutdown & Open/Short Register (0x09)) and a hardware shutdown via the RSTN pin.

The software shutdown disables all LEDs and stops the internal operation of the logic. A shutdown mode via the RSTN pin additionally powers down the power-on-reset (POR) of the device. In this shutdown mode the AS1130 consumes only 100nA (typ.).

Register Description

Register Selection

Within this register the access to one of the RAM sections, the Dot Correction or to the Control register is selected. After one section is selected this section is valid as long as an other section is selected.

Figure 31:
Register Selection Address Map

Register Section	Address									Data									Description
	HEX	A7	A6	A5	A4	A3	A2	A1	A0	HEX	D7	D6	D5	D4	D3	D2	D1	D0	
NOP										0x00	0	0	0	0	0	0	0	0	No operation
On/Off Frame 0										0x01	0	0	0	0	0	0	0	1	On/Off information for each frame (up to 36 frames)
On/Off Frame 1										0x02	0	0	0	0	0	0	1	0	
On/Off Frame 2										0x03	0	0	0	0	0	0	1	1	
….										…..									
On/Off Frame 34										0x23	0	0	1	0	0	0	1	1	
On/Off Frame 35										0x24	0	0	1	0	0	1	0	0	
Blink & PWM Set 0	0xFD	1	1	1	1	1	1	0	1	0x40	0	1	0	0	0	0	0	0	Blink & PWM Information Sets (up to 6 sets)
Blink & PWM Set 1										0x41	0	1	0	0	0	0	0	1	
Blink & PWM Set 2										0x42	0	1	0	0	0	0	1	0	
Blink & PWM Set 3										0x43	0	1	0	0	0	0	1	1	
Blink & PWM Set 4										0x44	0	1	0	0	0	1	0	0	
Blink & PWM Set 5										0x45	0	1	0	0	0	1	0	1	
Dot Correction										0x80	1	0	0	0	0	0	0	0	Selection of Dot Correction Register
Control Register										0xC0	1	1	0	0	0	0	0	0	Selection of Control Register

Data Definition of the Single Frames

One frame consists of 2 datasets, the On/Off dataset and the Blink & PWM dataset. Where more On/Off frames can be linked to one PWM set. Depending on the used PWM sets more or less On/Off frames can be stored inside the AS1130 (see Figure 32).

Each On/Off frame needs to define the used Blink & PWM dataset.

Figure 32:
RAM Configuration

| RAM Configuration	Blink & PWM Set	On/Off Frame	On/Off Frame with Dot Correction
1	0	35..0	34..0
2	1,0	29..0	28..0
3	2,1,0	23..0	22..0
4	3..0	17..0	16..0
5	4..0	11..0	10..0
6	5..0	5..0	4..0

It is necessary to define the RAM configuration before data can be written to the frame datasets. The RAM configuration is defined in the AS1130 config register (see Figure 45) via bit 2:0 and bit 4 for Dot Correction.

Note(s): After a first write of data to the frames, the configuration is locked in the AS1130 config register and can be changed only after a reset of the device. A change of the RAM configuration requires to re-write the frame datasets.

12x11 LED Matrix

The AS1130 is configured to control one big LED matrix.

Figure 33:
AS1130 - Dot Matrix Structure
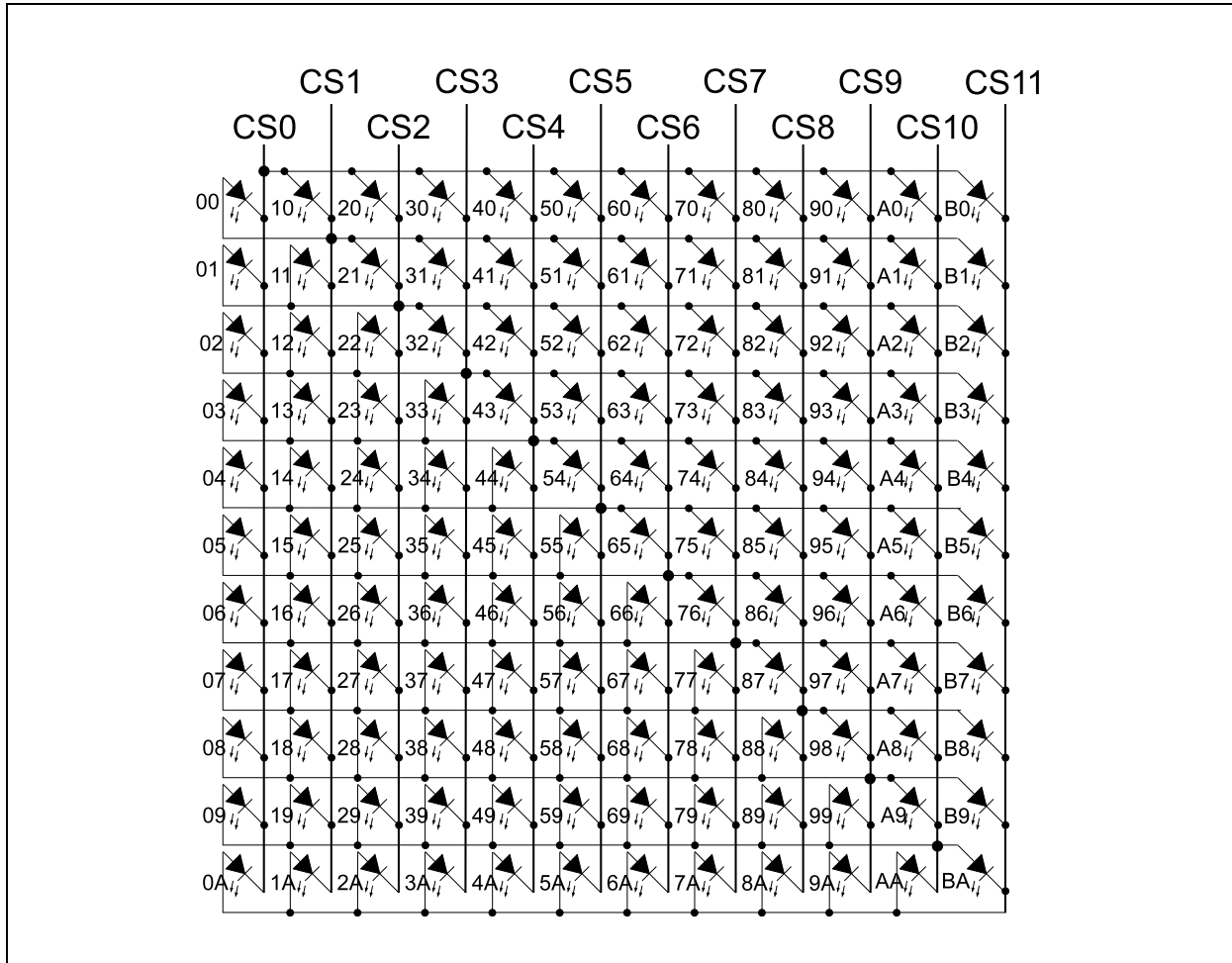
In Figure 34 it is described which databit represents which LED in the matrix. Per default all databits are '0', meaning no LED is on. A '1' puts the LED on.

Each Current Segment of the LED Matrix consists of 11 LEDs, therefore 2 bytes of data are required for one Current Segment. CS0 is defined by the two bytes with address 0x00 and 0x01 and also includes the address of the used Blink & PWM dataset for this frame.