Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AS1328

3A, 1.5MHz Synchronous DC/DC Step-Down Converter

1 General description

The AS1328 is a high-efficiency, synchronous buck converter that can deliver up to 3A. The device is available in adjustable- and fixed-output voltage versions. The wide input voltage range (2.7V to 5.5V), automatic Powersave Mode and minimal external component requirements make the AS1328 perfect for any single Li-Ion battery-powered application.

Typical quiescent current with no load is 25µA and decreases to ≤1µA in shutdown mode. The highly efficient duty cycle (100%) provides low dropout operation, prolonging battery life in portable systems.

The AS1328 is available with user adjustable output voltage between 0.6V and VIN via an external resistor divider.

The switching frequency (1.5MHz) allows the use of a small surface mount inductor.

A user adjustable Softstart function limits the input current during start-up.

The AS1328 is available in a TQFN (3x3mm) 16-pin package.

AS1328 offers several power monitoring functions.

Part Name	Description
AS1328A	Power-Okay Function
AS1328B	Low Battery Detection
AS1328C	Power-Okay Function with 215ms delay

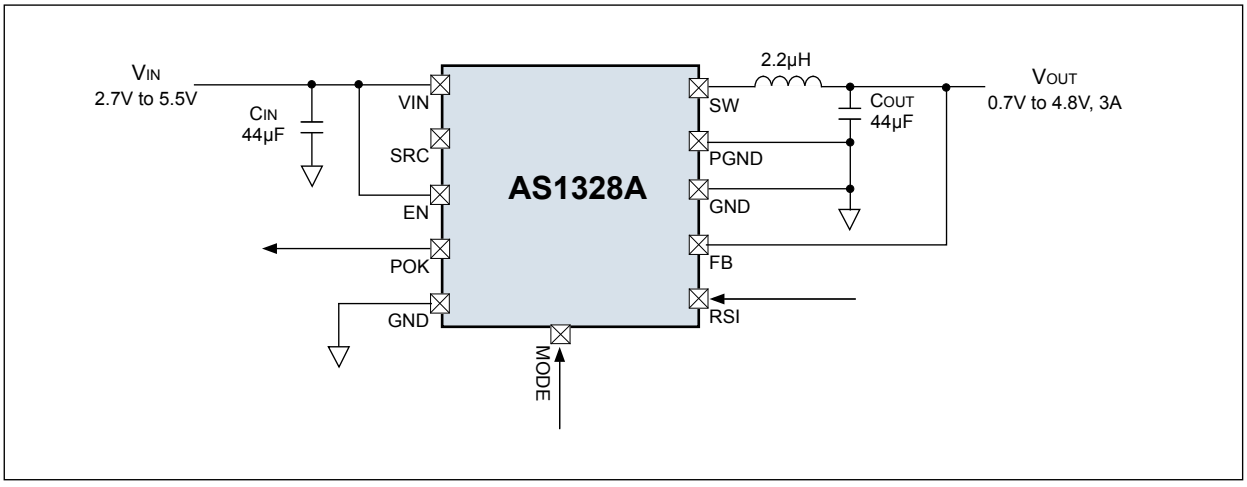
2 Key features

- High Efficiency: up to 96%
- Input Voltage Range: 2.7V to 5.5V
- Output Voltage Range (factory set): 0.7V to 4.8V
- User-Adjustable Output Voltage Range: 0.6V to VIN
- Output Current: 3A
- Low battery detection or Power Okay function
- Constant Frequency Operation (1.5MHz) or Powersave Operation
- Softstart Function
- No Schottky diode required
- Automatic Powersave Operation
- Low Dropout Operation: 100% Duty Cycle
- 215ms POK timeout (optional)
- Low Quiescent Supply Current: 25µA
- Shutdown Current: ≤1µA
- Thermal protection
- TQFN (3x3mm) 16-pin Package.

3 Applications

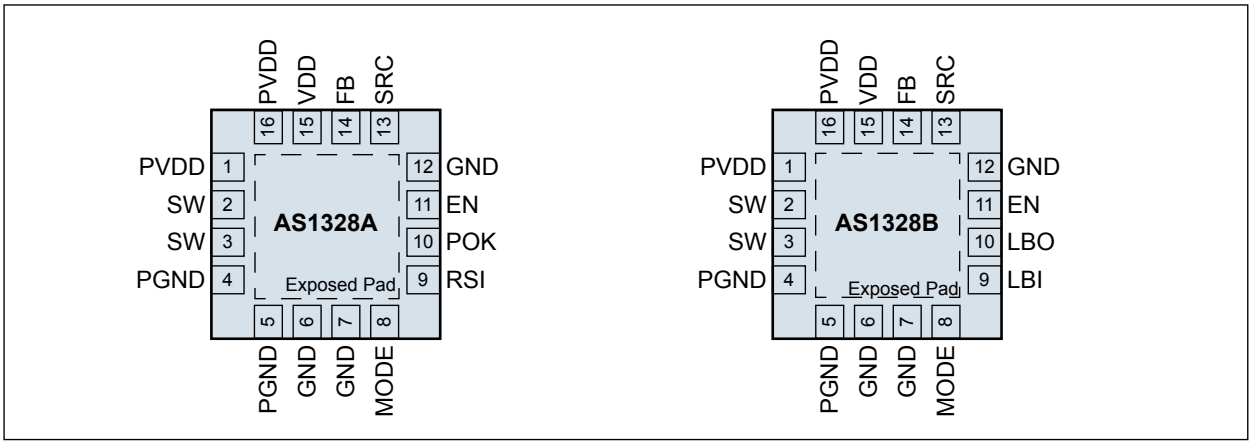
The device is ideal for mobile communication devices, laptops and PDAs, SSD, point of load supply of µP and FPGA based systems, medical instruments or any other application with high current requirements.

Figure 1. AS1328 - Typical application diagram



4 Pin assignment

Figure 2. Pin assignment (top view) of the two versions AS1328A (POK function) and AS1328B (LBI function)



4.1 Pin description

Table 1. Pin description

Pin Number	Pin Name	Description	
1, 16	PVDD	Power Supply Voltage. Supply Voltage for the power output stage. This pin must be closely decoupled to PGND with a > 2x22µF ceramic capacitor.	
15	VDD	Supply Voltage. Supply Voltage for the DC-DC core: possibly a RC filter can be inserted from PVDD to VDD to improve switching noise rejection.	
11	EN	Active-High Enable Input. Pulling this pin to logic high enables the device, a logic low level puts the device in shutdown mode. In shutdown mode all functions are disabled, drawing supply current <1µA. EN voltage is preferably referred to VDD and GND pins instead of PVDD and PGND. **Note:** This pin should not be left floating.	
9	RSI	AS1328A	Reset Input for POK. This input resets the 215ms timer of the POK signal. As long as RSI is low the POK signal is low if the nominal output voltage is out of range. A high input to RSI will reset the 215ms POK timer (where available) and delay the signal as long as RSI stays high. A RSI high-to-low transition restarts the 215ms counter as long as the output voltage is within regulation. **Note:** Do not leave this pin floating.
	LBI	AS1328B	Low Battery Comparator Input. Input of a 1.2V threshold comparator. Connect it to GND if not used. The voltage at this pin must be referred to GND.
10	POK	AS1328A	Power-OK Output. Open Drain Output. Leave this pin unconnected if the Power-OK feature is not used. Otherwise use an external pull-up resistor. Logic low: out of regulation; logic high: within regulation. The POK signal reacts after a 215ms delay (POK_d) or no delay. Both variants (POK and POK_d) are available.
	LBO	AS1328B	Low Battery Comparator Output. Open Drain Output. Leave this pin unconnected if the LBO feature is not used. Otherwise use an external pull-up resistor. This output is low when the voltage on LBI is less than 1.2V. The logic level is not valid in shutdown and during startup.
14	FB	Feedback Pin. Feedback input to the error amplifier. For the factory set output voltage connect this pin directly to V_{OUT}. For the user adjustable out put voltage connect a resistor divider tap to this pin. Connect the ground terminal of the resistor divider to GND and not to PGND. The output voltage can be adjusted from 0.6V to V_{IN} by: $V_{OUT} = 0.6V[1 + (R_1/R_2)]$ A capacitor should be connected in parallel to R1 to ensure stability and improved load transient response.	
6, 7, 12	GND	Analog Ground. GND and PGND should have only one point connection.	
4, 5	PGND	Power Ground. Connect all grounds to this pin.	
2, 3	SW	Switch Node Connection to Inductor. These pins must be shorted together on the PCB to connect one terminal of the external inductor to the drains of the internal synchronous power MOSFET switches.	
8	MODE	Mode Pin. Logic-controlled mode input for automatic Powersave Operation of the regulator. High: automatic Powersave Operation; Low: fixed frequency operation.	
13	SRC	Slew Rate Control. This pin controls the soft start function of the AS1328. If not used, leave this pin floating or connect it to V_{DD} in case of a noisy environment. For a user defined start-up time, connect a ceramic capacitor C_{SS} from SRC to GND. The capacitor will be charged with 4µA nominal current. Alternatively, the SRC pin can also be forced by a voltage source.	
Exposed Pad		Exposed Pad. The exposed pad must be connected to PGND. Ensure a good connection to the PCB to achieve an optimal thermal performance.	

5 Absolute maximum ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
VIN to GND	-0.3	7	V	
SW to GND	-0.3(DC) -1.5 (100ns)	VIN + 0.3 (DC) VIN+1 (100ns)	V	
EN, FB to GND	-0.3	VIN	V	
P-Channel Switch Source Current (DC)		4	A	
N-Channel Switch Source Current (DC)		4	A	
Peak SW Sink and Source Current		6	A	
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 78
Electrostatic Discharge				
Electrostatic Discharge HBM	1.5		kV	Norm: MIL 883 E method 3015
Temperature Ranges and Storage Conditions				
Thermal Resistance ΘJA		36.7	ºC/W	on PCB
Junction Temperature		+125	ºC	
Storage Temperature Range	-55	+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/ JEDEC J-STD-020“Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices”.
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	1			Represents an unlimited floor life time

6 Electrical characteristics

VIN = EN = 5V (or VIN > VOUT + 0.5V whatever is higher), CIN = COUT = 2x22µF, L = 2.2µH (unless otherwise specified). Typical values are @ TAMB = +25ºC. All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TA	Operating Temperature Range		-40		+85	°C
TJ	Operating Junction Temperature Range		-40		+125	°C
VIN	Input Voltage Range		2.7		5.5	V
IQ	Quiescent Supply Current[1]	Dropout Operation; VOUT/VIN = 90%, ILOAD = 0A		250		µA
		Powersave Mode; MODE=high, RSI=low, VOUT = 105% x VOUT(NOM), ILOAD = 0A, TAMB = +25ºC		25		
IOUT	Output Current		3			A
ISHDN	Shutdown Current	MODE=high, RSI=high, VEN = 0V, VIN = 5.5V, TAMB = +25ºC		0.1	1	µA
Regulation						
VOUT	Regulated Output Voltage Range	User adjustable output version	0.6		VIN	V
ACC	Regulated Output Voltage Accuracy	Fixed output version, DC average value, ILOAD = 100mA	-1		+1	%
VFB	Regulated Feedback Voltage		0.59	0.6	0.61	V
IFB	FB pin Current	Only for User-Adjustable Output Voltage version	-100		+100	nA
ΔVLNR	VIN Line Regulation[2]	MODE=low, VIN = 2.7V (or VIN > VOUT + 0.5V whatever is higher) to 5.5V, ILOAD = 100mA		0.1		%/V
ΔVLOADREG	Output Voltage Load Regulation	MODE=low, ILOAD = 1µA to 3A		0.1		%/A
DC-DC switches						
τon	Minimum on-pulse duration	ILOAD = 1A		100		ns
IPK	Peak Inductor Current[3]		3.5	4.5		A
RPFET	P-Channel FET RDS(ON)			35		mΩ
RNFET	N-Channel FET RDS(ON)			35		mΩ
ILSW	Switch Leakage Current	VEN = 0V, VSW = 0V or 5V, VIN = 5V, TAMB = +25ºC	-1	0.01	+1	µA
		VEN = 0V, VSW = 0V or 5V, VIN = 5V, TAMB = +85ºC		1		µA
Control inputs						
VIH	Logic Input Threshold		1.2			V
VIL					0.4	
IEN	EN Input Leakage Current	VEN = 0V to 5.5V, VIN = 5.5V	-0.1	0.01	+0.1	µA

Table 3. Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Power-OK output						
V_{POKL}	POK Voltage Threshold Low	Rising Edge T_{PKLR}	94	95	96	% $V_{OUT(NOM)}$
		Falling Edge T_{PKLF}	88	90	92	
V_{POKH}	POK Voltage Threshold High	Rising Edge T_{PKHR}	113	115	117	% $V_{OUT(NOM)}$
		Falling Edge T_{PKHF}	109	110	111	
t_{DELAY}	POK Delay Time[4]	in AS1328A (delay version)	170	215	260	ms
		in AS1328A (no delay version)		20		µs
V_{OL}	POK Output Low Voltage	I_{SINK} = 1mA, V_{FB} = 0.7V			0.3	V
I_{POK}	POK Output High Leakage Current	V_{POK} = V_{IN}, T_{AMB} = +25°C		0.01	1	µA
Low battery control						
V_{LBI}	LBI voltage threshold	LBI voltage decreasing	1.17	1.2	1.23	mV
ΔV_{LBI}	LBI hysteresis			25		
I_{LBI}	LBI input current	EN = V_{IN} or GND		0.01	0.1	µA
Oscillator						
f_{OSC}	Oscillator Frequency		1.2	1.5	1.8	MHz
Thermal shutdown						
T_{SHDN}	Thermal Shutdown			150		°C
ΔT_{SHDN}	Thermal Shutdown Hysteresis			25		°C

1. The dynamic supply current is higher due to the gate charge delivered at the switching frequency.
2. The device is tested in a proprietary test mode.
3. The measurement is guaranteed by design.
4. The device is tested in a proprietary test mode.

7 Typical operating characteristics

CIN = COUT = 2x22µF, L = 2.2µH; typical values are at TAMB = +25°C (unless otherwise specified).

Figure 3. Efficiency vs. Output Current; VOUT = 2.8V, MODE = 1

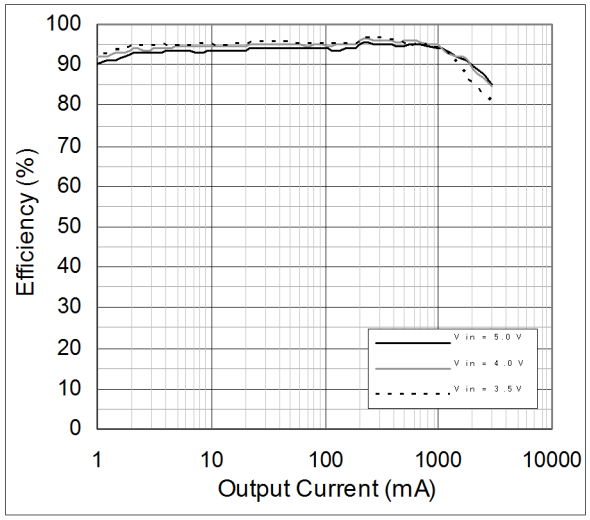


Figure 4. Efficiency vs. Output Current; VOUT = 2.8V, MODE = 0

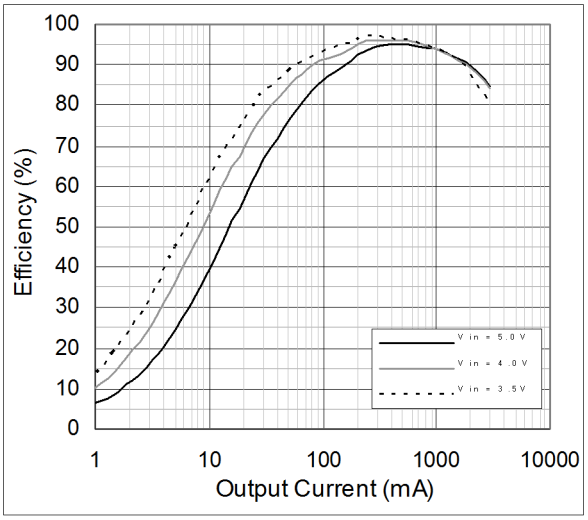


Figure 5. Efficiency vs. Output Current; VOUT = 1.2V, MODE = 1

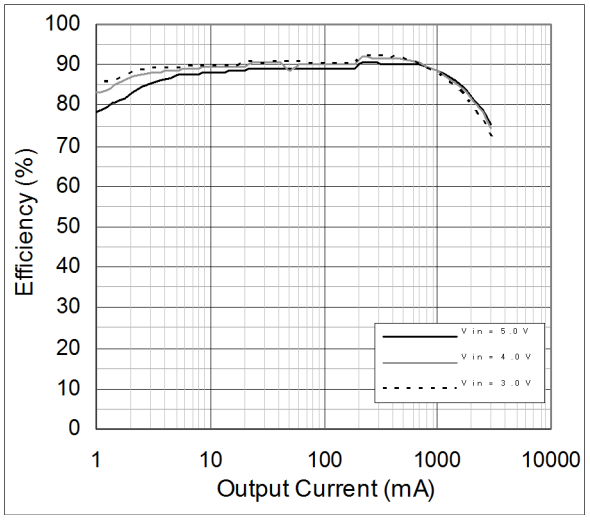


Figure 6. Efficiency vs. Output Current; VOUT = 1.2V, MODE = 0

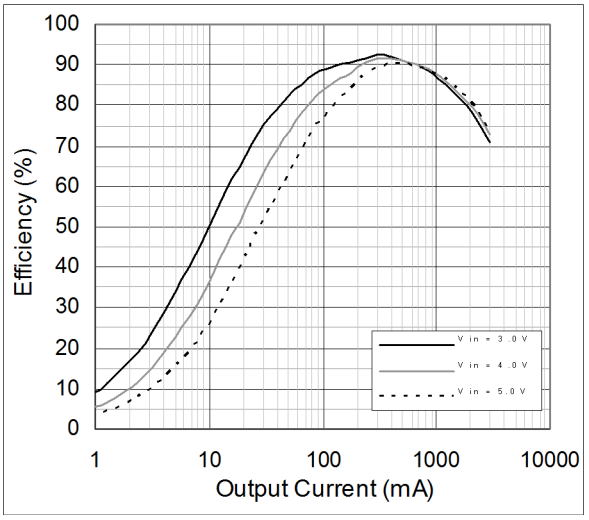


Figure 7. Efficiency vs. Input Voltage; VOUT = 2.8V, MODE = 1

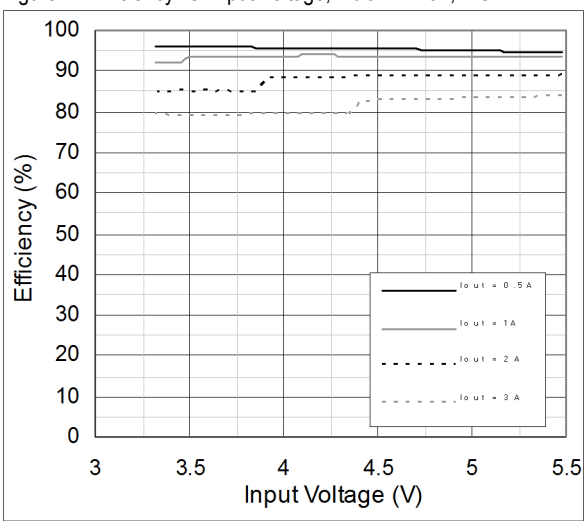


Figure 8. Efficiency vs. Input Voltage; VOUT = 2.8V, MODE = 0

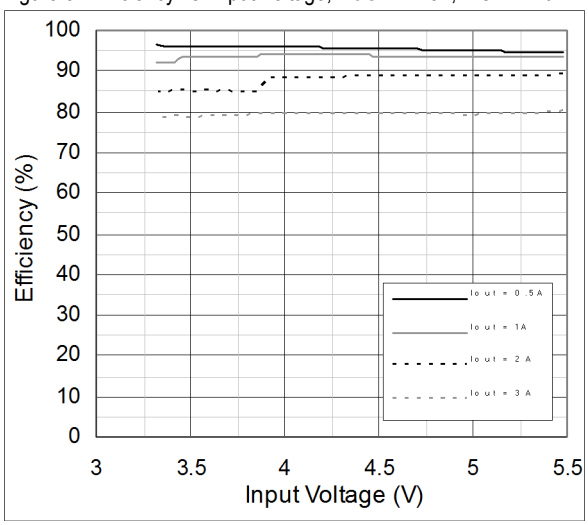


Figure 9. Efficiency vs. Input Voltage; VOUT = 1.2V, MODE = 1

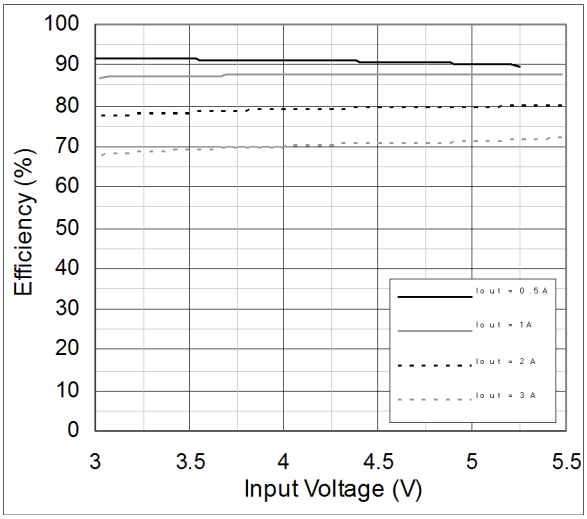


Figure 10. Efficiency vs. Input Voltage; VOUT = 1.2V, MODE = 0

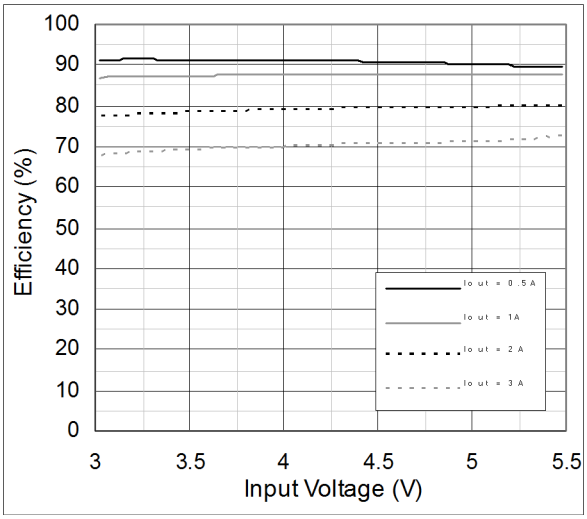


Figure 11. Load Regulation; VOUT = 2.8V, MODE = 1

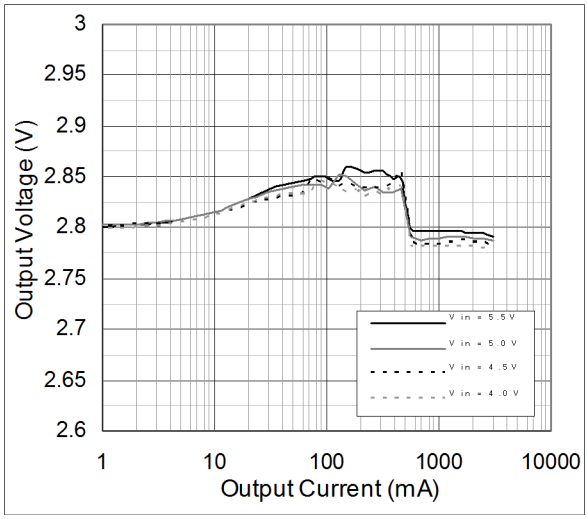


Figure 12. Load Regulation; VOUT = 2.8V, MODE = 0

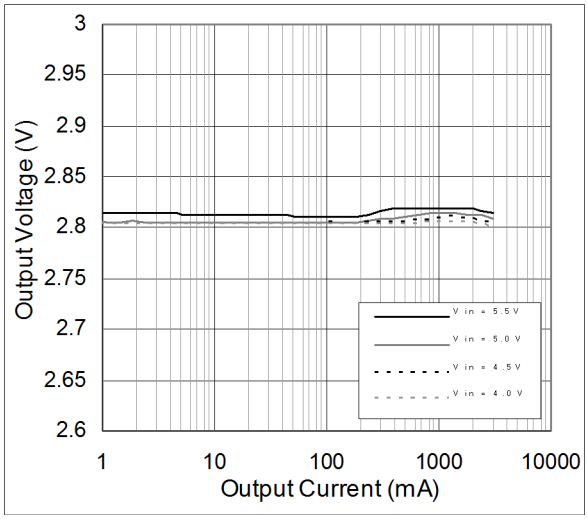


Figure 13. Load Regulation; VOUT = 1.2V, MODE = 1

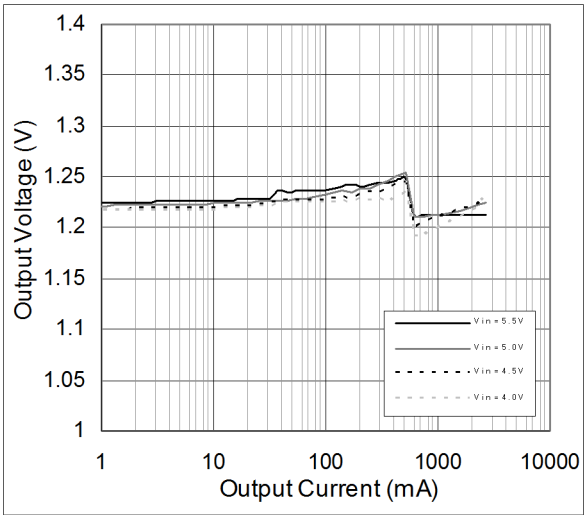


Figure 14. Load Regulation; VOUT = 1.2V, MODE = 0

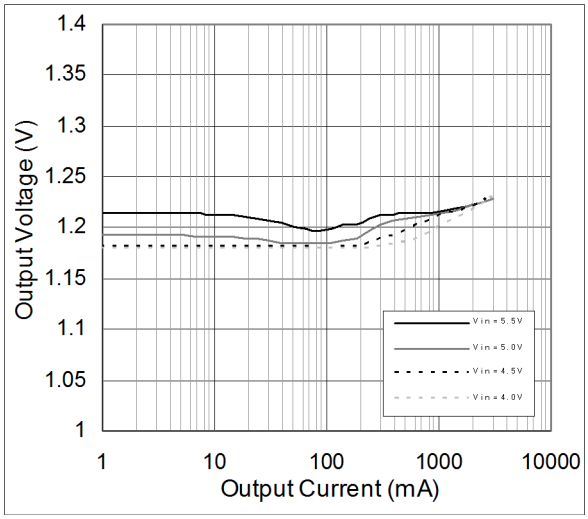


Figure 15. Line Regulation; VOUT vs. VIN, VOUT = 2.8V, MODE = 1

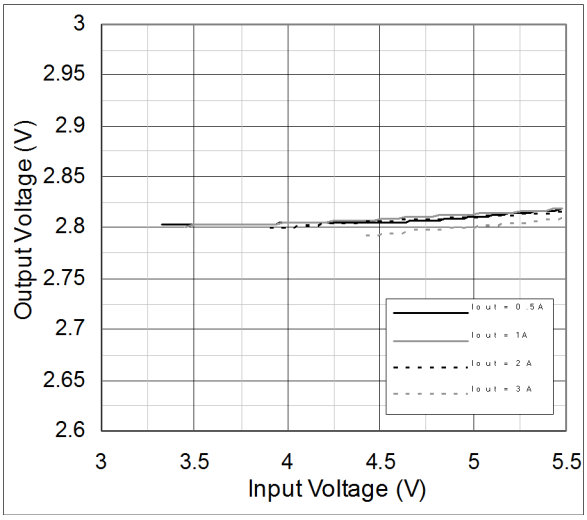


Figure 16. Line Regulation; VOUT vs. VIN, VOUT = 2.8V, MODE = 0

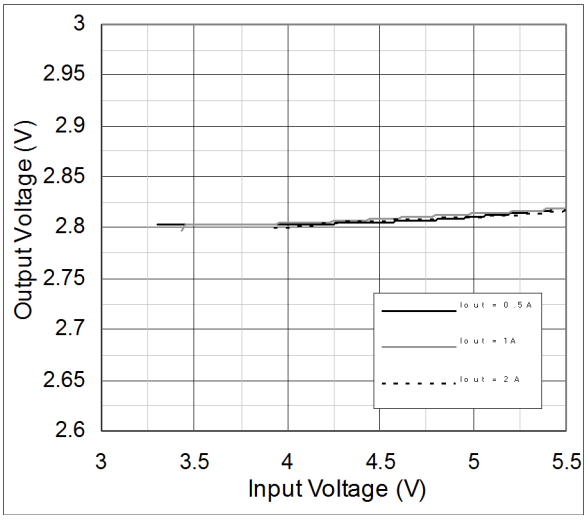


Figure 17. Line Regulation; VOUT vs. VIN, VOUT = 1.2V, MODE = 1

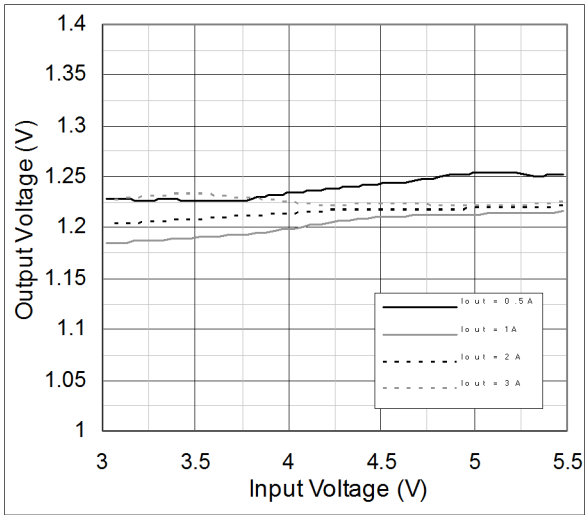


Figure 18. Line Regulation; VOUT vs. VIN, VOUT = 1.2V, MODE = 0

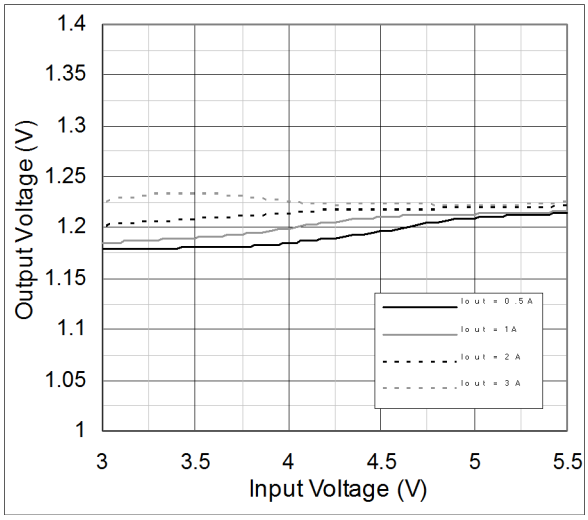


Figure 19. Line Transient Response; VIN = 3V to 5V, IOUT = 1A

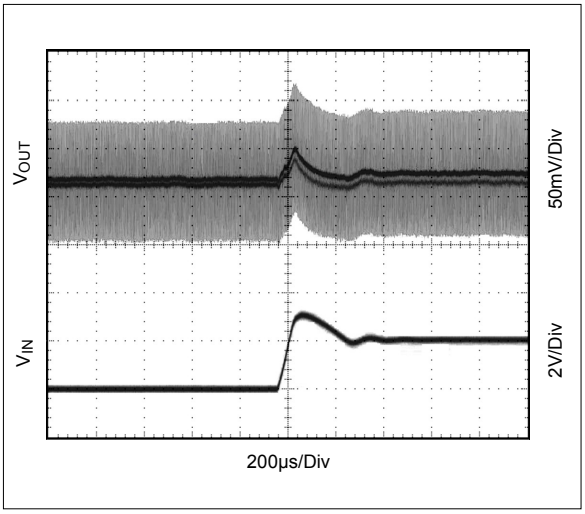


Figure 20. Line Transient Response; VIN = 5V to 3V, IOUT = 1A

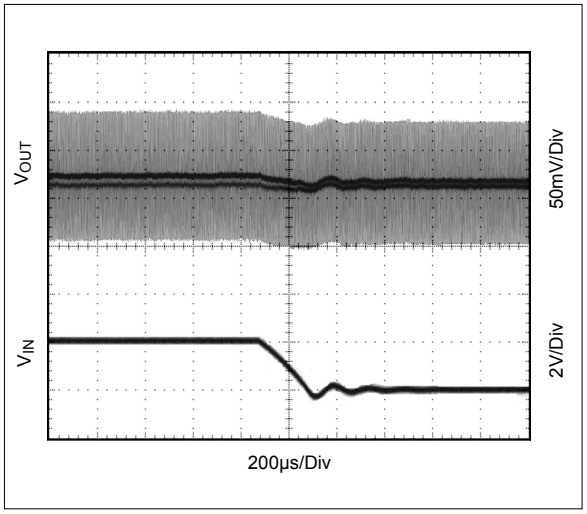


Figure 21. Load Step 0A to 1A

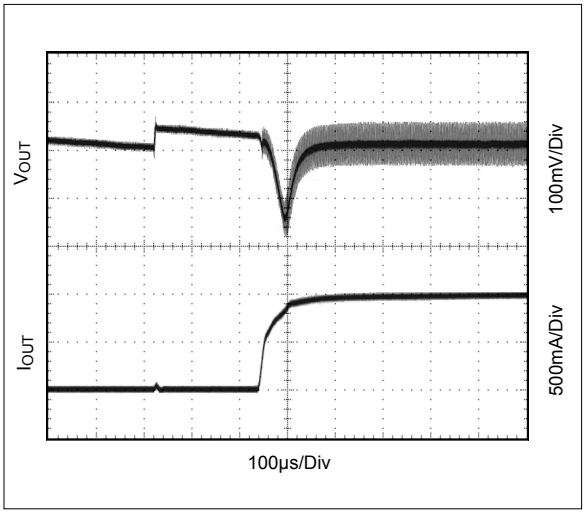


Figure 22. Load Step 1A to 0A

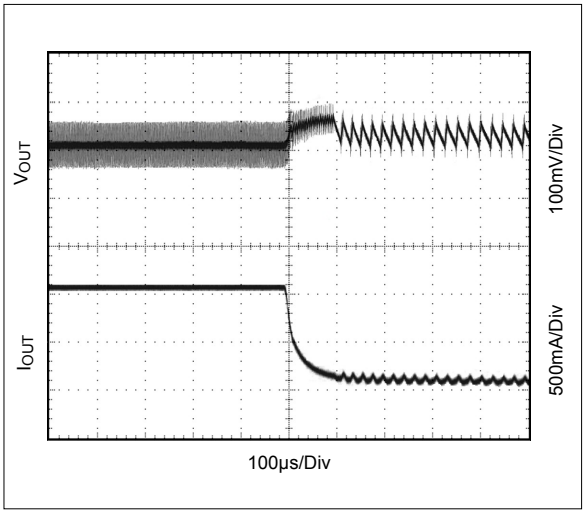


Figure 23. Startup waveform

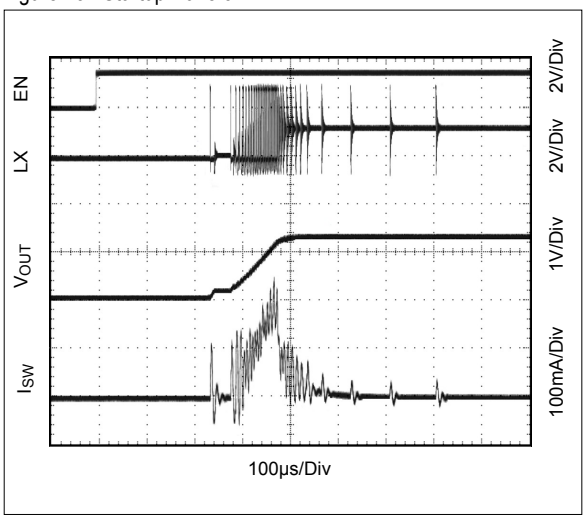


Figure 24. Soft-Start

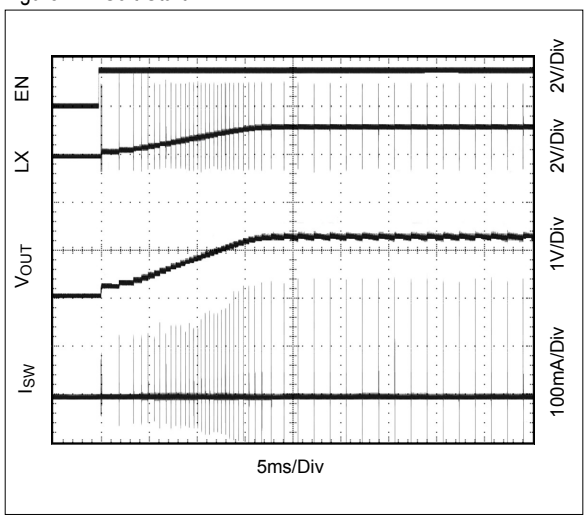
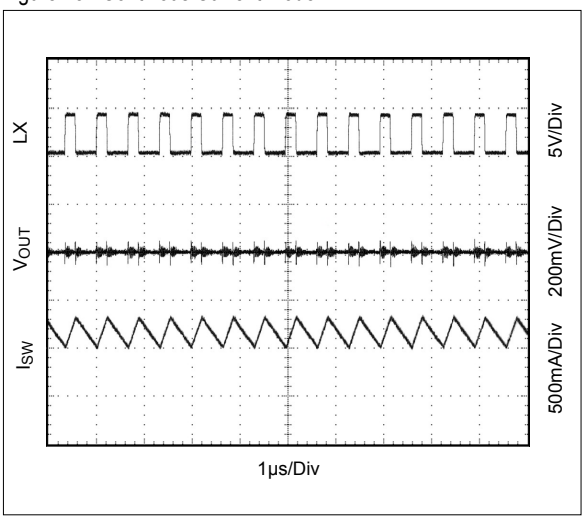


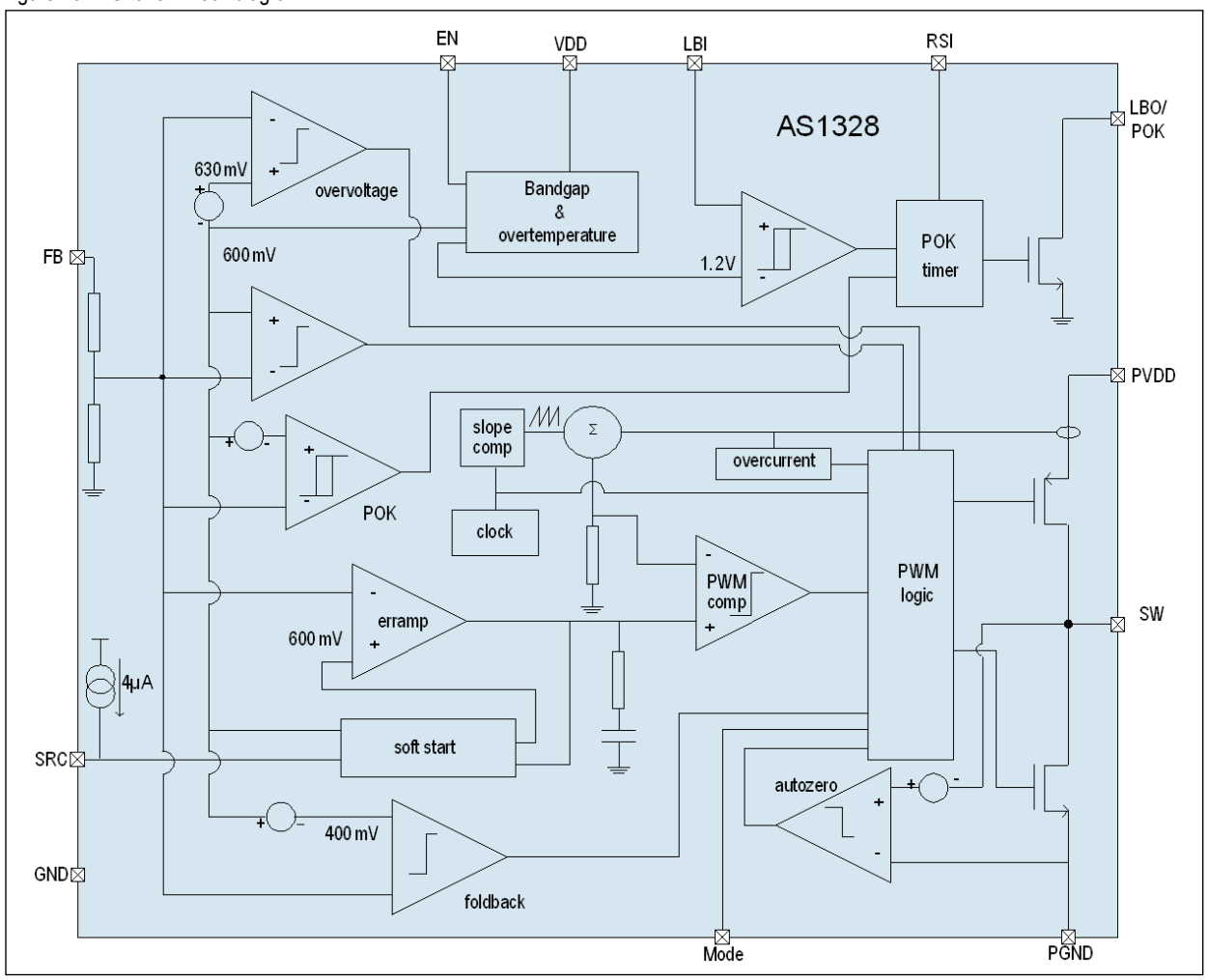
Figure 25. Continous Current Mode



8 Detailed description

The AS1328 is a high-efficiency buck converter that is based on an internally compensated current-mode architecture. This reduces the number of the external components and relaxes the requirements on their values to ensure stability. The two synchronous internal complementary MOSFET switches eliminate the need of an external Schottky diode and improve system efficiency. This allows a compact PCB layout and ensures optimal efficiency performance. The small on-resistance (35mΩ nominal) of the switches allows high efficiency up to 3A, which corresponds to the maximum continuous output current value.

Figure 26. AS1328 - Block diagram



The 1.5MHz operating frequency allows to use a small inductor keeping reduced values for the current ripple. The small inductor value also offers a great advantage for reducing losses as well as ensuring a prompt response under transient load variations.

Via the pin MODE, the device can be set in PWM mode for ripple minimization or alternatively exploit the inner automatic powersave feature by means of which the device remarkably reduces its operating frequency at light loads. Large efficiency value is thus ensured also in the lower range of the load current.

The output voltage can be set by an external resistor divider or it is fixed from factory setting. The device is available with a fixed output voltage in 50mV steps from 0.7V up to 2.9V and in 100mV steps from 2.9V to 4.8V (see Ordering information on page 29). On the regulated DC voltage an accuracy of 1% is guaranteed for all versions.

Soft start feature is provided by loading pin SRC with an external capacitor Css. For Css higher than 10nF it is possible to increase, proportionally to Css value, the startup time of the device which is limited to 1ms by an inner slewing limitation in the reference voltage. In addition, by forcing pin SRC with less than 500mV bias reference, it is possible to make the output voltage tracking the DC voltage at SRC pin.

Nominal operating duty cycle of the converter, which fixes the output voltage range vs. input voltage, ranges from 15% to 95%. For output voltages requiring a duty cycle above 95%, their value can still be obtained by modulating the PMOS on-time as an average result after some cycles at full conduction and others running at 95% duty cycle.

Cycle by cycle peak inductor current limitation (max value 4.5A), thermal protection, output over-voltage sensing, UVLO, Enable features are common to all the available variants of the device.

The AS1328 is available in different variants depending on specific features: besides the already mentioned external output voltage setting, Power OK (POK) option and Low battery detection (LBI operation) can be required for precisely monitoring the regulated output voltage, an external voltage reference or the supply voltage. The AS1328A offers the POK- and the AS1328B offers the LBI-Function. Both functions cannot be offered together.

The AS1328A is available in two variants. In one variant the POK signal is asserted only depending on internal circuitry delay, while in the other version the POK asserts after a 215ms delay. See Power-OK functionality (AS1328A only) on page 15 for further information.

Main control loop

During normal operation, the internal PMOS power switch is turned on at each rising edge of the system clock, running at 1.5MHz. The SW output of the DC-DC converter gets connected to VIN by means of the power PMOS switch and the current in the coil starts increasing at a rate depending on VIN, the regulated voltage VOUT and the coil. This increase causes the current ripple which is typical in a DC-DC converter. The instantaneous current in the coil oscillates around the average value with a triangular waveform and the ripple is the maximum excursion from this value. Due to the current mode architecture, the current in the PMOS is mirrored: a scaled replica is sent to a sense resistor at the input of the PWM comparator where a ramp is generated. Moreover, in order to prevent oscillation at duty cycle larger than 50%, a current ramp, called slope compensation, is added at the same PWM comparator input.

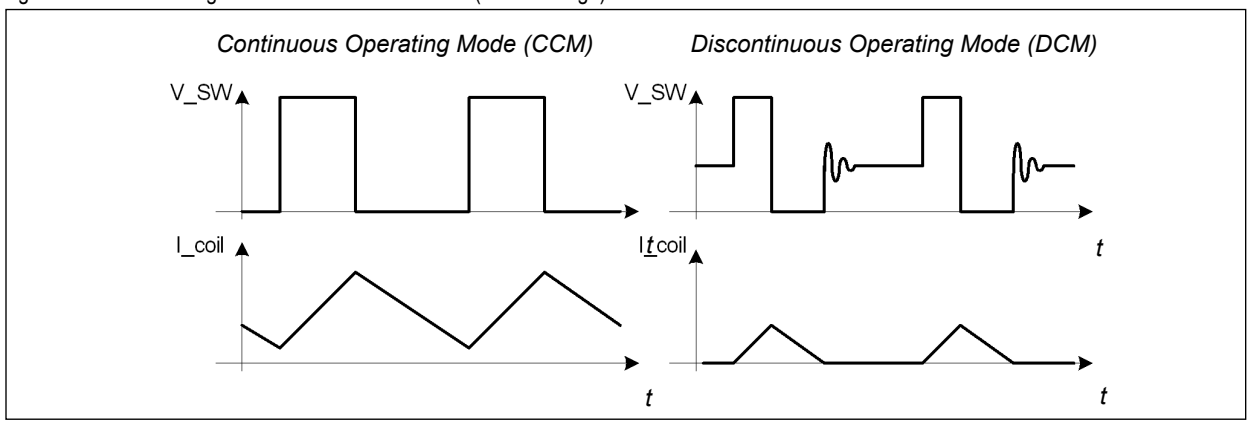
The other input of the PWM comparator is a slow varying signal, resulting from the integration onto the loop filter of error amplifier output. This stage, acting as a transconductor, injects in the loop filter a current proportional to the difference between the regulated output at node FB and an on-chip reference voltage. Eventually a resistor divider, located between the input of the error amplifier and the output regulated voltage at pin FB, sets the desired DC voltage at the load.

Because of the ramping value of the PMOS current, the PWM comparator trips when the drop across the sense resistor gets larger than the slowly varying error amplifier output. This transition turns off the power PMOS and, in turn, it switches on the NMOS after a short delay, to prevent crowbar. The NMOS current starts decreasing at a rate depending on VOUT and the coil size while still being positive because of the continuity from the coil.

NMOS conduction takes place up to a given point, depending on MODE pin value.

In case MODE is logic high (see Figure 27), the current in the NMOS is not allowed to become negative: a very accurate comparator senses the drop across the power NMOS to open it as soon as node SW becomes positive vs. PGND pin, signifying a discharging current from the load. The output SW remains floating until the next positive clock edge, which closes the power PMOS switch and starts a new cycle. This usually happens when the ripple current is at least twice the average value. This situation is commonly referred as “Discontinuous Operating Mode” (DCM). In case of larger load current and lower ripple, the current in the NMOS is not able to reverse polarity before the clock period elapses: in this case the NMOS is disconnected only by the positive edge of the system clock to start a new similar cycle with the activation of the power PMOS. This situation is usually known as “Continuous Operating Mode” (CCM).

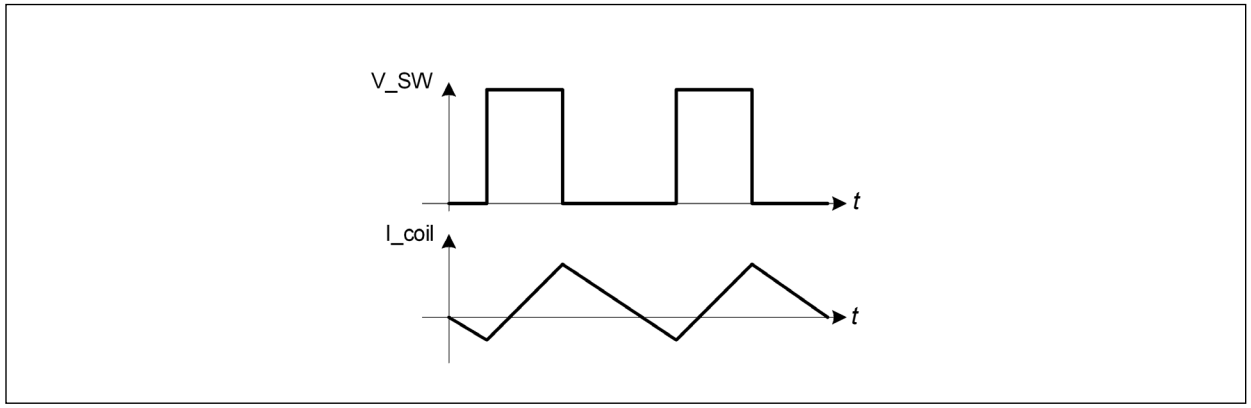
Figure 27. Switch voltage and coil current waveforms (MODE = high)



Note: Ringing is due to the LC resonant circuit at the load when both PMOS and NMOS are turned off.

In case MODE is logic low (see Figure 28), the process continues up to the next clock cycle. At this event the NMOS is disconnected and a new cycle starts. This means that, in case of light average load and large ripple, the current in the coil may even become negative and the load is temporarily discharged.

Figure 28. Switch voltage and coil current waveforms (MODE = low)



Note: The coil current is allowed to become negative and to discharge the load.

The loop operates in negative feedback. When the load current increases, VOUT tends to decrease relative to the nominal value. This causes the error amplifier output voltage to increase, asking for higher peaks in the ramp at the PWM comparator input before terminating the PMOS conduction. This means a current increase from the PMOS that tends to track the load variation.

Because of the large gain, the virtual ground at the error amplifier forces the FB node to be a multiple, depending on the voltage divider from FB pin, of the on-chip reference voltage at the other input terminal of the error amplifier.

Powersave Operation (MODE = high)

Powersave Operation is automatically triggered when MODE signal is high, while it is disabled by forcing MODE as low.

When the load current is small, the output capacitor does not need to recover the lost charge at each clock period. Due to the Powersave Operation it is possible to skip some clock cycles. This reduces the power consumption and keeps the efficiency high at any load.

Automatic triggering of Powersave Mode is guaranteed by two main facts: first, a minimum amount of charge that is injected into the load at each clock cycle; second (once MODE set at high), it is not allowed to discharge the load by blocking a negative current in the power NMOS.

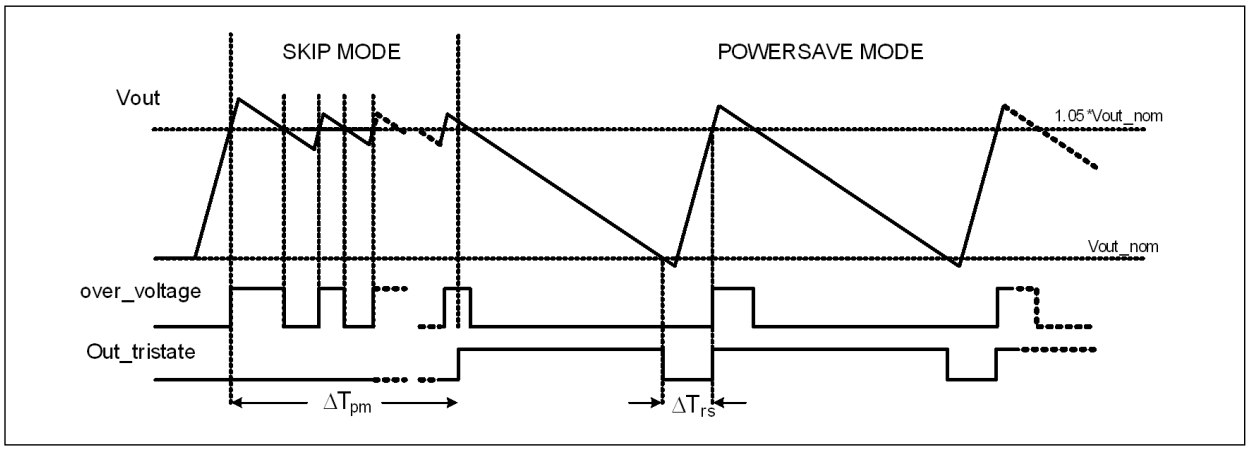
As a result, if the load current is not high enough to drain all the charge delivered by the PMOS in one clock cycle, the output will tend to diverge. Depending on VIN and VOUT values, this occurs when the load current stays below a value Ith that has an approximate range between 200mA and 600mA.

When an internal comparator, whose threshold is set 5% above the nominal value of the output voltage, detects an over-voltage event, the PMOS is immediately shut down. PMOS on-pulses are skipped until the output voltage drops below the over-voltage threshold. In case the load current has not significantly varied in the meantime, the next pulses will bring again the output voltage above the 5% of the threshold. This will initiate a new skip cycle where other PMOS on-pulses cannot be triggered. This sequence, called skip mode, is marked by an oscillation in a very narrow voltage range lying around 5% above the nominal value of VOUT.

As soon as the load current increases above the threshold Ith, the skip phase is terminated as the output does no longer diverge and an over-voltage event cannot take place.

Anyhow, the skip phase cannot last for a long time even if the load current still remains too low. The system replaces the skip operating mode with the Powersave Mode after a delay ΔTpm (typical a few tenth microseconds) which depends on the DC-DC converter loop bandwidth and the previous events of the system. In Powersave Mode the clock re-triggers a PMOS pulse only when the output voltage drops below its nominal value, no longer below the 5% of the threshold as previously described. If compared to skip mode, the Powersave Mode prolongs the interval when the DC-DC converter is not dissipating and this time is inversely proportional to the load current.

Figure 29. Typical waveform in Powersave Mode



The cycle in Figure 29 starts with a skip mode whose duration is limited. After a delay ΔTpm, the output driver switches to tristate and a restart is triggered after VOUT drops below the nominal value. Successive over_voltage events trigger automatically a powersave cycle, without passing through a skip mode, if the previous one has been terminated very lately. Over_voltage and Out_tristate signals are internal to the device and not available externally.

At clock restart after a powersave cycle, if the load current remains lower than Ith, the output voltage still increases. The over_voltage event puts the system automatically in Powersave Mode without passing through the initial skip mode cycle if the delay ΔTrs between the crossing of the nominal threshold and the over_voltage is less than a given amount.

The Powersave Mode only ends when the load current rises above the threshold and the output is no longer able to diverge. In this operating mode the DC-DC converter dissipates a minimum of energy. The output driver is not charged nor discharged for a long time and most of the analog circuitry is switched off to ensure less than 25µA current dissipation. The benefits over the system efficiency is very large.

Note: In powersave mode, the voltage ripple is larger than the one observed in normal operation, as it ranges from the nominal value to 5% in excess; at the same time, the ripple frequency is much smaller (it is no longer depending on the system clock and it's mostly determined by the output capacitor value and the load current).

Fixed Frequency Operation (MODE = low)

If the pin MODE is pulled to logic low, the Powersave Mode is disabled. In this operation mode the NMOS and the PMOS are always complementarily switching on and off, accordingly to the relationship D = VOUT / VIN, where D is the duty cycle of the on-pulses of the PMOS. As the minimum allowed duty cycle D is less than the minimum VOUT / VIN (according to the typical operation conditions), it is not possible that the output can diverge.

The possibility of driving also a negative current through the NMOS drains the residual charge coming from the minimum PMOS on-pulses that the load current cannot eventually remove. With mode low, the output rises above 5% of the threshold only in case of a large variation in the load current. Hence, unlike Powersave Mode, the skip mode is still present to avoid large overshoot which could lower the reliability. The PMOS is off for all the time, the output stays above 5% of the threshold and the NMOS is not allowed to discharge with a negative current. By avoiding the integration of negative currents in the coil, which might be large in module, this solution shows good damping properties and a smooth recovery for the output voltage.

Short-circuit protection

The AS1328 offers a foldback function. In case the output voltage is less than 2/3 of the nominal value and a first over-current event is detected, the clock frequency of the DC-DC converter drops to 1/8 of the nominal value. This means that, while the peak current is still limited to the over-current threshold, the larger ripple (which is proportional to the frequency) reduces the average value of the current from the DC-DC converter. The reduction depends on the value of the supply voltage VIN and the inductor.

As soon as VOUT increases above the foldback threshold, the clock frequency returns to the original value (1.5MHz nominal)

It is worth noting that, unlike traditional solutions, here it is not sufficient to detect an output voltage which is below the foldback threshold. It is also necessary to detect at least one over-current event before initiating the foldback condition. This prevents large negative spikes at the output from temporarily setting the system in foldback which would slow down the recovery. At the same time it keeps fairly large foldback thresholds for the output voltage. A higher foldback threshold poses the system on a safer side as it delivers much smaller currents in case the load resistance might have an intermediate value between the minimum allowed load and a short circuit.

Over-current protection

The AS1328 implements internal over-current protection. If the coil current exceeds a nominal threshold value (4.5A) a fast comparator triggers an internal signal which switches off the power PMOS. This signal is reset as soon as the power transistor is switched off, allowing the power PMOS to be switched on again within the next clock cycle. So the over-current protection of the device is working cycle by cycle.

The maximum DC load current of the AS1328 (3A) plus half the current ripple cannot exceed the over-current threshold (3.5A in worst case).

The over-current threshold of the AS1328 does not suffer from any reduction at high duty cycles because of the use of a fast current comparator whose input signal is unaffected by the slope compensation ramp. This ensures more accurate and prompter response of the current limiter.

High Duty Cycle and Dropout operation

If the conduction of the PMOS has a duty cycle less than 95% the device operates regularly (see Main control loop on page 12).

For output voltages requiring a duty cycle above 95%, the device operates in average of the different operating modes. The power PMOS remains permanently on for more successive clock cycles. As this makes the output voltage too high, the error amplifier output drifts lower to produce a smaller duty cycle, below or equal to 95%. The consequent reduction of VOUT re-triggers the permanent on-condition for the PMOS. As a result an average duty cycle is settled, able to keep the output voltage under regulation with a larger ripple, compared to the usual operating condition.

In case the input voltage drops below the output nominal value, the state machine that regulates the operation at high duty cycle forces the PMOS to stay permanently on. As a result the regulation loop is open and the situation is defined as dropout (similar to a LDO).

The difference between the input and the output voltage is called the dropout voltage. VDROP is the product of the on-resistance of the internal PMOS (RPMOS) and the load current. The parasitic resistance of the inductor is in series to RPMOS and influences the dropout as well.

Note: At a low VIN, the RPMOS switch increases and higher dropout values are found.

The 100% duty cycle operation achieves a long battery life time by taking full advantage of the entire battery range. Due to the absence of a clocked signal at both power MOSFETS gates, the converter power consumption is largely reduced which aids in extending battery life time.

Shutdown

Connecting EN to GND or logic low, places the AS1328 in shutdown mode and reduces the supply current to ≤1µA. In shutdown the control circuitry and the internal NMOS and PMOS turn off and SW becomes high impedance, disconnecting the input from the output. The output capacitance and load current determine the voltage decay rate. For normal operation connect EN to VIN or logic high.

Note: Pin EN should not be left floating.

Power-OK functionality (AS1328A only)

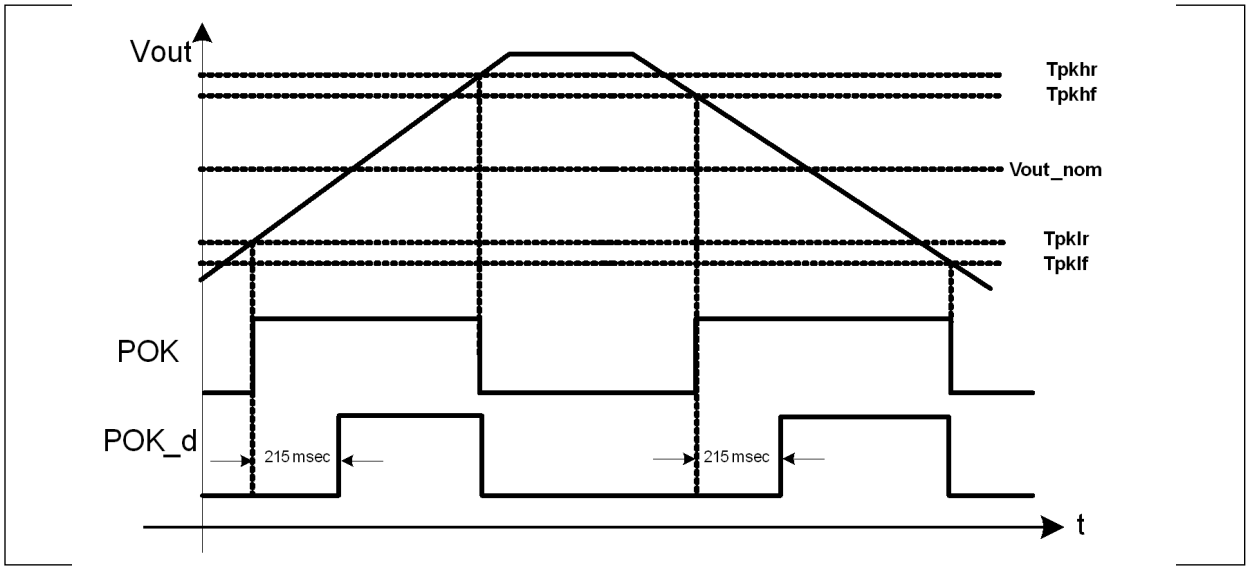
The AS1328A provides a Power-OK (POK) feature. The output voltage is monitored to stay within certain limits as shown in Figure 30.

A small hysteresis (2%) is implemented for the upper and lower limit thresholds to avoid multiple ringing of the POK output.

The POK pin is an open drain output and it's recommended to connect a 100kΩ resistor as pull-up resistor to VDD. The pull-up resistor is not meaningfully influencing the LOW level output at this pin. Higher values are allowed because of the very small leakage current from this pin.

The response time of the POK circuitry switching to LOW is only limited by a small internal filter which has been added to avoid signal bouncing in a noisy environment. The AS1328A offers two different options about the time for the LOW to HIGH transition. One option has a very similar response time for both transitions (POK signal in Figure 30), the other one (POK_d signal in Figure 30) implements a 215ms counter before the output is asserted.

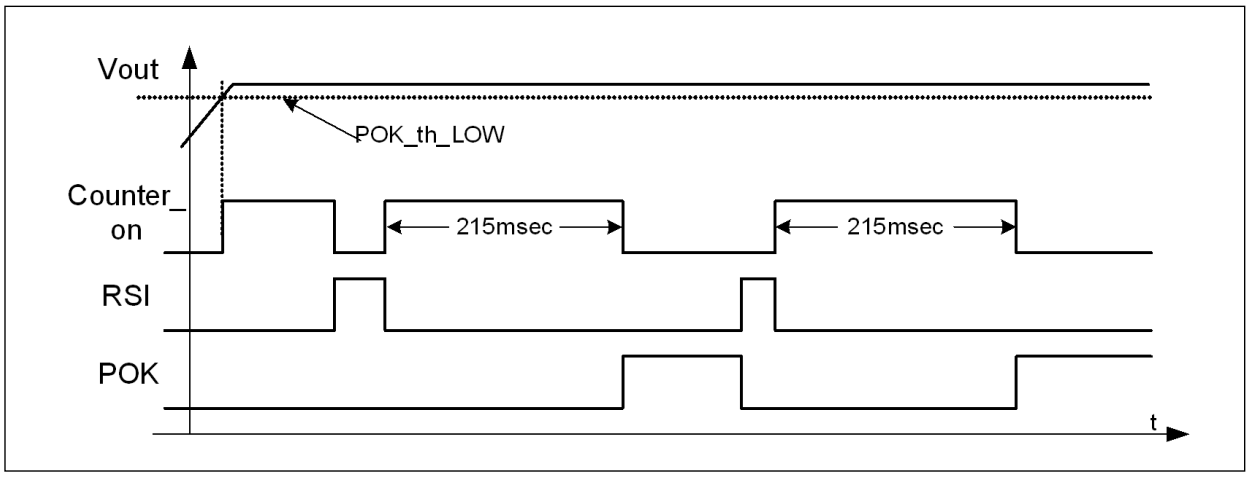
Figure 30. POK signals



RSI signal (AS1328A only)

The RSI feature allows the manual reset of the POK signal. As long as the input to RSI is high, the POK signal remains LOW, regardless of the output voltage condition. Particular interest is assumed by the option with the 215ms counter delay before asserting POK signal: a low to high transition of the RSI signal resets the internal counter (signal Counter_on in Figure 31 on page 16) which will assert the POK output only 215ms after RSI signal is released.

Figure 31. POK behavior and sequencing under RSI in the 215ms delay variant



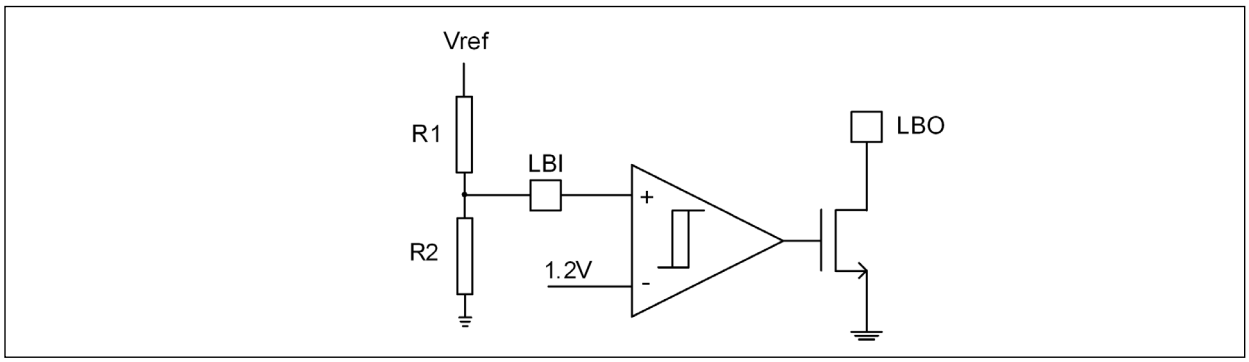
Note: Counter_on is an internal signal (it is not externally available) that enables the counter for 215ms delay generation.

Low Battery function (AS1328B only)

The Low Battery Function of the AS1328B allows to compare an external voltage at the Low Battery Input pin (LBI) with an internal reference voltage of 1.2V (typ.). The Low Battery Output pin (LBO), is low if the external voltage is lower than 1.2V and high otherwise. The input voltage at LBI pin must be referred to GND, not to PGND.

The LBO pin is an open drain output and has the same characteristics as the POK pin. The low leakage at the LBI pin allows the usage of large values for the external resistor to set up the switching threshold of LBO.

Figure 32. Low Battery Function Comparator



Softstart function

The AS1328 implements two softstart features.

The first one is a slow ramp which clamps the output of the error amplifier to control the inrush current. By limiting the increase rate of the on-pulse duration of the power PMOS, it automatically prevents a large current flow since the beginning of the DC-DC converter operation.

For a second step it's also possible to adjust the slew-rate of the output voltage ramp with a capacitor C_{SS} at SRC pin. The output of the converter will track the slow ramping signal at the SRC pin. The same can be achieved by forcing the SRC pin with a ramping voltage source.

Thermal shutdown

Due to its high efficiency design, the AS1328 does not dissipate much heat in most applications. However, in applications where the AS1328 is running at high ambient temperature the heat dissipated may exceed the maximum junction temperature of the device.

As soon as the junction temperature reaches approximately 150ºC, the AS1328 goes in thermal shutdown. In this mode the internal PMOS & NMOS switch are turned off. The device will power up again, as soon as the temperature falls below +135°C.

Undervoltage Lockout (UVLO)

The AS1328 has a built-in protection in case V_{IN} drops too low. The system is shutdown to prevent possible misfunction. An internal hysteresis ensures robustness to this function.

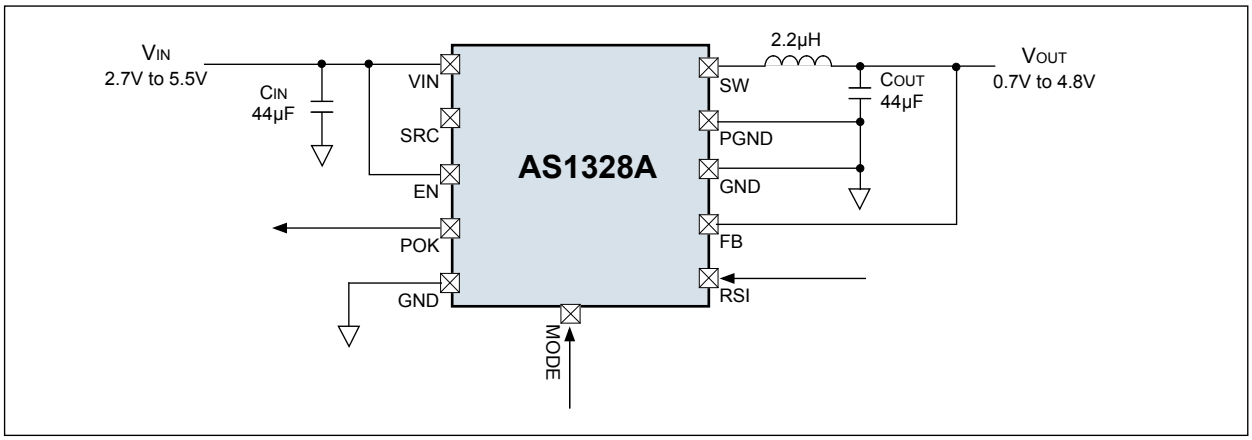
9 Application information

The AS1328 is perfect for mobile communications equipment, LED matrix displays, bar-graph displays, instrument-panel meters, dot matrix displays, set-top boxes, white goods, professional audio equipment, medical equipment, industrial controllers to name a few applications.

Fixed Output Voltage

For the fixed output voltage (available from 0.7V to 4.8V, see Ordering information on page 29) connect pin FB to VOUT (see Figure 33).

Figure 33. AS1328 - Fixed Output Version



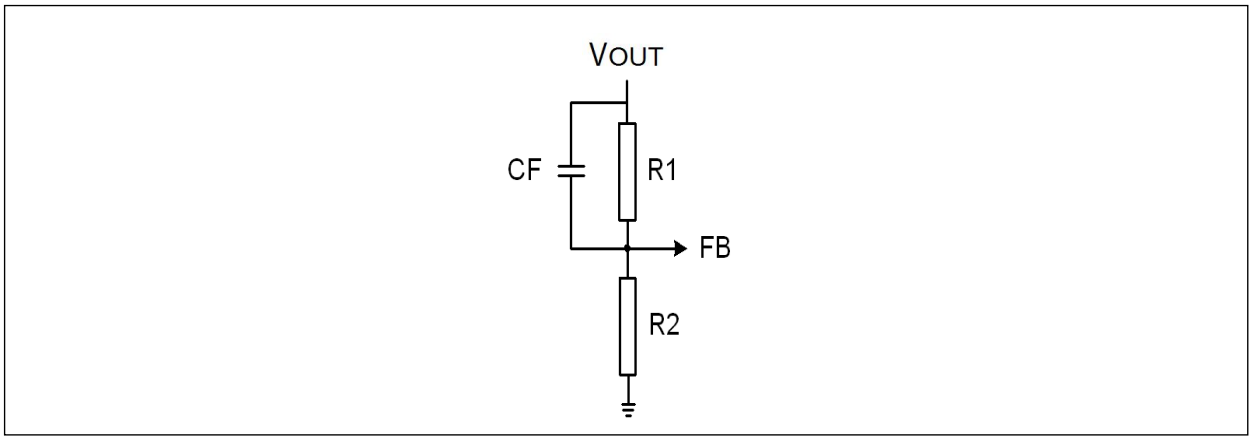
Adjustable Output Voltage

For the adjustable output voltage version connect a voltage divider to pin FB (see Figure 34).

The voltage divider from VOUT to GND programs the output voltage from 0.6V to VIN via pin FB as:

$$V_{OUT} = 0.6V(1 + (R_1/R_2)) \quad \text{(EQ 1)}$$

Figure 34. AS1328 - External net for the Adjustable Output Version



The upper terminal of resistor R_1 must be connected directly to the load capacitor positive terminal, while the lower terminal for R_2 must be connected the signal ground GND. About R_1 and R_2 resistor values, the upper limits come from the leakage current at FB pin. Usually values less than 1MW provide accurate enough solutions.

In addition, thinking of the stability of the system, it is welcome to add a capacitor CF in parallel to R_1. This improves the phase margin and improves load transient performances by bringing the output spike from the load to FB pin without any significant attenuation.

In order to accomplish this, it is welcome to have R_2*CF time constant inside the gain bandwidth of the device. Usually the choice R_2*CF = 100ms is sufficient. Higher values should be carefully evaluated as the settling time will be limited by the time constant R_1*CF. In case R_1/R_2 is quite large (i.e. large V_{OUT} values), the settling may become longer than the one foreseen by the internal soft start circuitry. Of course this limit can be remarkably relaxed in case an external soft start capacitor Css is used.

Soft start capacitor selection (C_{SS})

The SRC pin is capable of sourcing a pull-up current of 4µA. Until the voltage does not reach 600mV, SRC provides the reference voltage to startup the DC-DC converter.

A nominal 1ms startup time structure is implemented on-chip, hence capacitors lower than 4µA*1ms/0.6V = 6.7nF are not effective in changing the startup time of the device.

Higher values for C_{SS} will determine a soft start time t_{SS} for the DC-DC converter as follows:

$$t_{SS} = 0.6V * C_{SS}/4\mu A \qquad \text{(EQ 2)}$$

under the assumption t_{SS}>>1ms.

For example: a C_{SS} of 100nF would make nearly 15ms as soft start time.

As an alternative to the capacitor C_{SS}, a voltage source V_{SRC} can be used to force the SRC pin. Two constraints must be considered to ensure accuracy:

- V_{SRC} must be able to drain 4µA nominal current;
- after start-up, V_{SRC} must stop at a higher voltage than 0.6V, to not affecting the steady state value; a suggested safety margin is to settle V_{SRC} above 1V.

Note: In case V_{SRC} steady state value is below 450mV, it is possible to have a scaled down version of the output voltage (V_{SRC}/0.6 smaller than the nominal value).

External component selection

Inductor selection

The choice for the coil must take into account several and sometimes contradictory requirements.

Usually the selection suggests small values for the following reasons:

1) improved load transient response: a larger coil is less prone to change its current;

2) efficiency at heavy loads: the series parasitic of the coil directly contributes to power dissipation depending on i_L^2. As a larger coil value means more turns of wire and hence a larger series parasitic, a small value for L is welcome when efficiency is a key parameter;

3) stability and jitter: in a current mode DC-DC converter, stability is ensured with large margins because the replica of the ramping current in the power PMOS is sent to the input of the PWM comparator. A smaller slope, i.e. a larger coil, makes the switching time of the comparator more sensitive to noise. In this way the duty cycle would suffer from jitter. To make matter worse, if the coil is large, the replica of the ramping current becomes quite smaller than the slope compensation ramp and the system tends to behave like a voltage mode converter where stability constraints are usually stricter and the device may oscillate.

Anyhow it is not possible to ignore those following reasons which recommend a larger coil value.

Peak current limitation

The positive current ripple brings the PMOS current temporarily higher than the average one. Care must be taken not to reach the over-current limit. If a large ripple is accepted, larger margins must be taken between the maximum DC load current I_{OUTMAX} and the over-current threshold $I_{OVERCURRENT}$ as follows.

$$0,5 \times \Delta i_R \leq I_{OVERCURRENT} - I_{OUTMAX} \quad \textit{(EQ 3)}$$

Being Δi_R the ripple current given by the following:

$$\Delta i_R = \frac{V_{IN} - V_{OUT}}{L} \times T_{ON} \quad \textit{(EQ 4)}$$

At the same time, as soon as the load current equals half of the ripple current, the current in the coil would reverse polarity and the NMOS must be disconnected to prevent the load from being discharged. This means that a larger coil extends the range where the converter operates in continuous mode.

Output voltage ripple reduction

While node SW is digitally switching from positive to negative rail, the LC circuit acts as a filter to “clean” the regulated output voltage V_{OUT}. Clearly a larger inductor improves the amount of filtering and provides a less disturbed reference voltage. Anyhow, voltage ripple reduction is usually optimized by acting on the load capacitor value instead and leaving the inductor value free to comply with other requirements.

Slope compensation effectiveness

A current mode converter oscillates at duty cycle above 50% if no slope compensation is adopted. Slope compensation ramp is injected in parallel to the replica PMOS ramping current in order to accomplish the desired stabilization of the loop. Small values for the inductor could make the on-chip slope compensation (which is a design parameter and cannot be modified by the user) insufficient. In addition the on-chip circuitry might suffer from dynamic range limitation, if the device operates at small supply voltage. After taking into consideration all the above mentioned requirements, in the table below the user can find the suggested coil values.

Table 4. Recommended values for Output Capacitor and Inductor

VOUT [V]	COUT [µF]	minimum Inductor [µH]	maximum Inductor [µH]
< 1.5	> 2x22	1.0	2.2
< 2.5	> 2x22	1.5	3.3
< 3.6	> 2x22	2.2	4.7
< 5	> 2x22	3.3	4.7

The dependence of the suitable range for L depends on V_{OUT} to provide optimal value for slope compensation. Accordingly to the basic requirement

$$Slope\ compensation\ ramp\ > \frac{V_{OUT}}{2L} \quad \textit{(EQ 5)}$$

it is remarkable to underline that in case the equality

$$Slope\ compensation\ ramp\ = \frac{V_{OUT}}{2L} \quad \textit{(EQ 6)}$$

holds, it is possible to show that excellent AC PSRR can be provided. On the other side, if the slope compensation is twice the boundary as shown in Equation (EQ 6), any error in the sensed current is removed in one clock cycle.

The values in Table 4 are the recommended ones to comply with reasonable trade off between the several possible performances. Focusing on some particular applications, it may be possible to slightly differ from what the table reports. While there are very little margins if moving to smaller coils, it is possible to search for higher coil values, once paying attention to the above mentioned pro and contra.

Reliability issue for the inductor value

The selected inductor must be rated for its DC resistance and saturation current. In Equation (EQ 4) the ripple current Δi_R in PWM mode is reported. The saturation current I_{Lsat} of the inductor should be rated higher than the maximum inductor current I_{Lmax} accordingly to the following, straightforward, relationship:

$$I_{Lsat} > I_{Lmax} = I_{OUT} + \frac{\Delta i_R}{2} \quad \textit{(EQ 7)}$$

Where:

I_{Lsat} = Inductor saturation current

I_{Lmax} = Maximum inductor current

I_{OUT} = Maximum DC load current

Δi_R = Peak to peak inductor ripple current.

At inductor saturation, the inductance value drops abruptly and would alter the DC-DC converter characteristic.

Output capacitor selection

Value of the output capacitor

Output capacitor selection is usually less critical than the inductor one. Larger values are usually welcome from the design point of view: improved stability, smaller spikes after a load transient event, smaller voltage ripple make this choice extremely amenable. As the only drawback, we might note that at quite large load capacitors the in-rush current might meaningfully increase. At the same time, clearly, presence of capacitor series parasitic, PCB board area occupation as well as cost issues must be taken into consideration before moving to high values.

The AS1328 design is optimized for a load capacitor equal to 2x22µF. Of course values up to 100µF can be used as well without problems.

ESR resistance of the output capacitor

The selection of the output capacitor is also alleviated by the current mode architecture. Unlike voltage mode converters, stability does not rely upon the presence of fairly large values of the series parasitic resistance r_{ESR}. ESR resistance contributes to the output voltage ripple ΔV_{OUT} as foreseen by the expression below:

$$\Delta V_{OUT} = \Delta i_R \times \left(r_{ESR} + \frac{1}{8 \times C_{OUT} \times f} \right) \quad \textit{(EQ 8)}$$

where it is clear that low ESR, high value capacitor choice is a key feature for voltage ripple reduction. Because of their lowest ESR contribution, ceramic capacitors and X7R or X5R dielectrics are recommended.

Reliability of the output capacitor

At high load currents, where the device operates in PWM mode, the RMS ripple current in the output capacitor is calculated as:

$$I_{RMSC_{OUT}} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad \textit{(EQ 9)}$$

This value must be taken into account to ensure reliability for the load capacitor.

Input capacitor selection

In analogy to the output capacitor also here we consider three main features: value of the capacitance, ESR and ESL parasitic impedance and RMS current for reliability issues.

Value of the input capacitor

Anytime the power PMOS turns on, the current must be suddenly sourced by the supply line V_{IN}. Usually it is not sufficient to use a large capacitor. First of all it must be located as near as possible to the supply pin. If, as a rule of thumb, a capacitor as large as the output one provides acceptable performance, care must be taken also to ensure low series impedance either resistive (ESR) or inductive (ESL), otherwise they will be responsible of spikes and ringing that the capacitor cannot attenuate. Use of X5R or X7R dielectric is still recommended both for low parasitic and excellent thermal characteristics.

It is better to use ceramic capacitor with a higher rated voltage than necessary, otherwise their value will become too small at the highest voltage drop. Anyhow be careful, as higher rated voltage capacitors usually are affected by larger series parasitic.

If possible, it is also good to add in parallel a small ceramic capacitor to bypass the series parasitic of the main one. Moreover, in case high accuracy is required, an arrangement like the one proposed in Figure 35 on page 25 is welcome to separate power and core lines.

Reliability of the input capacitor

Due to the pulsed nature of the waveform, the current which crosses the input capacitor is much larger than the one across the load capacitor, determined only by the ripple. As a result, it can be shown that the maximum RMS current in the input capacitor is given by the following formula:

$$I_{RMSCIN} = I_{LOAD}\sqrt{D \times (1 - D)} \quad \textit{(EQ 10)}$$

Where: D is the duty cycle.

This formula shows that the RMS current has a maximum at 50% Duty Cycle and it may be as large as half the load current.

Thermal considerations

Thanks to the high efficiency of AS1328, power dissipation is limited. Anyhow, high external temperature might be critical: R_{PMOS} becomes remarkably worst and increases dissipation and on-chip temperature.
A built-in thermal protection stops the device in case of excessive on-chip temperature. This puts a limit on the maximum external temperature of the device, or, alternatively, on the maximum load current at high external temperature.
The following example shows that AS1328 design and package characteristics are good enough to ensure reasonable safety margins for most operating conditions. Anyhow the example is not inclusive of any worst condition so that it is recommended to carry out a similar thermal analyses depending case by case.
Let us suppose that the device is running at I_{LOAD} =3A and the external temperature T_A is 90°C. Assume also a supply voltage equal to 3.3V.
At heavy loads, the chip dissipation P_{DISS} is almost entirely due to the on resistance of the power transistors:

$$P_{DISS} = [D * R_{PMOS} + (1-D)* R_{NMOS}] * I_{LOAD}^2$$

Being D the duty cycle, RPMOS and RNMOS the on-resistance of the PMOS and the NMOS respectively.

If we assume, for sake of simplicity, that the on-resistance is the same for the PMOS and NMOS, $R_{DS(ON)}$, the dissipated power in the chip can be simply written as:

$$P_{DISS} = R_{DS(ON)} * I_{LOAD}^2$$

The thermal resistance Θ_{JA} of the package allows us to calculate the junction temperature T_J accordingly to the formula:

$T_J = T_A + P_{DISS} * \Theta_{JA} = T_A + R_{DS(ON)} * I_{LOAD}^2 * \Theta_{JA}$

Replacing the value obtained for $R_{DS(ON)}$ (50mΩ) at T_A = 90°C and 3.3V supply and Θ_{JA} = 36.7°C/W it results:

T_J = 0.450W * 36.7°C/W + 90°C = 107°C

Hence some safety margins are provided versus the specified limit of 125°C.
At higher temperature this margin reduces not only because T_J tracks T_A, but also because $R_{DS(ON)}$ is worse.
In addition, even if this looks a surprise if compared to a common feeling about power dissipation, more problems come from a smaller supply voltage as $R_{DS(ON)}$ gets larger.

In case the junction temperature reaches approximately 160°C, both power switches will be turned off and the SW node becomes high impedance. The circuit will restart, with a new start-up sequence, only after the temperature drops below 135°C nominal.
To maximize the thermal performance the Exposed Pad should be soldered to a ground plane.

Recommended external components

When choosing ceramic capacitors for CIN and COUT, the X5R or X7R dielectric formulations are recommended. These dielectrics have the best temperature and voltage characteristics for a given value and size. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies and therefore should not be used.

Table 5. Recommended external components

Name	Part Number	Value	Rating	Type	Size	Manufacturer
CIN, COUT	GRM21BR60J226ME39	22µF	6.3V	X5R	0805	Murata www.murata.com
L	XFL4020-102MEC	1.0µH	4.5A	11mΩ	4.0x4.0x2.10mm	Coilcraft www.coilcraft.com
L	XFL4020-152MEC	1.5µH	4.1AA	14mΩ	4.0x4.0x2.10mm	Coilcraft www.coilcraft.com
L	LPS6225-222MLC	2.2µH	3.9A	45mΩ	6.8x6.0x2.4mm	Coilcraft www.coilcraft.com
L	XAL6030-332MEC	3.3µH	4.9A	20mΩ	6.56x6.36x3.1mm	Coilcraft www.coilcraft.com
L	MSS1048-472NLC	4.7µH	4.36A	12mΩ	10.2x10.0x4.8mm	Coilcraft www.coilcraft.com
L	XAL6060-472MEC	4.7µH	5A	14.9mΩ	6.56x6.36x6.1mm	Coilcraft www.coilcraft.com

Efficiency

The efficiency of a regulator is the ratio between the power in the load and the total dissipated one.

The choice of the external components might play a role also regarding this parameter. Besides all the losses which are internal to the device, it is mandatory to take care about PCB design and external components selection to achieve optimal performances.

- Any trace on the PCB which is crossed by the load current plays the same role as the power MOSFET on-resistance in determining conduction losses.
- The same consideration holds for the parasitic resistance of a coil, which makes a non negligible contribution.
- A minor, but still significant, contribution might come also from ESR parasitic from both CIN and COUT capacitors. CIN undergoes a RMS current which is a fraction of the load one and, depending on the duty cycle of the regulation, it may be as high as half of the load current. Being COUT crossed by the ripple current, which is quite smaller than the load one, its contribution is usually inferior to the one from the input capacitor.

Total efficiency versus load current

At heavy loads, as dissipation from the power MOS on-resistance is the dominating contribution, a higher supply value reduces the channel resistivity and improves efficiency. As the loss due to on-resistance depends on I_{LOAD}^2 while the power in the load is simply proportional to ILOAD, the efficiency tends to decrease with the load current.

At light loads, when the DC-DC converter internal switching losses are the most important ones, a higher supply voltage increases the dissipation and a lower efficiency comes. Moreover, being switching losses independent from the load current, a load current increase in its lower range improves the efficiency. At very light loads, a very remarkable reduction in efficiency is found in case powersave feature is not exploited.

Efficiency in Powersave Mode

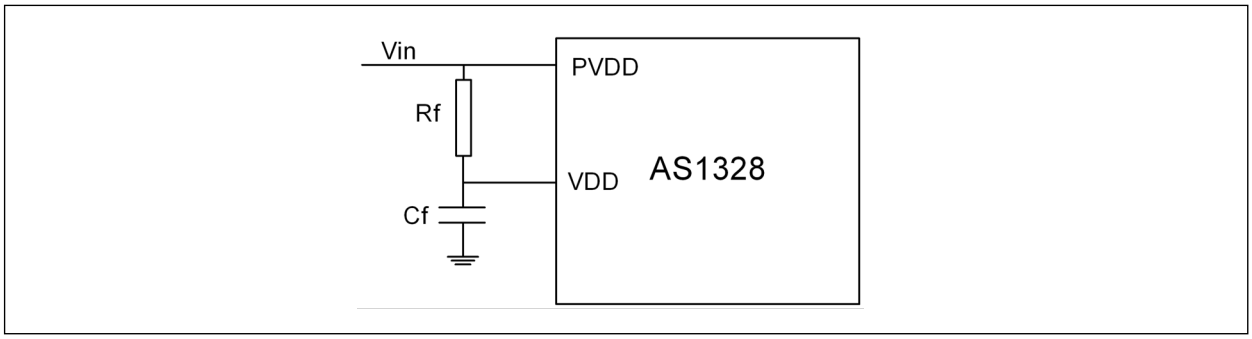
The previous consideration about light loads shows the benefits coming from Powersave Mode: at very light loads (less than 200mA – 600mA, depending on operating conditions) the clock is stopped and all the switching losses are cancelled. Also the I^2R losses from the power MOSFET and the coil disappear because the output driver is in high impedance. The only significant contributions come from the device quiescent current and the dissipation taking place when the output driver is temporarily powered up at the same rate as the ripple frequency. The associated power consumption is quite small, thus allowing still appreciable values for the efficiency. Being both the quiescent current and the switching losses increasing vs. VIN, a lower supply ensures better performance.

Note: MODE=0 option does not simply imply that powersave operation cannot be triggered. It also allows the partial discharge of the load capacitor in DCM mode. This fact contributes to an even worse efficiency.

Split rail operation

The AS1328 separates the output driver supply pin PVDD from the core one VDD. System noise rejection and accuracy are largely improved by means of a filter as shown in Figure 35. Due to the small power consumption in the core, it is possible to put a small resistance Rf in series to the core supply. Recommended value for Rf = 1Ω. At the same time, a capacitor Cf equal to 1µA guarantees that the switching noise at PVDD does not meaningfully affect the core supply VDD.

Figure 35. Split power and signal supply for improved noise rejection



Layout considerations

The AS1328 requires proper layout and design techniques for optimum performance.

- The power traces (GND, SW and VIN) should be kept as short, direct and wide as is practical.
- Pin FB should be connected directly to the Output Voltage.
- The positive plate of CIN should be connected as close to VIN as is practical since CIN provides the AC current to the internal power MOSFETs.
- Switching node SW should be kept far away from any sensitive node as FB, SRC and LBI.
- The negative plates of CIN and COUT should be kept as close to each other as is practical. A starpoint to GND is recommended.
- Inputs at pins LBI and SRC as well as the external resistor divider for the adjustable version at FB pin must be referred to the signal ground GND, not PGND.
- Same consideration holds for all other digital input signals. AS1328 digital input drivers are supplied by VDD and GND instead of PVDD and PGND. Due to the large noise margin of a digital signal, this solution is simply welcome but not mandatory.