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# AS1374

## Dual 200mA, Low-Noise, High-PSRR, Low Dropout Regulator

## General Description

The AS1374 is a low-noise, low-dropout linear regulator with two separated outputs. Designed to deliver 200mA continuous output current at each output pin, the LDOs can achieve a low 120mV dropout for 200mA load current and are designed and optimized to work with low-cost, small-capacitance ceramic capacitors.

An integrated P-channel MOSFET pass transistor allows the devices to maintain extremely low quiescent current (30µA).

The AS1374 uses an advanced architecture to achieve ultra-low output voltage noise of 20µVRMS and a power-supply rejection-ratio of better than 85dB (@ 1kHz).

Two active-High enable pins allows to switch on or off each output independently from each other.

The AS1374 requires only 1µF output capacitor for stability at any load.

The device is available in a 6-bump WLCSP package.

*Ordering Information and Content Guide appear at end of datasheet.*

### Key Benefits & Features

The benefits and features of AS1374, Dual 200mA, Low-Noise, High-PSRR, Low Dropout Regulator are listed below:

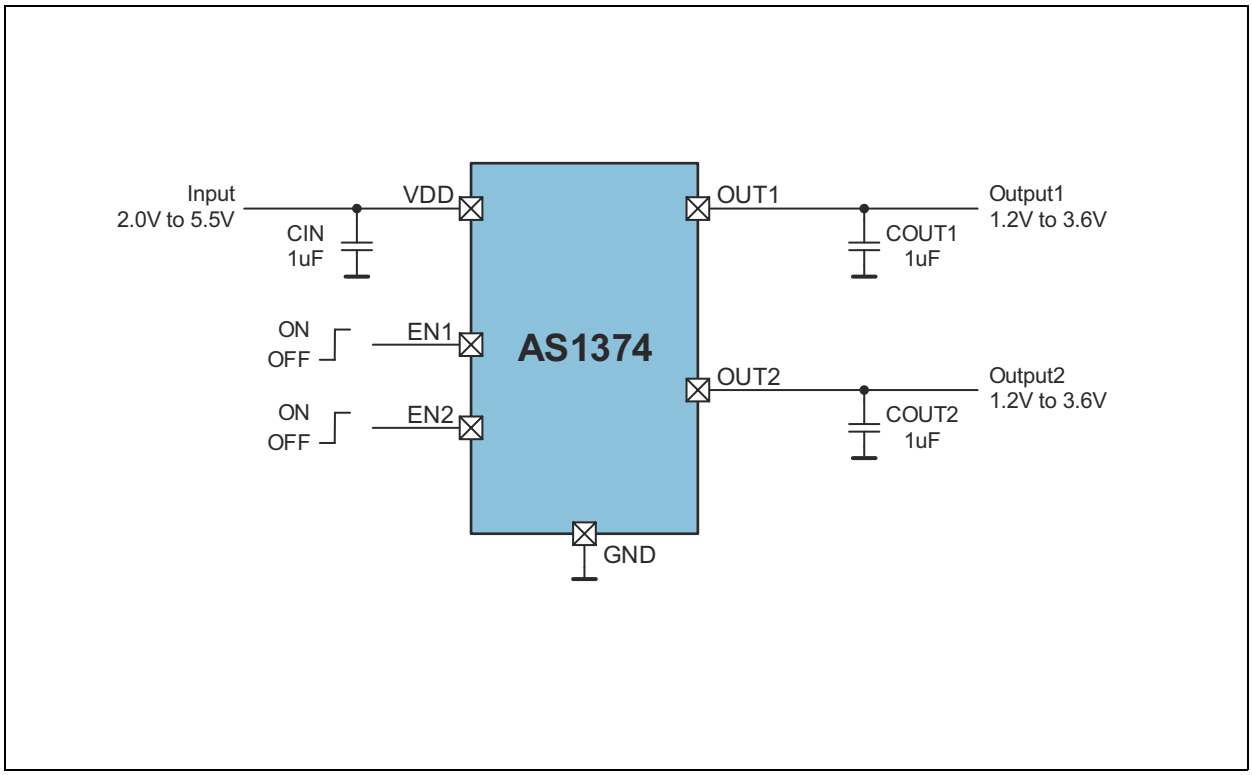
**Figure 1:**
**Added Value of Using AS1374**

| Benefits | Features |
|---|---|
| • Ideal for battery-powered applications | • Input voltage from 2.0V to 5.5V<br>• Low quiescent current of 30µA<br>• Low dropout of 120mV at 200mA load |
| • Supports a variety of end applications | • Output voltage from 1.2V to 3.6V<br>• Guaranteed output current of 200mA<br>• Pull-down option in shutdown (factory set) |
| • Overtemperature and overcurrent protection and shutdown | • Integrated temperature and output power monitoring |
| • Cost-effective, small PCB area needed | • Small external components needed<br>• Small 6-balls WLCSP package |

## Applications

The devices are ideal for mobile phones, wireless phones, PDAs, handheld computers, mobile phone base stations, Bluetooth portable radios and accessories, wireless LANs, digital cameras, personal audio devices, and any other portable, battery-powered application.

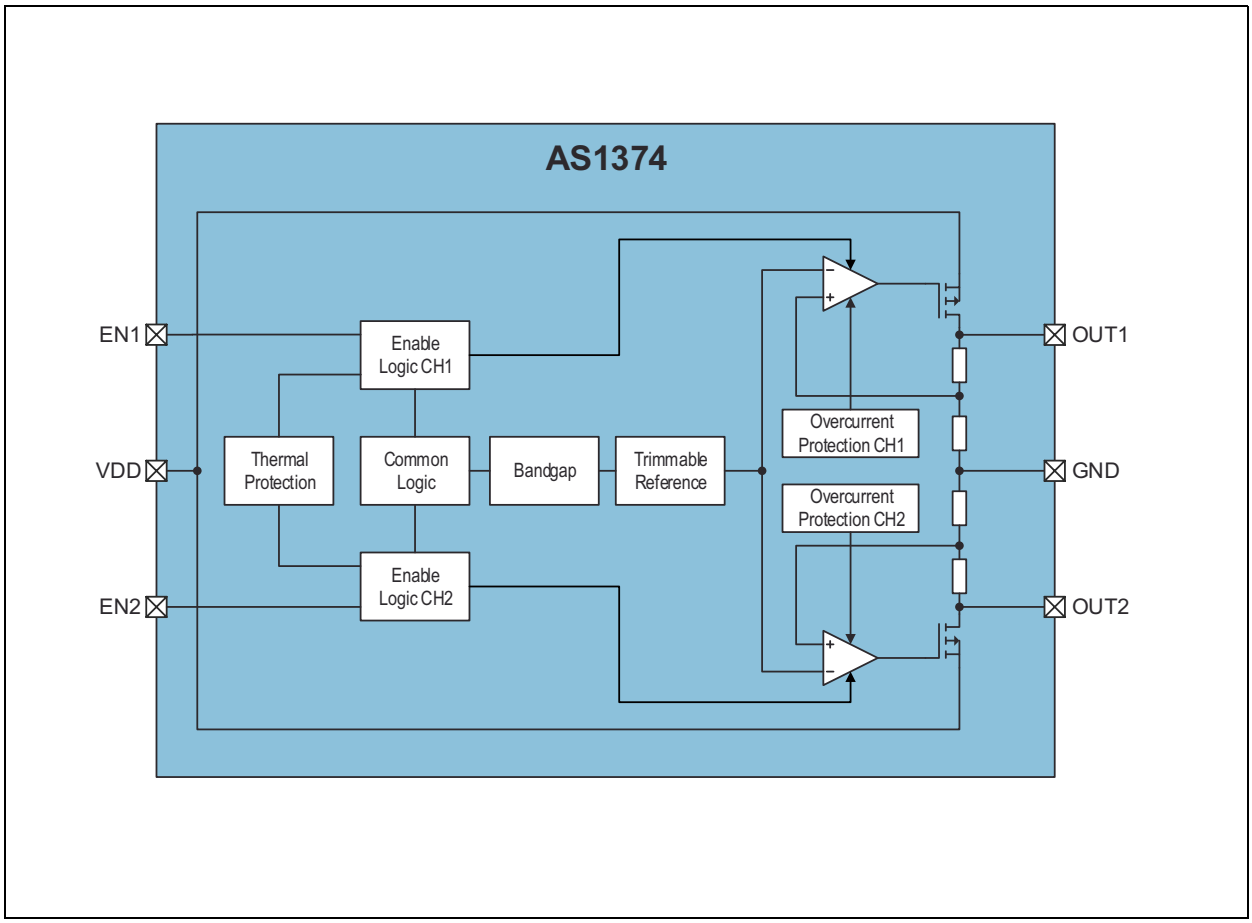
**Figure 2:**
**A1374 Typical Application Circuit**



## Block Diagram

The functional blocks of this device are shown below:

**Figure 3:**
**A1374 Block Diagram**



## Pin Assignment

Figure 4:
Pin Diagram

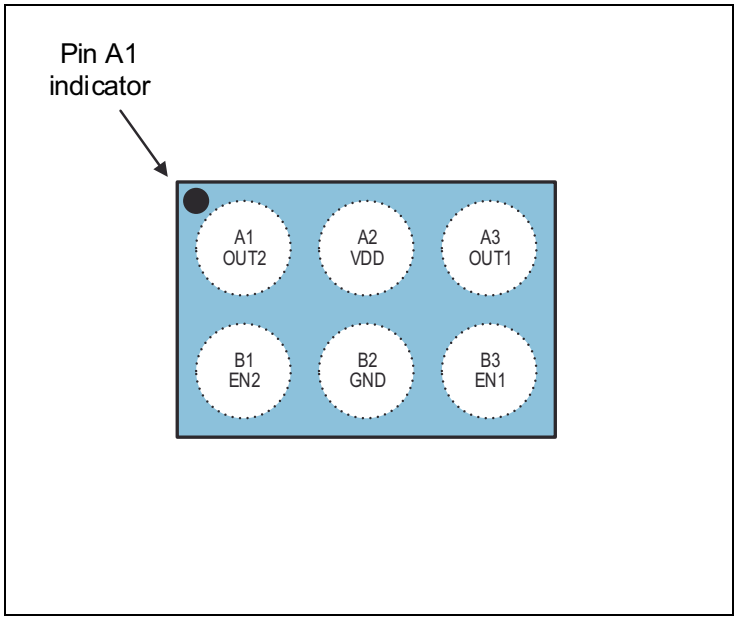



Figure 5:
Pin Descriptions

| Pin Number | Pin Name | Description |
|---|---|---|
| A1 | OUT 2 | Regulated Output Voltage 2. Bypass this pin with a capacitor to GND. See Application Information for capacitor selection. |
| A2 | VDD | Input Supply |
| A3 | OUT 1 | Regulated Output Voltage 1. Bypass this pin with a capacitor to GND. See Application Information for capacitor selection. |
| B1 | EN 2 | Enable 2. Pull this pin to logic low to disable Regulated Output 2 voltage. |
| B2 | GND | Ground |
| B3 | EN 1 | Enable 1. Pull this pin to logic low to disable Regulated Output 1 voltage. |

## Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 6:**
**Absolute Maximum Ratings**

| Parameter | Min | Max | Units | Comments |
|---|---|---|---|---|
| **Electrical Parameters** | | | | |
| VDD to GND | -0.3 | 7 | V | |
| All other pins to GND | -0.3 | VDD + 0.3 | V | |
| Output short-circuit duration | | Infinite | | |
| Input current (latch-up immunity) | -100 | 100 | mA | JEDEC 78 |
| **Electrostatic Discharge** | | | | |
| Electrostatic discharge HBM | ±2 | | kV | MIL 883 E method 3015 |
| **Temperature Ranges and Storage Conditions** | | | | |
| Thermal resistance $\Theta_{JA}$ | | 201.7 | °C/W | Junction-to-ambient thermal resistance is very dependent on application and board-layout. In situations where high maximum power dissipation exists, special attention must be paid to thermal dissipation during board design. |
| Junction temperature | | 125 | °C | |
| Storage temperature range | -55 | 150 | °C | |
| Package body temperature | | 260 | °C | The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* |
| Relative humidity non-condensing | 5 | 85 | % | |
| Moisture sensitivity level | 1 | | | Maximum floor life time of Unlimited |

## Electrical Characteristics

$V_{IN} = V_{OUT} + 0.5V$, $V_{OUT} = 2.85V$, $C_{IN} = C_{OUT} = 1\mu F$, Typical values are at $T_{AMB} = 25°C$ (unless otherwise specified). All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

**Figure 7:**
**Electrical Characteristics**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{AMB}$ | Operating Temperature Range | | -40 | | 85 | °C |
| $V_{IN}$ | Input Range | | 2 | | 5.5 | V |
| $\Delta V_{OUT}$ | Output Voltage Accuracy | $I_{OUT}$ = 1mA, $T_{AMB}$ = 25°C | -1 | | +1 | % |
| | | $I_{OUT}$ = 100µA to 200mA, $T_{AMB}$ = 25°C | -1.5 | | +1.5 | |
| | | $I_{OUT}$ = 100µA to 200mA | -2.5 | | +2.5 | |
| $I_{OUT}$ | Maximum Output Current | Each channel | 200 | | | mA |
| $I_{GND}$ | Ground Current | One channel on, $I_{OUT}$ = 50µA | | 25 | 50 | µA |
| | | One channel on, $I_{OUT}$ = 200mA | | 30 | 55 | µA |
| $I_{LIMIT}$ | Current Limit | OUT = short | 210 | 300 | 400 | mA |
| | Dropout Voltage[1] | 2V ≤ $V_{OUT}$ < 2.5V, $I_{OUT}$ = 100mA | | 80 | 150 | mV |
| IQ | Quiescent Current | Both channels on, $I_{OUT}$ = 0.05mA | | 30 | 90 | µA |
| | | Both channels ON, $V_{IN} = V_{OUTNOM}$ - 0.1V, $I_{OUT}$ = 0mA | | 50 | | |
| $V_{LNR}$ | Line Regulation | $VI_N$ = ($V_{OUT}$ +0.5V) to 5.5V, $I_{OUT}$ = 1mA | | 0.02 | | %/V |
| $V_{LDR}$ | Load Regulation | $I_{OUT}$ = 1 to 200mA | | 0.0005 | | %/mA |
| $I_{SHDN}$ | Shutdown Current | OUT 1 and OUT 2 disable | | 0.01 | 2 | µA |
| PSRR | Ripple Rejection | f = 1kHz, $I_{OUT}$ = 10mA | | 85 | | dB |
| | | f = 10kHz, $I_{OUT}$ = 10mA | | 65 | | |
| | | f = 100kHz, $I_{OUT}$ = 10mA | | 50 | | |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Output Noise Voltage (RMS) | f = 100Hz to 100kHz, $I_{LOAD}$ = 20mA | | 20 | | µV |
| **Enable** | | | | | | |
| | Enable Input Bias Current | | | 0.01 | | µA |
| | Enable Exit Delay (2) | Both channels initially OFF | | 150 | | µs |
| | | One channel initially OFF | | 200 | | |
| | Enable Logic Low Level | | | | 0.4 | V |
| | Enable Logic High Level | | 1.4 | | | V |
| **Thermal Protection** | | | | | | |
| $T_{SHDN}$ | Thermal Shutdown Temperature | | | 160 | | °C |
| $\Delta T_{SHDN}$ | Thermal Shutdown Hysteresis | | | 15 | | °C |
| $C_{OUT}$ | Output Capacitor | Load Capacitor Range | 0.47 | | 10 | µF |
| | | Maximum ESR Load | | | 500 | mΩ |

**Note(s):**

1. Dropout is defined as VIN - VOUT when VOUT is 100mV below the value of VOUT for VIN = VOUT + 0.5V.
2. Time needed for VOUT to reach 90% of final value.

## Typical Operating Characteristics

$V_{IN} = V_{OUT} + 0.5V$, $V_{OUT} = 2.85V$, $C_{IN} = C_{OUT} = 1\mu F$, $T_{AMB} = 25°C$ (unless otherwise specified).

**Figure 8:**
**Output Voltage vs. Temperature**

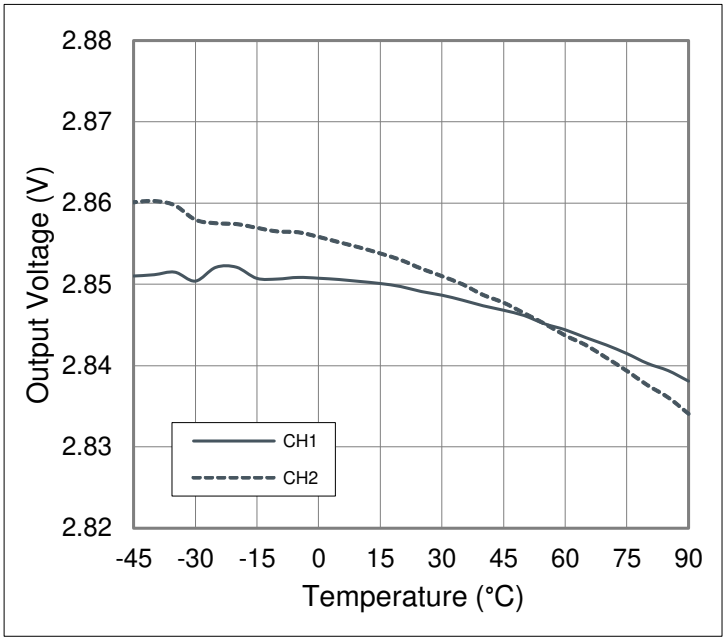



**Figure 9:**
**Output Voltage vs. Input Voltage**

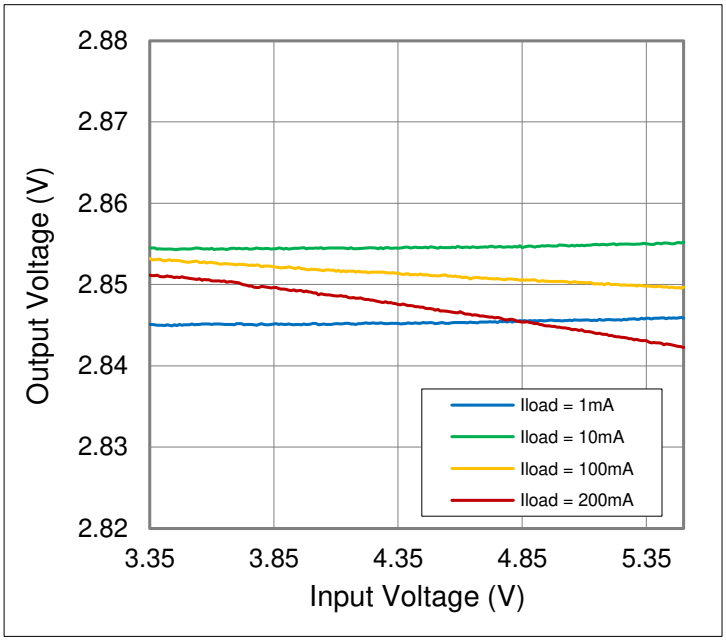


**Figure 10:**
**Output Voltage vs. Load Current**

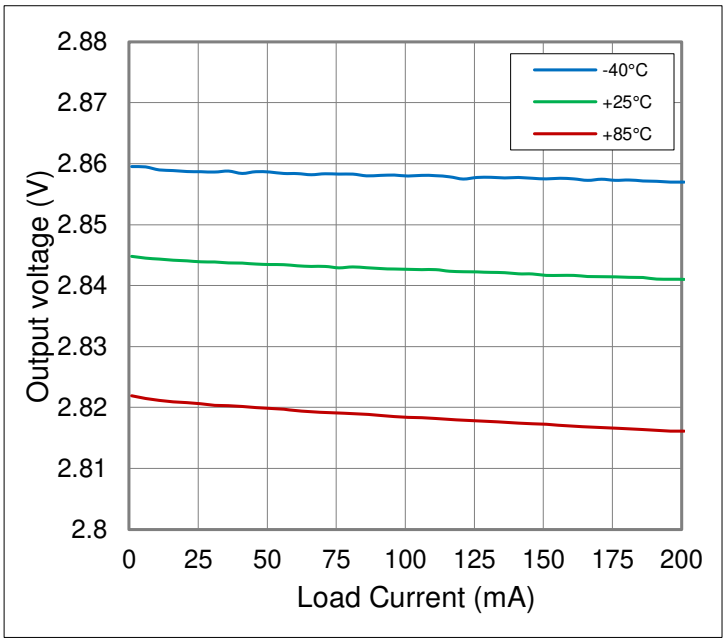



**Figure 11:**
**Output Voltage vs. Input Voltage - Dropout**

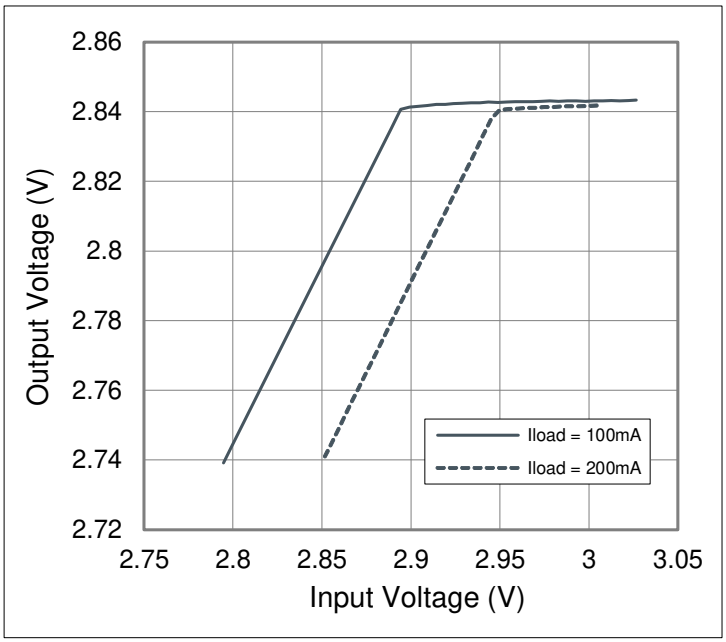


**Figure 12:**
**Dropout Voltage vs. Load Current**

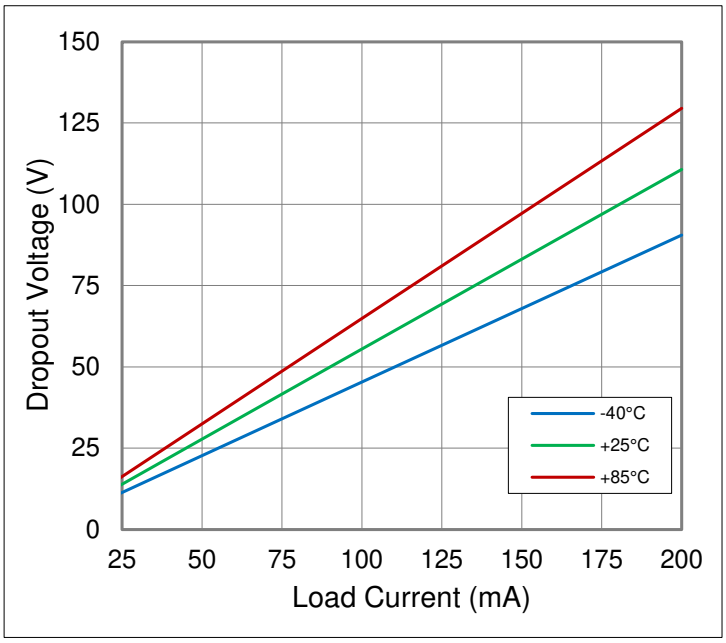



**Figure 13:**
**PSRR vs. Frequency**

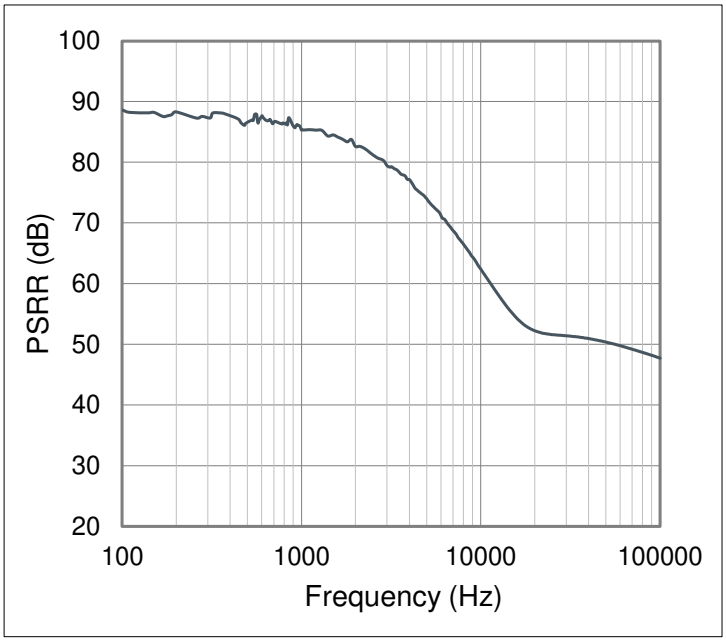


**Figure 14:**
**Ground Pin Current vs. Load Current**

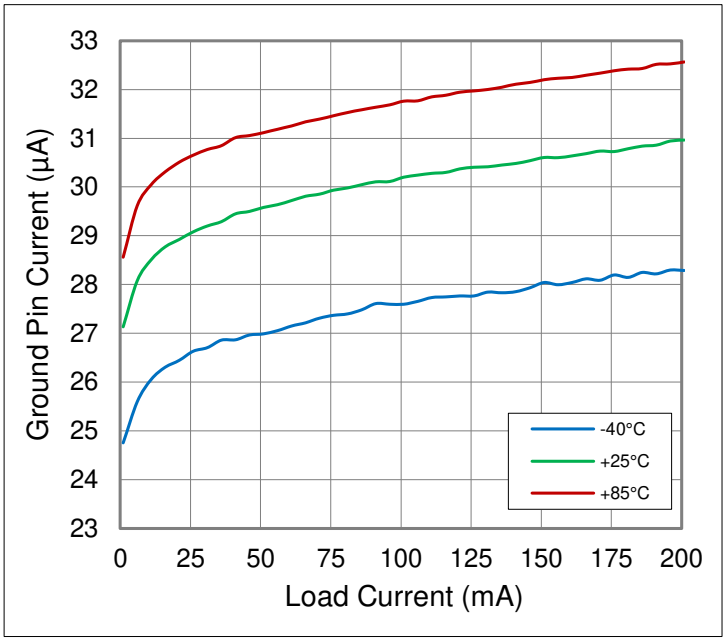



**Figure 15:**
**Ground Pin Current vs. Temperature**

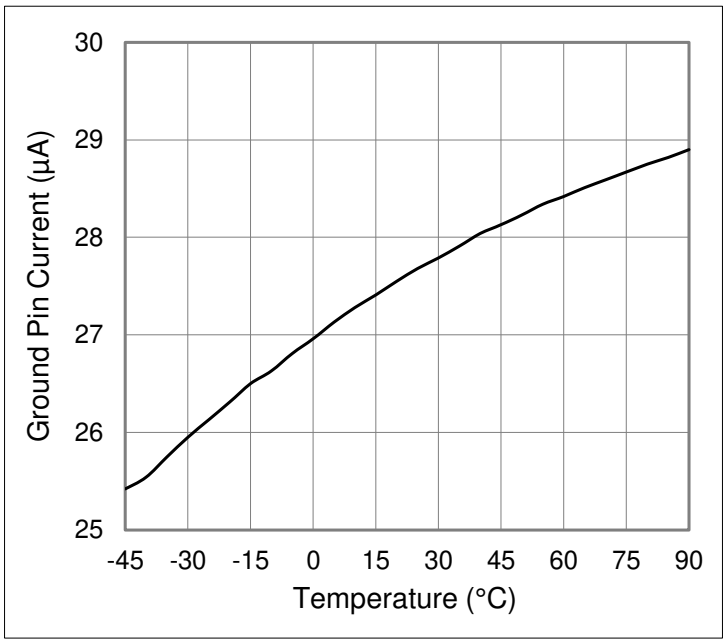


**Figure 16:**
**Ground Pin Current vs. Input Voltage; One Channel On, No Load**

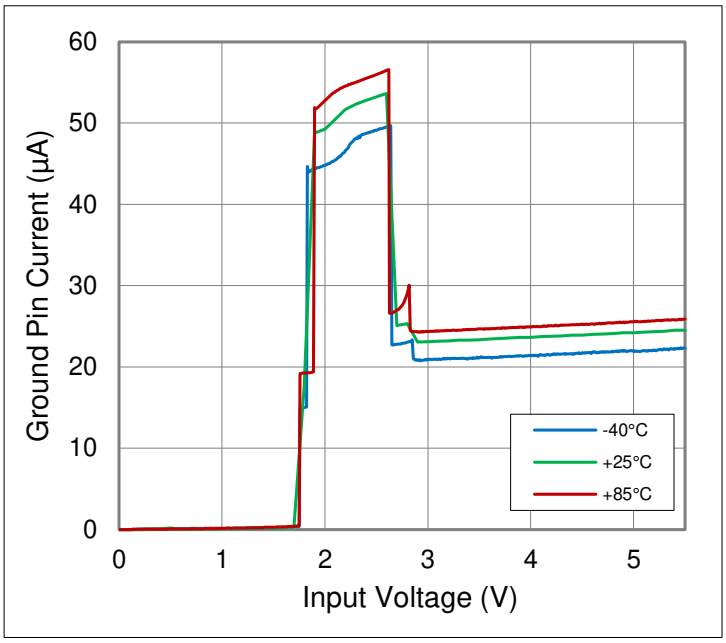



**Figure 17:**
**Ground Pin Current vs. Input Voltage; One Channel On, $I_{LOAD}$ = 200mA**

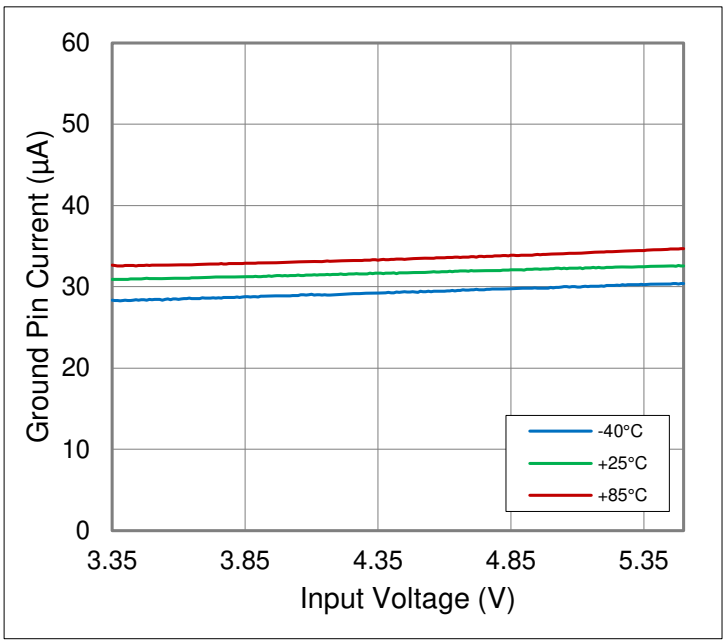


**Figure 18:**
**Ground Pin Current vs. Input Voltage; Both Channels on, No Load**

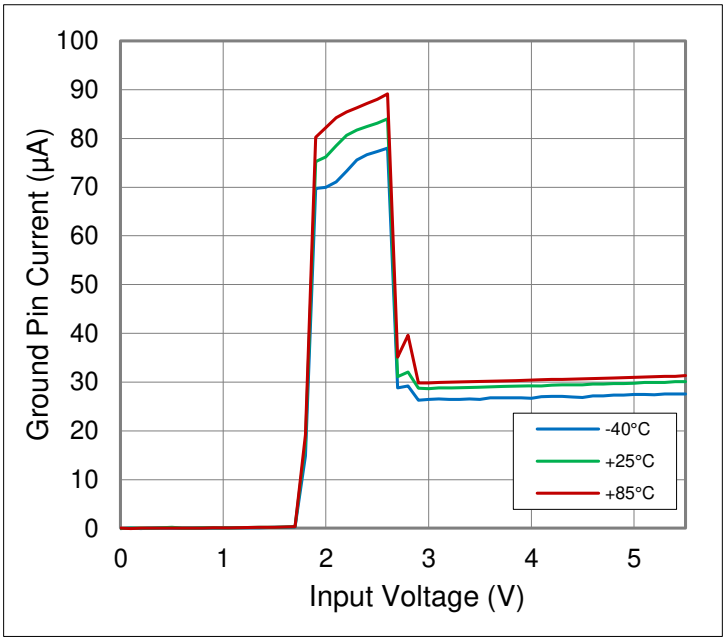



**Figure 19:**
**Ground Pin Current vs. Input Voltage; Both Channels On, $I_{LOAD}$ = 200mA**

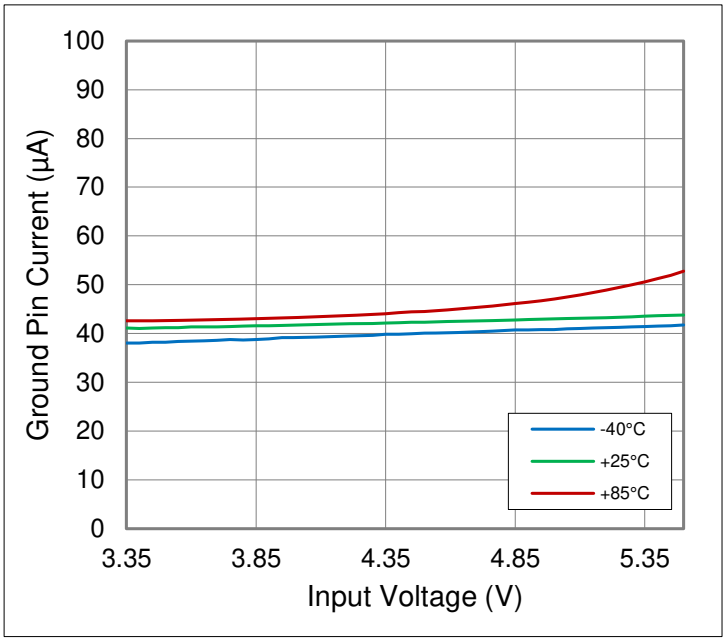


**Figure 20:**
**Shutdown Current vs. Input Voltage**

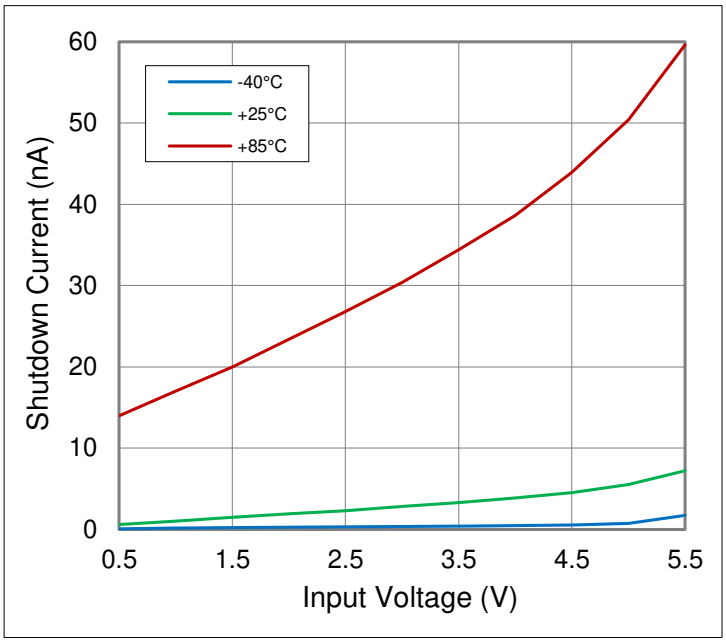



**Figure 21:**
**Load Regulation vs. Temperature**

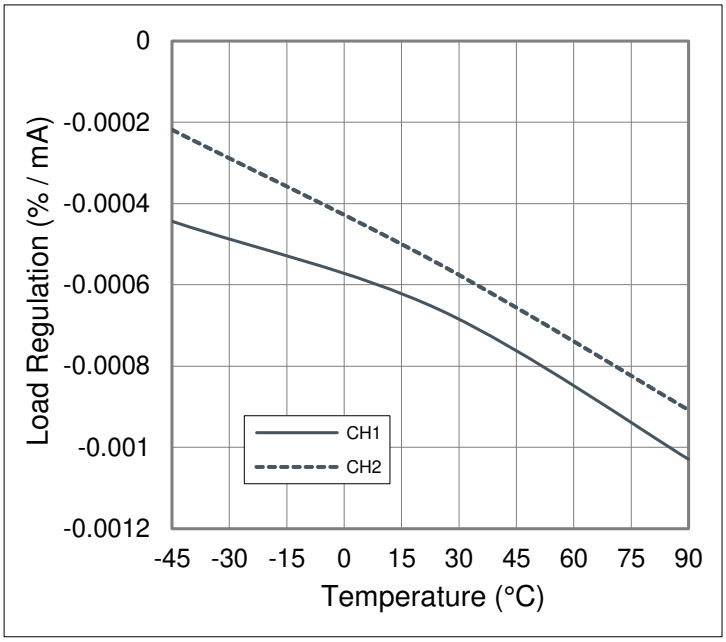


**Figure 22:**
**Line Regulation vs. Load Current**

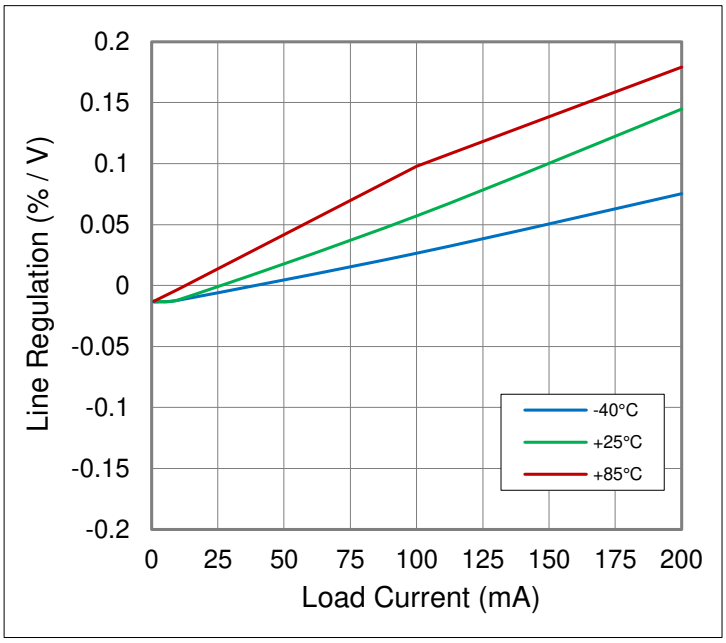



**Figure 23:**
**Line Regulation vs. Temperature**

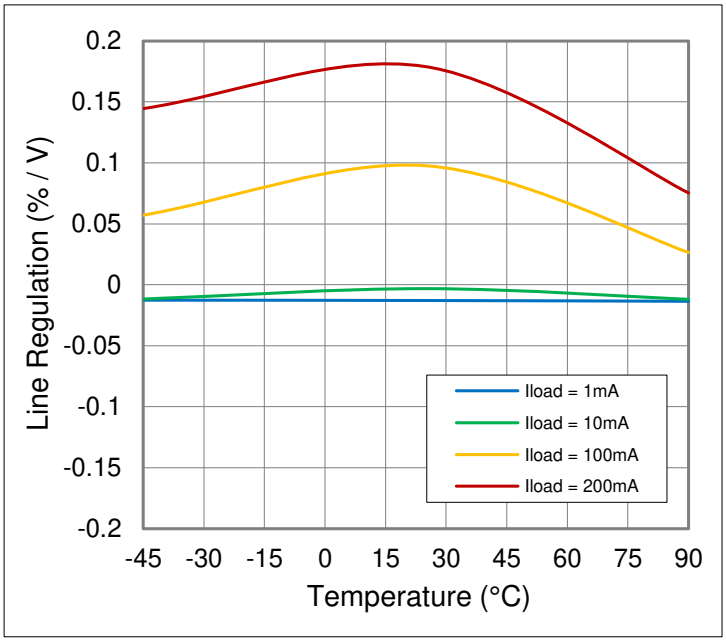


**Figure 24:**
**Load Transient Response, Crosstalk, Between CH1 and CH2, $I_{OUT}$ = 200mA**

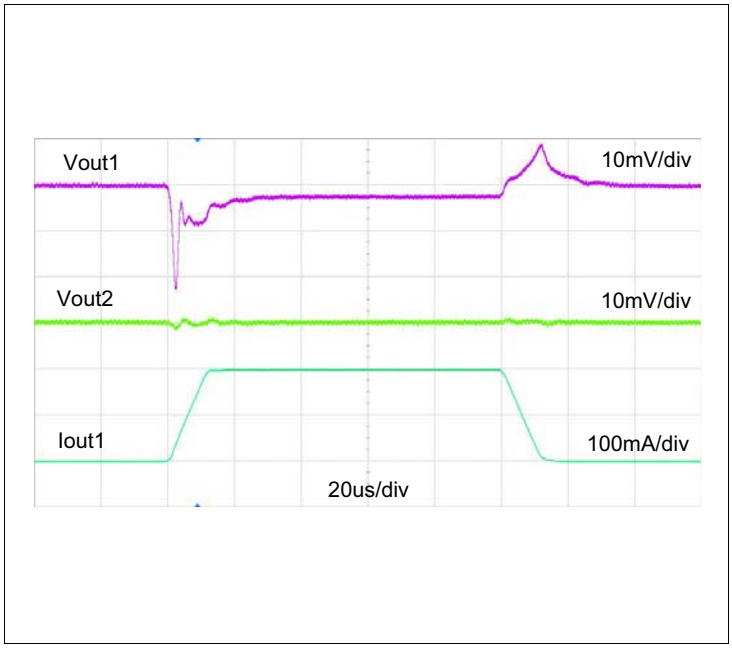



**Figure 25:**
**Load Transient Response Near Dropout, $I_{OUT}$ = 200mA**

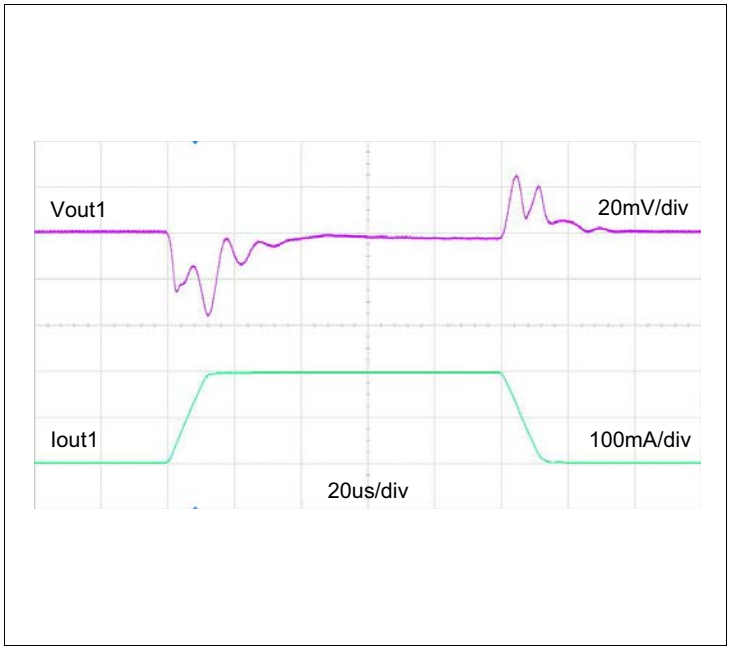


**Figure 26:**
**Line Transient Response**

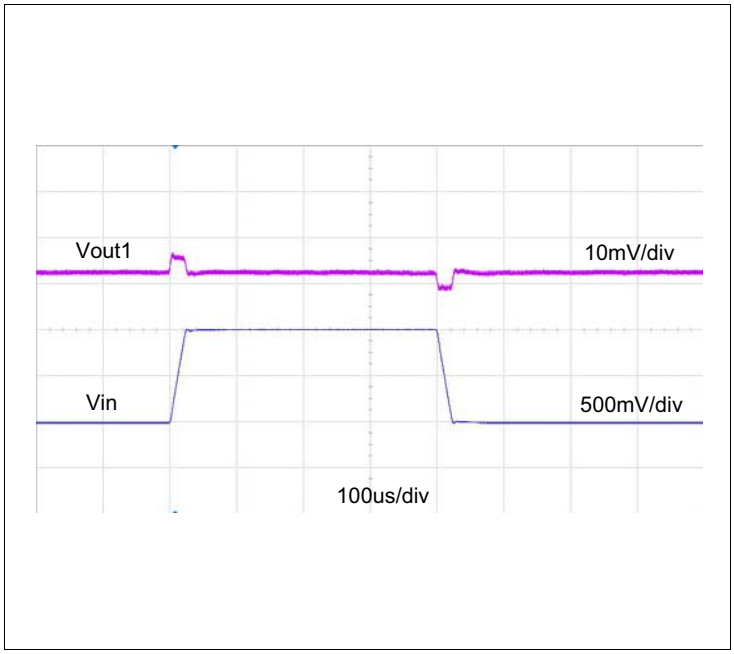



**Figure 27:**
**Shutdown**

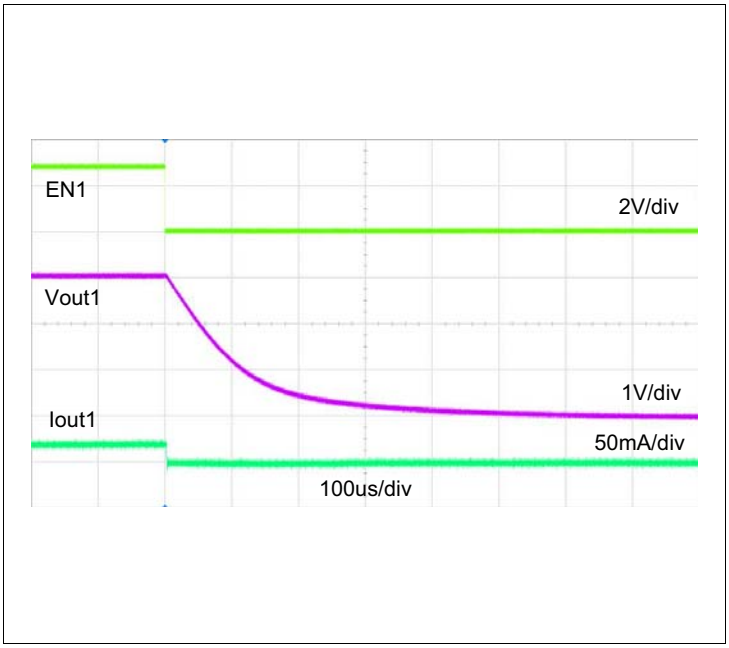


**Figure 28:**
**Startup of CH1 When CH2 is Off**

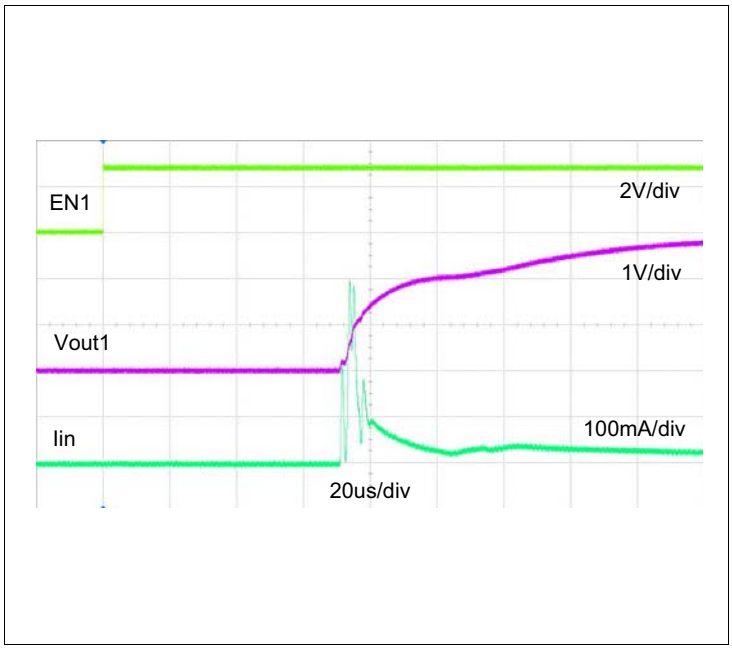
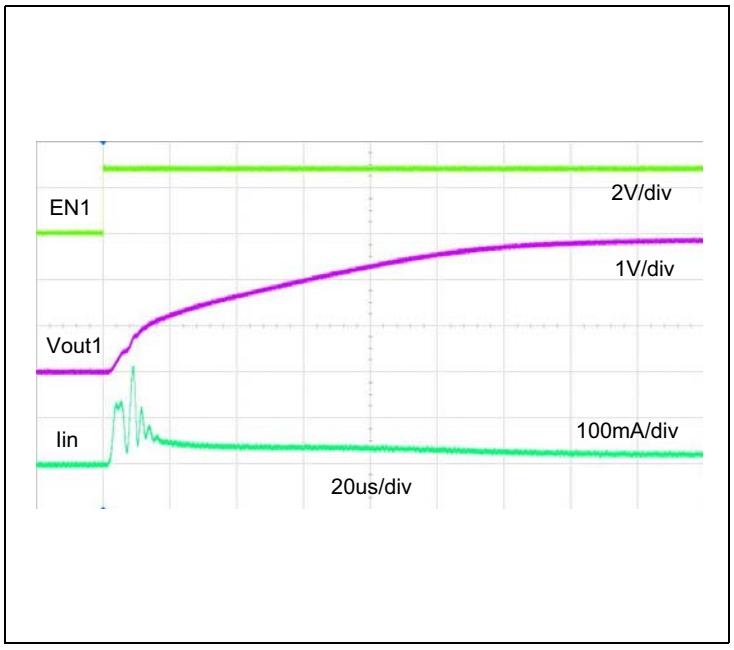



**Figure 29:**
**Startup of CH1 When CH2 is On**



# Detailed Description

Figure 3 shows the block diagram of the AS1374. It identifies the basics of a series linear regulator employing a P-Channel MOSFET as the control element. A stable voltage reference (REF in Figure 3) is compared with an attenuated sample of the output voltage. Any difference between the two voltages (reference and sample) creates an output from the error amplifier that drives the series control element to reduce the difference to a minimum. The error amplifier incorporates additional buffering to drive the relatively large gate capacitance of the series pass P-Channel MOSFET, when additional drive current is required under transient conditions. Input supply variations are absorbed by the series element, and output voltage variations with loading are absorbed by the low output impedance of the regulator.

## Output Voltage

The AS1374 deliver preset output voltages from 1.2V to 3.6V, in 50mV increments (see Ordering Information).

## Enable

The AS1374 feature an active high enable mode to shutdown each output independently. Driving EN 1 low disables Output 1, driving EN 2 low disables Output 2. The disabled Output enters a high-impedance state.

## Current Limit

The AS1374 include a current limiting circuitry to monitor and control the P-channel MOSFET pass transistor's gate voltage, thus limiting the device output current to 300mA.

**Note(s):** See Figure 7 for the recommended min and max current limits. The output can be shorted to ground indefinitely without causing damage to the device.

## Thermal Protection

Integrated thermal protection circuitry limits total power dissipation in the AS1374. When the junction temperature ($T_J$) exceeds 160°C, the thermal sensor signals the shutdown logic, turning off the P-channel MOSFET pass transistor and allowing the device to cool down. The thermal sensor turns the pass transistor on again after the device's junction temperature drops by 15°C, resulting in a pulsed output during continuous thermal-overload conditions.

**Note(s):** Thermal protection is designed to protect the devices in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of 150°C.

# Application Information

## Dropout Voltage

Dropout is the input to output voltage difference, below which the linear regulator ceases to regulate. At this point, the output voltage change follows the input voltage change. Dropout voltage may be measured at different load currents, but is usually specified at maximum output. As a result, the MOSFET maximum series resistance over temperature is obtained. More generally:

(EQ1) $V_{DROPOUT} = I_{LOAD} \times R_{SERIES}$

Dropout is probably the most important specification when the regulator is used in a battery application. The dropout performance of the regulator defines the useful “end of life” of the battery before replacement or re-charge is required.

**Figure 30:**
**Graphical Representation of Dropout Voltage**

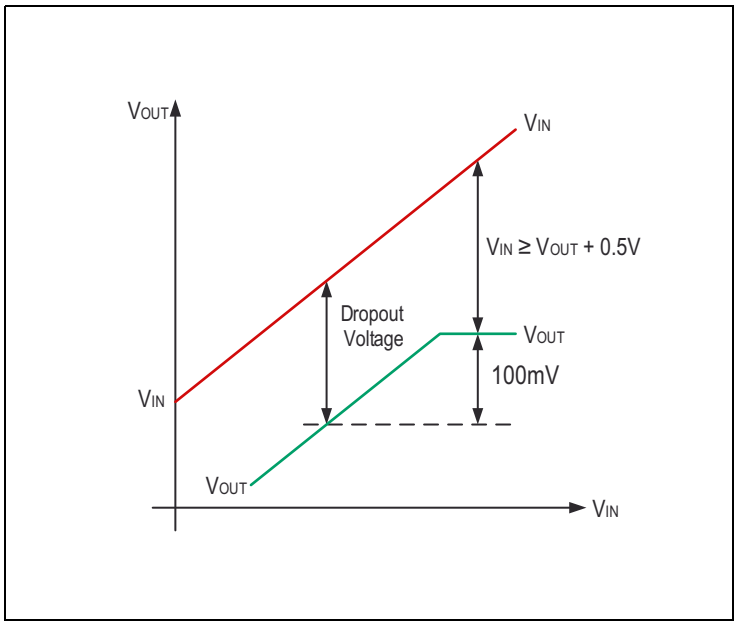



Figure 30 shows the variation of $V_{OUT}$ as $V_{IN}$ is varied for a certain load current. The practical value of dropout is the differential voltage ($V_{OUT}$ - $V_{IN}$) measured at the point where the LDO output voltage has fallen by 100mV below the nominal, fully regulated output value. The nominal regulated output voltage of the LDO is that obtained when there is 500mV (or greater) input-output voltage differential.

## Efficiency

Low quiescent current and low input-output voltage differential are important in battery applications amongst others, as the regulator efficiency is directly related to quiescent current and dropout voltage. Efficiency is given by:

(EQ2) $$\text{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{V_{IN}(I_Q + I_{LOAD})} \times 100\,\%$$

Where:
IQ = Quiescent current of LDO

## Power Dissipation

Maximum power dissipation (PD) of the LDO is the sum of the power dissipated by the internal series MOSFET and the quiescent current required to bias the internal voltage reference and the internal error amplifier, and is calculated as:

(EQ3) $$PD_{(MAX)}(\text{Seriespass}) = I_{LOAD(MAX)}(V_{IN(MAX)} - V_{OUT(MIN)})\ \text{Watts}$$

Internal power dissipation as a result of the bias current for the internal voltage reference and the error amplifier is calculated as:

(EQ4) $$PD_{(MAX)}(\text{Bias}) = V_{IN(MAX)} I_Q\ \text{Watts}$$

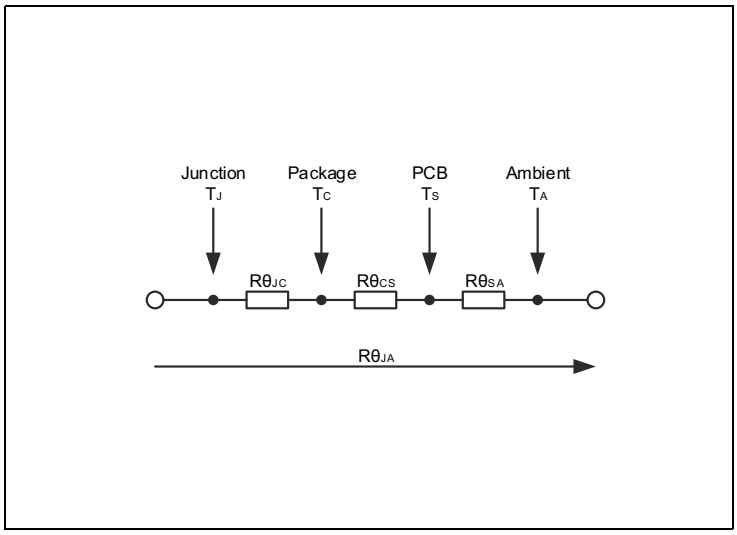
Total LDO power dissipation is calculated as:

(EQ5) $$PD_{(MAX)}(\text{Total}) = PD_{(MAX)}(\text{Seriespass}) + PD_{(MAX)}(\text{Bias})\ \text{Watts}$$

## Junction Temperature

Under all operating conditions, the maximum junction temperature should not be allowed to exceed 125°C (unless otherwise specified in the datasheet). Limiting the maximum junction temperature requires knowledge of the heat path from junction to case ($\theta_{JC}$°C/W fixed by the IC manufacturer), and adjustment of the case to ambient heat path ($\theta_{CA}$°C/W) by manipulation of the PCB copper area adjacent to the IC position.

**Figure 31:**
**Steady State Heat Flow Equivalent Circuit**




Total Thermal Path Resistance:

**(EQ6)** $R\theta_{JA} = R\theta_{JC} + R\theta_{CS} + R\theta_{SA}$

Junction Temperature ($T_J$ °C) is determined by:

**(EQ7)** $T_J = (PD_{(MAX)} \times R\theta_{JA}) + T_{AMB}$ °C

## Explanation of Steady State Specifications

### *Line Regulation*

Line regulation is defined as the change in output voltage when the input (or line) voltage is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the input voltage changes. Line regulation is a measure of the DC open loop gain of the error amplifier. More generally:

**(EQ8)** $$\text{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \text{ and is a pure number}$$

In practise, line regulation is referred to the regulator output voltage in terms of % / $V_{OUT}$. This is particularly useful when the same regulator is available with numerous output voltage trim options.

**(EQ9)** $$\text{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{100}{V_{OUT}} \text{ \% / V}$$

### *Load Regulation*

Load regulation is defined as the change of the output voltage when the load current is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the load changes. Load regulation is a measure of the DC closed loop output resistance of the regulator. More generally:

**(EQ10)** $$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \text{ and is units of Ohms } (\Omega)$$

In practise, load regulation is referred to the regulator output voltage in terms of % / mA. This is particularly useful when the same regulator is available with numerous output voltage trim options.

**(EQ11)** $$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \times \frac{100}{V_{OUT}} \text{ \% / mA}$$

### *Setting Accuracy*

Accuracy of the final output voltage is determined by the accuracy of the ratio of R1 and R2, the reference accuracy and the input offset voltage of the error amplifier. When the regulator is supplied pre-trimmed, the output voltage accuracy is fully defined in the output voltage specification.

When the regulator has a SET terminal, the output voltage may be adjusted externally. In this case, the tolerance of the external resistor network must be incorporated into the final accuracy calculation. Generally:

**(EQ12)** $$V_{OUT} = (V_{SET} \pm \Delta V_{SET})\left(1 + \frac{R1 \pm \Delta R1}{R2 \pm \Delta R2}\right)$$

The reference tolerance is given both at 25°C and over the full operating temperature range.

### *Total Accuracy*

Away from dropout, total steady state accuracy is the sum of setting accuracy, load regulation and line regulation. Generally:

**(EQ13)** Total % Accuracy = Setting % Accuracy + Load Regulation % + Line Regulation %

## Explanation of Dynamic Specifications

### *Power Supply Rejection Ratio (PSRR)*

Known also as Ripple Rejection, this specification measures the ability of the regulator to reject noise and ripple beyond DC. PSRR is a summation of the individual rejections of the error amplifier, reference and AC leakage through the series pass transistor. The specification, in the form of a typical attenuation plot with respect to frequency, shows up the gain bandwidth compromises forced upon the designer in low quiescent current conditions. Generally:

**(EQ14)** $PSRR = 20\mathrm{Log}\frac{\delta V_{OUT}}{\delta V_{IN}}$ dB using lower case $\delta$ to indicate AC values

Power supply rejection ratio is fixed by the internal design of the regulator. Additional rejection must be provided externally. The AS1374 is designed to deliver low noise and high PSRR, with low quiescent currents in battery-powered systems. The power-supply rejection is 85dB at 1kHz and 50dB at 100kHz. When operating from sources other than batteries, improved supply-noise rejection and transient response are achieved by increasing the values of the input and output capacitors. Additional passive LC filtering at the input can provide enhanced rejection at high frequencies.

### *Output Capacitor ESR*

The series regulator is a negative feedback amplifier, and as such is conditionally stable. The ESR of the output capacitor is usually used to cancel one of the open loop poles of the error amplifier in order to produce a single pole response. Excessive ESR values may actually cause instability by excessive changes to the closed loop unity gain frequency crossover point. The range of ESR values for stability is usually shown either by a plot of stable ESR versus load current, or a maximum value in the datasheet.

Some ceramic capacitors exhibit large capacitance and ESR variations with variations in temperature. Z5U and Y5V capacitors may be required to ensure stability at temperatures below $T_{AMB}$ = -10°C. With X7R or X5R capacitors, a 1µF capacitor should be sufficient at all operating temperatures.

Larger output capacitor values (10µF) help to reduce noise and improve load transient-response, stability and power-supply rejection.

### Input Capacitor

An input capacitor at $V_{IN}$ is required for stability. It is recommended that a 1.0µF capacitor be connected between the AS1369 power supply input pin $V_{IN}$ and ground (capacitance value may be increased without limit subject to ESR limits). This capacitor must be located at a distance of not more than 1cm from the $V_{IN}$ pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

### Noise

The regulator output is a DC voltage with noise superimposed on the output. The noise comes from three sources; the reference, the error amplifier input stage, and the output voltage setting resistors. Noise is a random fluctuation and if not minimized in some applications, will produce system problems.

### Transient Response

The series regulator is a negative feedback system, and therefore any change at the output will take a finite time to be corrected by the error loop. This "propagation time" is related to the bandwidth of the error loop. The initial response to an output transient comes from the output capacitance, and during this time, ESR is the dominant mechanism causing voltage transients at the output. More generally:

(EQ15) $$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times R_{ESR}$$ Units are Volts, Amps, Ohms.

Thus an initial +50mA change of output current will produce a -12mV transient when the ESR=240mΩ. Do remember to keep the ESR within stability recommendations when reducing ESR by adding multiple parallel output capacitors.

After the initial ESR transient, there follows a voltage droop during the time that the LDO feedback loop takes to respond to the output change. This drift is approx. linear in time and sums with the ESR contribution to make a total transient variation at the output of:

(EQ16) $$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times \left( R_{ESR} + \frac{T}{C_{LOAD}} \right)$$

Units are Volts, Seconds, Farads, Ohms.

Where:
$C_{LOAD}$ is output capacitor
T= Propagation Delay of the LDO

This shows why it is convenient to increase the output capacitor value for a better support for fast load changes. Of course the formula holds for t < "propagation time", so that a faster LDO needs a smaller cap at the load to achieve a similar transient response.