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# AS3400 AS3410 AS3430
## Low Power Ambient Noise-Cancelling Speaker Driver

# 1 General Description

The AS3400/10/30 are speaker driver with Ambient Noise Cancelling function for handsets, headphones or ear pieces. It is intended to improve quality of e.g. music listening, a phone conversation etc. by reducing background ambient noise.

The fully analog implementation allows the lowest power consumption, lowest system BOM cost and most natural received voice enhancement otherwise difficult to achieve with DSP implementations. The device is designed to be easily applied to existing architectures.

An internal OTP-ROM can be optionally used to store the microphones gain calibration settings.

The AS3400/10/30 can be used in different configurations for best trade-off of noise cancellation, required filtering functions and mechanical designs.

The simpler feed-forward topology is used to effectively reduce low frequency background noise. The feed-back topology with either 1 or 2 filtering stages can be used to reduce noise for a larger frequency range, and to even implement transfer functions like speaker equalization, Baxandall equalization, high/low shelving filter and to set a predefined loop bandwidth.

The filter loop is optimized by the user for specific handset electrical and mechanical designs by dimensioning simple R, C components.

Most handset implementations will make use of a single noise detecting microphone. Two microphones could be used to allow for increased flexibility of their location in the handset mechanical design. Using the bridged mode allows to even drive high impedance headsets.

# 2 Key Features

### Microphone Input

- 128 gain steps @ 0.375dB and MUTE with AGC
- Differential, low noise microphone amplifier
- Single ended or differential mode
- Improved supply for electret microphone
- MIC gain OTP programmable

### High Efficiency Headphone Amplifier

- 2x34mW, 0.1% THD @ 16Ω, 1.5V supply, 100dB SNR
- Bridged mode for e.g. 300Ω loads
- Click and pop less start-up and mode switching

### Line Input

- Volume control via serial interface or volume pin
- 64 steps @ 0.75dB and MUTE, pop-free gain setting
- Single ended stereo or mono differential mode

### ANC processing

- Feed-forward cancellation
- Feed-back cancellation with filter loop transfer function definable via simple RC components
- Simple in production SW calibration
- 12-30dB noise reduction (headset dependent)
- 10-2000Hz wide frequency active noise attenuation (headset dependent)

### Monitor Function

- For assisted hearing, i.e. to monitor announcements
- Fixed (OTP prog.) ambient sound amplification to compensate headphone passive attenuation
- Volume controlled ambient sound amplification mixed with fixed (OTP prog.) attenuation of LineIn

### Incremental Functions

- ANC with or without music on the receiving path
- Improved dynamic range playback
- OTP ROM for automatic trimming during production (4 times programable)

### Performance Parameter

- 5/3.8mA @ 1.5V stereo/mono ANC; <1µA quiescent
- Extended PSRR for 217Hz

### Interfaces

- 2-wire serial control mode & volume inputs
- Calibration via Line-In or 2-wire serial interface (patent pending)
- Single cell or fixed 1.0-1.8V supply with internal CP

### Package

- AS3400, AS3410 QFN24 [4x4mm] 0.5mm pitch
- AS3430 QFN32 [5.x5mm] 0.5mm pitch

# 3 Applications

The devices are ideal for Ear pieces, Headsets, Hands-Free Kits, Mobile Phones, and Voice Communicating Devices.

*Figure 1. AS3410 Feed Forward ANC Block Diagram*

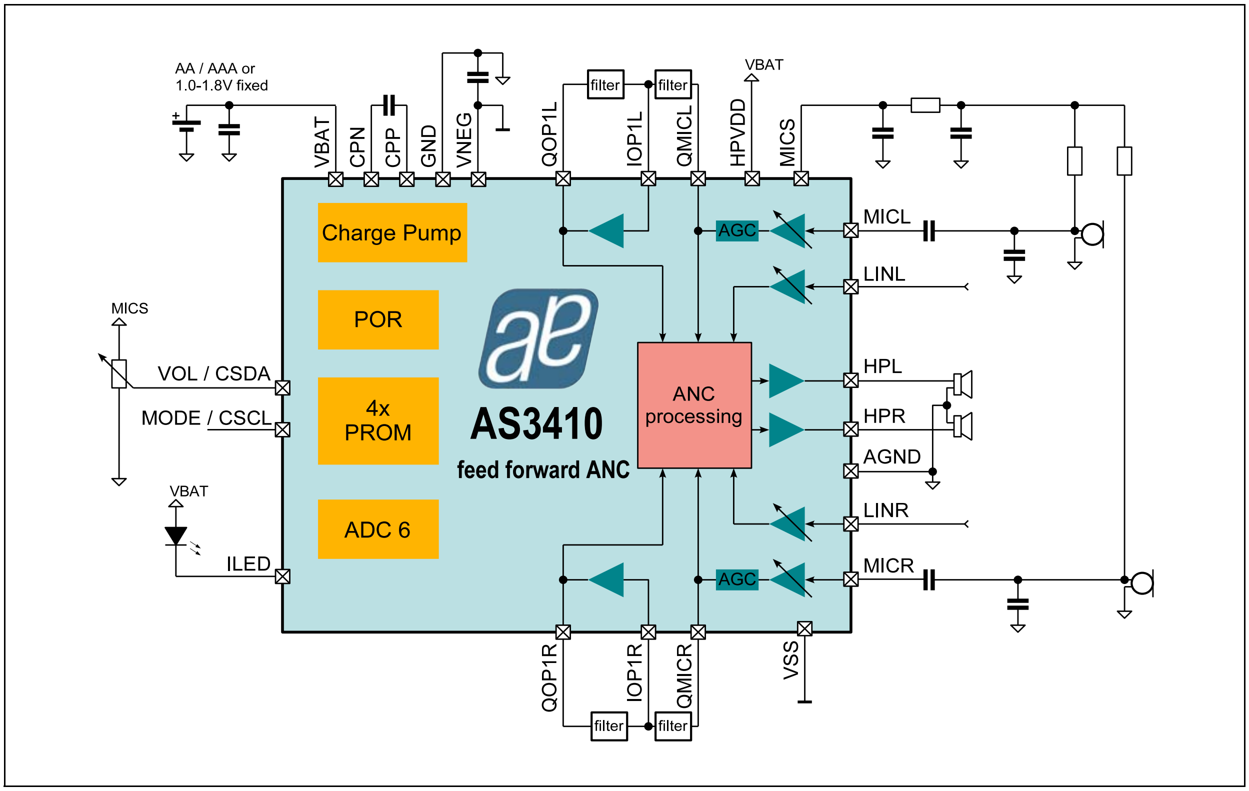



*Figure 2. AS3430 Feed-Back Block Diagram*

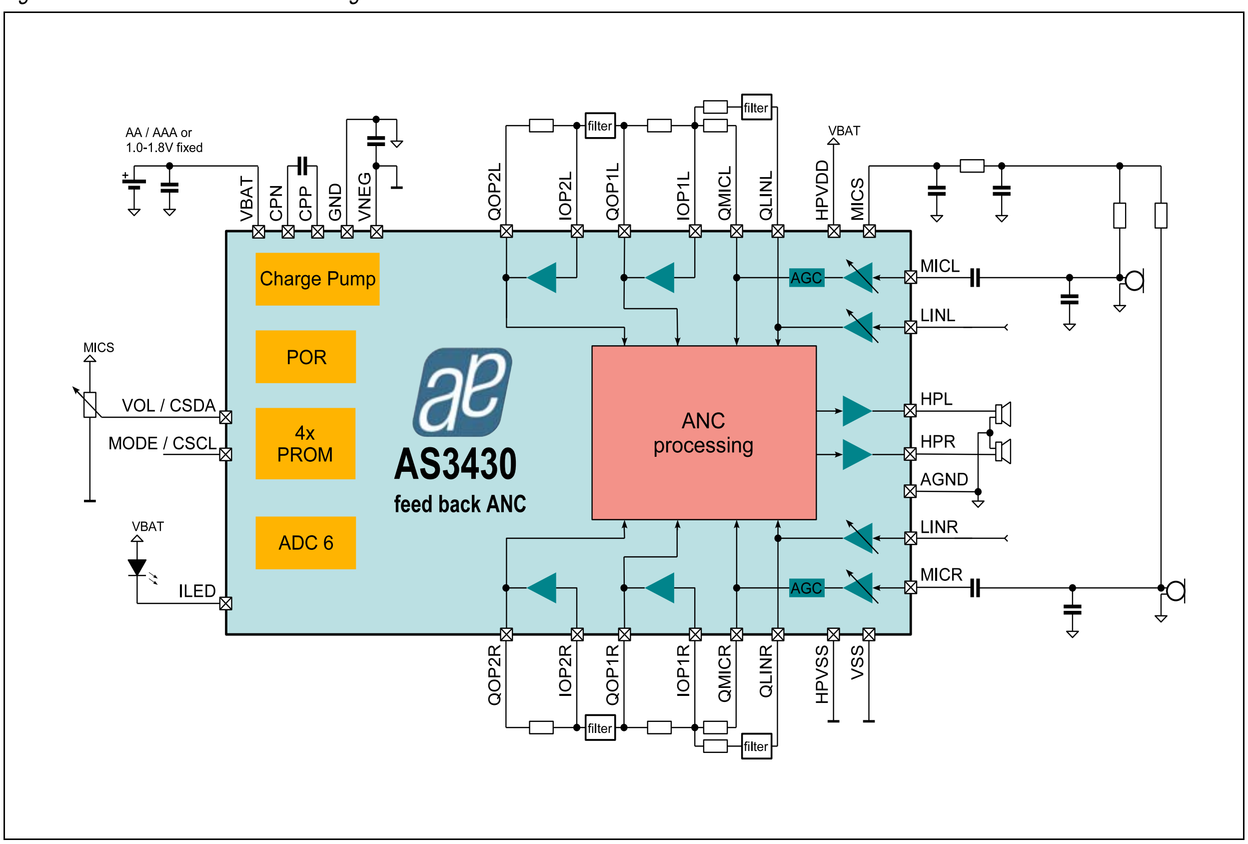


Figure 3. AS3400 Feed-Back Block Diagram

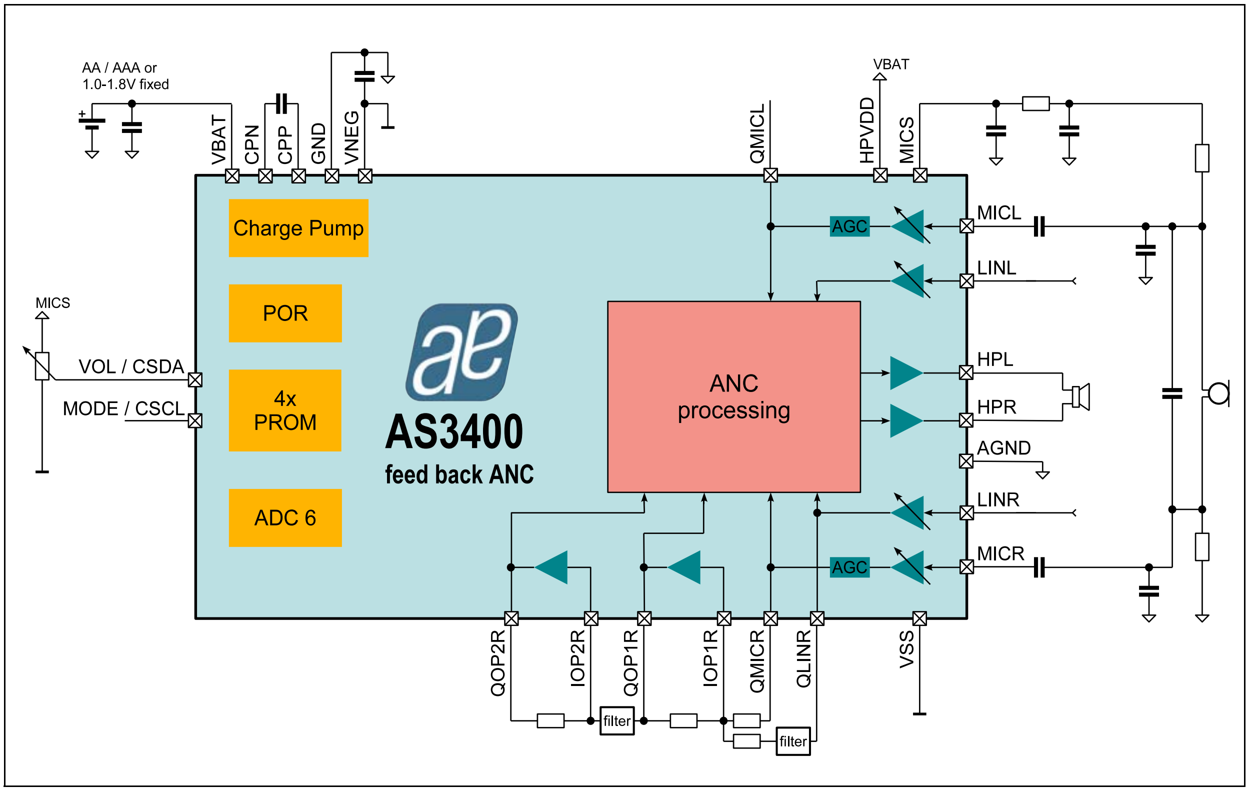
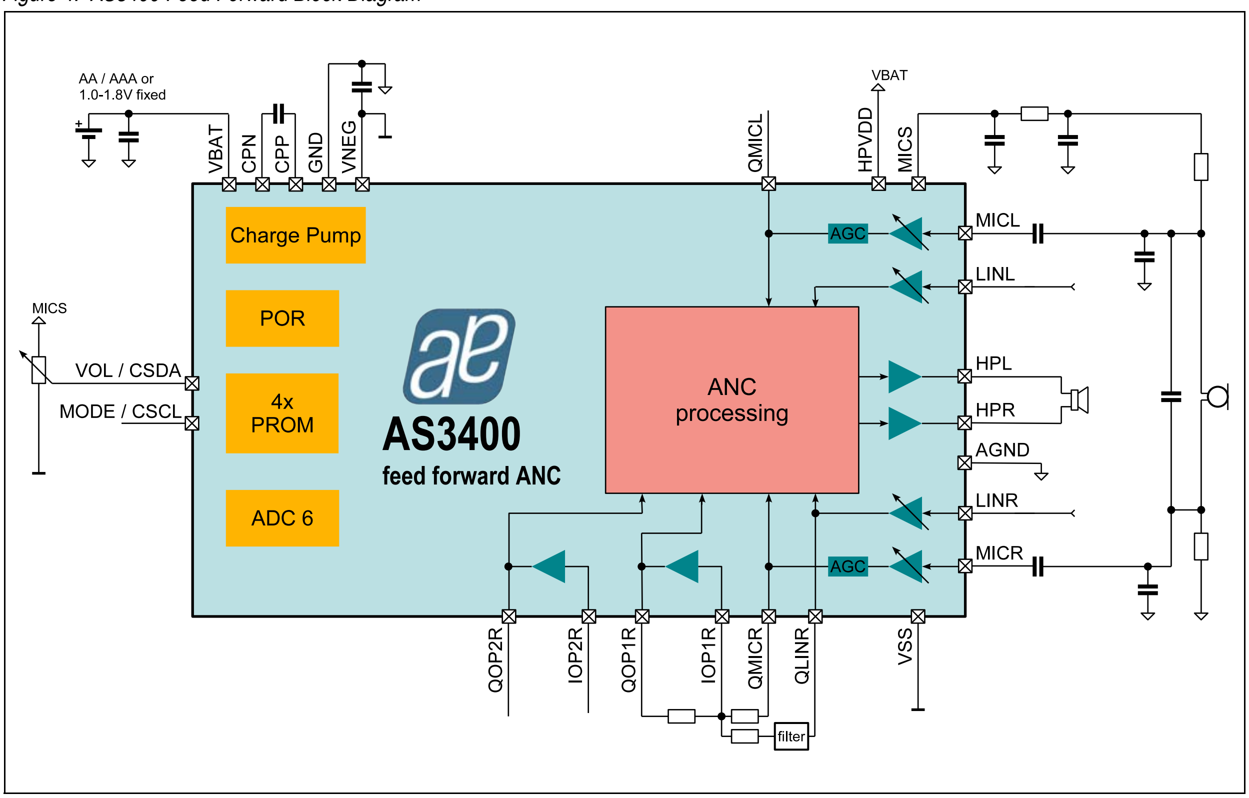



Figure 4. AS3400 Feed Forward Block Diagram

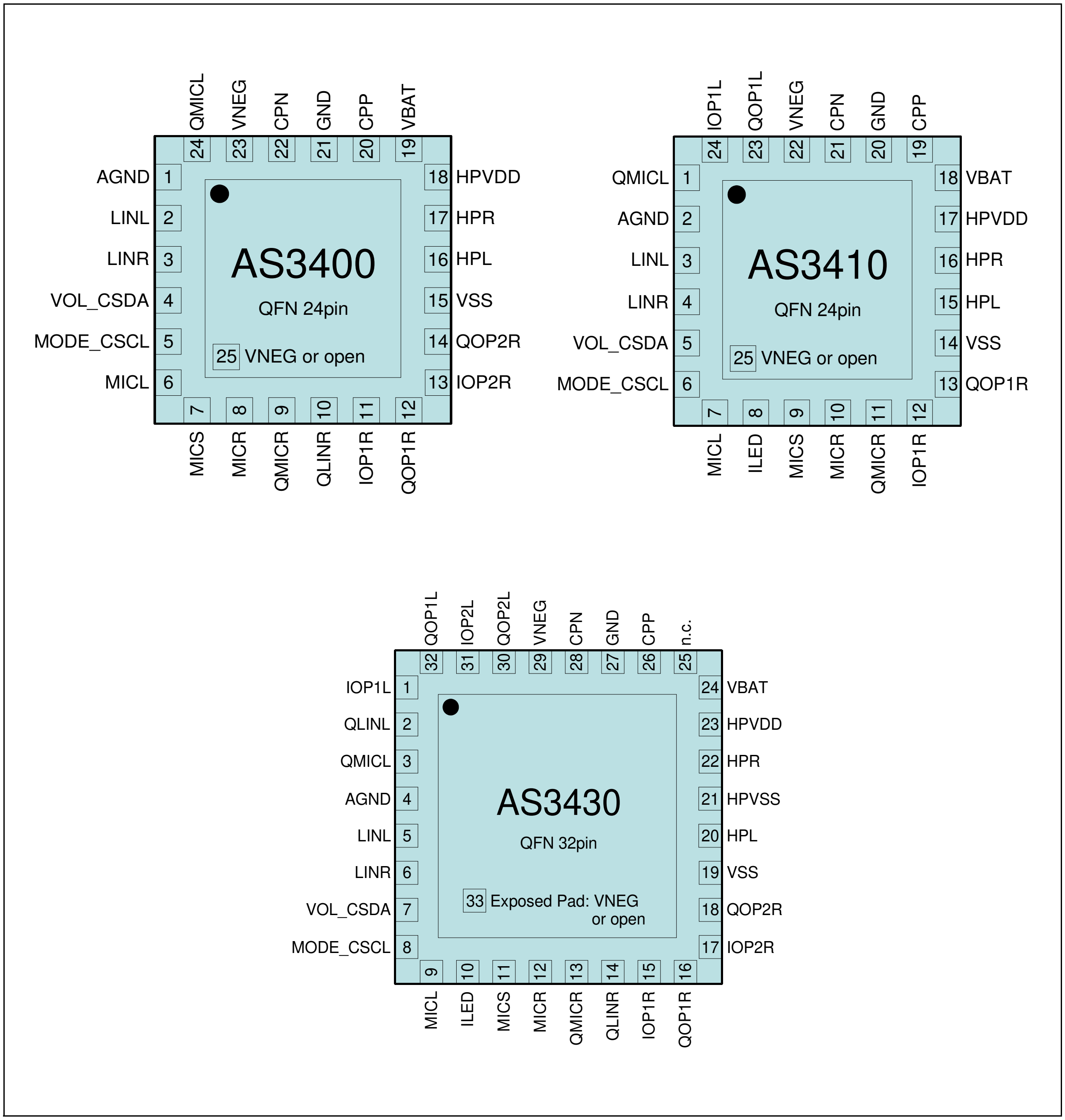


## Contents

# 4 Pin Assignments

**Note:** Pin assignment may change in preliminary data sheets.

*Figure 5. Pin Assignments (Top View)*



## 4.1 Pin Descriptions

**Note:** Pin description may change in preliminary data sheets.

*Table 1. Pin Description for AS3400 AS3410 AS3430*

| Pin Name | Pin Number | | | Type | Description |
|---|---|---|---|---|---|
| | AS3400 | AS3410 | AS3430 | | |
| IOP1L | - | 24 | 1 | ANA IN | Filter OpAmp1 Input Left Channel |
| QLINL | - | - | 2 | ANA OUT | Line In GainStage Output Left Channel |
| QMICL | 24 | 1 | 3 | ANA OUT | MIC GainStage Output Right Channel |
| AGND | 1 | 2 | 4 | ANA IN | Analog Reference |
| LINL | 2 | 3 | 5 | ANA IN<br>DIG IN | Line In Left Channel<br>During Appl Trim Mode Write – CSDA<br>During Appl Trim Mode Burn – VNEG |
| LINR | 3 | 4 | 6 | ANA IN<br>DIG IO | LineIn Right Channel<br>During Appl Trim Mode Write – CSCL<br>During Appl Trim Mode Burn – Clock |
| VOL_CSDA | 4 | 5 | 7 | MIXED IO | Serial Interface Data<br>ADC Input for volume regulation |
| MODE_CSCL | 5 | 6 | 8 | DIG IN | Mode Pin (PowerUp/Dn, Monitor)<br>Serial Interface Clock |
| MICL | 6 | 7 | 9 | ANA IN | Microphone In Left Channel |
| ILED | - | 8 | 10 | ANA OUT | Current Output for on-indication LED |
| MICS | 7 | 9 | 11 | ANA OUT | Microphone Supply |
| MICR | 8 | 10 | 12 | ANA IN | Microphone Input Right Channel |
| QMICR | 9 | 11 | 13 | ANA OUT | MIC GainStage Output Right Channel |
| QLINR | 10 | - | 14 | ANA OUT | Line In GainStage Output Right Channel |
| IOP1R | 11 | 12 | 15 | ANA IN | FilterOpAmp1 Input Right Channel |
| QOP1R | 12 | 13 | 16 | ANA IN | Filter OpAmp1 Output Right Channel |
| IOP2R | 13 | - | 17 | ANA IN | Filter OpAmp2 Input Right Channel |
| QOP2R | 14 | - | 18 | ANA OUT | Filter OpAmp2 Output Right Channel |
| VSS | 15 | 14 | 19 | SUP IN | Core and Periphery Circuit VSS Supply |
| HPL | 16 | 15 | 20 | ANA OUT | Headphone Output Left Channel |
| HPVSS | - | - | 21 | SUP IN | Headphone VSS Supply |
| HPR | 17 | 16 | 22 | ANA OUT | Headphone Output Right Channel |
| HPVDD | 18 | 17 | 23 | SUP IN | Headphone VDD Supply |
| VBAT | 19 | 18 | 24 | SUP IN | VNEG ChargePump Positive Supply |
| n.c. | - | - | 25 | - | |
| CPP | 20 | 19 | 26 | ANA OUT | VNEG ChargePump Flying Capacitor Positive Terminal |
| GND | 21 | 20 | 27 | GND | VNEG ChargePump Negative Supply |
| CPN | 22 | 21 | 28 | ANA OUT | VNEG ChargePump Flying Capacitor Negative Terminal |
| VNEG | 23 | 22 | 29 | SUP IO | VNEG ChargePump Output |

*Table 1. Pin Description for AS3400 AS3410 AS3430*

| Pin Name | Pin Number | | | Type | Description |
|---|---|---|---|---|---|
| | AS3400 | AS3410 | AS3430 | | |
| QOP2L | - | - | 30 | ANA OUT | Filter OpAmp2 Output Left Channel |
| IOP2L | - | - | 31 | ANA IN | Filter OpAmp2 Input Left Channel |
| QOP1L | - | 23 | 32 | ANA OUT | Filter OpAmp1 Output Right Channel |
| | 25 | 25 | 33 | | Exposed Pad: connect to VNEG or leave it unconnected |

# 5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 9 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

*Table 2. Absolute Maximum Ratings*

| Parameter | Min | Max | Units | Comments |
|---|---|---|---|---|
| Reference Ground | | | | Defined as in GND |
| Supply terminals | -0.5 | 2.0 | V | Applicable for pin VBAT, HPVDD |
| Ground terminals | -0.5 | 0.5 | V | Applicable for pins AGND |
| Negative terminals | -2.0 | 0.5 | V | Applicable for pins VNEG, VSS, HPVSS |
| Voltage difference at VSS terminals | -0.5 | 0.5 | V | Applicable for pins VSS, HPVSS |
| Pins with protection to VBAT | VNEG -0.5 | 5.0 VBAT+0.5 | V | Applicable for pins CPP, CPN |
| Pins with protection to HPVDD | VSS -0.5 | 5.0 HPVDD+0.5 | V | Applicable for pins LINL/R, MICL/R, ILED, HPR, HPL, QMICL/R, QLINL/R, IOPx, QOPx |
| other pins | VSS -0.5 | 5 | | Applicable for pins MICS, VOL_CSDA, MODE_CSCL |
| Input Current (latch-up immunity) | -100 | 100 | mA | Norm: JEDEC 17 |
| **Continuous Power Dissipation ($T_A$ = +70ºC)** | | | | |
| Continuous Power Dissipation | - | 200 | mW | $P_T$[1] for QFN16/24/32 package |
| **Electrostatic Discharge** | | | | |
| Electrostatic Discharge HBM | | +/-2 | kV | Norm: JEDEC JESD22-A114C |
| **Temperature Ranges and Storage Conditions** | | | | |
| Junction Temperature | | +110 | ºC | |
| Storage Temperature Range | -55 | +125 | ºC | |
| Humidity non-condensing | 5 | 85 | % | |
| Moisture Sensitive Level | 3 | | | Represents a max. floor life time of 168h |
| Package Body Temperature | | 260 | ºC | The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* |

1. Depending on actual PCB layout and PCB used

# 6 Electrical Characteristics

VBAT = 1.0V to 1.8V, $T_A$ = -20ºC to +85ºC. Typical values are at VBAT = 1.5V, $T_A$ = +25ºC, unless otherwise specified.

*Table 3. Electrical Characteristics*

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_A$ | Ambient Temperature Range | | -20 | +85 | °C |
| **Supply Voltages** | | | | | |
| GND | Reference Ground | | 0 | 0 | V |
| VBAT, HPVDD | Battery Supply Voltage | normal operation with MODE pin high | 1.0 | 1.8 | V |
| | | Two wire interface operation | 1.4 | 1.8 | V |
| VNEG | ChargePump Voltage | | -1.8 | -0.7 | V |
| VSS | Analog neg. Supply Voltages HPVSS, VSS, VNEG | | -1.8 | -0.7 | V |
| $V_{DELTA-}$ | Difference of Ground Supplies GND, AGND | To achieve good performance, the negative supply terminals should be connected to low impedance ground plane. | -0.1 | 0.1 | V |
| $V_{DELTA--}$ | Difference of Negative Supplies VSS, VNEG, HPVSS | Charge pump output or external supply | -0.1 | 0.1 | V |
| $V_{DELTA+}$ | Difference of Positive Supplies | VBAT-HPVDD | -0.25 | 0.25 | V |
| **Other pins** | | | | | |
| $V_{MICS}$ | Microphone Supply Voltage | MICS | 0 | 3.6 | V |
| $V_{HPVDD}$ | Pins with diode to HPVDD | MICL/R, ILED, HPR, HPL, QMICL/R, QLINL/R, IOPx, QOPx | VSS | 3.6 | V |
| $V_{VBAT}$ | Pins with diode to VBAT | CPP, CPN | VNEG | VBAT | V |
| $V_{CONTROL}$ | Control Pins | MODE_CSCL, VOL_CSDA | VSS | 3.7 | V |
| $V_{TRIM}$ | Line Input & Application Trim Pins | LINL, LINR | VNEG -0.5 or -1.8 | HPVDD +0.5 or 1.8 | V |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{leak}$ | Leakage current | VBAT<0.8V | | | 20 | µA |
| | | VBAT<0.6V | | | 10 | µA |
| **Block Power Requirements @ 1.5V VBAT** | | | | | | |
| $I_{SYS}$ | Reference supply current | Bias generation, oscillator, ILED current sink, ADC6 | | 0.25 | | mA |
| $I_{LIN}$ | LineIn gain stage current | no signal, stereo | | 0.64 | | mA |
| $I_{MIC}$ | Mic gain stage current | no signal, stereo | | 2.10 | | mA |
| $I_{HP}$ | Headphone stage current | no signal | | 1.70 | | mA |
| $I_{VNEG}$ | VNEG charge pump current | no load | | 0.25 | | mA |
| $I_{MICS}$ | MICS charge pump current | no load | | 0.06 | | mA |
| $I_{MIN}$ | Minimal supply current | Sum of all above blocks | | 5.00 | | mA |
| $I_{OP1}$ | OP1 supply current | no load | | 0.64 | | mA |
| $I_{OP2}$ | OP2 supply current | no load | | 0.64 | | mA |
| $I_{ILED}$ | ILED current sink current | 100% duty cycle | | 2.50 | | mA |
| $I_{MICB}$ | Microphone bias current | 200µA per microphone via charge pump | | 1.30 | | mA |

# 7 Typical Operating Characteristics

VBAT = +1.5V, $T_A$ = +25ºC, unless otherwise specified.

*Figure 6. LIN to HPH: THD+N vs. Output Power*

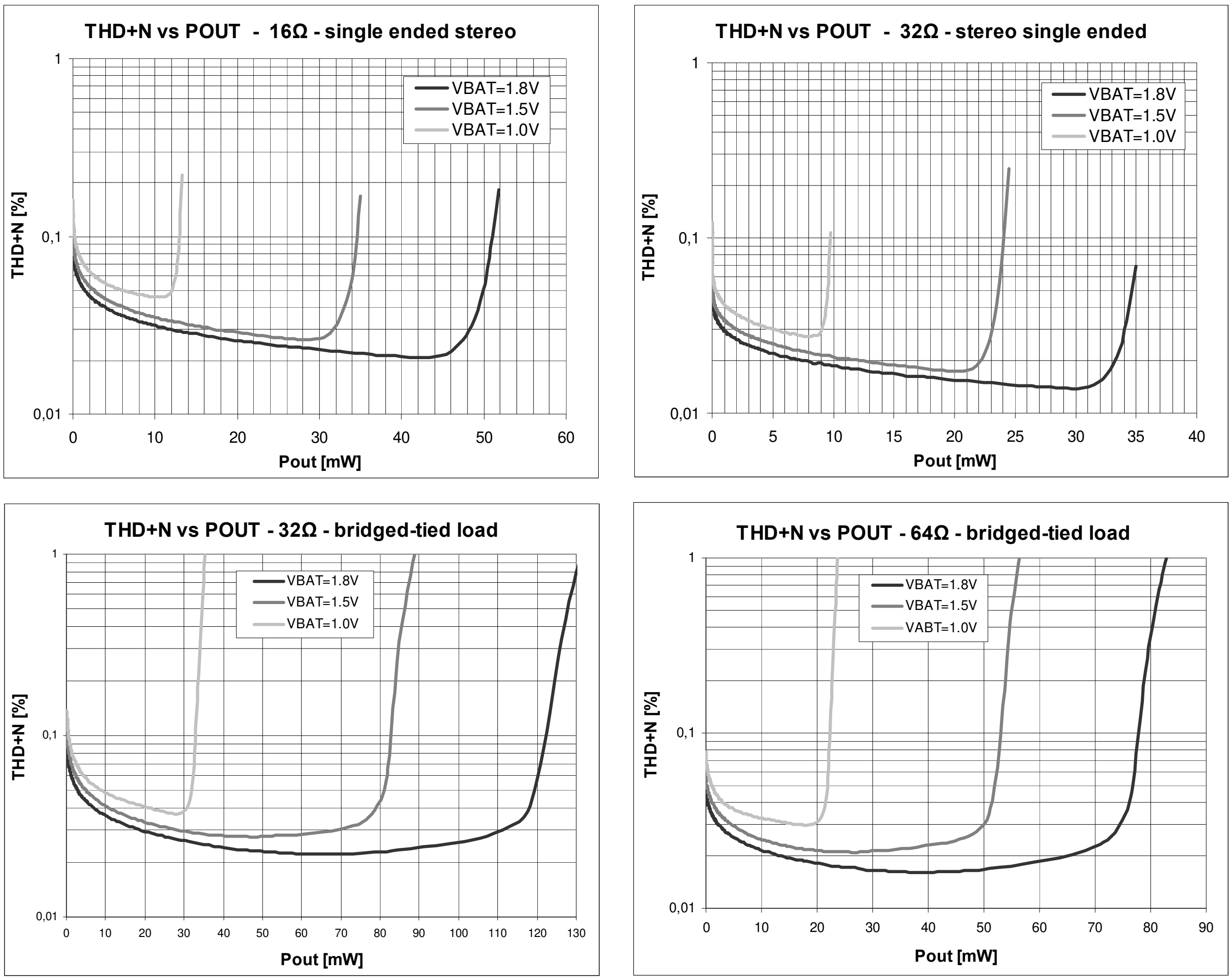



*Figure 7. VNEG Charge Pump*

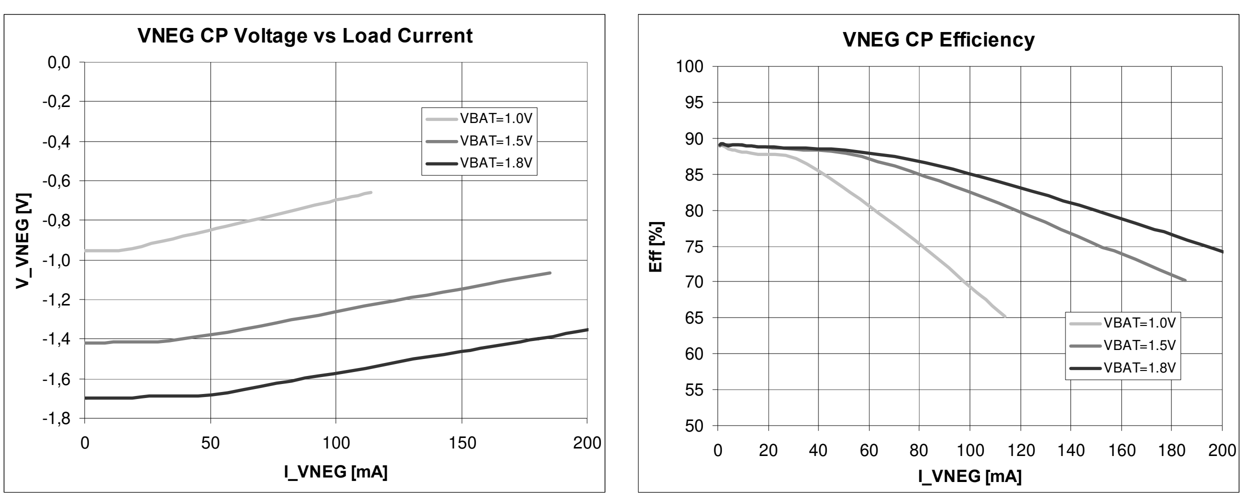


*Figure 8. Microphone Supply Generation*

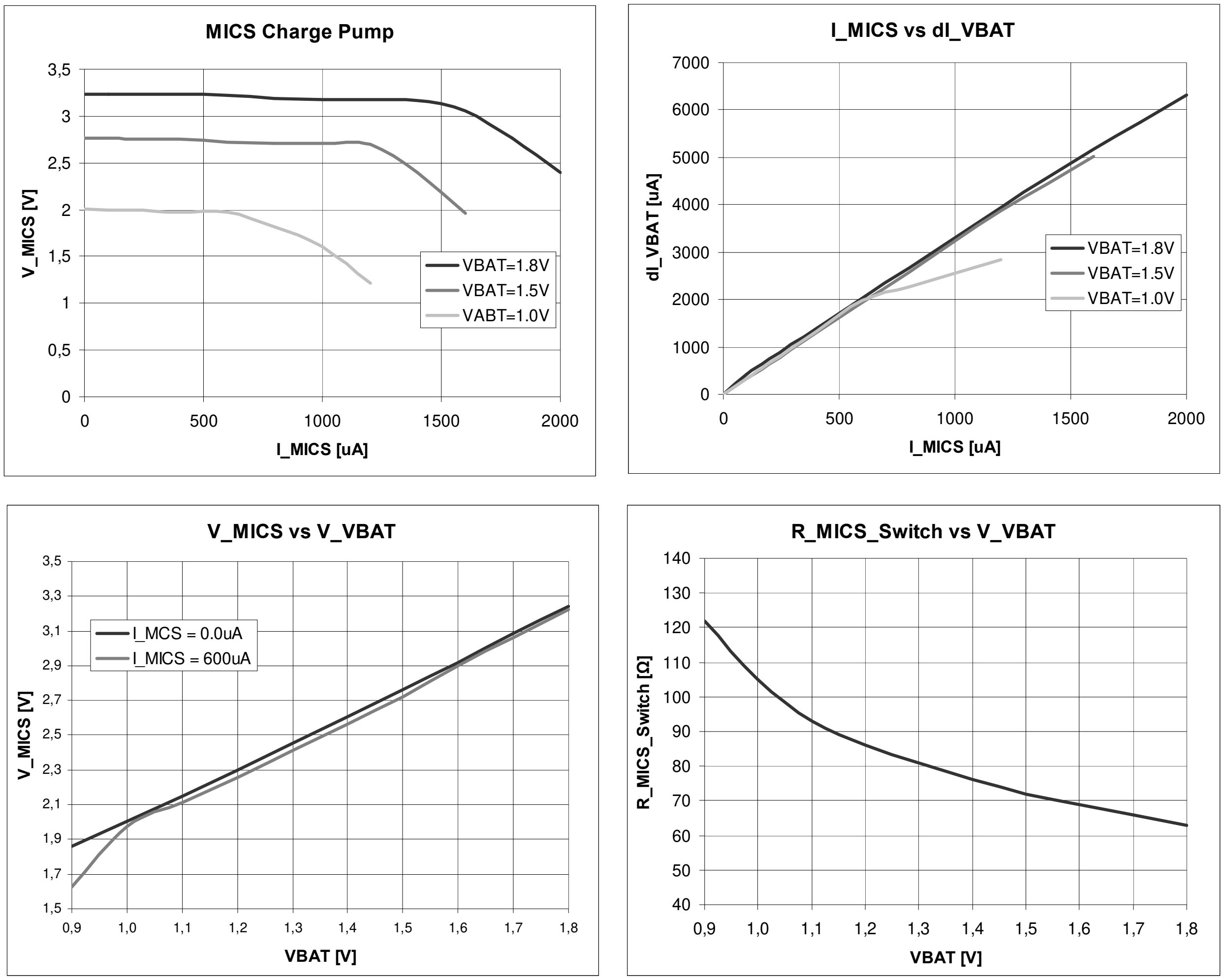



*Figure 9. ILED Current Sink (100% PWM setting)*

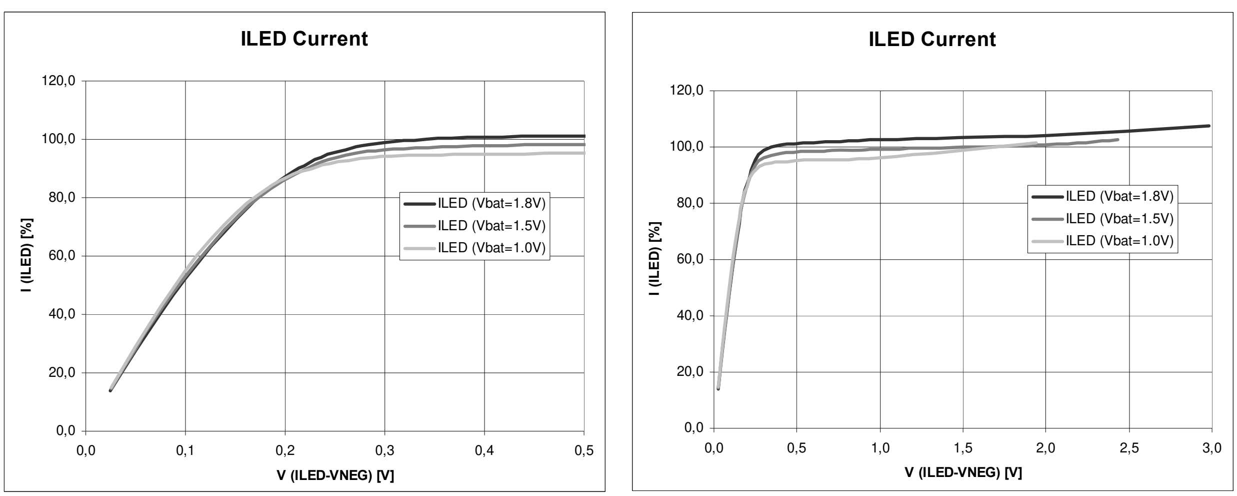
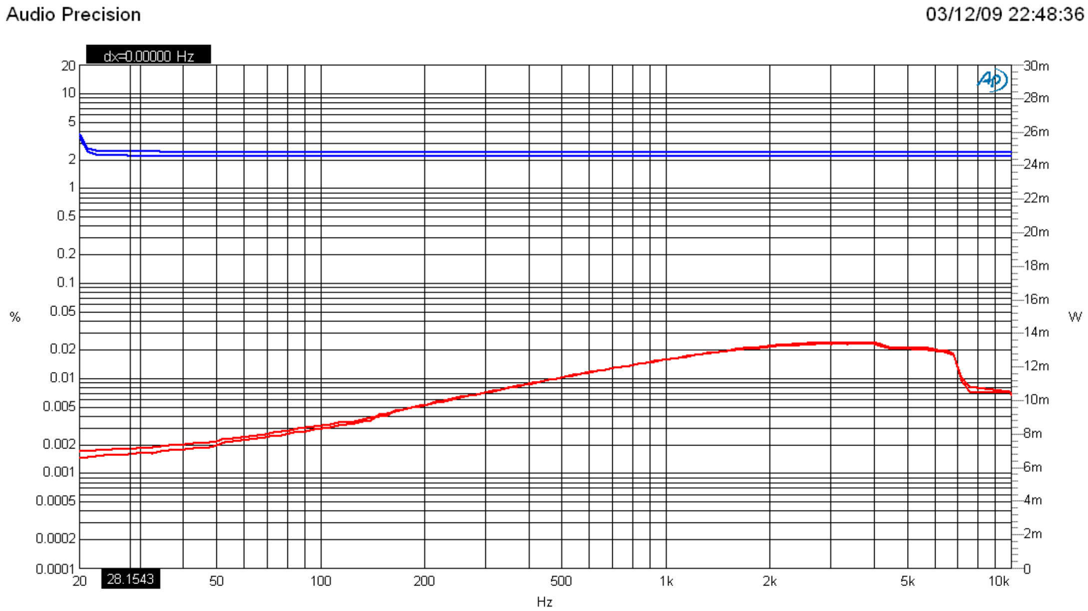


*Figure 10. THD vs. Frequency @ 1.5V, 16Ω, 25mW*




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment | Cursor1 | Cursor2 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | Red | Solid | 2 | DSP Anlr.THD+N Ratio A | Left | | .. | .. |
| 1 | 2 | Blue | Solid | 2 | DSP Anlr.Level A | Right | | .. | .. |
| 1 | 3 | Blue | Solid | 2 | DSP Anlr.Level B | Right | | .. | .. |
| 1 | 4 | Red | Solid | 2 | DSP Anlr.THD+N Ratio B | Left | | .. | .. |

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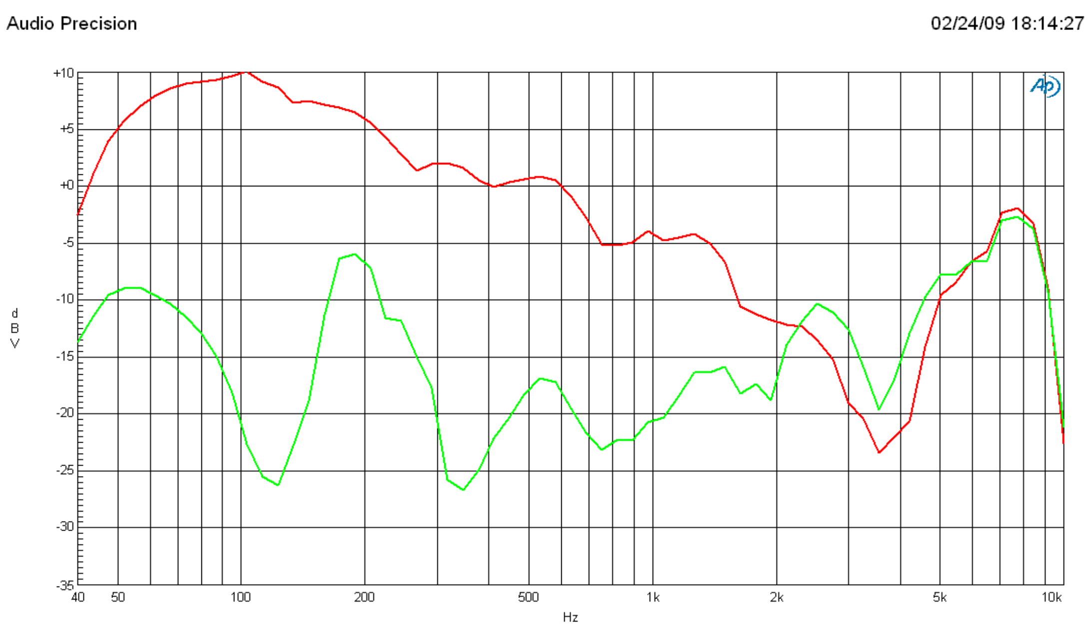
*Figure 11. Typical Performance Data, FF Configuration*




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 5 | 1 | Red | Solid | 2 | DSP Anlr.Bandpass B!Smooth | Left | AMS PassiveL |
| 7 | 1 | Green | Solid | 2 | DSP Anlr.Bandpass B!Smooth | Left | AMS Active 1001 L |

Filter3_Board_Proto1.at27

# 8 Detailed Description

This section provides a detailed description of the device related components.

## 8.1 Audio Line Input

The chip features one line input. The blocks can work in mono differential or in stereo single ended mode.

In addition to the 12.5-25kΩ input impedance, LineIn has a termination resistor of 10kΩ which is also effective during MUTE to charge eventually given input capacitors.

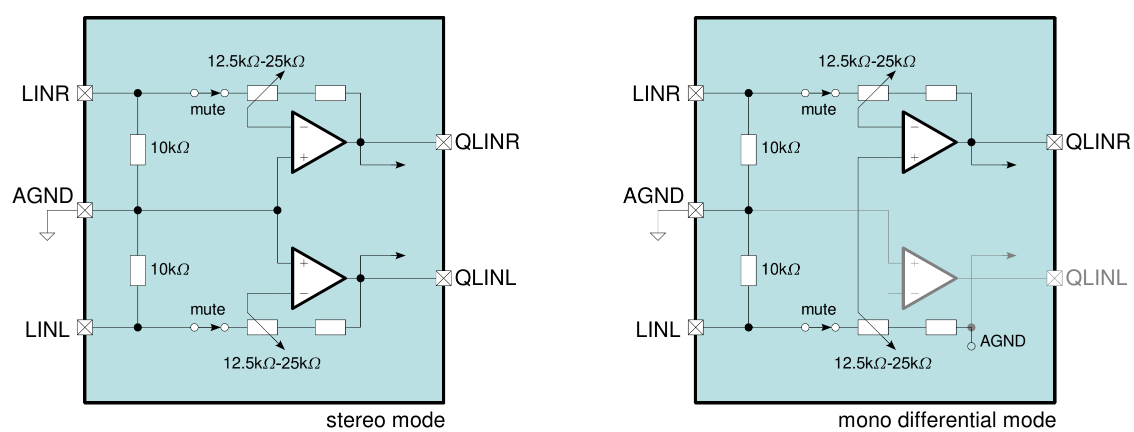
### 8.1.1 Gain Stage

The Line In gain stage is designed to have 63 gain steps of 0.75dB with a max gain of 0dB plus MUTE.

In default, the gain will be ramped up from MUTE to 0dB during startup. There is a possibility to make the playback volume user controlled by the VOL pin with an ADC converted VOL voltage or UP/DN buttons.

In monitor mode, the gain stage can be set to an fixed default attenuation level for reducing the loudness of the music.

*Figure 12. Line Inputs*




### 8.1.2 Parameter

VBAT=1.5V, $T_A$= 25ºC, unless otherwise specified.

*Table 4. Line Input Parameter*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{LIN}$ | Input Signal Level | | | 0.6* VBAT | VBAT | $V_{PEAK}$ |
| $R_{LIN}$ | Input Impedance | 0dB gain (12.5k // 10k) | | 5.6 | | kΩ |
| | | -46.5dB gain (25k // 10k) | | 7.2 | | kΩ |
| | | MUTE | | 10 | | kΩ |
| $\Delta_{RLIN}$ | Input Impedance Tolerance | | | ±30 | | % |
| $C_{LIN}$ | Input Capacitance | | | 5 | | pF |
| $A_{LIN}$ | Programmable Gain | | -46.5 | | +0 | dB |
| | Gain Steps | Discrete logarithmic gain steps | | 0.75 | | dB |
| | Gain Step Accuracy | | | 0.5 | | dB |
| $A_{LINMUTE}$ | Mute Attenuation | | | 100 | | dB |

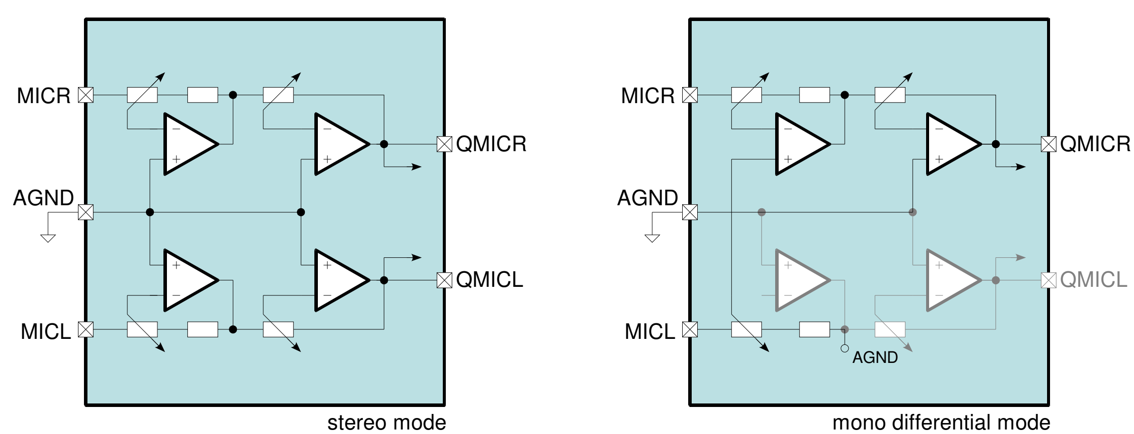
*Table 4. Line Input Parameter (Continued)*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $\Delta_{ALIN}$ | Gain Ramp Rate | PotiMode, Tinit=100ms | | 20 | | ms/step |
| | | ButtonMode, Tinit=400ms | | 80 | | |
| | | MonitorMode | | 8 | | |
| $V_{ATTACK}$ | Limiter Activation Level | HPL/R start of neg. clipping | | | | $V_{PEAK}$ |
| $V_{DECAY}$ | Limiter Release Level | HPL/R | | VNEG +0.3 | | $V_{PEAK}$ |
| $t_{ATTACK}$ | Limiter Attack Time | | | 4 | | µs |
| $t_{DECAY}$ | Limiter Decay Time | | | 8 | | ms |

## 8.2 Microphone Input

The AFE offers two microphone inputs and one low noise microphone voltage supply (microphone bias). The inputs can be switched to single ended or differential mode.

*Figure 13. Microphone Input*




### 8.2.1 Gain Stage & Limiter

The Mic GainStage has programmable Gain within -6dB…+41.625dB in 128 steps of 0.375dB.

As soft-start function is implemented for an automatic gain ramping implemented with steps of 4ms to fade in the audio at the end of the start-up sequence.

A limiter automatically attenuates high input signals. The AGC has 127 steps with 0.375dB with a dynamic range of the full gain stage.

In monitor mode, the gain stage can be set to an fixed (normally higher) gain level or be controlled by the VOL pin.

### 8.2.2 Supply

The MICS charge pump is providing a proper microphone supply voltage for the AAA supply. Since AAA batteries are operating down to 1.0V, the direct battery voltage cannot be used for mic-supply. There are 2 modes.

The first mode SWITCH-MODE for 1.8V supply is to have just a switch from VBAT to MICS. With this switch, the microphone current is switched off in idle mode.

The second mode CHAREGPUMP_MODE for AAA batteries is the real charge pump mode, in this mode a positive voltage is generated of about 2* VBAT.

It is also possible to switch off the microphone supply if not needed (e.g. playback without ANC)

### 8.2.3 Parameter

VBAT=1.5V, $T_A$= 25ºC unless otherwise specified.

*Table 5. Microphone Input Parameter*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{MICIN}0$ | Input Signal Level | $A_{MIC}$ = 30dB | | 20 | | $mV_P$ |
| $V_{MICIN}1$ | | $A_{MIC}$ = 36dB | | 10 | | $mV_P$ |
| $V_{MICIN}2$ | | $A_{MIC}$ = 42dB | | 5 | | $mV_P$ |
| $R_{MICIN}$ | Input Impedance | MICP to AGND | | 7.5 | | kΩ |
| $\Delta_{MICIN}$ | Input Impedance Tolerance | | | -7<br>+33 | | % |
| $C_{MICIN}$ | Input Capacitance | | | 5 | | pF |
| $A_{MIC}$ | Programmable Gain | | -6 | | +41.6 | dB |
| | Gain Steps | Discrete logarithmic gain steps | | 0.375 | | dB |
| | Gain Step Precision | | | 0.15 | | dB |
| $\Delta_{AMIC}$ | Gain Ramp Rate | Tinit=64ms | | 4 | | ms/step |
| $V_{ATTACK}$ | Limiter Activation Level | $V_{PEAK}$ related to VBAT or VNEG | | 0.67 | | 1 |
| $V_{DECAY}$ | Limiter Release Level | | | 0.4 | | 1 |
| $A_{MICLIMIT}$ | Limiter Gain Overdrive | 127 @ 0.375dB | | 41.625 | | dB |
| $t_{ATTACK}$ | Limiter Attack Time | | | 5 | | µs/step |
| $t_{DECAY-DEB}$ | Limiter Decay Debouncing Time | | | 64 | | ms |
| $t_{DECAY}$ | Limiter Decay Time | | | 4 | | ms/step |
| | | | | | | |
| $V_{MICS}$ | Microphone Supply Voltage | | | VBAT*2-<br>240mV | | V |
| $I_{MICSMIN}$ | Min. Microphone Supply Current | VBAT=+1.0V<br>VNEG=-0.7V<br>MICS=+1.75V | | 650 | | µA |
| $R_{OUT\_CP}$ | CP Output Resistance | | | 1300 | | Ω |

## 8.3 Headphone Output

The headphone output is a true ground output using VNEG as negative supply, designed to provide the audio signal with 2x12mW @ 16Ω-64Ω, which are typical values for headphones. It is also capable to operate in bridged mode for higher impedance (e.g. 300Ω) headphone. In this mode the left output is carrying the inverted signal of the right output shown in Figure 15.

*Figure 14. Headphone Output Single Ended Mode*

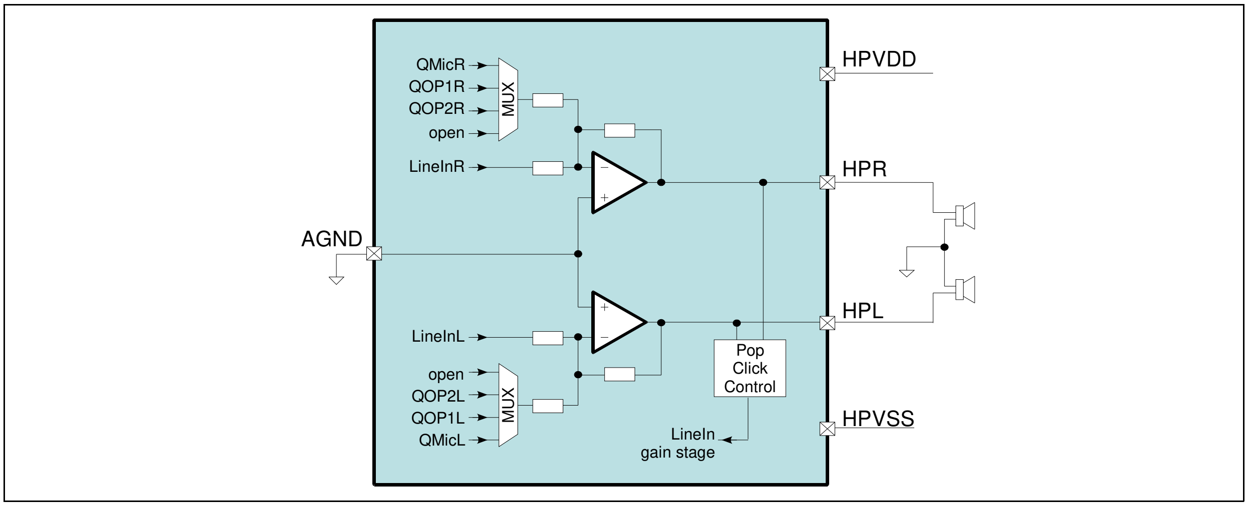
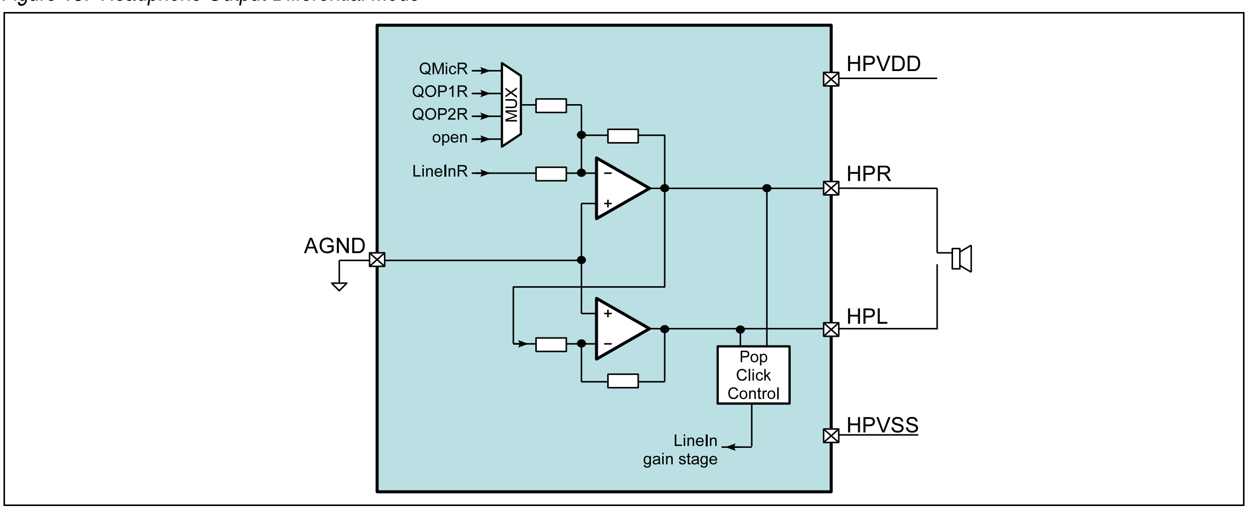



*Figure 15. Headphone Output Differential Mode*




### 8.3.1 Input Multiplexer

The signal from the line-input gain stage gets summed at the input of the headphone stage with the microphone gain stage output, the first filter opamp output or the second filter opamp output. The microphone gain stage output is used per default. It is also possible to playback without ANC by only using the line-input gain stage with no other signal on the multiplexer.

For the monitor mode, the setting of this input multiplexer can be changed to another source, normally to the microphone.

### 8.3.2 No-Pop Function

The No-Pop startup of the headphone stage takes 60ms to 120ms dependent on the supply voltage.

### 8.3.3 No-Clip Function

The headphone output stage gets monitored by comparator stages which detect if the output signal starts to clip.

This signal is used to reduce the LineIn gain to avoid distortion of the output signal. A hystereses avoids jumping between 2 gain steps for a signal with constant amplitude.

### 8.3.4 Over-Current Protection

The over-current protection has a threshold of 150-200mA and a debouncing time of 8µs. The stage is forced to OFF mode in an over-current situation. After this, the headphone stage tries to power up again every 8ms as long as the over-current situation still exists or the stage is turned off manually.

### 8.3.5 Parameter

VBAT=1.5V, $T_A$= 25ºC, unless otherwise specified.

*Table 6. Headphone Output Parameter*

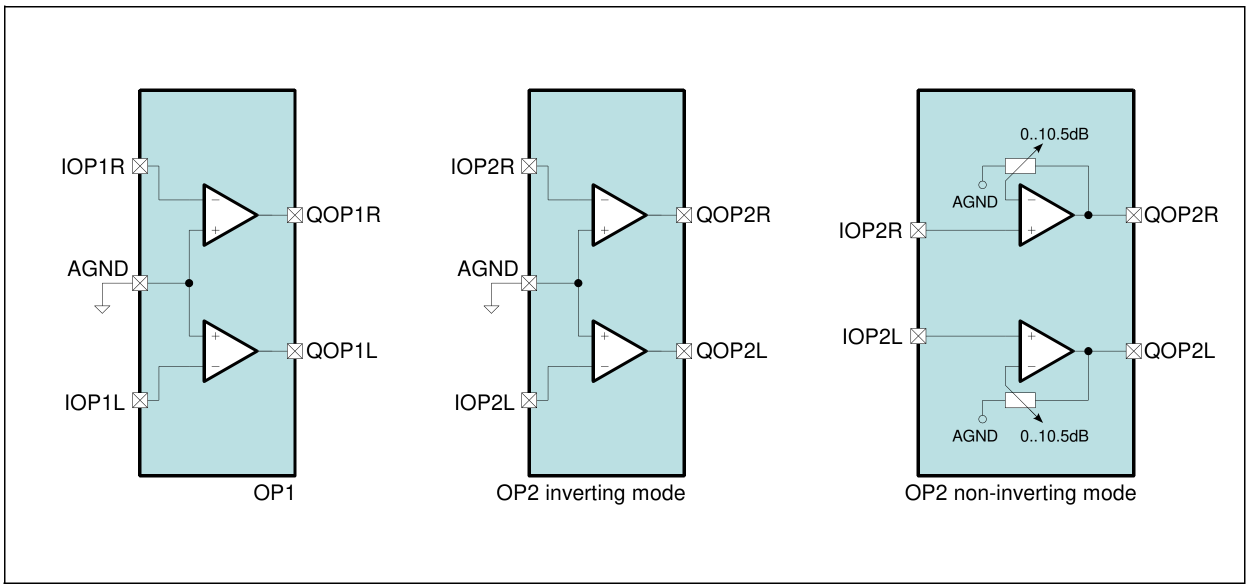
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{L\_HP}$ | Load Impedance | Stereo mode | 16 | | | Ω |
| $C_{L\_HP}$ | Load Capacitance | Stereo mode | | | 100 | pF |
| $P_{HP}$ | Nominal Output Power | RL=64Ω | 12 | | | mW |
| | | RL=32Ω | 24 | | | mW |
| | | RL=16Ω | 34 | | | mW |
| $P_{SRRHP}$ | Power Supply Rejection Ratio | 200Hz-20kHz, 720mVpp, RL=16Ω | | 90 | | dB |

## 8.4 Operational Amplifier

While AS3410 offers only one operational amplifier for feed-forward ANC, AS3400 and AS3430 feature an additional second operational amplifier stage to perform feed-back ANC or any other additional needed filtering.

Both operational amplifiers stages can be activated and used individually. While OP1 stage is always configured as inverting amplifier, OP2 stage can be also switched to a non-inverting mode with an adjustable gain of 0...+10.5dB.

*Figure 16. Operational Amplifiers*



### 8.4.1 Parameter

VBAT=1.5V, $T_A$= 25ºC, unless otherwise specified.

*Table 7. Headphone Output Parameter*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{L\_OP}$ | Load Impedance | Single ended | 1 | | | kΩ |
| $C_{L\_OP}$ | Load Capacitance | Single ended | | | 100 | pF |
| $GBW_{OP}$ | Gain Band Width | | | 4.3 | | MHz |
| $V_{OS\_OP}$ | Offset Voltage | | | | 6 | mV |
| $V_{EIN\_HP}$ | Equivalent Input Noise | 200Hz-20kHz | | 2.6 | | μV |

## 8.5 SYSTEM

The system block handles the power up and power down sequencing, as well as, the mode switching.

### 8.5.1 Power Up/Down Conditions

The chip powers up when one of the following conditions is true:

*Table 8. Power UP Conditions*

| # | Source | Description |
|---|---|---|
| 1 | MODE pin | In stand-alone mode, MODE pin has to be driven high to turn on the device |
| 2 | I2C start | In I2C mode, a I2C start condition turns on the device |

The chip automatically shuts off if one of the following conditions arises:

*Table 9. Power DOWN Conditions*

| # | Source | Description |
|---|---|---|
| 1 | MODE pin | Power down by driving MODE pin to low |
| 2 | SERIF | Power down by SERIF writing 0h to register 20h bit <0> |
| 3 | Low Battery | Power down if VBAT is lower than the supervisor off-threshold |
| 4 | VNEG CP OVC | Power down if VNEG is higher than the VNEG off-threshold |

### 8.5.2 Start-up Sequence

The start-up sequence depends on the used mode.

In stand-alone mode the sequence runs automatically, in I2C mode the sequence runs till a defined state and waits then for an I2C command. Either the automatic sequence is started by setting the CONT_PWRUP bit in addition to the PWR_HOLD bit. If only the PWR_HOLD is set all enable bits for headphone, microphone, etc have to be set manually.

*Figure 17. Stand-Alone Mode Start-Up Sequence*

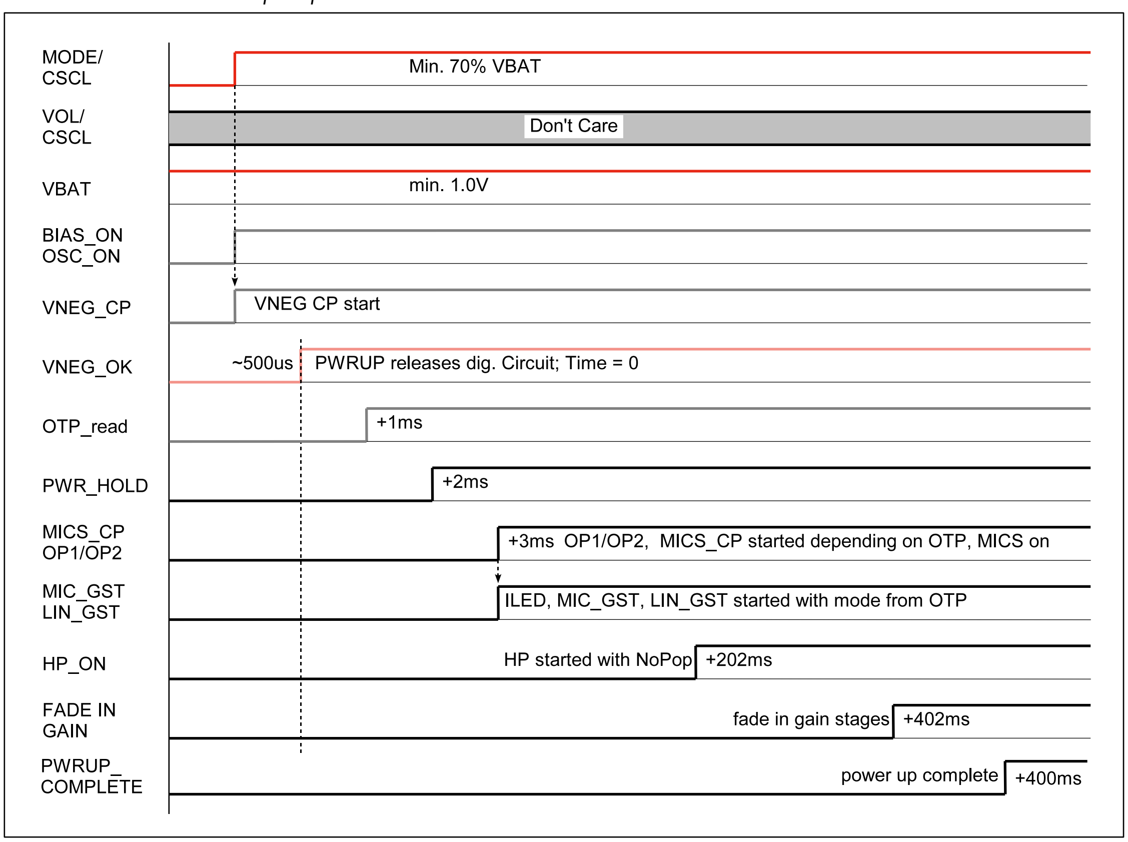
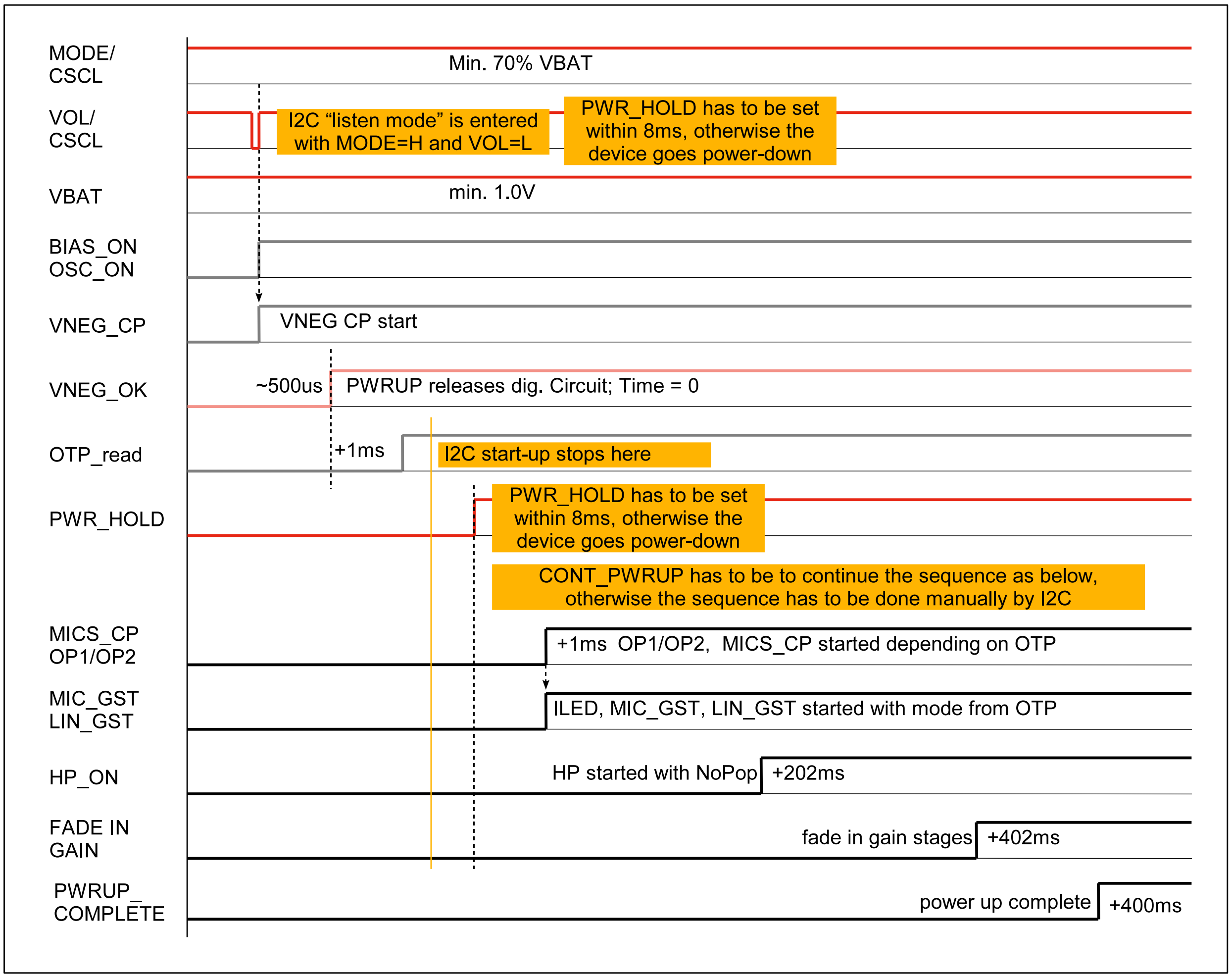


*Figure 18. I2C Mode Start-Up Sequence*




The total start-up time (inlcuding fade-in of the gain stages) can be reduced from 900ms to 600ms by OTP setting.

### 8.5.3 Mode Switching

When the chip is in stand-alone mode (no I2C control), the mode can be switched with different levels on the MODE pin.

*Table 10. Operation Modes*

| MODE | MODE pin | Description |
|---|---|---|
| OFF | LOW (VSS) | Chip is turned off |
| ANC | HIGH (VBAT) | Chip is turned on and active noise cancellation is active |
| MONITOR | VBAT/2 | Chip is turned on and monitor mode is active<br>In Monitor mode, a different (normally higher) microphone preamplifier gain can be chosen to get an amplification of the surrounding noise. This volume can be either fixed or be controlled by the VOL input.<br>To get rid of the low pass filtering needed for the noise cancellation, the headphone input multiplexer can be set to a different (normally to MIC) source.<br>In addition, the LineIn gain can be lowered to reduce the loudness of the music currently played back. |

In I2C mode, the monitor mode can be activated be setting the corresponding bit in the system register.

#### 8.5.4 Status Indication

AS3410and AS3430 features a on-status information via the current output pin ILED. The current can be controlled in 3 steps and be switched off, by setting the PWM to 0%, 25%, 50% or 100% duty cycle of a 50kHz signal.

If LOW_BAT is active, ILED switches to blinking with 1Hz, 50% duty cycle and 50% current setting.

### 8.6 VNEG Charge Pump

The VNEG charge pump uses one external 1uF capacitor to generate a negative supply voltage out of the battery input voltage to supply all audio related blocks. This allows a true-ground headphone output with no more need of external dc-decoupling capacitors.

#### 8.6.1 Parameter

VBAT=1.5V, $T_A$= 25ºC, unless otherwise specified.

*Table 11. Headphone Output Parameter*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | VBAT | 1.0 | 1.5 | 1.8 | V |
| $V_{OUT}$ | Output voltage | VNEG | -0.7 | -1.5 | -1.8 | V |
| $C_{EXT}$ | External flying capacitor | | | 1 | | µF |

### 8.7 OTP Memory & Internal Registers

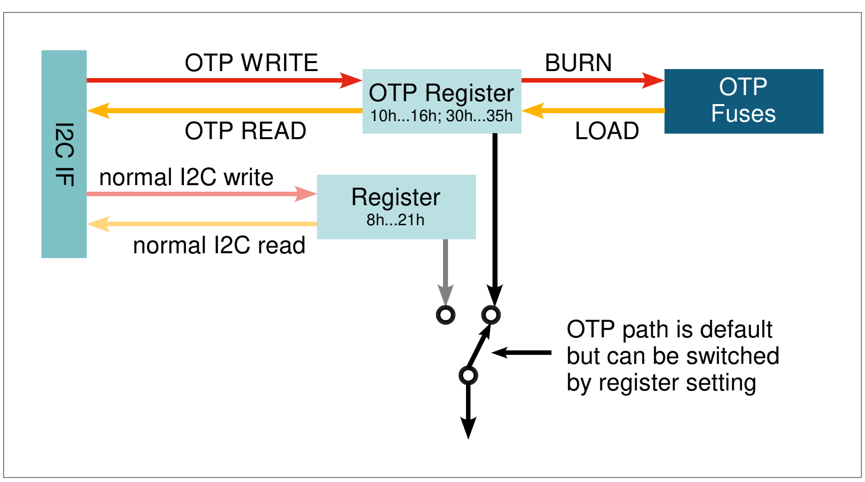
The OTP memory consists of OTP register and the OTP fuses.The OTP register can be written as often as wanted but will lose the content on power off. The OTP fuses are intended to store basic chip configurations as well as the microphone gain settings to optimize the ANC performance and get rid of sensitivity variations of different microphones. Burning the fuses can only be done once and is a permanent change, which means the fuses keep the content even if the chip is powered down. This AS3400/10/30 offers 4 register set for storing the microphone gain making it possible to change the gain 3 times for re-calibration or other purposes.

When the chip is controlled by a microcontroller via I2C, the OTP memory don't has to be used.

#### 8.7.1 Register & OTP Memory Configuration

Figure 19 is showing the principal register interaction.

*Figure 19. Register Access*



Registers 0x8, 0x9, 0xA, 0xB, 0xC and 0x21 have only effect when the corresponding "REG_ON" bit is set, otherwise the chip operates with the OTP Register settings which are loaded from the OTP fuses at every start-up.

All registers settings can be changed several times, but will loose the content on power off. When using the I2C mode, the chip configuration has to be loaded from the microcontroller after every start-up. In stand alone mode the OTP fuses have to be programmed for a permanent change of the chip configuration.

A single OTP cell can be programmed only once. Per default, the cell is "0"; a programmed cell will contain a "1". While it is not possible to reset a programmed bit from "1" to "0", multiple OTP writes are possible, but only additional unprogrammed "0"-bits can be programmed to "1".

Independent of the OTP programming, it is possible to overwrite the OTP register temporarily with an OTP write command at any time. This setting will be cleared and overwritten with the hard programmed OTP settings at each power-up sequence or by a LOAD operation.

The OTP memory can be accessed in the following ways:

***LOAD Operation.*** The LOAD operation reads the OTP fuses and loads the contents into the OTP register. A LOAD operation is automatically executed after each power-on-reset.

***WRITE Operation.*** The WRITE operation allows a temporary modification of the OTP register. It does not program the OTP. This operation can be invoked multiple times and will remain set while the chip is supplied with power and while the OTP register is not modified with another WRITE or LOAD operation.

***READ Operation.*** The READ operation reads the contents of the OTP register, for example to verify a WRITE command or to read the OTP memory after a LOAD command.

***BURN Operation.*** The BURN operation programs the contents of the OTP register permanently into the OTP fuses. Don't use old or nearly empty batteries for burning the fuses.

**Attention:** If you once burn the OTP_LOCK bit, no further programming, e.g. setting additional "0" to "1", of the OTP can be done.

For production, the OTP_LOCK bit must be set to avoid an unwanted change of the OTP content during the livetime of the product.

### 8.7.2 OTP Fuse Burning

In most stand alone applications, the I2C pins are not accessible. Burning the fuses can be done by switching the line inputs into a special mode to access the chip by I2C over the line input connections. This allows trimming of the microphone gain with no openings in the final housing and so no influence to the acoustic of the headset.

This mode is called "Application Trimm" mode, or short "APT". (Patent Pending)

During the application trimm mode LINR has to provide the clock, while LINL has to provide the data for the I2C communication.

Please note that the OTP register cannot be accessed directly but have to be enabled before a read or write access. This is independent whether you access the OTP register via the normal I2C pins or in application trimm mode via LINL and LINR. Please refer to the detailed register description to get more information on how the registers can be accessed.

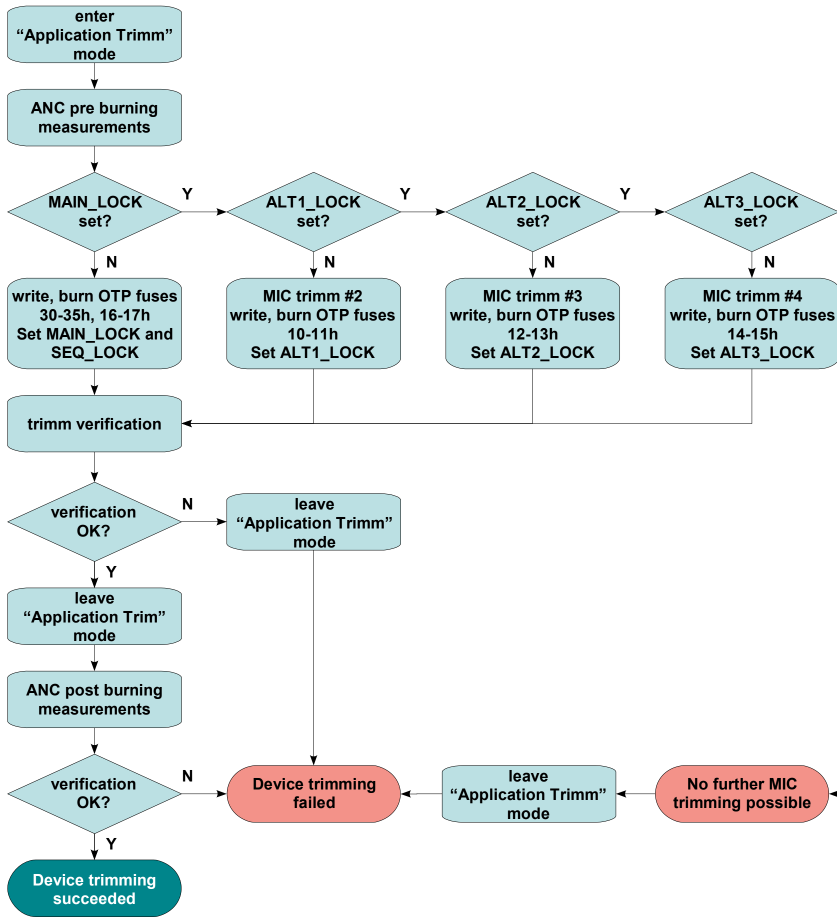
To achieve a proper burning of the fuses, the negative supply has to be buffered by applying an external negative supply during burning. This voltage can also be applied to the LINL terminal. An internal switch is connecting LINL and VNEG during the fuse burning. LINR has to provide the clock for burning the fuses.

The below flow chart shows the principle steps of the OTP burning process. The application trimm mode can only be entered at a specific timing during the start-up sequence.

The device offers the possibility to change microphone gain settings 3 times by using alternative registers. The selection which register set is being used to set the microphone gain is done by the "lock" bits of the corresponding registers.

A more detailed description of the individual steps is available in an application note.

*Figure 20. OTP Burning Process*




## 8.8 2-Wire-Serial Control Interface

There is an I2C slave block implemented to have access to 64 byte of setting information.

The I2C address is: Adr_Group8 - audio processors

- 8Eh_write
- 8Fh_read

### 8.8.1 Protocol

*Table 12. 2-Wire Serial Symbol Definition*

| Symbol | Definition | RW | Note |
|---|---|---|---|
| S | Start condition after stop | R | 1 bit |
| Sr | Repeated start | R | 1 bit |
| DW | Device address for write | R | 1000 1110b (8Eh) |
| DR | Device address for read | R | 1000 1111b (8Fh) |
| WA | Word address | R | 8 bit |

*Table 12. 2-Wire Serial Symbol Definition*

| Symbol | Definition | RW | Note |
|---|---|---|---|
| A | Acknowledge | W | 1 bit |
| N | No Acknowledge | R | 1 bit |
| reg_data | Register data/write | R | 8 bit |
| data (n) | Register data/read | W | 8 bit |
| P | Stop condition | R | 1 bit |
| WA++ | Increment word address internally | R | during acknowledge |
| (shaded) | AS3400 AS3410 AS3430 (=slave) receives data | | |
| (white) | AS3400 AS3410 AS3430 (=slave) transmits data | | |

*Figure 21. Byte Write*

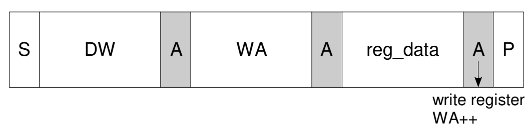
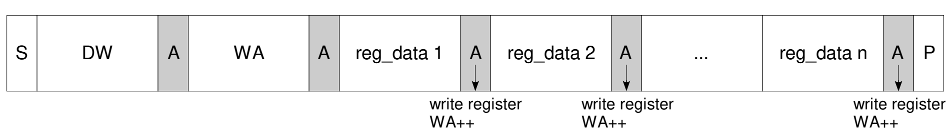



*Figure 22. Page Write*

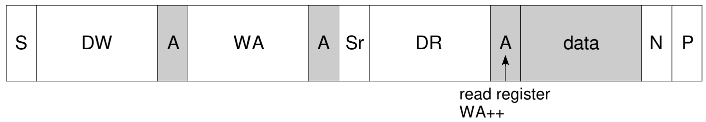



Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

*Figure 23. Random Read*

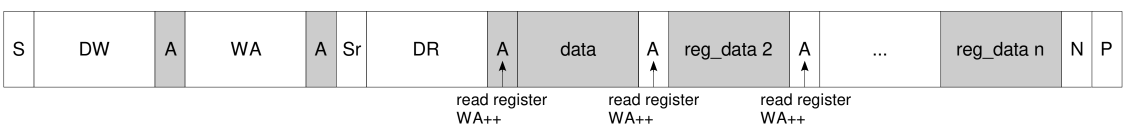



Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

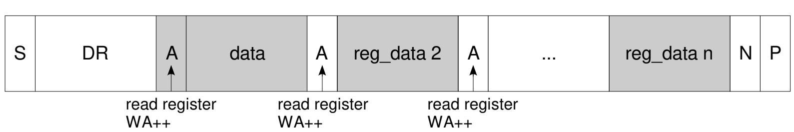
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

*Figure 24. Sequential Read*




Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

*Figure 25. Current Address Read*




To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.