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AS3421 AS3422

Low Power Ambient Noise-Cancelling Speaker Driver

1 General Description

The AS3421/22 are speaker driver with Ambient Noise Cancelling function for headsets, headphones or ear pieces. It is intended to improve quality of e.g. music listening, a phone conversation etc. by reducing background ambient noise.

The fully analog implementation allows the lowest power consumption, lowest system BOM cost and most natural received voice enhancement otherwise difficult to achieve with DSP implementations. The device is designed to be easily applied to existing architectures.

An internal OTP-ROM can be optionally used to store the microphone gain calibration settings as well as all application specific settings.

The AS3421/22 can be used in different configurations for best trade-off of noise cancellation, required filtering functions and mechanical designs.

The simpler feed-forward topology is used to effectively reduce frequencies typically up to 2-3kHz. The feed-back topology with either 1 or 2 filtering stages has it strengths especially at very low frequencies. The typical bandwidth for feedback system is from 20Hz up to 1kHz which is a little bit lower than with feed forward systems.

The filter loop for both systems is determined by measurements, for each specific headset individually, and depends very much on mechanical designs. The gain and phase compensation filter network is implemented with cheap resistors and capacitors for lowest system costs.

AS3421/22 features also an audio playback only mode which allows the user to easily switch between ANC on and off mode. In ANC off mode unused blocks are automatically switch off to guaranty lowest power consumption in each operating mode.

2 Key Features

Microphone Input

- 128 gain steps @ 0.375dB and MUTE with AGC
- Differential, low noise microphone amplifier
- Single ended or differential mode
- Improved supply for electret microphone
- MIC gain OTP programmable

High Efficiency Headphone Amplifier

- 2x23mW, 0.1% THD+N @ 32Ω, 1.5V supply, 100dB SNR
- Bridged mode for e.g. 300Ω loads
- Click and pop less start-up and mode switching

Line Input

- Volume control via serial interface or push buttons
- 64 steps @ 0.75dB and MUTE, pop-free gain setting
- Fully differential stereo line inputs

ANC processing

- Feed-forward cancellation
- Feed-back cancellation with filter loop transfer function definable via simple RC components
- Simple in production SW calibration
- 12-30dB noise reduction (headset dependent)
- 10-3000Hz wide frequency active noise attenuation (headset dependent)

Monitor Function

- For assisted hearing, i.e. to monitor announcements
- Fixed (OTP prog.) ambient sound amplification to compensate headphone passive attenuation

Incremental Functions

- ANC with or without music on the receiving path
- Music Playback mode for lowest power consumption
- OTP ROM for automatic trimming during production (4 times programmable)

Performance Parameter

- 7mA @ 1.5V stereo ANC; <1µA quiescent
- Extended PSRR for 217Hz
- Increased TDMA noise immunity

Interfaces

- 2-wire serial control mode & volume inputs
- Calibration via Line-In or 2-wire serial interface
- Fixed 1.0-1.8V supply with internal CP

Package

- AS3421 QFN24 [4x4mm] 0.5mm pitch
- AS3422 QFN32 [5x5mm] 0.5mm pitch

3 Applications

The devices are ideal for wireless devices like stereo Bluetooth headsets as well as stereo wireless headsets.

Figure 1. AS3421 Feed Forward ANC Block Diagram

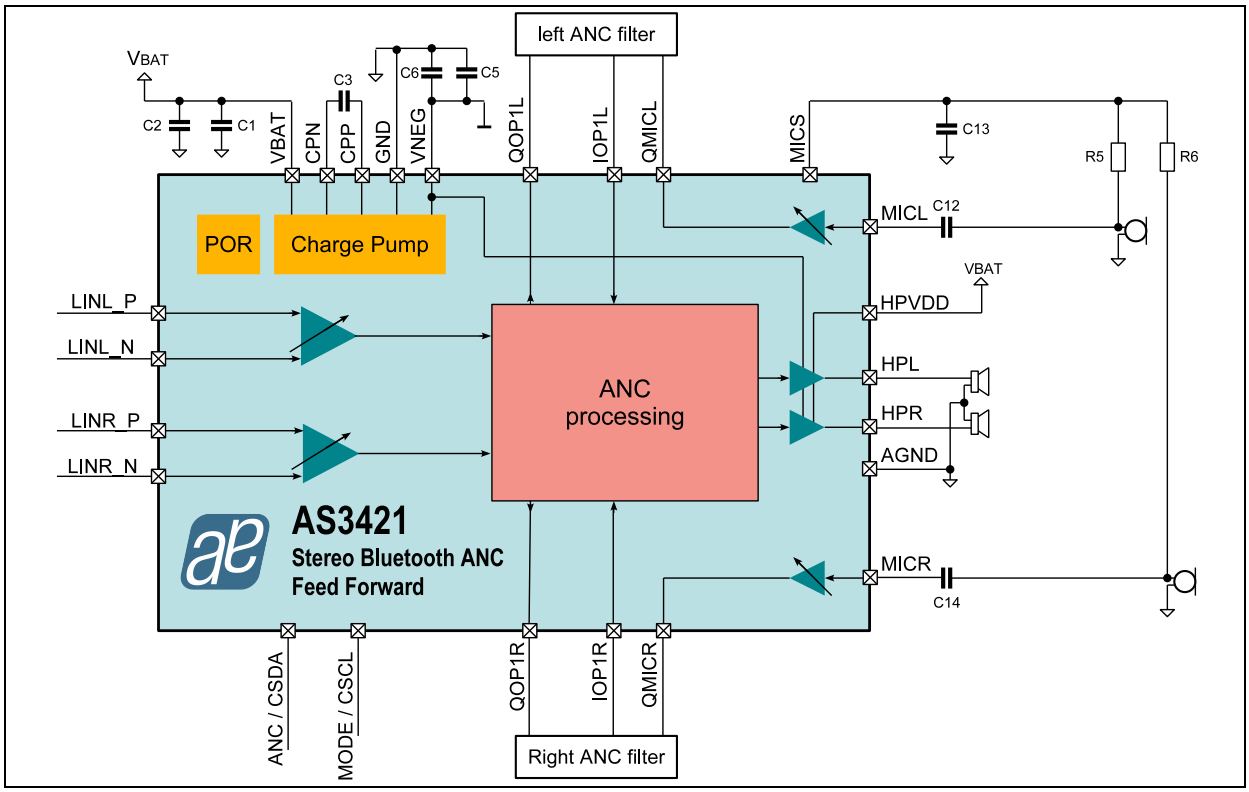
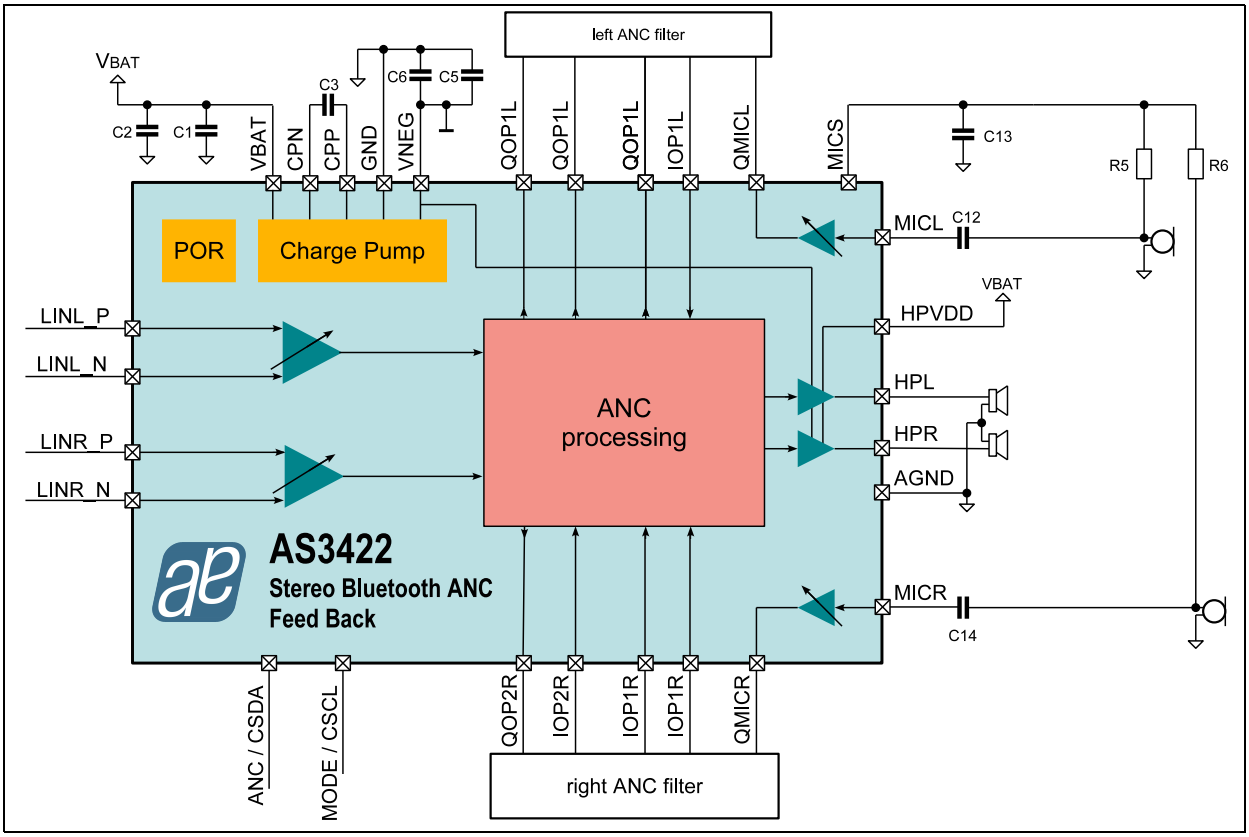


Figure 2. AS3422 Feed-Back Block Diagram

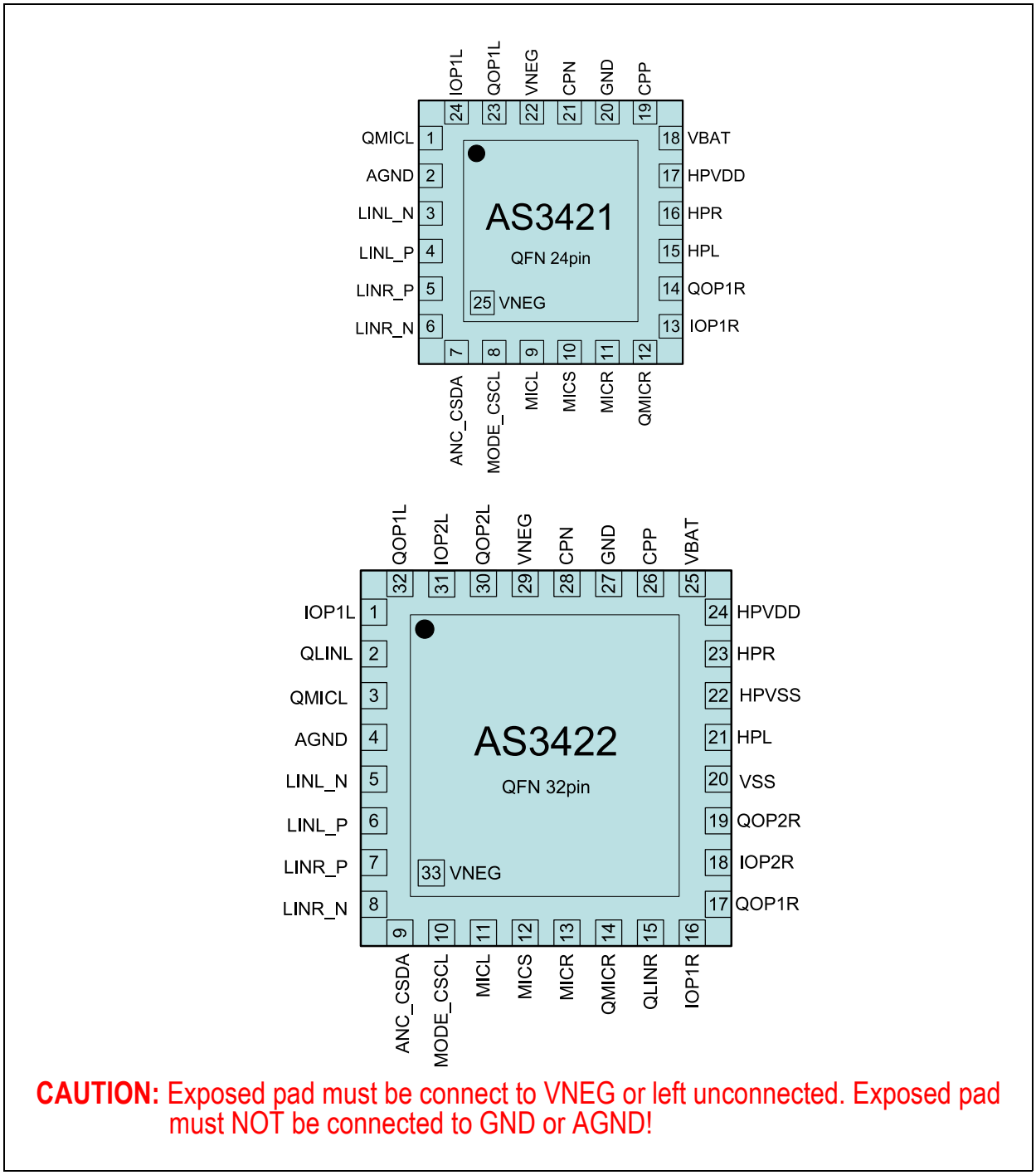


4 Contents

5 Pin Assignments

Note: Pin assignment may change in preliminary data sheets.

Figure 3. Pin Assignments (Top View)



CAUTION: Exposed pad must be connect to VNEG or left unconnected. Exposed pad must NOT be connected to GND or AGND!

5.1 Pin Descriptions

Note: Pin description may change in preliminary data sheets.

Table 1. Pin Description for AS3421 AS3422

Pin Name	Pin Number		Type	Description
	AS3421	AS3422		
IOP1L	24	1	ANA IN	Filter OpAmp1 Input Left Channel
QLINL		2	ANA OUT	Line In Gain Stage Output Left Channel
QMICL	1	3	ANA OUT	MIC GainS tage Output Right Channel
AGND	2	4	ANA IN	Analog Reference
LINL_N	3	5	ANA IN	Negative Line In pin of Left Channel
LINL_P	4	6	ANA IN	Positive Line In pin of Left Channel
LINR_P	5	7	ANA IN	Positive Line In pin of Right Channel
LINR_N	6	8	ANA IN	Negative Line In pin of Right Channel
ANC_CSDA	7	9	MIXED IO	Serial Interface Data ANC Pin (Enable/Disable ANC function)
MODE_CSCL	8	10	DIG IN	Mode Pin (Power Up/Down, Monitor) Serial Interface Clock
MICL	9	11	ANA IN	Microphone In Left Channel
MICS	10	12	ANA OUT	Microphone Supply
MICR	11	13	ANA IN	Microphone Input Right Channel
QMICR	12	14	ANA OUT	MIC Gain Stage Output Right Channel
QLINR		15	ANA OUT	Line In Gain Stage Output Right Channel
IOP1R	13	16	ANA IN	FilterOpAmp1 Input Right Channel
QOP1R	14	17	ANA IN	Filter OpAmp1 Output Right Channel
IOP2R		18	ANA IN	Filter OpAmp2 Input Right Channel
QOP2R		19	ANA OUT	Filter OpAmp2 Output Right Channel
VSS		20	SUP IN	VSS supply terminal
HPL	15	21	ANA OUT	Headphone Output Left Channel
HPVSS		22	SUP IN	Headphone amplifier VSS supply terminal
HPR	16	23	ANA OUT	Headphone Output Right Channel
HPVDD	17	24	SUP IN	Headphone VDD Supply
VBAT	18	25	SUP IN	Positive supply terminal of IC
CPP	19	26	ANA OUT	VNEG ChargePump Flying Capacitor Positive Terminal
GND	20	27	GND	VNEG ChargePump Negative Supply
CPN	21	28	ANA OUT	VNEG ChargePump Flying Capacitor Negative Terminal
VNEG	22	29	SUP IO	VNEG ChargePump Output
QOP2L		30	ANA OUT	Filter OpAmp2 Output Left Channel
IOP2L		31	ANA IN	Filter OpAmp2 Input Left Channel
QOP1L	23	32	ANA OUT	Filter OpAmp1 Output Right Channel
VNEG	25	33	SUP IN	Exposed Pad: connect to VNEG or leave it unconnected

6 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Reference Ground				Defined as in GND
Supply terminals	-0.5	2.0	V	Applicable for pin VBAT, HPVDD
Ground terminals	-0.5	0.5	V	Applicable for pins AGND
Negative terminals	-2.0	0.5	V	Applicable for pins VNEG, VSS, HPVSS
Voltage difference at VSS terminals	-0.5	0.5	V	Applicable for pins VSS, HPVSS
Pins with protection to VBAT	VNEG -0.5	5.0 VBAT+0.5	V	Applicable for pins CPP, CPN
Pins with protection to HPVDD	VSS -0.5	5.0 HPVDD+0.5	V	Applicable for pins LINL_P/N, LINR_P/N, MICL/R, HPR, HPL, QMICL/R, QLINL/R, IOPx, QOPx
other pins	VSS -0.5	5		Applicable for pins MICS, ANC_CSDA, MODE_CSCL
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 17
Continuous Power Dissipation (T_A = +70ºC)				
Continuous Power Dissipation	-	200	mW	P_T[1] for QFN16/24/32 package
Electrostatic Discharge				
Electrostatic Discharge HBM		+/-2	kV	Norm: JEDEC JESD22-A114C
Temperature Ranges and Storage Conditions				
Junction Temperature		+110	ºC	
Storage Temperature Range	-55	+125	ºC	
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	3			Represents a max. floor life time of 168h
Package Body Temperature		260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".*

1. Depending on actual PCB layout and PCB used

7 Electrical Characteristics

VBAT = 1.0V to 1.8V, T_A = -20ºC to +85ºC. Typical values are at VBAT = 1.5V, T_A = +25ºC, unless otherwise specified. All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
T_A	Ambient Temperature Range		-20	+85	°C
Supply Voltages					
GND	Reference Ground		0	0	V
VBAT, HPVDD	Battery Supply Voltage	normal operation with MODE pin high	1.0	1.8	V
		Two wire interface operation	1.4	1.8	V
VNEG	ChargePump Voltage		-1.8	-0.7	V
VSS	Analog neg. Supply Voltages HPVSS, VSS, VNEG		-1.8	-0.7	V
V_{DELTA-}	Difference of Ground Supplies GND, AGND	To achieve good performance, the negative supply terminals should be connected to low impedance ground plane.	-0.1	0.1	V
$V_{DELTA--}$	Difference of Negative Supplies VSS, VNEG, HPVSS	Charge pump output or external supply	-0.1	0.1	V
V_{DELTA+}	Difference of Positive Supplies	VBAT-HPVDD	-0.25	0.25	V
Other pins					
V_{MICS}	Microphone Supply Voltage	MICS	0	3.6	V
V_{HPVDD}	Pins with diode to HPVDD	MICL/R, HPR, HPL, QMICL/R, QLINL/R, IOPx, QOPx	VSS	3.6	V
V_{VBAT}	Pins with diode to VBAT	CPP, CPN	VNEG	VBAT	V
$V_{CONTROL}$	Control Pins	MODE_CSCL, ANC_CSDA	VSS	3.7	V
V_{TRIM}	Line Input & Application Trim Pins	LINL_P, LINL_N, LINR_P, LINR_N	VNEG -0.5 or -1.8	HPVDD +0.5 or 1.8	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{leak}	Leakage current	VBAT<0.8V			20	µA
		VBAT<0.6V			10	µA
Block Power Requirements @ 1.5V VBAT						
I_{OFF}	Off mode current	MODE pin low, device switched off		1		µA
I_{SYS}	Reference supply current	Bias generation, oscillator, ADC6, VNEG		0.25		mA
I_{LIN}	LineIn gain stage current	no signal, stereo		0.5		mA
I_{MIC}	Mic gain stage current	no signal, stereo		2.10		mA
I_{HP}	Headphone stage current	no signal		1.70		mA
I_{MICS}	MICS charge pump current	no load		30		µA
I_{MIN}	Minimal supply current	Sum of all above blocks		4.6		mA
I_{OP1}	OP1 supply current	no load		0.64		mA
I_{OP2}	OP2 supply current	no load		0.64		mA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{MICB}	Microphone bias current	200µA per microphone via charge pump		0.9		mA
I_{PB}	Low Power Playback Mode	V_{BAT} = 1.8V		2,8		mA
		V_{BAT} = 1.5V		2,5		mA
		V_{BAT} = 1.0V		2		mA

8 Typical Operating Characteristics

V_{BAT} = +1.5V, C_1=100nF, C_2=10µF, C_3=1µF, C_6=100nF, C_5=10µF, C_{13}=10µF, C_{12}=2.2µF, C14=2.2µF T_A = +25ºC and HP_MUX_OTP set to '3' unless otherwise specified.

Figure 4. THD+N vs. Pout; Line to HPH; 16Ω single ended stereo

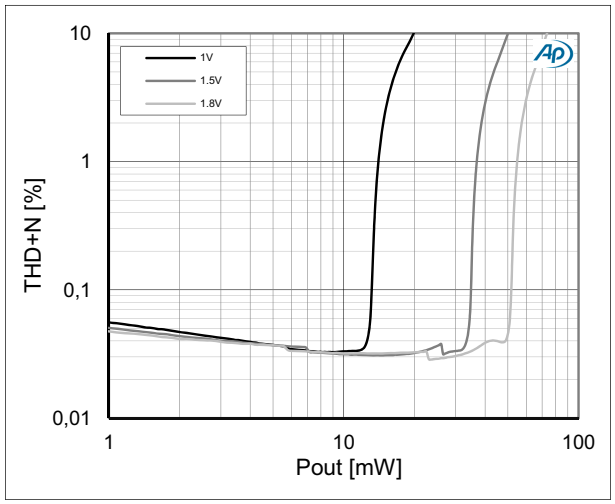


Figure 5. THD+N vs. Pout; Line to HPH; 32Ω single ended stereo

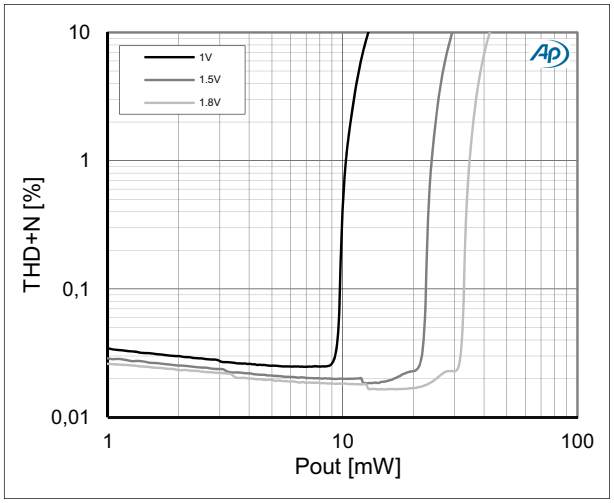


Figure 6. THD+N vs. f; Line to HPH; 1mW load per channel

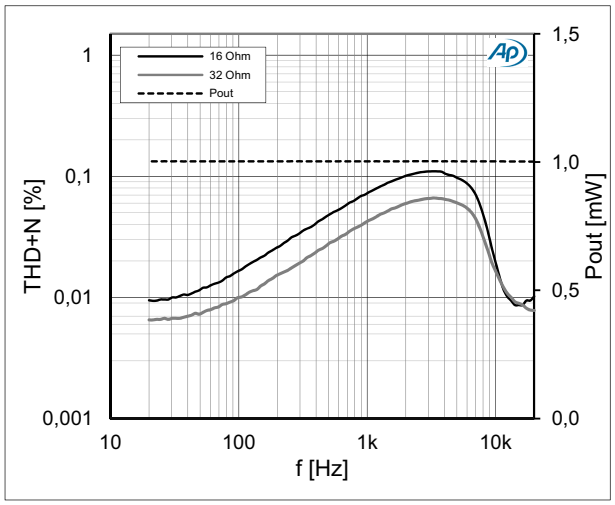


Figure 7. THD+N vs. f; Line to HPH; 10mW load per channel

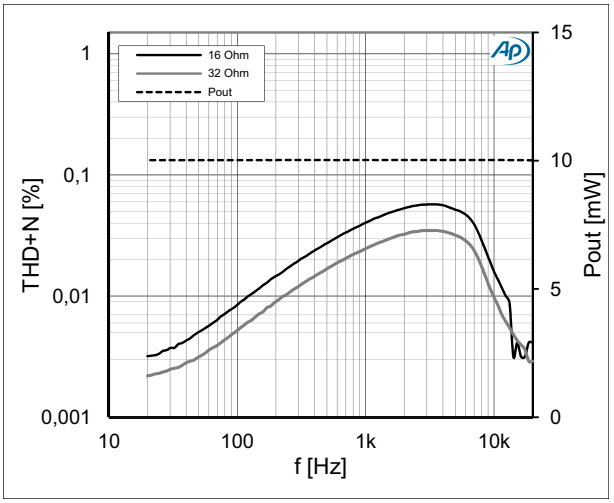


Figure 8. THD+N vs. f; 20mW and 30mW per channel

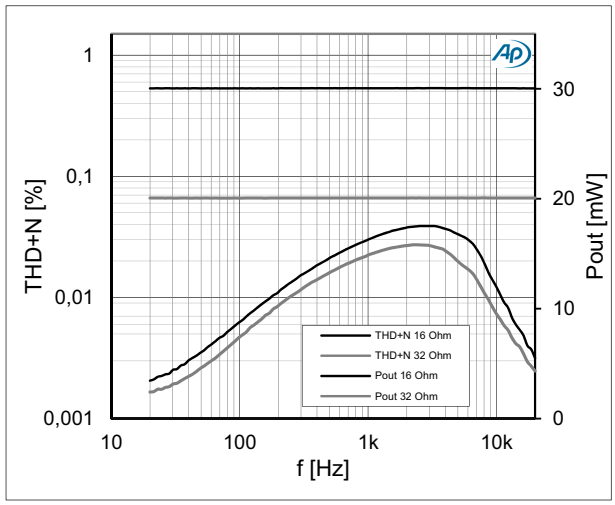


Figure 9. Frequency Response 30mW@16Ω; Line to HPH

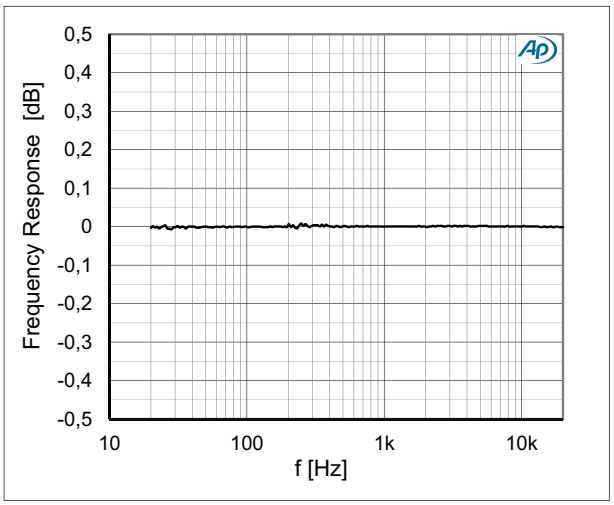


Figure 10. Frequency Response 20mW@32Ω, Line to HPH

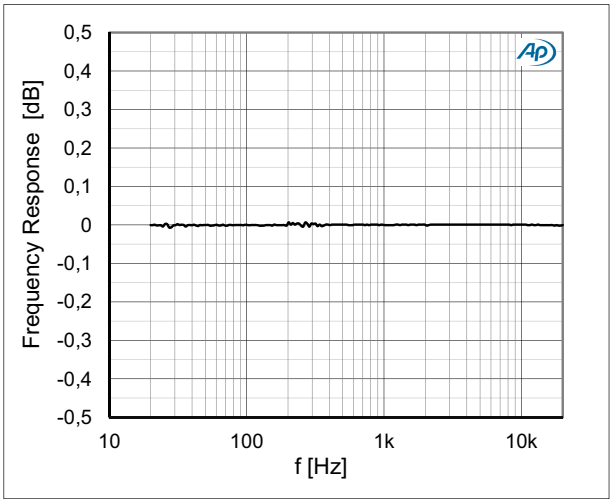


Figure 11. Microphone Supply FFT

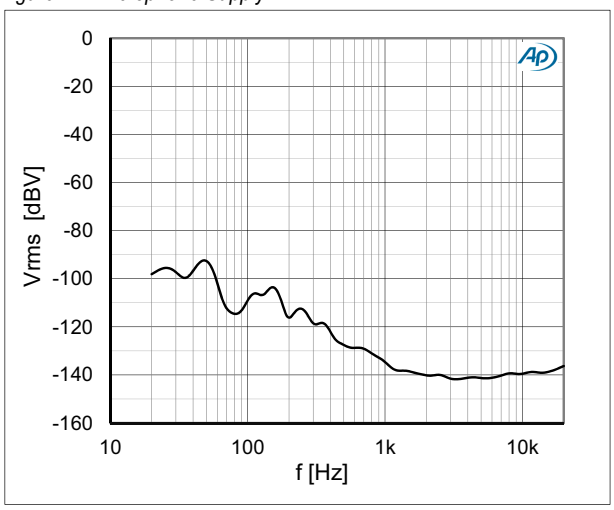


Figure 12. VNEG CP Voltage vs. CP load current with different VBAT supply voltages

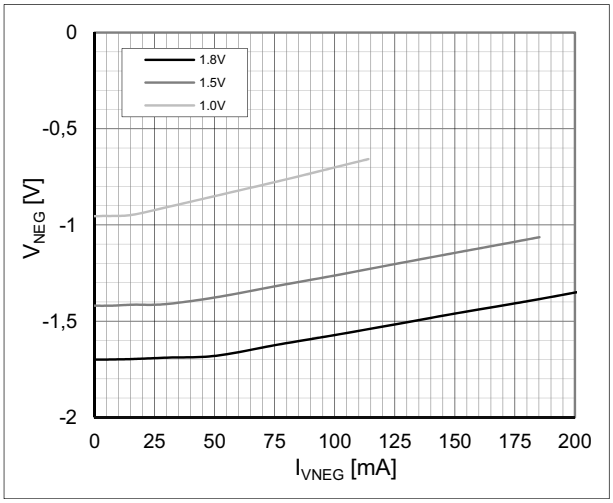


Figure 13. VNEG Efficiency vs.IVNEG with different VBAT supply voltages

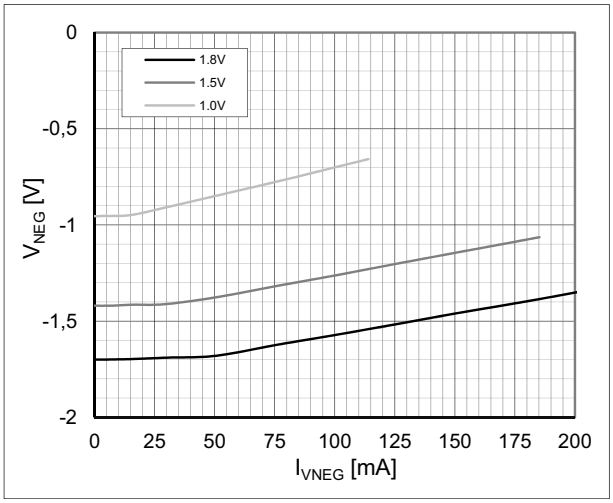


Figure 14. VMIC_OUT vs. IMIC_OUT

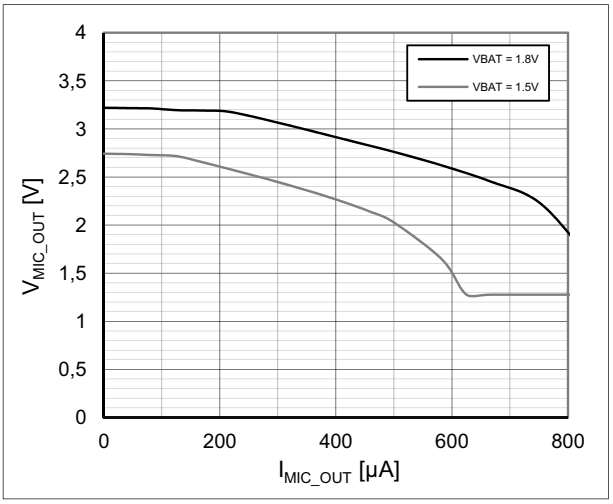


Figure 15. Typical Performance Data, Feed Forward configuration with an over the ear headset

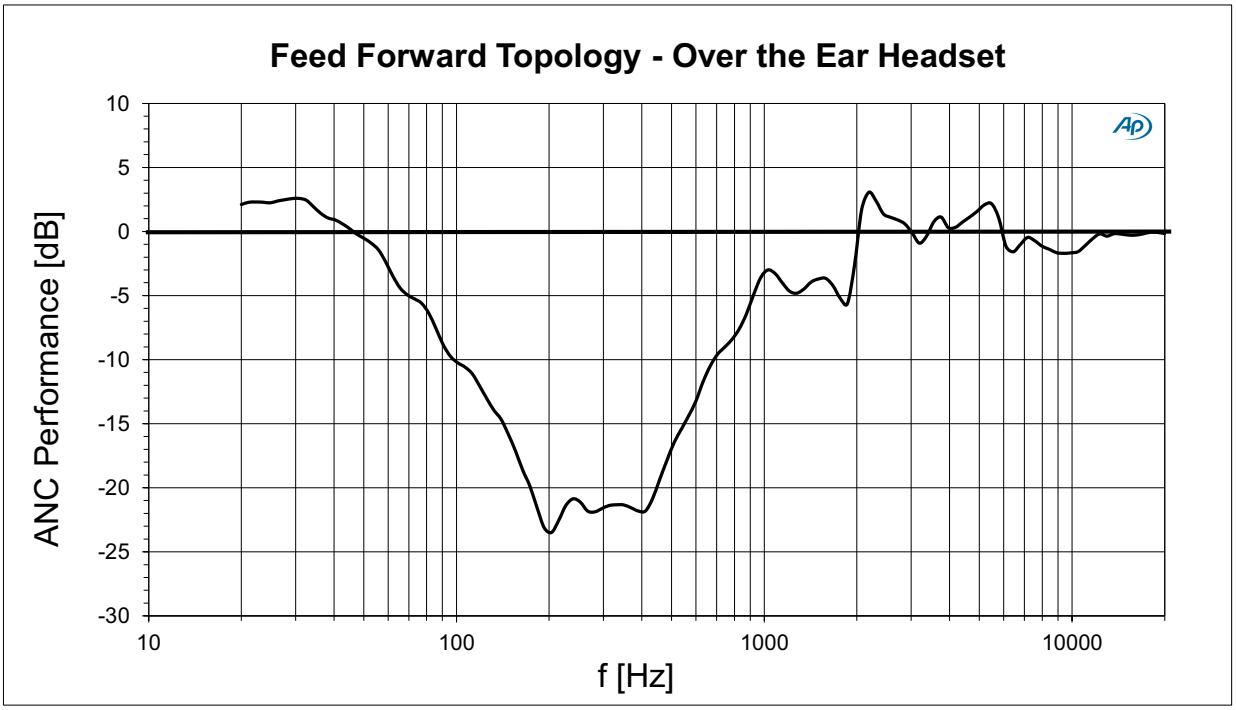
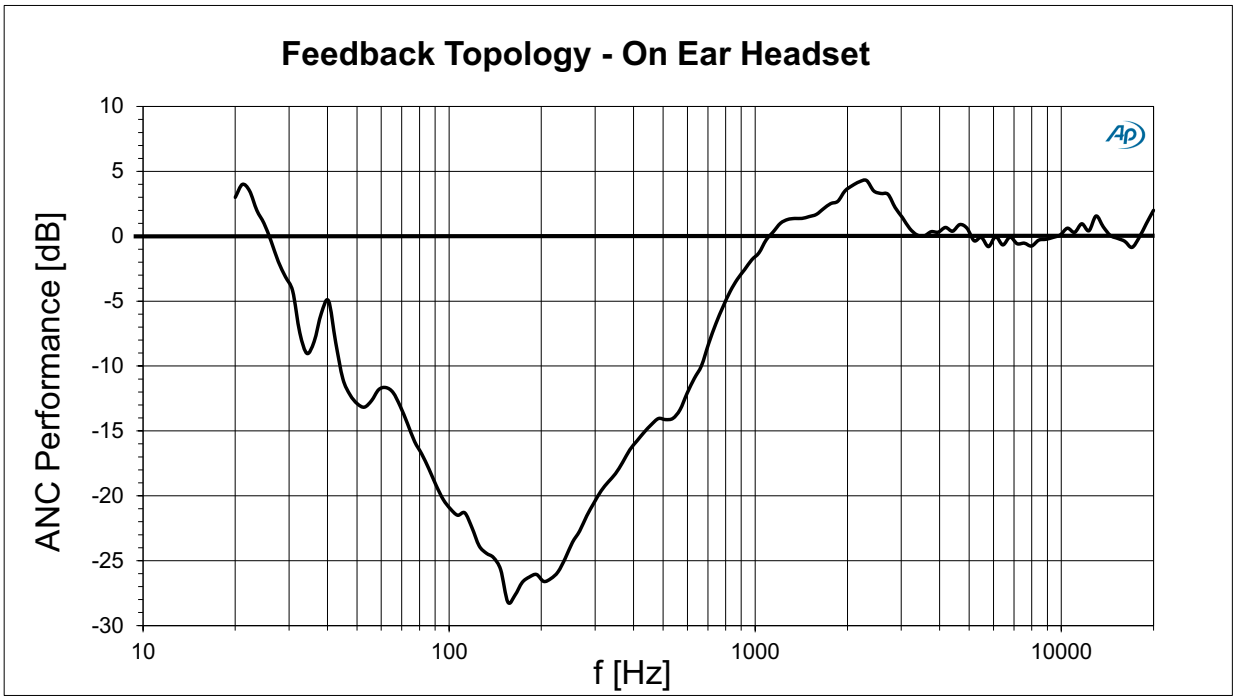


Figure 16. Typical Performance Data, Feedback configuration with an on ear headset



9 Detailed Description

This section provides a detailed description of the device related components.

9.1 Audio Line Input

The chip features one line input. The blocks can work in mono differential or in stereo single ended mode.

In addition to the 12.5-25kΩ input impedance, LineIn has a termination resistor of 10kΩ which is also effective during MUTE to charge eventually given input capacitors.

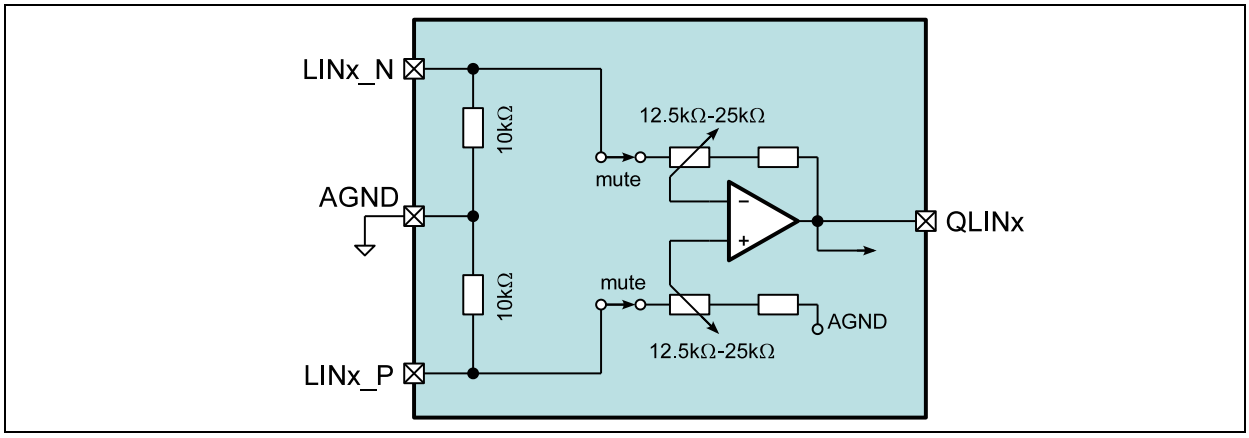
9.1.1 Gain Stage

The Line In gain stage is designed to have 63 gain steps of 0.75dB with a max gain of 0dB plus MUTE per default. By setting the bit Line Gain +3dB in register 0x33 the gain range can be changed from -46.5dB....0dB to -43.5dB ....+3dB.

In default, the gain will be ramped up from MUTE to 0dB during startup. There is a possibility to make the playback volume user controlled by the VOL pin with an ADC converted VOL voltage or UP/DOWN buttons. If the device is configured to control the line input volume via push-buttons the device ramps the gain from -46.5dB to 0dB if no button is pressed. If a user presses a button while ramping up the ramping mechanism will be stopped automatically.

In monitor mode, the gain stage can be set to an fixed default attenuation level for reducing the loudness of the music. To avoid unwanted pop noise in this special mode the internal state machine support very smooth gain fading to avoid unwanted acoustic effects.

Figure 17. Fully Differential Stereo Line Inputs



9.1.2 Parameter

VBAT=1.5V, T_A= 25ºC, unless otherwise specified.

Table 4. Line Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{LIN}	Input Signal Level			0.6* VBAT	VBAT	V_{PEAK}
R_{LIN}	Input Impedance	0dB gain (12.5k // 10k)		5.6		kΩ
		-46.5dB gain (25k // 10k)		7.2		kΩ
		MUTE		10		kΩ
Δ_{RLIN}	Input Impedance Tolerance			±30		%
C_{LIN}	Input Capacitance			5		pF
A_{LIN}	Programmable Gain		-46.5		+0	dB
	Gain Steps	Discrete logarithmic gain steps		0.75		dB
	Gain Step Accuracy			0.5		dB
$A_{LINMUTE}$	Mute Attenuation			100		dB

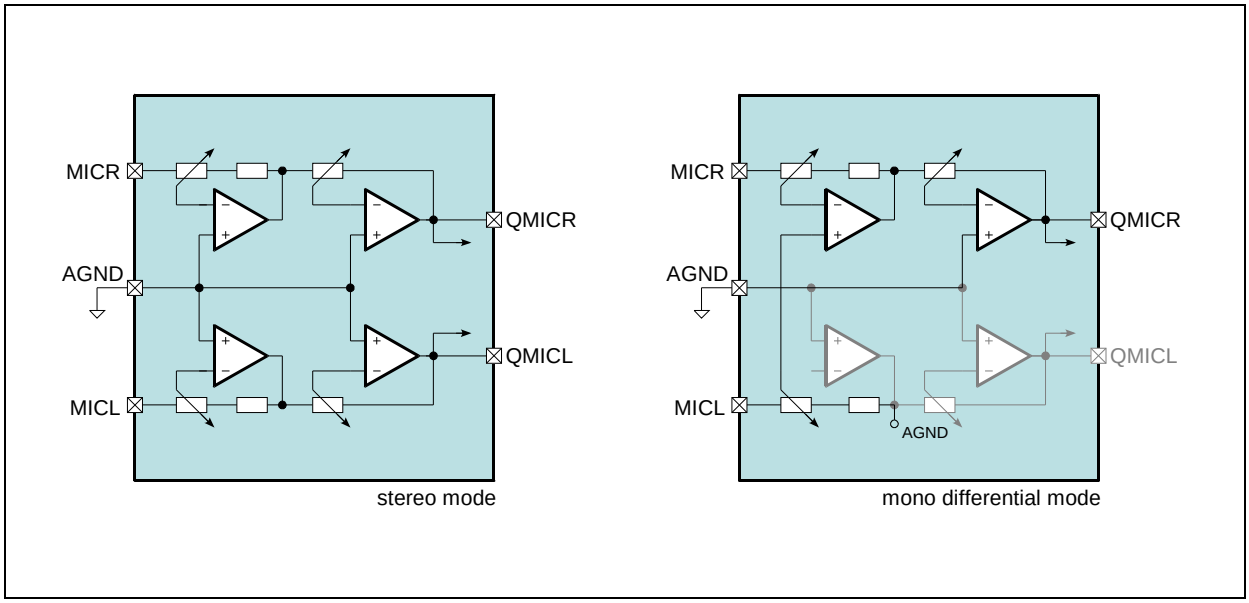
Table 4. Line Input Parameter (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Δ_{ALIN}	Gain Ramp Rate	Button Mode, Tinit=400ms		80		ms/step
		Monitor Mode		8		
V_{ATTACK}	Limiter Activation Level	HPL/R start of neg. clipping				V_{PEAK}
V_{DECAY}	Limiter Release Level	HPL/R		VNEG +0.3		V_{PEAK}
t_{ATTACK}	Limiter Attack Time			4		µs
t_{DECAY}	Limiter Decay Time			8		ms

9.2 Microphone Input

The AFE offers two microphone inputs and one low noise microphone voltage supply (microphone bias). The inputs can be switched to single ended or differential mode.

Figure 18. Microphone Input



9.2.1 Gain Stage & Limiter

The Mic Gain Stage has programmable Gain within -11.25dB…+36dB in 128 steps of 0.375dB.

As soft-start function is implemented for an automatic gain ramping implemented with steps of 4ms to fade in the audio at the end of the start-up sequence.

A limiter automatically attenuates high input signals. The AGC has 127 steps with 0.375dB with a dynamic range of the full gain stage. In some design it is necessary to switch of the AGC functionality. This can be done in register 0x17 by setting bit '1'.

In monitor mode, the gain stage can be set to an fixed (normally higher) gain level or be controlled by the VOL pin.

9.2.2 Microphone Supply

The MICS charge pump is providing a proper microphone supply voltage for low supply voltage supply. The integrated microphone supply supports basically 3 different modes.

The first mode, also called SWITCH-MODE, for 1.8V supply is to have a direct connection with an integrated switch from VBAT to MICS. The microphone supply pin of AS3421/22 is in this mode directly connected to V_{BAT}. For some applications a 1.8V microphone supply is high enough to operate a microphone properly. This mode is more commonly used in devices with a fixed power supply like in Bluetooth headsets. The internal microphone charge pump is switched off in this mode. This can help also reducing the external filter capacitors for the microphone supply. Please mind that the sensitivity of your microphone can be reduced in this mode.

The second mode, with the name CHAREGPUMP_MODE, is the most commonly used mode which is per default enabled. In this mode the internal charge pump is enabled. The charge pump doubles the supply voltage of AS3421/22 with a high output impedance of the charge pump in order to make external passive filters more effective. If doubling the supply voltage is not enough the microphone supply can be switched to a special regulated mode which increases the output voltage but with a little bit higher output noise. This setting can be found in register 0x35.

The third mode is the OFF MODE. This mode allows the user to switch of the microphone supply if not needed (e.g. playback without ANC)

9.2.3 Parameter

VBAT=1.5V, T_A= 25ºC unless otherwise specified.

Table 5. Microphone Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{MICIN}0$	Input Signal Level	A_{MIC} = 24dB		40		mV_P
$V_{MICIN}1$		A_{MIC} = 30dB		20		mV_P
$V_{MICIN}2$		A_{MIC} = 36dB		10		mV_P
R_{MICIN}	Input Impedance	MICP to AGND		7.5		kΩ
Δ_{MICIN}	Input Impedance Tolerance			-7 +33		%
C_{MICIN}	Input Capacitance			5		pF
A_{MIC}	Programmable Gain		-11.25		+36	dB
	Gain Steps	Discrete logarithmic gain steps		0.375		dB
	Gain Step Precision			0.15		dB
Δ_{AMIC}	Gain Ramp Rate	Tinit=64ms		4		ms/step
V_{ATTACK}	Limiter Activation Level	V_{PEAK} related to VBAT or VNEG		0.67		1
V_{DECAY}	Limiter Release Level			0.4		1
$A_{MICLIMIT}$	Limiter Gain Overdrive	127 @ 0.375dB		36		dB
t_{ATTACK}	Limiter Attack Time			5		µs/step
$t_{DECAY-DEB}$	Limiter Decay Debouncing Time			64		ms
t_{DECAY}	Limiter Decay Time			4		ms/step
V_{MICS}	Microphone Output Voltage	no output load		2.7		V
I_{MICS}	Microphone Supply Current	no output load		30		µA
R_{OUT_CP}	CP Output Resistance	400µA load		900		Ω
I_{MIC_MIN}	Microphone Output Current	Recommended minimum microphone output current @ Vbat = 1.5V		170		µA
		Recommended minimum microphone output current @ Vbat = 1.8V		300		µA
I_{MIC_MAX}	Microphone Output Current	Recommended maximum microphone output current @Vbat = 1.5V		500		µA
		Recommended maximum microphone output current @Vbat = 1.8V		700		µA

9.3 Headphone Output

The headphone output is a true ground output using VNEG as negative supply, designed to provide the audio signal with 2x12mW @ 16Ω-64Ω, which are typical values for headphones. It is also capable to operate in bridged mode for higher impedance (e.g. 300Ω) headphone. In this mode the left output is carrying the inverted signal of the right output shown in Figure 20.

Figure 19. Headphone Output Single Ended Mode

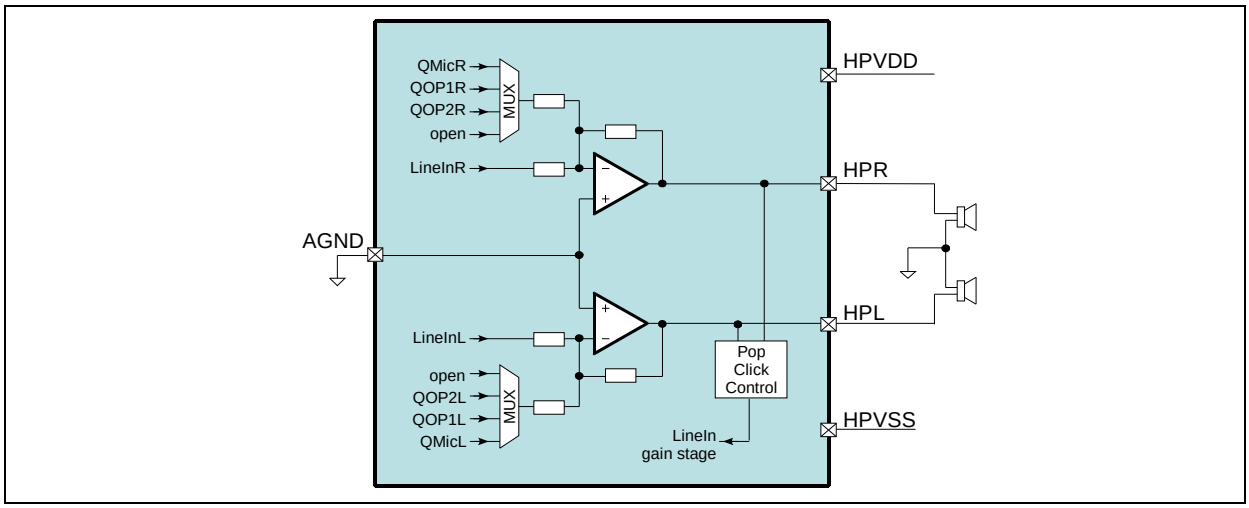
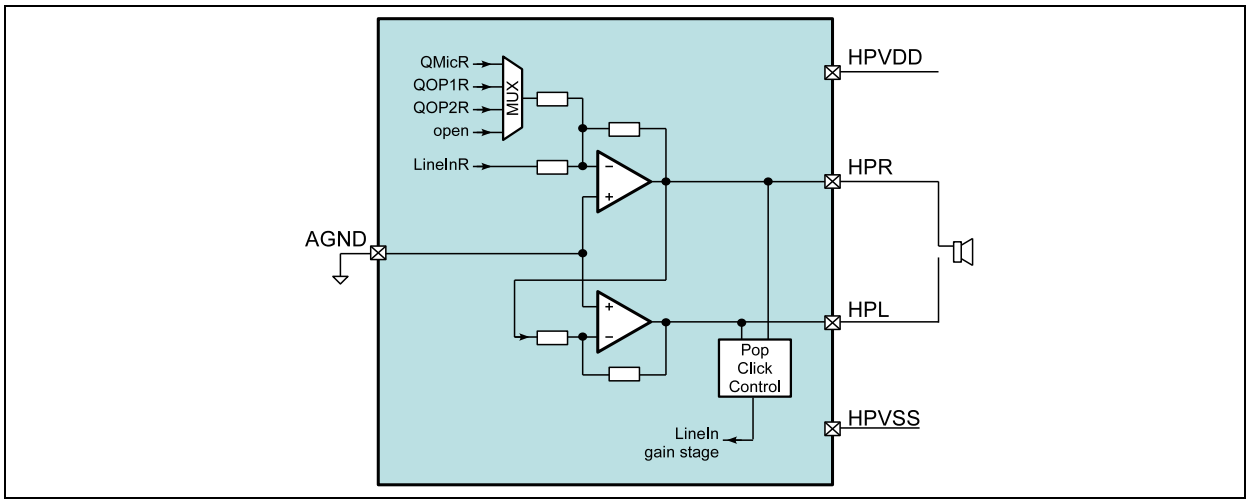


Figure 20. Headphone Output Differential Mode



9.3.1 Input Multiplexer

The signal from the line-input gain stage gets summed at the input of the headphone stage with the microphone gain stage output, the first filter opamp output or the second filter opamp output. The microphone gain stage output is used per default. It is also possible to playback without ANC by only using the line-input gain stage with no other signal on the multiplexer.

For the monitor mode, the setting of this input multiplexer can be changed to another source, normally to the microphone.

9.3.2 No-Pop Function

The No-Pop startup of the headphone stage takes 60ms to 120ms dependent on the supply voltage.

9.3.3 No-Clip Function

The headphone output stage gets monitored by comparator stages which detect if the output signal starts to clip.

This signal is used to reduce the LineIn gain to avoid distortion of the output signal. A hystereses avoids jumping between 2 gain steps for a signal with constant amplitude.

9.3.4 Over-Current Protection

The over-current protection has a threshold of 150-200mA and a debouncing time of 8µs. The stage is forced to OFF mode in an over-current situation. After this, the headphone stage tries to power up again every 8ms as long as the over-current situation still exists or the stage is turned off manually.

9.3.5 Parameter

VBAT=1.5V, T_A= 25ºC, unless otherwise specified.

Table 6. Headphone Output Parameter

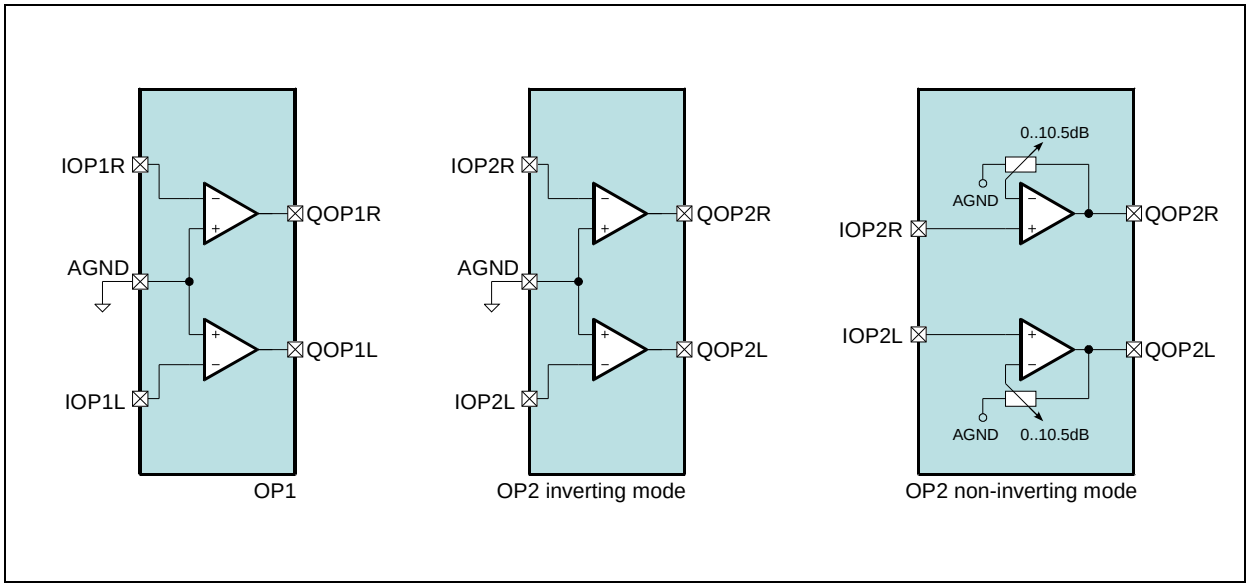
Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{L_HP}	Load Impedance	Stereo mode	16			Ω
C_{L_HP}	Load Capacitance	Stereo mode			100	pF
P_{HP}	Nominal Output Power	RL=64Ω	12			mW
		RL=32Ω	24			mW
		RL=16Ω	34			mW
P_{SRRHP}	Power Supply Rejection Ratio	200Hz-20kHz, 720mVpp, RL=16Ω		90		dB

9.4 Operational Amplifier

While AS3421 offers only one operational amplifier for feed-forward ANC, AS3422 features an additional operational amplifier stage to support feed-back ANC or any other additional needed filtering.

Both operational amplifiers stages can be activated and used individually. While OP1 stage is always configured as inverting amplifier, OP2 stage can be also switched to a non-inverting mode with an adjustable gain of 0...+10.5dB.

Figure 21. Operational Amplifiers



9.4.1 Parameter

VBAT=1.5V, T_A= 25ºC, unless otherwise specified.

Table 7. Headphone Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{L_OP}	Load Impedance	Single ended	1			kΩ
C_{L_OP}	Load Capacitance	Single ended			100	pF
GBW_{OP}	Gain Band Width			4.3		MHz
V_{OS_OP}	Offset Voltage				6	mV
V_{EIN_HP}	Equivalent Input Noise	200Hz-20kHz		2.6		µV

9.5 SYSTEM

The system block handles the power up and power down sequencing, as well as, the mode switching.

9.5.1 Power Up/Down Conditions

The chip powers up when one of the following conditions is true:

Table 8. Power UP Conditions

#	Source	Description
1	MODE_CSCL pin	In stand-alone mode, MODE pin has to be driven high to turn on the device
2	I2C start	In I2C mode, a I2C start condition turns on the device

The chip automatically shuts off if one of the following conditions arises:

Table 9. Power DOWN Conditions

#	Source	Description
1	MODE pin	Power down by driving MODE_CSCL pin to low
2	SERIF	Power down by SERIF writing 0h to register 20h bit <0>
3	Low Battery	Power down if VBAT is lower than the supervisor off-threshold
4	VNEG CP OVC	Power down if VNEG is higher than the VNEG off-threshold

9.5.2 Start-up Sequence

The start-up sequence depends on the used mode.

In stand-alone mode the sequence runs automatically, in I2C mode(I2C MODE bit has to be pre-trimmed) the sequence runs till a defined state and waits then for an I2C command. Either the automatic sequence is started by setting the CONT_PWRUP bit in addition to the PWR_HOLD bit. If only the PWR_HOLD is set all enable bits for headphone, microphone, etc have to be set manually.

Figure 22. Stand-Alone Mode Start-Up Sequence

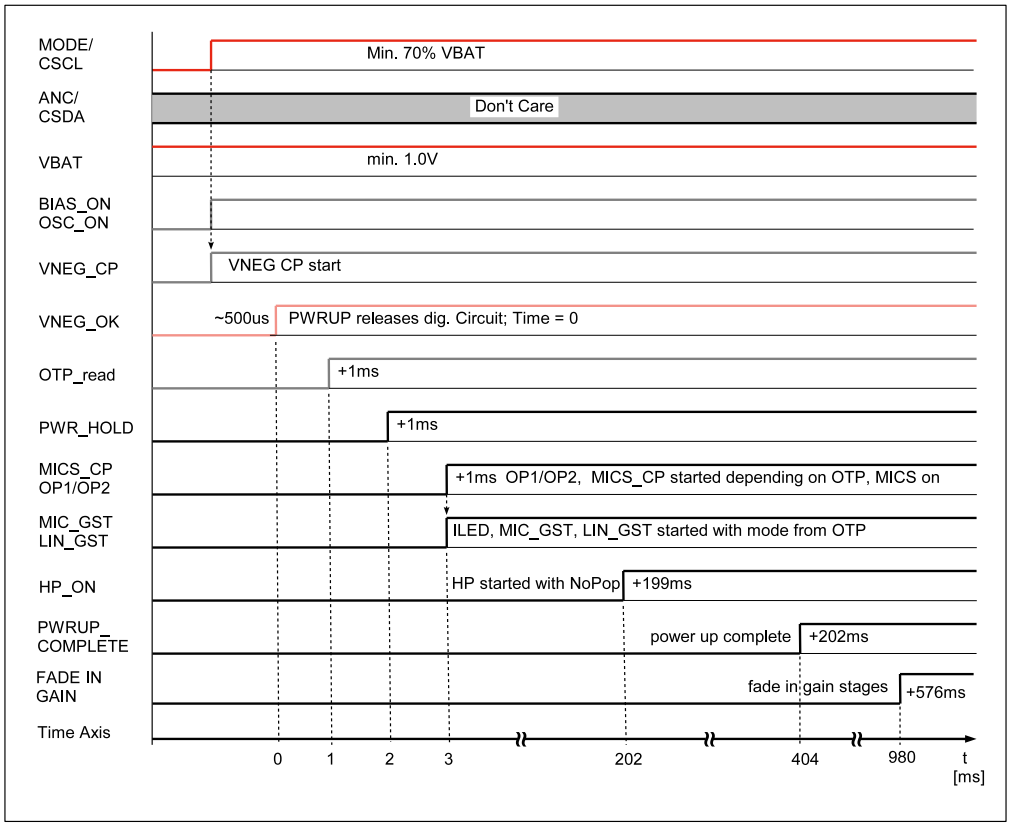
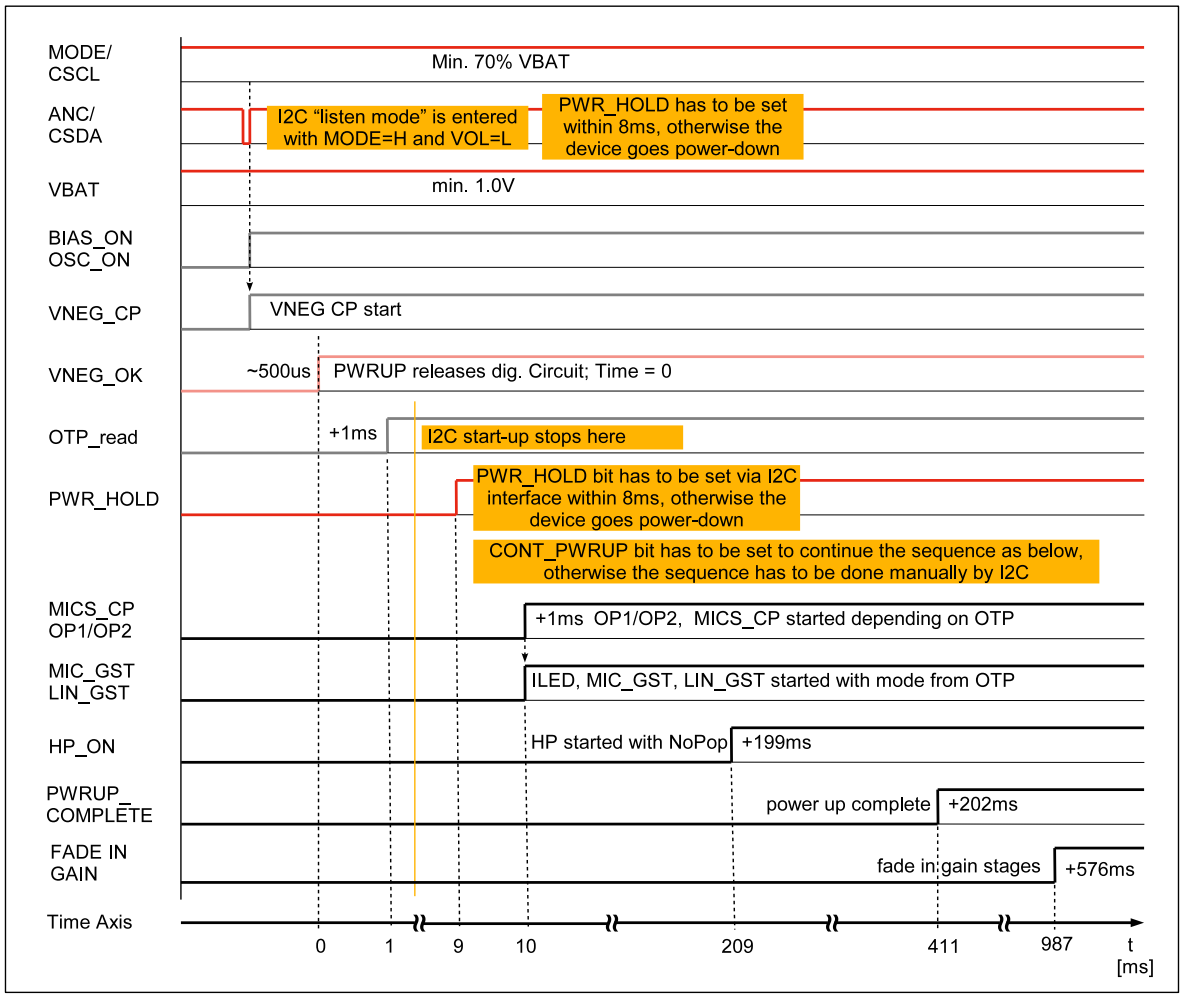


Figure 23. I2C Mode Start-Up Sequence



The total start-up time (including fade-in of the gain stages) can be reduced to 600ms by OTP setting.

9.5.3 MODE_CSCL Switching

When the chip is in stand-alone mode (no I2C control), the mode can be switched with different levels on the MODE pin.

Table 10. MODE_CSCL Operation Modes

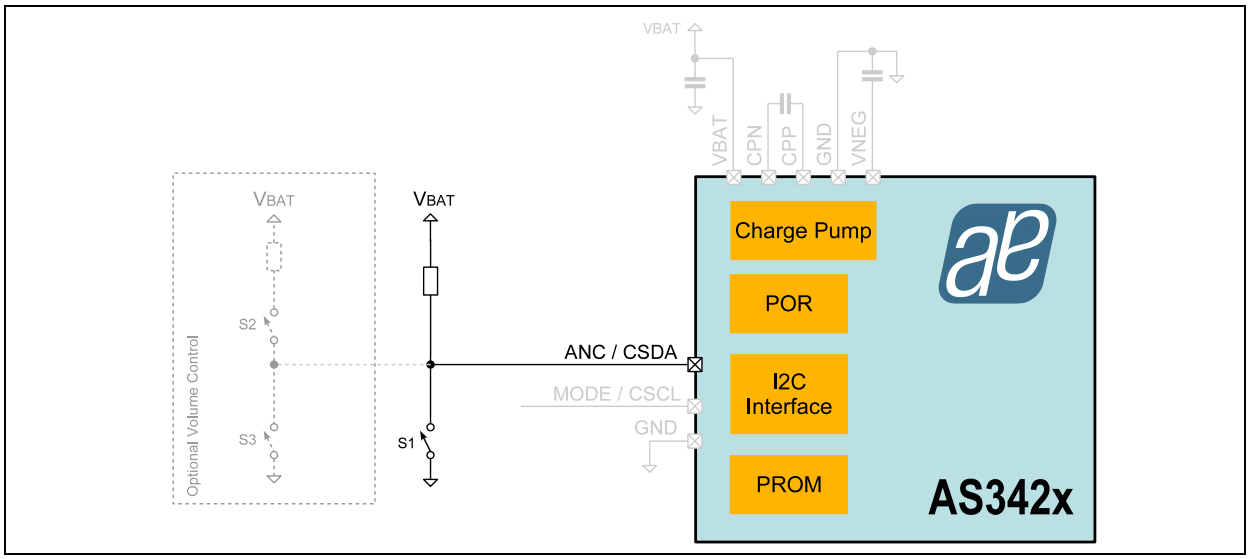
MODE	MODE_CSCL pin	Description
OFF	LOW (VSS)	Chip is turned off
ANC	HIGH (VBAT)	Chip is turned on and active noise cancellation is active
MONITOR	VBAT/2	Chip is turned on and monitor mode is active In Monitor mode, a different (normally higher) microphone preamplifier gain can be chosen to get an amplification of the surrounding noise. This volume can be either fixed or be controlled by the VOL input. To get rid of the low pass filtering needed for the noise cancellation, the headphone input multiplexer can be set to a different (normally to MIC) source. In addition, the LineIn gain can be lowered to reduce the loudness of the music currently played back.

In I2C mode, the monitor mode can be activated be setting the corresponding bit in the system register.

9.5.4 ANC_CSDA Switching

For Bluetooth applications it is sometimes a requirement to switch off the ANC function while listening to music or having a phone call. Because the fully differential audio outputs of the Bluetooth chip are directly connected to the line input of the AS3421/22 it is not possible to simply switch off the ANC chip to do music playback without ANC.In order to avoid an expensive bypass path with mechanical or electrical switches the AS3421/22 features a special low power audio playback mode. In this mode the device enters a low power mode where the ANC function is disabled and the blocks which are not necessary in this mode are automatically switched off to safe system power. This audio playback mode can be entered by simply pulling the ANC_SCDA pin to low.

Figure 24. ANC / CSDA Switching



An example how to implement this feature is shown in Figure 24. In default operation (ANC enabled) the ANC_CSDA pin is pulled high. If the device should enter the low power playback mode the pin is pulled low with the switch S1. Once the pin is pulled low the device enters after 200ms the playback mode. As long as the pin is low the device stays in the playback only mode. If the feature is for some reason not required it can also be disabled by setting the bit NO_PB_MODE_OTP in register 0x33. Once this bit is set to '1' the status of pin ANC_CSDA has no influence on the device any more.

Besides the low power playback mode the ANC_CSDA pin supports also volume control via push buttons. In order to enable this feature the corresponding bit VOL_BUTTON_MODE_OTP is register 0x33 has to be set to '1'. Once this bit is set, the device can not support the low power playback mode via ANC_CSDA pin any more. An example on how to connect the push buttons for volume control is shown in Figure 24 with the push buttons S2 and S3.

Table 11. ANC_CSDA Operation Modes

NO_PB_MODE_OTP Bit	VOL_BUTTON_MODE_OTP Bit	ANC_CSDA Pin	Description
0	0	high	Normal ANC operation
0	0	high -> low	Device enters low power playback mode
0	0	low -> high	Device returns to normal ANC operation
1	0	X	Normal ANC operation. No influence on operation via ANC_CSDA pin.
X	1	high	Volume Control Mode via Button - Volume up
X	1	High Imp.	Volume Control Mode via Button - No Volume change
X	1	low	Volume Control Mode via Button - Volume down

9.6 VNEG Charge Pump

The VNEG charge pump uses one external 1uF capacitor to generate a negative supply voltage out of the battery input voltage to supply all audio related blocks. This allows a true-ground headphone output with no more need of external dc-decoupling capacitors.

9.6.1 Parameter

VBAT=1.5V, T_A= 25ºC, unless otherwise specified.

Table 12. Headphone Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input voltage	VBAT	1.0	1.5	1.8	V
V_{OUT}	Output voltage	VNEG	-0.7	-1.5	-1.8	V
C_{EXT}	External flying capacitor			1		µF

9.7 OTP Memory & Internal Registers

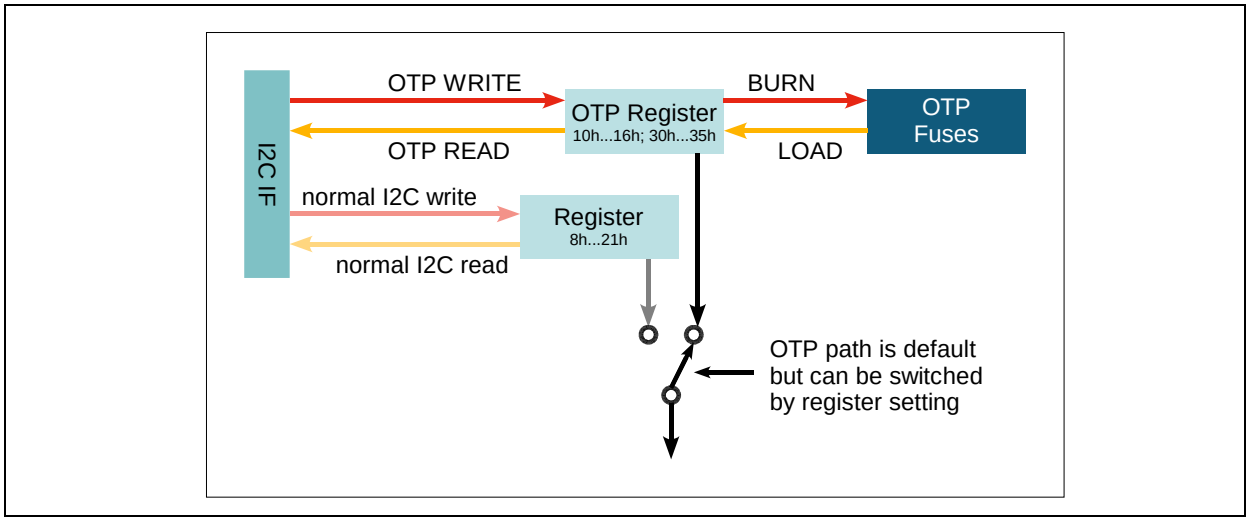
The OTP memory consists of OTP register and the OTP fuses.The OTP register can be written as often as wanted but will lose the content on power off. The OTP fuses are intended to store basic chip configurations as well as the microphone gain settings to optimize the ANC performance and get rid of sensitivity variations of different microphones. Burning the fuses can only be done once and is a permanent change, which means the fuses keep the content even if the chip is powered down. This AS3421/22 offers 4 register set for storing the microphone gain making it possible to change the gain 3 times for re-calibration or other purposes.

When the chip is controlled by a microcontroller via I2C, the OTP memory don't has to be used. The chip configuration can be stored in the flash memory of the Bluetooth- or wireless chipset.

9.7.1 Register & OTP Memory Configuration

Figure 25 is showing the principal register interaction.

Figure 25. Register Access



Registers 0x8, 0x9, 0xA, 0xB, 0xC and 0x21 have only effect when the corresponding "REG_ON" bit is set, otherwise the chip operates with the OTP Register settings which are loaded from the OTP fuses at every start-up.

All registers settings can be changed several times, but will loose the content on power off. When using the I2C mode, the chip configuration has to be loaded from the micro controller after every start-up. In stand alone mode the OTP fuses have to be programmed for a permanent change of the chip configuration.

A single OTP cell can be programmed only once. Per default, the cell is "0"; a programmed cell will contain a "1". While it is not possible to reset a programmed bit from "1" to "0", multiple OTP writes are possible, but only additional unprogrammed "0"-bits can be programmed to "1".

Independent of the OTP programming, it is possible to overwrite the OTP register temporarily with an OTP write command at any time. This setting will be cleared and overwritten with the hard programmed OTP settings at each power-up sequence or by a LOAD operation.

The OTP memory can be accessed in the following ways:

LOAD Operation. The LOAD operation reads the OTP fuses and loads the contents into the OTP register. A LOAD operation is automatically executed after each power-on-reset.

WRITE Operation. The WRITE operation allows a temporary modification of the OTP register. It does not program the OTP. This operation can be invoked multiple times and will remain set while the chip is supplied with power and while the OTP register is not modified with another WRITE or LOAD operation.

READ Operation. The READ operation reads the contents of the OTP register, for example to verify a WRITE command or to read the OTP memory after a LOAD command.

BURN Operation. The BURN operation programs the contents of the OTP register permanently into the OTP fuses. Don't use old or nearly empty batteries for burning the fuses.

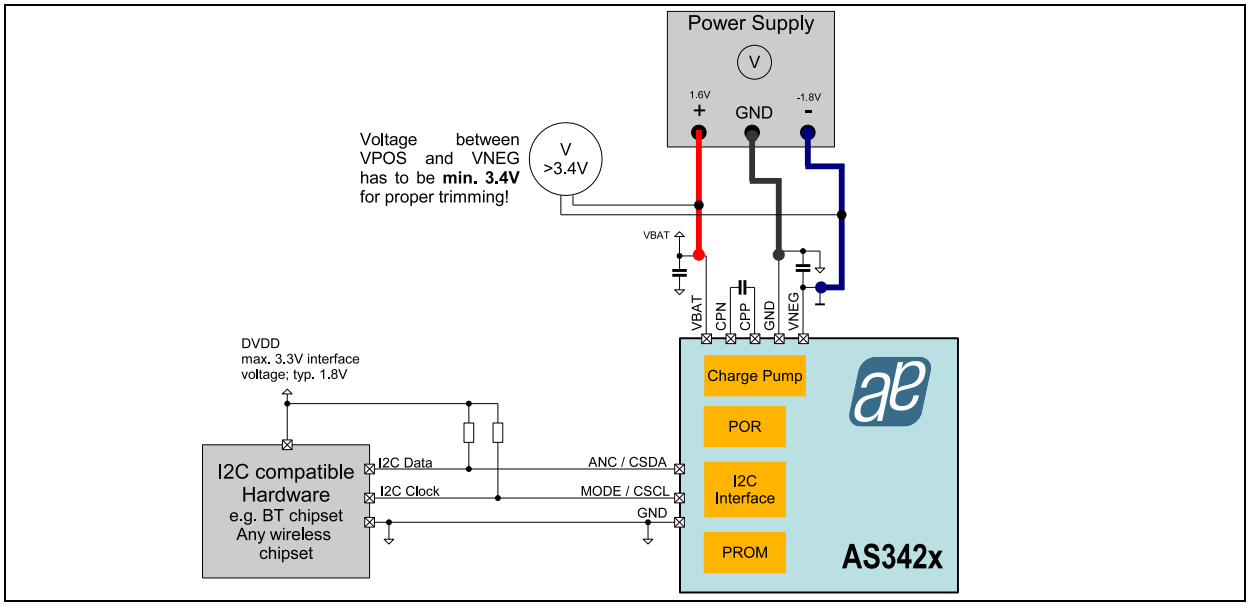
Attention: If you once burn the OTP_LOCK bit, no further programming, e.g. setting additional "0" to "1", of the OTP can be done.

For production, the OTP_LOCK bit must be set to avoid an unwanted change of the OTP content during the lifetime of the product.

9.7.2 OTP Fuse Burning

As many wireless applications like Bluetooth single chip solutions support programmable solutions as well as ROM versions it is in ROM versions necessary to store microphone gain compensation data and the general ANC configuration inside the ANC chip because there is not other way to configure the ANC chip during startup. In order to guaranty successful trimming of AS3421/22 it is necessary to provide a decent environment for the trimming process. In Figure 26 a principal block diagram is shown for trimming the AS3421/22 properly in production.

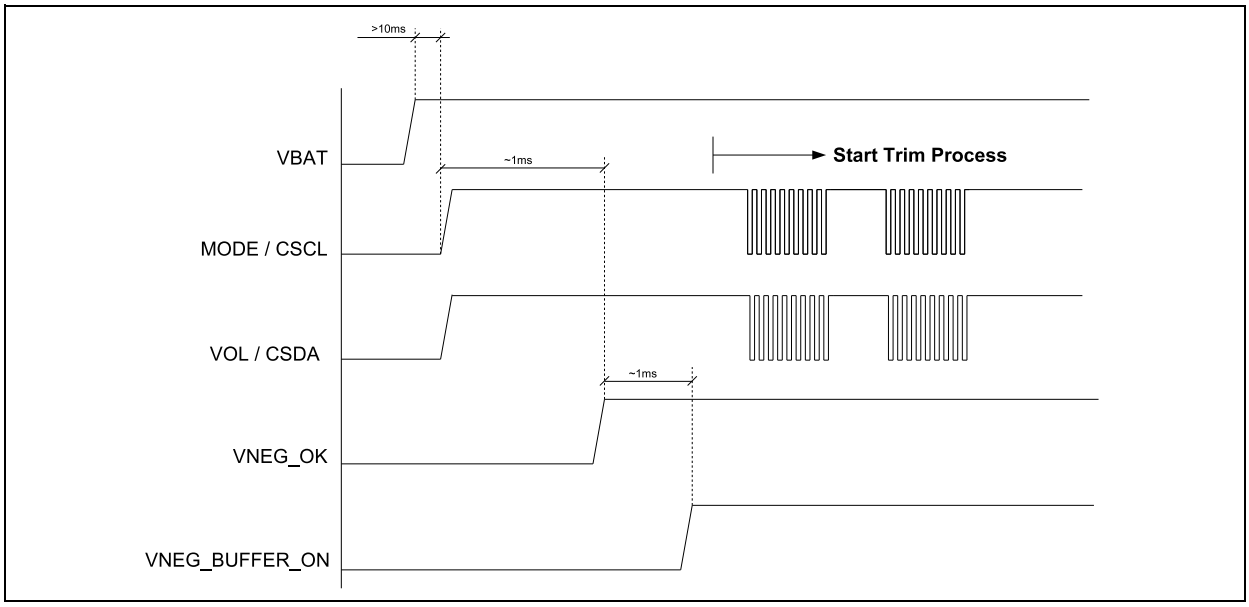
Figure 26. Block Diagram for Production Environment



The most important block is the external power supply. Usually it is possible to trim the AS3421/22 with a single supply voltage of min. 1.7V in laboratory environment but as soon as it comes to mass production we highly recommend buffering also VNEG supply of the chip. As highlighted in the block diagram it is mandatory to get a voltage difference between VPOS and VNEG of min. 3.4V to guaranty proper trimming of the device. no current sink capability, therefore it is possible to buffer it external with a negative power supply. The VNEG voltage applied to VNEG pin must be lower than the voltage created with the charge pump. This means if the typical VNEG output voltage is -1.5V you can easily apply externally -1.7V. The charge pump switches then automatically into skip mode.

Important for applying an external buffer and switching on the ANC device is the timing in order to avoid latch up on the ANC device. The timing diagram in Figure 2 shows clearly that it is important that there is a certain delay between VBAT and the MODE /CSCL pin necessary. This delay is mandatory in order to guaranty that the device starts up properly. In case AS350x is used the delay between VBAT and MODE/CSCL is not necessary. The MODE /CSCL pin powers the ANC device up and the whole sequence to power up the internal charge pump of AS34x0 and AS350x takes approximately 1ms. Once VNEG is settled the external VNEG buffer (e.g. power supply) can be enabled in order to support the charge pump especially during the trim process which can now be started.

Figure 27. Timing Diagram for VNEG Buffering

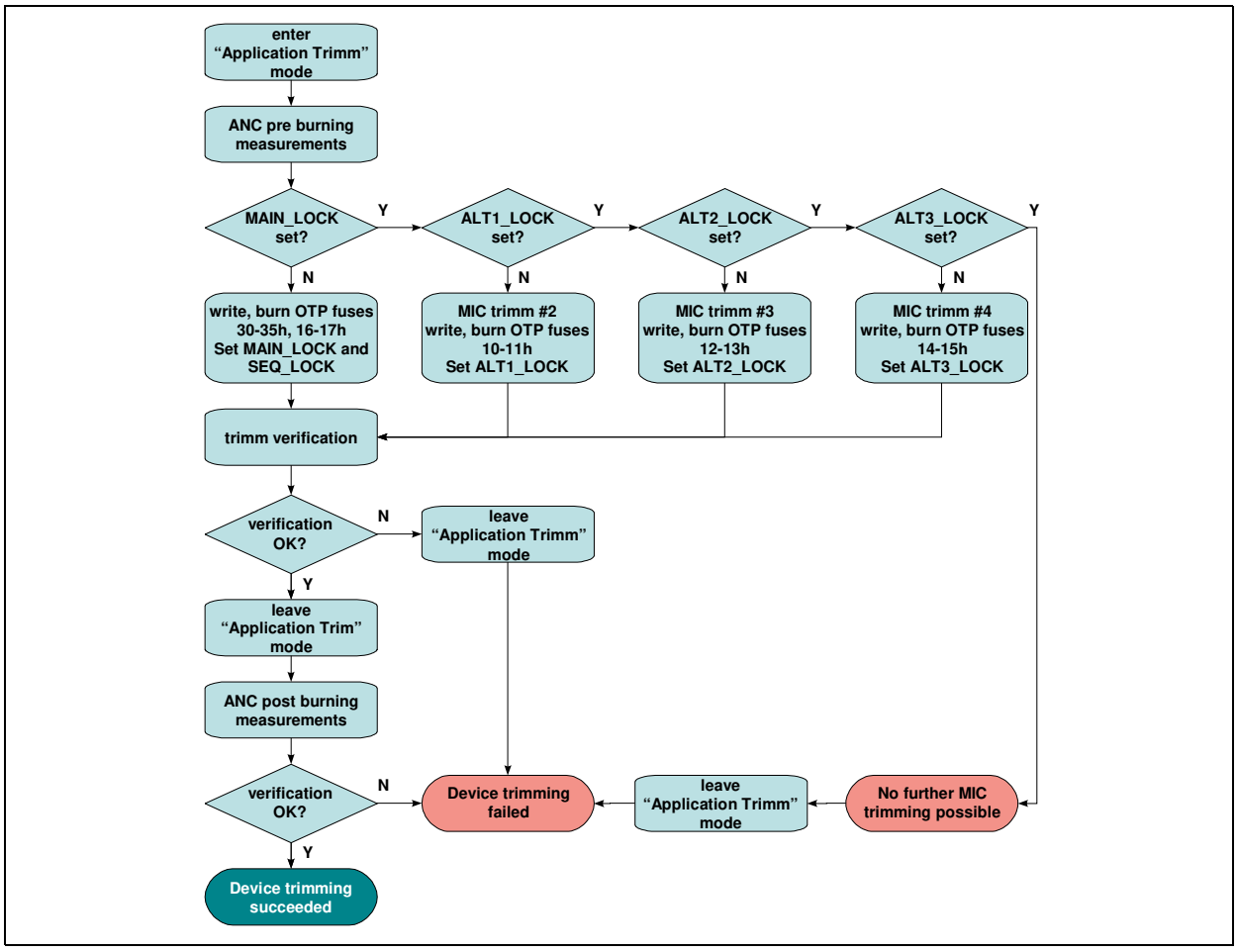


To guaranty a successful trimming process it is important to follow exactly the predefined trimming sequence shown inFigure 28. As a first step it is important to do a register dump of all OTP registers. This register backup in your system memory is a backup of all register setting and is necessary for the verification after the trim process to make sure that all bits are trimmed correctly. Once the register dump has been done it is important to check the OTP_LOCK in register 0x35. This register indicates if the device is already trimmed or not. In case this bit is set to '1' there is no more trimming possible. The device has obviously already been trimmed before. In case the bit is '0' there is initial or further trimming of the device possible. You enter the trim mode and start the trimming process. Once the trimming is done the most important step is comparing the values trimmed to the device with the original register dump we did right before we started with the actual trimming process. If the verification was successful we know that all bits have been trimmed correctly to AS3501/AS3502. What is important to mention is that the AS3502 and AS3501 have a couple of test bits inside which are per default set to '1'. We do not recommend overwriting these bytes.

Furthermore it is important to know that it is not possible to change bits once they are trimmed. With AS3501 and AS3502 it is possible to trim the device again if the MAIN_LOCK bit is not set to '1'. What is not possible is, is changing a bit from '1' back to zero. If an additional trimming is done it is only possible to change bits from '0' to '1'. An example would be the following. A register contains a value of 0x41. If the MAIN_LOCK bit is not set to '1' you can basically re-trim the part but it doesn't work to change the value from 0x41 to 0x40. What is possible would be a change from 0x41 to 0x43. It is important that all necessary bits are trimmed exactly like in the block diagram shown in Figure 28. The internal state machine needs the MAIN_LOCK bit as well as the ALTx_LOCK bits to determine the right microphone register at start-up of the device. If the MAIN_LOCK bit and the ALTx_LOCK bits are not set correctly the result can be malfunction of the device.

for detailed implementation of the I2C trimming there is also an application note available which describes the whole process in more detail and includes also some code examples.

Figure 28. OTP Burning Process



9.8 2-Wire-Serial Control Interface

There is an I2C slave block implemented to have access to 64 byte of setting information.

The I2C address is: Adr_Group8 - audio processors

- 8Eh_write
- 8Fh_read

9.8.1 Protocol

Table 13. 2-Wire Serial Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 1110b (8Eh)
DR	Device address for read	R	1000 1111b (8Fh)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit

Table 13. 2-Wire Serial Symbol Definition

Symbol	Definition	RW	Note
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	during acknowledge
	AS3421 AS3422 (=slave) receives data		
	AS3421 AS3422 (=slave) transmits data		

Figure 29. Byte Write

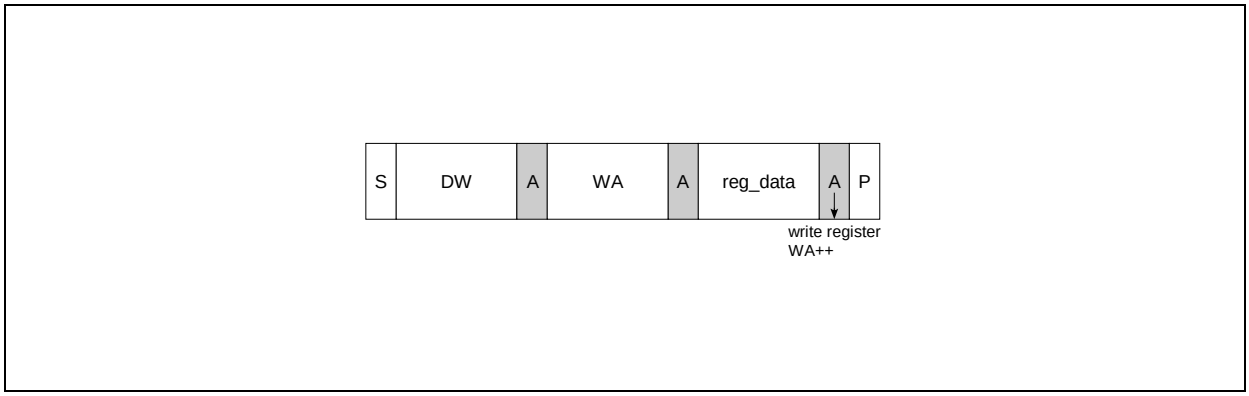
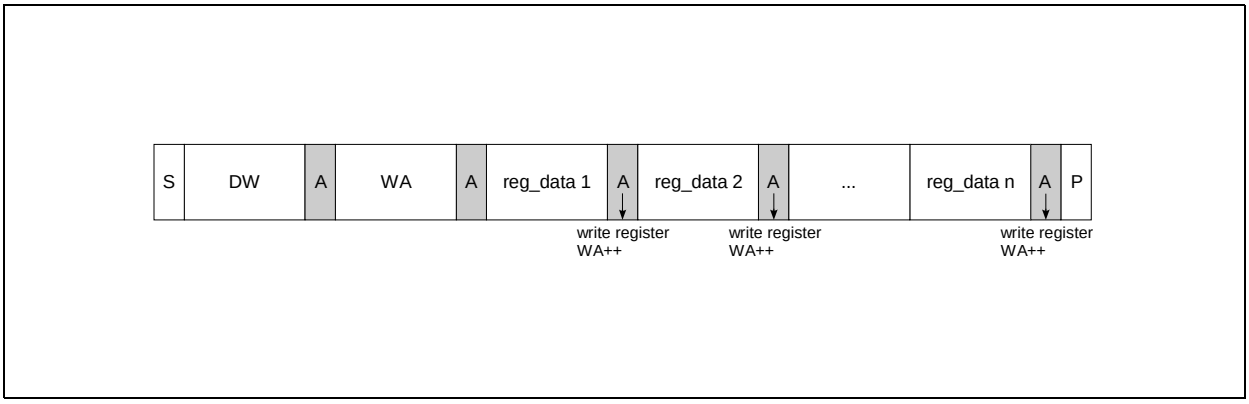


Figure 30. Page Write



Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.