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AS3514

Stereo Audio Codec with System Power Management

1 General Description

The AS3514 is a low power stereo audio codec and is designed for Portable Digital Audio Applications. It allows playback in CD quality and recording in FM-stereo quality. It has a variety of audio inputs and outputs to directly connect electret microphones, 16Ω headset, 4Ω speaker and auxiliary signal sources via a 10-channel mixer. It only consumes 22mW in playback mode.

Further the device offers advanced power management functions. All necessary ICs and peripherals in a flash based Digital Audio Player are supplied by the AS3514. The power management block generates 9 different supply voltages out of the battery supply. CPU, NAND flash, SRAM, memory cards, LCD back-light, USB RX/TX can be powered. The different supply voltages are programmable via the serial control interface. It also contains a charger and is designed for battery supplies from 1V to 5V.

The AS3514 has an on-chip, phase locked loop (PLL) controlled, clock generator. It generates 44.1kHz, 48kHz and other sample rates defined in MP3, AAC, WMA, OGG VORBIS etc. No additional external crystal or PLL is needed. Further the AS3514 has an independent 32kHz real time clock (RTC) on chip which allows a complete power down of the system CPU.

2 Key Features

Multi-bit Sigma Delta Converters
– DAC: 18bit with 94dB SNR ('A' weighted) , 48kHz
– ADC: 14bit with 82dB SNR ('A' weighted), 16kHz

2 Microphone Inputs
– 3 gain pre-setting (28dB/34dB/40dB) with AGC
– 32 gain steps @1.5dB and MUTE
– supply for electret microphone
– microphone detection
– remote control by switch

2 Line Inputs
– volume control via serial interface
– 32 steps @1.5dB and MUTE
– stereo or 2x mono or mono differential

Line Outputs
– volume control via serial interface
– 32 steps @1.5dB and MUTE
– 1Vp @10kΩ

Audio Mixer
– 10 channel input/output mixer with AGC
– mixes line inputs and microphones with DAC
– left and right channels independent

High Efficiency Headphone Amplifier
– volume control via serial interface
– 32 steps @1.5dB and MUTE
– 2x40mW @16Ω driver capability
– headphone and over-current detection
– phantom ground eliminates large capacitors

High Power Speaker Amplifier
– volume control via serial interface
– 32 steps @1.5dB and MUTE
– 2x500mW @8Ω driver capability
– over-current detection

Power Management
– step up for system supply (3.0V – 3.6V)
– step down for CPU core (0.85V – 1.8V, 200mA)
– step up for backlight (15V, 38.5mA)
– LDO for digital supply (2.9V, 200mA)
– LDO for analogue supply (2.9V, 200mA)
– LDO for peripherals (1.7V-3.3V, 200mA)
– LDO for peripherals (3.1V-3.3V, 200mA)
– LDO for RTC (1.0V-2.5V, 2mA)
– LDO for USB 1.1 transceiver (3.26V, 10mA)
– battery supervision
– 10sec emergency shut-down

Battery Charger
– automatic trickle charge (50mA)
– prog. constant current charging (100-400mA)
– prog. constant voltage charging (3.9V-4.25V)

Real Time Clock
– ultra low power 32kHz oscillator
– 32bit RTC sec counter
– selectable alarm (seconds or minutes)

General Purpose ADC
– 10bit resolution
– 16 inputs analogue multiplexer

Interfaces
– I²S digital audio interface
– 2 wire serial control interface
– watchdog via serial interface
– power good pin
– 128bit unique ID (OTP)
– 17 different interrupts

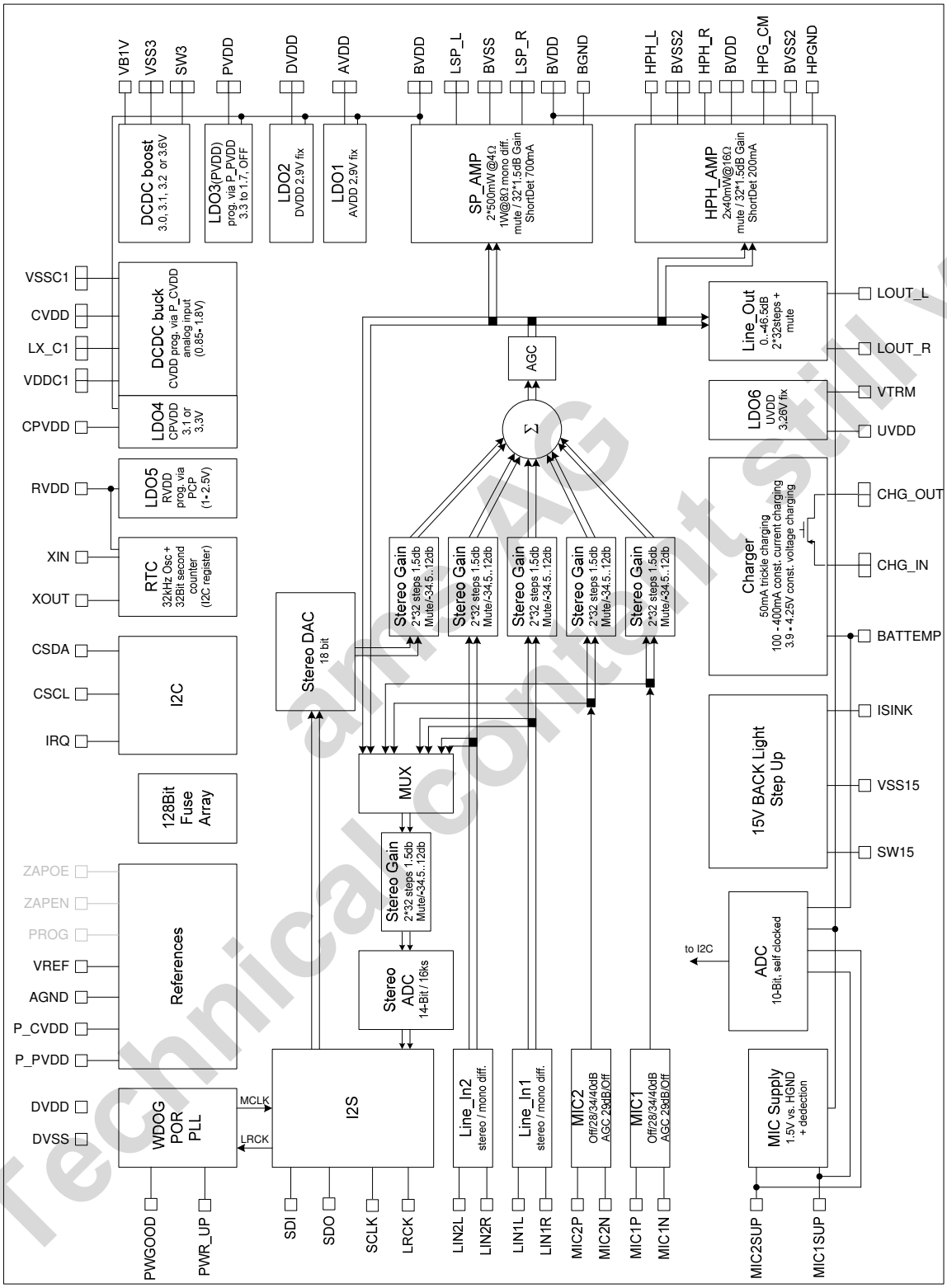
Package CTBGA64 [7.0x7.0x1.1mm] 0.8mm pitch

3 Application

Portable Digital Audio Player and Recorder
PDA, Smartphone

4 Block Diagram

Figure 1 AS3514 Block Diagram



Contents

Revision History

Revision	Date	Owner	Description
0.1	17.1.2005	pkm	first public release
0.2	15.4.2005	pkm	new LQFP pinning (chapter 8.2.2)
0.2	18.4.2005	pkm	added P_CVDD description as pin is missing now in the LQFP package (chapter 8.1)
0.2	19.4.2005	pkm	new PLL description, audio in/out chapters combined (chapter 6.6)
0.2	20.4.2005	pkm	new ordering information (chapter 9)
0.2	22.4.2005	pkm	added additional audio and performance parameter (chapter 6, 7)
0.2	3.5.2005	pkm	new DCDC buck description (chapter 0, 6.12)
0.21	5.5.2005	pkm	updated audio and performance parameter (chapter 6, 7)
0.21	5.5.2005	pkm	added AGC information for audio mixer (chapter 6.7)
0.21	5.5.2005	pkm	updated power up timing (chapter 6.12)
0.21	5.5.2005	pkm	updated absolute maximum ratings and operating conditions (chapter 5)
0.3	19.5.2005	pkm	changed power up sequence for chip version V12 (chapter 6.12)
0.3	20.5.2005	pkm	updated audio performance parameter (chapter 7)
0.3	20.5.2005	pkm	updated 15 DCDC description (chapter 6.14)
0.31	9.6.2005	pkm	updated soldering conditions (chapter 5)
0.31	9.6.2005	pkm	added ESD note to pin description (chapter 8.1)
0.9	15.3.2006	pkm	bug fix in left line in register (chapter 6.5)
0.91	12.5.2006	pkm	updated PMU block diagrams (chapter 6.x) updated BGA ball list and assignment (chapter 8.x)
0.92	20.11.2006	pkm	updated absolute maximum ratings (chapter 5)

5 Absolute Maximum Ratings (Non-Operating)

Stresses beyond the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or beyond those listed is not implied.

Caution: Exposure to absolute maximum rating conditions may affect device reliability.

Table 1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{IN_VB1V}	single cell supply voltage	-0.5	5.0	V	Applicable for pin VB1V
V_{IN_5V}	5V pins	-0.5	7.0	V	Applicable for pins BVDD, CHGIN, VBUS, BVDDC1
V_{IN_SW15}	15V pin	-0.5	17	V	Applicable for pins SW15
V_{IN_VSS}	Voltage difference at VSS terminals	-0.5	0.5	V	Applicable for pins VSS3, VSS15, BVSS, BVSS2, AVSS, DVSS, VSSC1
V_{IN_DVDD}	3.3V pins with diode to DVDD	-0.5	5.0 DVDD+0.5	V	Applicable for pins MCLK, LRCK, SCLK, SDI, P_PVDD, P_CVDD, BATTEMP, ISINK, IRQ, PWGOOD
V_{IN_xDVDD}	pins with no diode to DVDD	-0.5	7.0V	V	Applicable for pins CSCL, CSDA, PWR_UP
V_{IN_AVDD}	3.3V pins with diode to AVDD	-0.5	5.0 AVDD+0.5	V	Applicable for pins BGND, HPH_CM, HPGND, LOUT_L/R, VREF, AGND, LIN1L/R, LIN2L/R, MIC1P/N, MIC2P/N, MIC1SUP, MIC2SUP
V_{IN_REG}	voltage regulator pins with diodes to BVDD	-0.5	5.0 BVDD+0.5	V	Applicable for pins AVDD, DVDD, PVDD, CPVDD, CVDD, UVDD
V_{IN_RTC}	voltage regulator pin with diode to BVDD	-0.5	3.6 BVDD+0.5	V	Applicable for pins RVDD, XIN, XOUT
V_{IN_BVDD}	pins with diode to BVDD	-0.5	7.0 BVDD+0.5	V	Applicable for pins LSP_R/L, HPH_R/L, CHGOUT, SW3
I_{scr}	Input Current (latchup immunity)	-100	100	mA	Norm: JEDEC JESD78 A
ESD	Electrostatic Discharge HBM		+/-1	kV	Norm: MIL 883 E method 3015
P_t	Total Power Dissipation (all supplies and outputs)		1000	mW	CTBGA64, T_{amb}=70°C
T_{strg}	Storage Temperature	-55	125	°C	
H	Humidity non-condensing	5	85	%	

Table 2 Soldering Conditions

Symbol	Parameter	Min	Max	Unit	Note
T_{body}	Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only
T_{peak}	Solder Profile*	235	245	°C	
D_{well}		30	45	s	above 217 °C

* austriamicrosystems AG strongly recommends to use underfill.

5.1 Operating Conditions

Table 3 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Battery Supply Voltage	BVDD	3.0	5.5	V	
DCDC 3V Supply Voltage	VB1V	1.0	4.5	V	
USB Supply Voltage	UVDD	-	5.5	V	
Digital Supply Voltage	DVDD	2.8	3.6	V	
Analoge Supply Voltage	AVDD	2.8	3.6	V	
Charger Supply Voltage	CHG_IN	4.5	5.5	V	
Difference of Positive Supplies	AVDD-DVDD	-0.25	0.25	V	
Difference of Negative Supplies DVSS, AVSS, VSS3, VSS15, VSSC1, BVSS	Any Combination	-0.1	0.1	V	To achieve good performance, the negative supply terminals should be connected to low ohmic ground plane.
Ambient Temperature	T_{amb}	-20	85	°C	
Supply Current	BVDD	6.8	20	mA	In Audio Loop Mode
System Clock Frequency	LRCLK	8	48	kHz	According to 8-48kSps Audio Data

6 Detailed Functional Block Description

6.1 Line Output

6.1.1 General

The line output is designed to provide the audio signal with typical 1Vp at a load of minimum 10kΩ, which is a minimum value for line inputs. Additional this output amplifier is capable to drive a 32Ω load (e.g. an earpiece of a mobile phone. To achieve this the operation mode can be switched from single ended stereo to mono differential.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB.

6.1.2 Register Description

Enabling the output stage is done via a control bit in the audio settings register (AudioSet1 register 0x14h). The line out driver itself is controlled by the following two registers.

Right Line Out Register (00h)

Table 4 LINE_OUT_R Register

Bit	Name	Description
7,6	reserved	For testing purpose only, must be set to 0h
5	-	not used
4..0	LOR_VOL	volume settings for right line output, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The register is R/W; default value is 00h

Left Line Out Register (01h)

Table 5 LINE_OUT_L Register

Bit	Name	Description
7,6	LO_SES_DM	Single ended stereo or differential mono selection 11: tbd. 10: output switched to single ended stereo 01: output switched to differential mono **00: output switched to mute**
5	-	not used
4..0	LOL_VOL	volume settings for left line output, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The register is R/W; default value is 00h

6.1.3 Parameter

Table 6 Line Output Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
R_L	Output Load	stereo mode	10k			Ohm
		differential mode	32			Ohm
A0	Gain	programmable gain	-40.5		6	dB
$\triangle$Ax	Gain Step-Size			1.5		dB
SNR	Signal to Noise Ratio	stereo mode		100		dB
	Mute Attenuation			100		dB

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

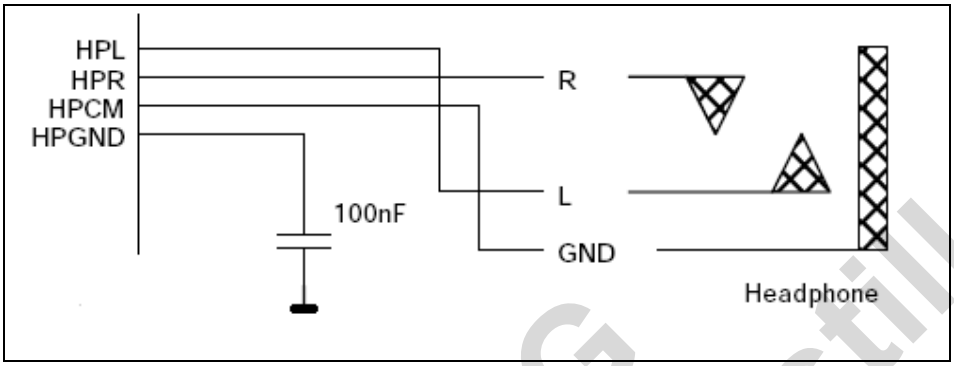
6.2 Headphone Output

6.2.1 General

The headphone output is designed to provide the audio signal with 2x40mW @ 16Ω or 2x20mW @32Ω, which are typical values for headphones.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –43.43dB to +1.07dB. The maximum output power of 40mW @ 16Ω is achieved, by setting the mixer output to 1Vp and using the gain of 1.07dB.

Figure 2 Headphone-Output



6.2.2 Phantom Ground

HPCM pin is the buffered HPGND output. It can be used to drive the loads without external blocking capacitors between HPL / HPR and HPCM. If the load is between HPR / HPL and BVSS, 100uF of de-coupling capacitors are needed. The phantom ground can be switched off to save power if not needed.

6.2.3 No-Pop Function

To avoiding click and pop noise during power-up and shutdown, the output is automatically set to mute when the output stage is disabled.

HPGND pin, which needs a 100nF capacitor outside, gets charged on power-up with 2uA to AGND=1.45V. After start-up the DC level of the following pins are the same: HPR=HPL=HPCM=HPGND=AGND=1.45V. The Start-up time before releasing mute is about 90ms. To avoid pop-noise 150ms discharging time of HPGND after a shutdown, have to be waited before starting up again.

6.2.4 Over-current Protection

This output stage has an over-current protection, which disables the output for 256ms or 512ms. This value can be set in the headphone registers. The over-current protection limit of HPR and HPL pin is typical 145mA while HPCM pin has a 210mA threshold. If needed, the over-current condition can also be signalled via an interrupt to the controlling microprocessor.

6.2.5 Headphone Detection

With a control bit the headphone detection can be enabled. The detection is only working as long as the headphone stage is in power down mode and the load is applied between HPR / HPL and HPCM. the headphone detection can also trigger a corresponding interrupt.

6.2.6 Power Save Options

To save power, especially when driving 32 Ohm loads, a reduction of the bias current can be selected. Together with switching off the phantom ground this gives 4 possible operating modes.

Table 7 Headphone Power-Save Options

HPCM_OFF	IBR_HPH	IDD_HPH (typ.)	Load
0	0	2.2mA	16 Ohm
1	0	1.5mA	16 Ohm
0	1	1.5mA	32 Ohm
1	1	1.0mA	32 Ohm

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

6.2.7 Parameter

Table 8 Power Amplifier Block Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
R_L	Output Load	stereo mode	16			Ohm
Pout	Maximum Output Power	R_L= 32Ω		20		mW
		R_L= 16Ω		40		mW
A0	Gain	programmable gain	-43.43		1.07	dB
$\triangle$Ax	Gain Step-Size		0.8	1.5	2.2	dB
PSRR	Power Supply Rejection Ratio	200Hz-20kHz, 720mVpp, R_L= 16Ω		90		dB
	Short Current Protection Level			145		mA
I_{OUT_pd}	I_{OUT} power down	HPGND is forced high	-20		20	uA
T_{power_up}				90		ms
SNR	Signal to Noise Ratio			100		dB
	Mute Attenuation			100		dB

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

6.2.8 Register Description

To get an interrupt on an over-current event, the corresponding bit in the IRQ_ENRD1 register (0x26h) has to be set. Also the interrupt request for HP detection has to be set in this register. The power-save options are controlled via AudioSet3 register (0x16h). All other headphone driver settings are controlled by the following two registers.

Right Headphone Register (02h)

Table 9 HPH_OUT_R Register

Bit	Name	Description
7,6	HP_OVC_TO	speaker over current time out: 11: 0 ms 10: 512 ms 01: 128 ms **00: 256 ms**
5	-	-
4..0	HPR_VOL	volume settings for right headphone output, adjustable in 32 steps @ 1.5dB 11111: 1.07 dB gain 11110: -0.43 dB gain .. 00001: -43.93dB gain **00000: -45.43 dB gain**

The register is R/W; default value is 00h

Left Headphone Register (03h)

Table 10 HPH_OUT_L Register

Bit	Name	Description
7	HP_Mute	**0: normal operation** 1: headphone output set to mute (mute is on during power-up)
6	HP_ON	**0: speaker stage not powered** 1: power up headphone stage
5	HPdetON	**0: no headphone detection** 1: enable headphone detection
4..0	HPL_VOL	volume settings for left headphone output, adjustable in 32 steps @ 1.5dB 11111: 1.07 dB gain 11110: -0.43 dB gain .. 00001: -43.93dB gain **00000: -45.43 dB gain**

The register is R/W; default value is 00h

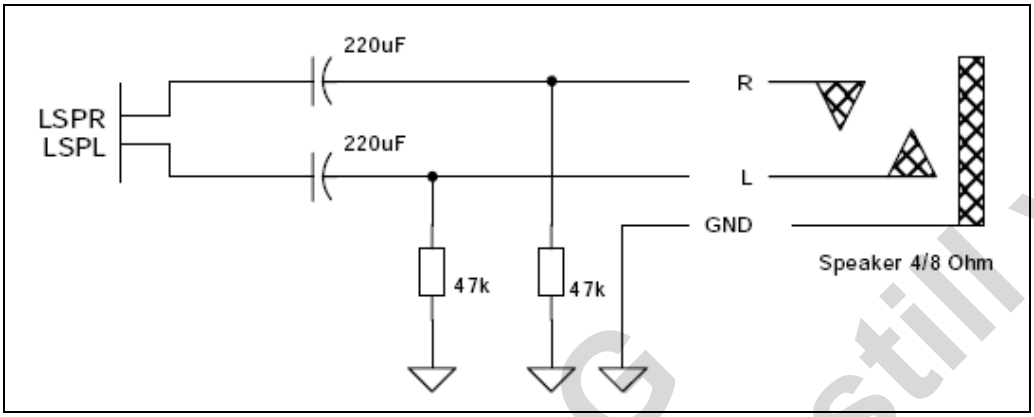
6.3 Speaker Output

6.3.1 General

The speaker output is designed to provide the stereo audio signal with 2x500mW @ 4Ω.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB. The maximum output power of 500mW @ 4Ω is achieved, by setting the mixer output to 1Vp and using the gain of +6dB.

Figure 3 Speaker Output



6.3.2 No-Pop Function

BGND pin, which needs a 100nF capacitor outside, gets charged on power-up to BVDD/2.To avoiding click and pop noise during power-up and shutdown, the output is automatically set to mute when the output stage is disabled.

The Start-up time before releasing mute is about 100ms. To avoid pop-noise the 150ms discharging time of SPR / SPL after a shutdown (220µF capacitor in stereo single ended mode assumed), have to be waited before starting up again.

6.3.3 Over-current Protection

This output stage has an over-current protection, which disables the output for 0 to 512ms. This value can be set in the speaker registers. The over-current protection limit of SPR and SPL pin is typical 700mA. To get an interrupt on an over-current event, the corresponding bit in the IRQ_ENRD1 register (0x26h) has to be set.

6.3.4 Power Save Options

When driving > 4Ω, two power save options can be chosen.

The output driver stage can be set to only 25% drive capacity, which will reduce the maximum output power. Additionally the bias currents can be reduced to 50% in 3 steps.

Table 11 Speaker Power-Save Options

LSP_LP	IBR_LSP	IDD_HPH (typ.)	Load
0	00	8mA	4 Ohm
1	00	2.8mA	16-32 Ohm
1	01	2.4mA	16-32 Ohm
1	10	1.9mA	16-32 Ohm
1	11	1.5mA	16-32 Ohm

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

6.3.5 Parameter

Table 12 Speaker Amplifier Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
R_L	Output Load	stereo mode	4			Ohm
		mono differential mode	8			Ohm
Pout	Maximum Output Power	R_L= 8Ω		1		W
A0	Gain	programmable gain	-40.5		6	dB
ΔAx	Gain Step-Size		0.8	1.5	2.2	dB
PSRR	Power Supply Rejection Ratio	200Hz-20kHz, 720mVpp, no load		75		dB
	Short Current Protection Level			700		mA
I_{OUT_pd}	I_{OUT} power down	BGND is forced high	-20		20	uA
T_{power_up}				100		ms
SNR	Signal to Noise Ratio			100		dB
	Mute Attenuation			100		dB

BVDD = 5V, T_A= 25°C unless otherwise mentioned

6.3.6 Register Description

To get an interrupt on an over-current event, the corresponding bit in the IRQ_ENRD1 register (0x25h) has to be set. Changing the bias current or the output driver strength is done via AudioSet2 register (0x15h). All other speaker driver settings are controlled by the following two registers.

Right Speaker Register (04h)

Table 13 LSP_OUT_R Register

Bit	Name	Description
7,6	SP_OVC_TO	speaker over current time out: 11: 0 ms 10: 512 ms 01: 128 ms **00: 256 ms**
5	-	not used
4..0	SPR_VOL	volume settings for right speaker output, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The register is R/W; default value is 00h

Left Speaker Register (05h)

Table 14 LSP_OUT_L Register

Bit	Name	Description
7	SP_Mute	**0: normal operation** 1: speaker output set to mute (mute is on during power-up)
6	SP_ON	**0: speaker stage not powered** 1: power up speaker stage
5	-	not used
4..0	SPR_VOL	volume settings for left speaker output, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The register is R/W; default value is 00h

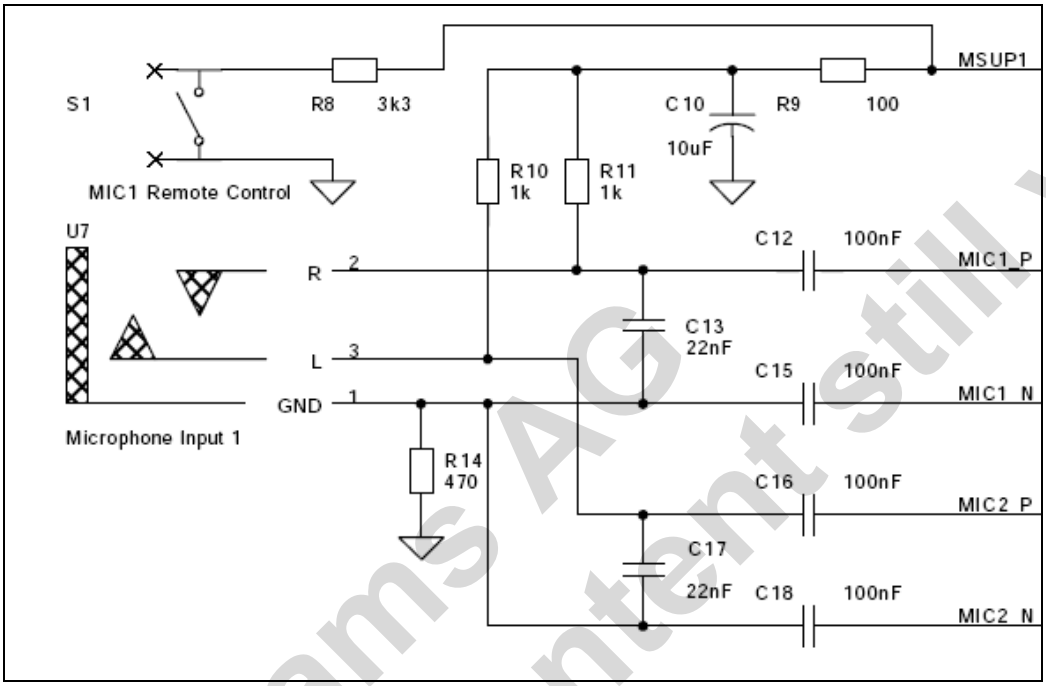
6.4 Microphone Inputs (2x)

6.4.1 General

AS3514 includes two identical microphone inputs. The blocks have differential inputs to a microphone amplifier with adjustable gain. This stage also includes an AGC.

The following volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB. The stage is set to mute by default. If the microphone input is not enabled, the volume settings are set to their default values. Changing of volume and mute control can only be done after enabling the input.

Figure 4 Microphone Input



6.4.2 AGC

The microphone amplifier includes an AGC, which is limiting the signal to 1Vp. The AGC has 15 steps with a dynamic range of about 29dB. The AGC is ON by default but can be disabled by a microphone register bit.

6.4.3 Supply & Detection

Each microphone input generates a supply voltage of 1.5V above HPHCM. The supply is designed for ≤2mA and has a 10mA current limit. In OFF mode the MICSUP terminal is pulled to AVDD with 30kohm. A current of typically 50uA generates an interrupt to inform the CPU, that a circuit is connected. When using HPHCM as headset ground the HPH–stage gives the interrupt. After enabling the HPH-stage through the CPU the microphone detection interrupt will follow.

6.4.4 Remote Control

Fast changes of the supply current of typically 500uA are detected as a remote button press, and an interrupt is generated. Then the CPU can start the measurement of the microphone supply current with the internal 10-bit ADC to distinguish which button was pressed. As the current measurement is done via an internal resistor, only two buttons generating a current of about 0.5mA and 1mA can be detected. With this 1mA as microphone bias is still available.

6.4.5 Parameter

Table 15 Microphone Inputs Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
A0	Gain	programmable gain	-40.5		6	dB
$\triangle$Ax	Gain Step-Size			1.5		dB
R_{inMIC}	Input Resistance	differential		15		kOhm
$A_{MIC}0$	MicAmp_Gain0			28		dB
$A_{MIC}1$	MicAmp_Gain1			34		dB
$A_{MIC}2$	MicAmp_Gain2			40		dB
	SoftClip_AGC_Range			15*2.0		dB
	Attack_Time			60		us
	Release_Time			120		ms
$V_{Innom}0$	Nominal_Input_Voltage0	MicInGain = 0dB, MicAmp_Gain0		40		mVp
$V_{Innom}1$	Nominal_Input_Voltage1	MicInGain = 0dB, MicAmp_Gain1		20		mVp
$V_{Innom}2$	Nominal_Input_Voltage2	MicInGain = 0dB, MicAmp_Gain2		10		mVp
SNR	Signal to Noise Ratio			100		dB
	Mute Attenuation			100		dB
Microphone Supply						
V_{MICsup}	Microphone Supply Voltage	0-2mA		2.95		V
I_{MIClim}	Mic. Supply Current Limit			10		mA
I_{MICdet}	Mic. Detection Current			50		uA
I_{REMdet}	Remote Detection Current				500	uA
V_{noise}	Voltage Noise			5.7		uV

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

6.4.6 Register Description

Enabling a microphone input is done via a control bit in the audio settings register (AudioSet1 register 0x14h). To get an interrupt on an microphone detection event, the corresponding bit in the IRQ_ENRD1 register (0x26h) has to be set, while a remote detection interrupt is controlled via IRQ_ENRD2 register (0x27h). All other microphone input settings are controlled by the following registers.

Right Microphone Registers (06h & 08h)

Table 16 MIC1_R & MIC2_R Register

Bit	Name	Description
7	M1_AGC_off M2_AGC_off	**0: automatic gain control enabled** 1: automatic gain control disabled
6,5	M1_Gain M2_Gain	**00: gain set to 28 dB** 01: gain set to 34 dB 10: gain set to 40 dB 11: gain set to tbd.
4..0	M1R_VOL M2R_VOL	volume settings for right microphone input, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The registers are R/W; default value is 00h

Left Microphone Register (07h & 09h)

Table 17 MIC1_L & MIC2_L Register

Bit	Name	Description
7	M1_Sup_off M2_Sup_off	**0: microphone supply enabled** 1: microphone supply disabled
6	M1_Mute_off M2_Mute_off	**0: microphone input set to mute** 1: normal operation
5	-	Not used
4..0	M1L_VOL M2L_VOL	Volume settings for left microphone input, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The registers are R/W; default value is 00h

6.5 Line Inputs (2x)

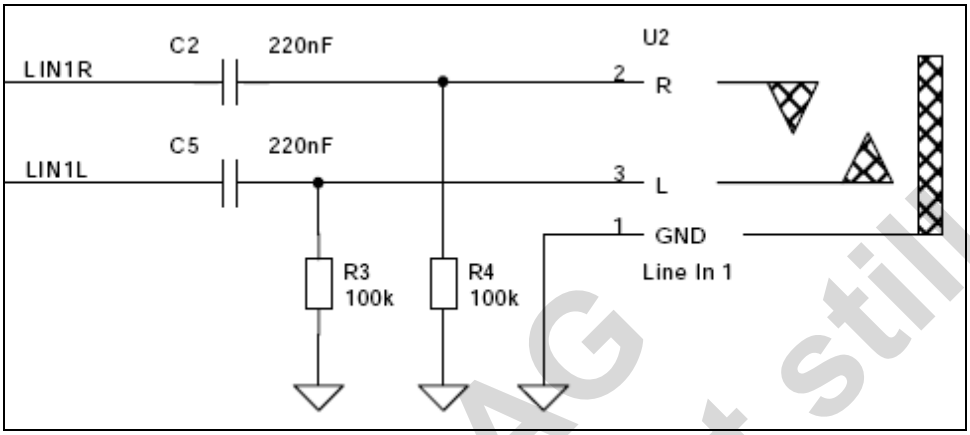
6.5.1 General

AS3514 includes two identical line inputs. The blocks can work in mono differential, 2x mono single ended or in stereo single ended mode.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –34.5dB to +12dB. The stage is set to mute by default. If the line input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

If using the inputs as mono differential, the volume setting for the right channel should be set to 0dB.

Figure 5 Line Input



6.5.2 Parameter

Figure 6 Line Input Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
A0	Gain	programmable gain	-34.5		12	dB
∆Ax	Gain Step-Size			1.5		dB
R_{inLINE}	Input Resistance	Mute		49		kOhm
		Min Gain, single ended stereo		100		kOhm
SNR	Signal to Noise Ratio			100		dB
	Mute Attenuation			100		dB

BVDD = 3.3V, T_A= 25°C, fs=48kHz unless otherwise mentioned

6.5.3 Register Description

Enabling a line-input is done via a control bit in the audio settings register (AudioSet1 register 0x14h). All other line input settings are controlled by the following registers.

Right Line In Registers (0Ah & 0Ch)

Table 18 LINE_IN1_R & LINE_IN2_R Register

Bit	Name	Description
7,6	-	
5	LI1R_Mute_off LI2R_Mute_off	**0: right line input is set to mute** 1: normal operation
4..0	LI1R_VOL LI2R_VOL	volume settings for right line input, adjustable in 32 steps @ 1.5dB 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

The registers are R/W; default value is 00h

Left Line In Register (0Bh & 0Dh)

Table 19 LINE_IN1_L & LINE_IN2_L Register

Bit	Name	Description
7,6	LI1_Mode LI2_Mode	Single ended stereo or differential mono selection **00: inputs switched to single ended stereo** 01: inputs switched to differential mono 10: inputs switched to single ended mono 11: tbd.
5	LI1L_Mute_off LI2L_Mute_off	**0: left line input is set to mute** 1: normal operation
4..0	LI1L_VOL LI2L_VOL	Volume settings for left line input, adjustable in 32 steps @ 1.5dB 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

The registers are R/W; default value is 00h

6.6 Digital Audio Interface

6.6.1 Input

Digital audio data can be fed into the AS3514 via the I2S interface These input data are then used by the 18-bit DAC to generate the analog audio signal.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB. The stage is set to mute by default. If the DAC input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

6.6.2 Output

This block consists of an audio multiplexer where the signal, which should be recorded, can be selected. The output is then fed through a volume control to the 14 bit ADC. The digital output is done via an I2S interface.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –34.5dB to +12dB. The stage is set to mute by default. If the ADC output is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

The I2S output uses the same clocks as the I2S input. The sampling rate therefore depends also on the input sampling rate.

6.6.3 Signal Description

The digital audio interface uses the standard I2S format:

- left justified
- MSB first
- one additional leading bit

The first 18 bits are taken for DAC conversion. The on-chip synchronization circuit allows any bit-count up 32bit. When there are less than 18 bits sampled, the data sample is completed with “0”s. The ADC output is always 16 bit. If more SCLK pulses are provided, only the first 16 will be significant. All following bit will be “0”.

SCLK has not to be necessarily synchronous to LRCK but the high going edge has to be separate from LRCK edges. The LRCK signal has to be derived from a jitter-free clock source, because the on-chip PLL is generating a clock for the digital filter, which has to be always in correct phase lock condition to the external LRCK.

Figure 7 I2S_Timing

Error! Not a valid link.

6.6.4 Power Save Options

The bias current of the DAC block can be reduced in three steps down to 50% to reduce the power consumption.

6.6.5 Clock Supervision

The digital audio interface automatically checks the LRCK. An interrupt can be generated when the state of the LRCK input changes. A bit in the interrupt register represents the actual state (present or not present) of the LRCK.

6.6.6 Parameter

Table 20 DAC Block Parameter

Symbol	Parameter	Notes	Min	Typ	Max	Unit
A0	Gain	programmable gain DAC input	-43.43		1.07	dB
		programmable gain ADC output	-34.5		12	dB
$\triangle$Ax	Gain Step-Size			1.5		dB
	Mute Attenuation			100		dB
I2S inputs / outputs						
V_{IL}		SCLK, LRCK, SDI (30%DVDD/2)	-	-	0.42	V
V_{IH}		SCLK, LRCK, SDI (70%DVDD/2)	1.02	-	DVDD	V
V_{OL}		SDO @ 2mA	-	-	0.3	V
V_{OH}		SDO @ 2mA	2.6	-	-	V
t_{su}	Set-up Time	SDI versus high going edge of SCLK	80			ns
t_{hd}	Hold Time	SDI versus high going edge of SCLK	80			ns
t_{s1}, t_{s2}	Separation Time	SCLK high going edges separation from LRCK edges	80			ns
t_{jitter}	clock Jitter	LRCK	-20		20	ns

BVDD = 3.3V, DVDD = 2.9V, T_A= 25°C unless otherwise mentioned

6.6.7 Register Description

Enabling the DAC or ADC is done via a control bit in the audio settings register (AudioSet1 register 0x14h). To get an interrupt on a LRCK state change, the corresponding bit in the IRQ_ENRD1 register (0x25h) has to be set. Changing the bias current and adding a dither signal is done via AudioSet2 register (0x15h). All other DAC or ADC settings are controlled by the following two registers.

Right DAC Register (0Eh)

Table 21 DAC_R Register

Bit	Name	Description
7..5	-	
4..0	DAR_VOL	volume settings for right DAC input, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The register is R/W; default value is 00h

Left DAC Register (0Fh)

Table 22 DAC_R Register

Bit	Name	Description
7	-	
6	DAC_Mute_off	**0: DAC input is set to mute** 1: normal operation
5	-	
4..0	DAL_VOL	volume settings for left DAC input, adjustable in 32 steps @ 1.5dB 11111: 6 dB gain 11110: 4.5 dB gain .. 00001: -39 dB gain **00000: -40.5 dB gain**

The register is R/W; default value is 00h

Right ADC Register (10h)

Table 23 ADC_R Register

Bit	Name	Description
7,6	ADCmux	**00: Stereo Microphone** 01: Line_IN1 10: Line_IN2 11: Audio SUM
5	-	
4..0	ADR_VOL	volume settings for right ADC input, adjustable in 32 steps @ 1.5dB 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

The register is R/W; default value is 00h

Left ADC Register (11h)

Table 24 ADC_L Register

Bit	Name	Description
7	AD_FS2	Divider selection for ADC clock **0: ADC sample clock is I2S LRCK / 2** 1: ADC sample clock is I2S LRCK / 4
6	ADC_Mute_off	**0: ADC input is set to mute** 1: normal operation
5	-	
4..0	ADL_VOL	Volume settings for left ADC input, adjustable in 32 steps @ 1.5dB 11111: 12 dB gain 11110: 10.5 dB gain .. 00001: -33 dB gain **00000: -34.5 dB gain**

The register is R/W; default value is 00h

PLL Mode Register (1Dh)

Table 25 PLLMode Register

Bit	Name	Description
7..3	-	Not used
2,1	PLLmode<1:0>	Sets the MCLK generation for different LRCK speeds: **00: LRCK: 24-48kHz** 01: reserved 10: LRCK: 8-23kHz 11: reserved
0	-	Not used

The register is R/W; default value is 00h

6.7 Audio Output Mixer

6.7.1 General

The mixer stage sums up the audio signals of the following stages

- Microphone Input 1
- Microphone Input 2
- Line Input 1
- Line Input 2
- Digital Audio Input (DAC)

The mixing ratios have to be with the volume registers of the corresponding input stages. Please be sure that the input signals of the mixer stage are not higher than 1Vp. If summing up several signals, each has of course to be lower.

This shall insure that the output signal is also not higher than 1Vp to get a proper signal for the output amplifier. This stage has an automatic gain control, which automatically avoids clipping.

6.7.2 AGC

The audio mixer includes an AGC, which is limiting the signal to 1Vp. The AGC has 12 steps with a dynamic range of about 18dB. The AGC is ON by default but can be disabled by a register bit.

6.7.3 Register Description

The mixer stage has no direct associated registers.

Enabling the Summing / Mixer stage is done via a control bit in the audio settings register (AudioSet1 register 0x14h). Disabling the AGC is done via AudioSet2 register (0x15h).

6.8 Audio Settings

6.8.1 Register Description

First AudioSet Register (14h)

Table 26 AudioSet1 Register

Bit	Name	Description
7	ADC_on	1: ADC for recording is enables **0: ADC disabled**
6	SUM_on	1: Summing / Mixing stage is enabled **0: Summing / Mixing stage is disabled (no audio output possible)**
5	DAC_on	1: DAC enabled **0: DAC disabled**
4	LOUT_on	1: Line output enabled **0: Line output disabled**
3	LIN2_on	1: Line input 2 enabled **0: Line input 2 disabled**
2	LIN1_on	1: Line input 1 enabled **0: Line input 1 disabled**
1	MIC2_on	1: Microphone input 2 enabled **0: Microphone input 2 disabled**
0	MIC1_on	1: Microphone input 1 enabled **0: Microphone input 1 disabled**

The register is R/W; default value is 00h

Second AudioSet Register (15h)

Table 27 AudioSet2 Register

Bit	Name	Description
7	BIAS_off	1: Bias disabled **0: Bias enabled**
6	DITH_off	1: no dither added **0: add dither to the audio stream**
5	AGC_off	1: Automatic gain control for summing stage disabled 0**: Automatic gain control for summing stage enabled**
4,3	IBR_DAC<1:0>	Bias current reduction settings for DAC: **00: 0%** 01: 25% 10: 40% 11: 50%
2	LSP_LP	Low power mode for speaker output: 1: speaker output driver set for 16Ohm load or more (25%) **0: speaker output driver set for 4Ohm to 16Ohm load (100%)**
1,0	IBR_LSP<1:0>	Bias current reduction settings for speaker output: **00: 0%** 01: 17% 10: 34% 11: 50%

The register is R/W; default value is 00h