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AS3517

Stereo Audio Codec with enhanced System Power Management

1 General Description

The AS3517 is a low power stereo audio codec and is designed for Portable Digital Audio Applications. It allows playback and recording in CD quality. It has a variety of audio inputs and outputs to directly connect electret microphones, 16Ω/32Ω headsets and auxiliary signal sources via a 10-channel mixer. It only consumes 20mW in playback mode.

Further the device offers advanced power management functions. All necessary ICs and peripherals in a Digital Audio Player with flash or harddisk memory are supplied by the AS3517. The different regulated supply voltages are programmable via the serial control interface. The power management block generates 11 different supply voltages out of a single battery supply. CPU, NAND flash, SRAM, memory cards, harddisk, LCD, LCD backlight, USB-HOST and USB-OTG can be powered. AS3517 also contains a charger. The single supply voltage may vary from 3.0V to 5.5V.

The AS3517 has an on-chip, phase locked loop (PLL) controlled, clock generator. It generates 44.1kHz, 48kHz and other sample rates defined in MP3, AAC, WMA, OGG VORBIS etc. No additional external crystal or PLL is needed in slave mode. Further the AS3517 has an independent 32kHz real time clock (RTC) on chip which allows a complete power down of the system CPU.

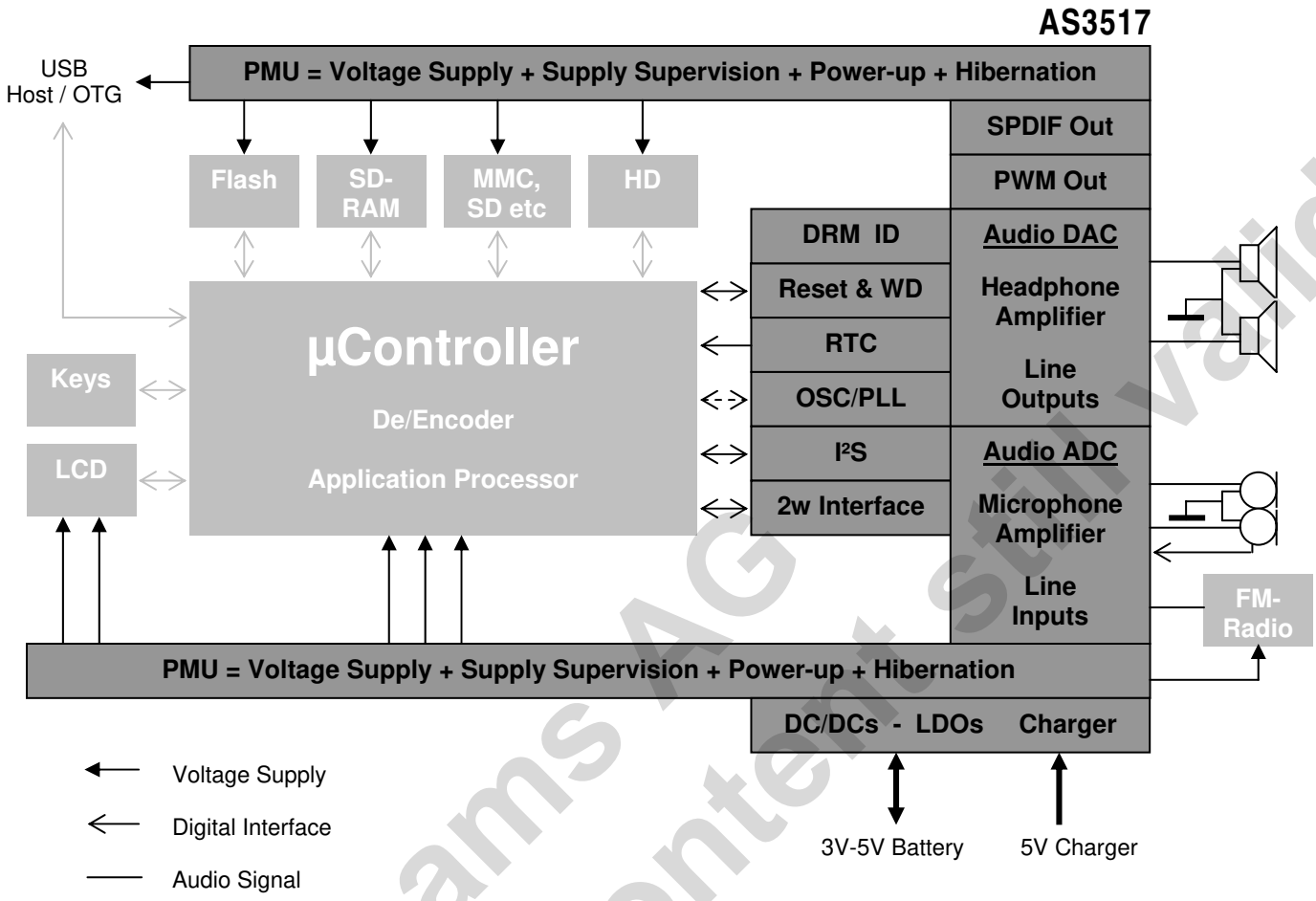
2 Key Features

- Multi-bit Sigma Delta Converters
  - DAC: 94dB SNR ('A' weighted) @ 2.9V
  - ADC: 90dB SNR ('A' weighted) @ 2.9V
  - Sampling Frequency: 8-48kHz
- 2 Microphone Inputs
  - 3 gain pre-setting (28dB/34dB/40dB) and AGC
  - 32 gain steps @1.5dB and MUTE
  - supply for electret microphone
  - microphone detection
  - remote control by switch
- 2 Line Inputs
  - volume control via serial interface
  - 32 steps @1.5dB and MUTE
  - stereo or 2x mono or mono differential
- Audio Mixer
  - 10 channel input/output mixer with AGC
  - mixes line inputs and microphones with DAC
  - left and right channels independent
- 2 Line Outputs
  - volume control via serial interface
  - 32 steps @1.5dB and MUTE
  - 1Vp @10kΩ
  - Stereo 2*5mW to 16ohm
  - Differential 10mW to 32ohm (earpiece)
- High Efficiency Headphone Amplifier
  - volume control via serial interface
  - 32 steps @1.5dB and MUTE
  - 2x60mW @16Ω driver capability
  - headphone and over-current detection
  - phantom ground eliminates large capacitors
- Power Management
  - step down for CPU core (0.65V-3.4V, 250mA)
  - step down for peripheral (0.65V-3.4V, 250mA)
  - step down for harddisk (0.65V-3.4V, 500mA)
  - step up for backlight (15V (25V), 38mA),
  - LDO for digital supply (2.9V, 200mA)
  - LDO for analog supply (2.9V, 200mA)
  - LDO for peripherals (1.2V-3.5V, 200mA)
  - LDO for peripherals (1.2V-3.5V, 200mA)
  - LDO for RTC (1.0V-2.5V, 2mA)
  - power supply supervision
  - hibernation modes
  - 5sec and 10sec emergency shut-down
- Battery Charger
  - automatic trickle charge (50mA)
  - prog. constant current charging (50-460mA)
  - prog. constant voltage charging (3.9V-4.25V)
- Real Time Clock
  - ultra low power 32kHz oscillator
  - 32bit RTC sec counter, 96 days auto wake-up
  - selectable alarm (seconds or minutes)
  - 128bit free SRAM for random settings
  - 32kHz clock output to peripheral
- Auxiliary Oscillator (only for master clock mode)
  - low power 12-24MHz oscillator
  - master clock input/output (e.g. from/to CPU)
- General Purpose ADC
  - 10bit resolution
  - 21 inputs analog multiplexer
- Interfaces
  - I²S digital audio interface and SPDIF
  - 2 wire serial control interface
  - reset pin, watchdog, power good pin
  - PWM output
  - 128bit unique ID (OTP)
  - 30 different interrupts
- Package CTBGA81 [9.0x9.0x1.15mm] 0.8mm pitch

3 Application

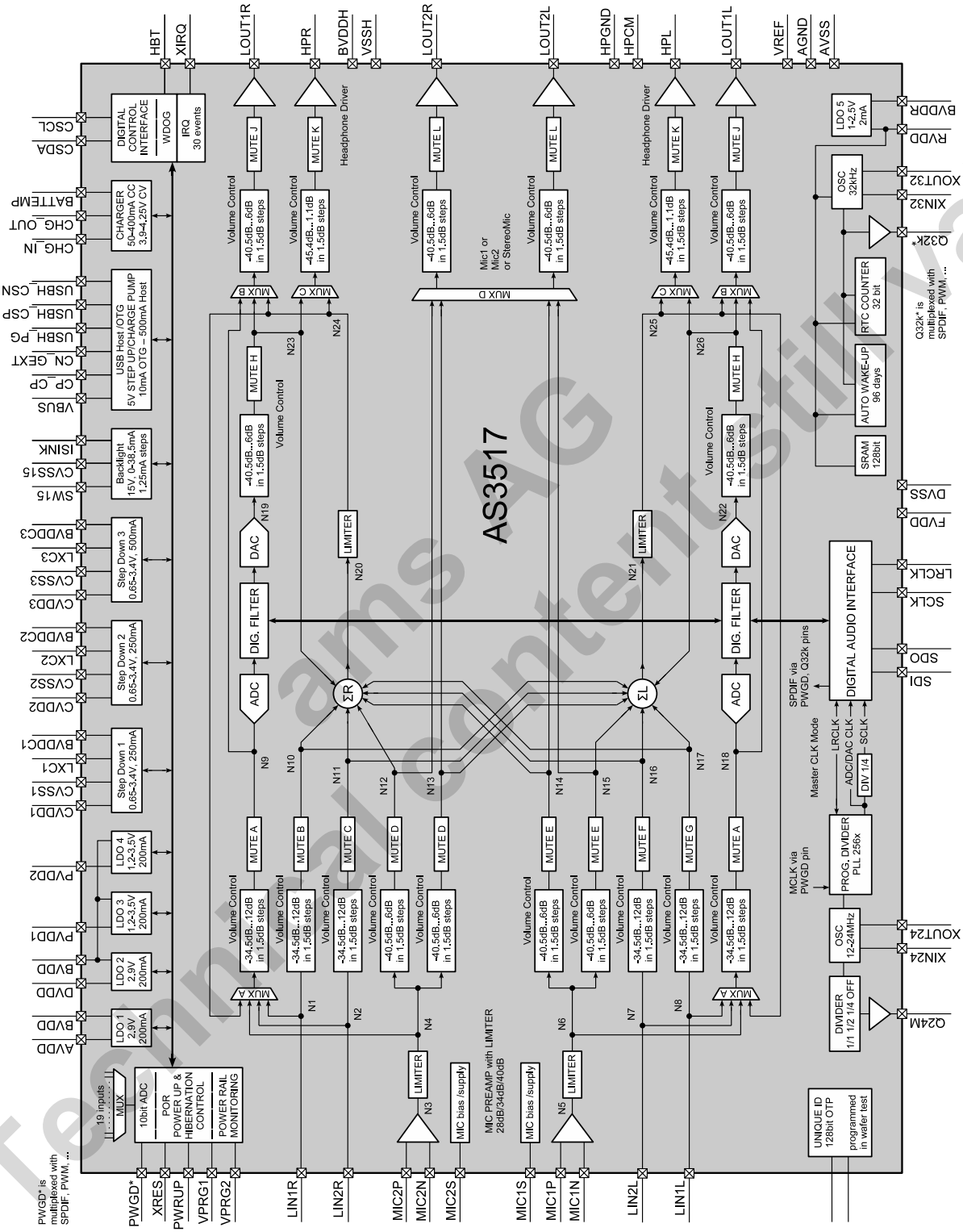
Portable Digital Audio Player and Recorder
PDA, Smartphone

4 Functional Overview



5 Block Diagram

Figure 1 AS3517 Block Diagram



Contents

Revision History

Revision	Date	Owner	Description
0.99	6.10.2006	pkm	Corrected version
1.0	12.10.2006	pkm	Changed block diagram of DCDC15
			Inserted register overview
			Corrected some typos
1.1	26.1.2007	pkm	Corrected block diagram (DAC mute)
			Corrected start-up sequence (VPROG1 and VPROG2 exchange)
1.2	6.4.2007	pkm	Added Typical Application Information
			Changed chip version for V17
			RTCT register reset corrected to RVDD-POR
			USB & CHGIN 0ms de-bounce time changed to 8ms
1.3	24.9.2008	pkm	Updated marking and ordering information

6 Pinout and Packaging

6.1 Pin Description

Table 1 Pinlist CTBGA81

Ball	PinName	Type	Function
G7	AGND	Analog I/O	Analog Reference Voltage (AVDD/2) buffer cap terminal
H7	AVDD	Supply	Analog Circuit VDD, connected to LDO1 on BGA substrate
J9	AVSS	Supply	Analog Circuit VSS
E2	BATTEMP	Analog I/O	Charger Battery Temperature Sensor input (100kΩ NTC)
D3	BVDD	Supply	Positive (Battery) Supply Terminal, 5.5V max.
E3	BVDD	Supply	Positive (Battery) Supply Terminal, 5.5V max.
B8	BVDDH	Supply	Positive (Battery) Supply Terminal of Headphone Amplifier, 5.5V max.
A8	BVDDC1	Supply	Positive (Battery) Supply Terminal of DCDC1, 5.5V max.
A4	BVDDC2	Supply	Positive (Battery) Supply Terminal of DCDC2, 5.5V max.
B4	BVDDC3	Supply	Positive (Battery) Supply Terminal of DCDC3, 5.5V max.
F2	BVDDR	Supply	RTC Positive (Battery) Supply terminal, 5.5V max
F1	CHG_IN	Analog Input	Charger Positive Supply Terminal, 5.5V max
E1	CHG_OUT	Analog Output	Charger Output prog. for Ichg 50-400mA or Vchg 3.9-4.25V
C1	CN_GEXT	Digital output	USB charge pump CN of flying cap / Output to control USB-Host DCDC N-Switch
C2	CP_CP	Digital output	USB charge pump CP of flying cap
G3	CSCL	Digital input with pull up	Clock Input of two wire interface
H3	CSDA	Digital I/O with pull up	Data I/O of two wire interface
B7	CVDD1	Analog Input	CVDD1 and Feedback pin
B5	CVDD2	Analog Input	CVDD2 and Feedback Pin
B3	CVDD3	Analog Input	CVDD3 and Feedback Pin
A6	CVSS1	Supply	CVDD1 StepDown Neg. Supply terminal
B6	CVSS2	Supply	CVDD2 StepDown Neg. Supply terminal
A2	CVSS3	Supply	CVDD3 Stepdown Neg. Supply terminal
B2	CVSS15	Supply	DCDC15V Neg. Supply terminal
G1	DVDD	Supply	Digital Circuit VDD, connected to LDO2 on BGA substrate
J2	DVSS	Supply	Digital Circuit VSS
H2	FVDD	Supply	ADC&DAC Digital Circuit VDD (1.8-3.6V)
F3	HBT	Digital input with pull down	Heartbeat Input for CPU supervision
C8	HPCM	Analog Output	Headphone Common GND Output for DC-coupled speakers
D9	HPGND	Analog I/O	Headphone Amplifier reference buffer cap terminal
A9	HPL	Analog Output	Headphone Amplifier Output Left Channel
C9	HPR	Analog Output	Headphone Amplifier Output Right Channel
B1	ISINK	Analog Output	DCDC15V Load Current Sink terminal (e.g. white LED)
D7	LIN1L	Analog Input	Line Input 1 Left Channel
D6	LIN1R	Analog Input	Line Input 1 Right Channel
F8	LIN2L	Analog Input	Line Input 2 Left Channel
F7	LIN2R	Analog Input	Line Input 2 Right Channel
C7	LOUT1L	Analog Output	Line Output Left Channel
C6	LOUT1R	Analog Output	Line Output Right Channel
D8	LOUT2L	Analog Output	Line Output Left Channel
E7	LOUT2R	Analog Output	Line Output Right Channel
G4	LRCLK	Digital I/O with pull down	I2S Left/Right Clock
A7	LXC1	Digital output	CVDD1 StepUp switch output to coil
A5	LXC2	Digital output	CVDD2 StepUp switch output to coil
A3	LXC3	Digital output	CVDD3 StepUp switch output to coil

Ball	PinName	Type	Function
H9	MIC1N	Analog Input	Microphone Input 1N
G9	MIC1P	Analog Input	Microphone Input 1P
G8	MIC1S	Analog I/O	Microphone Supply 1 (2.95V) / Remote Input 1
E9	MIC2N	Analog Input	Microphone Input 2N
F9	MIC2P	Analog Input	Microphone Input 2P
E8	MIC2S	Analog I/O	Microphone Supply 2 (2.95V) / Remote Input 2
D2	PVDD1	Analog Output	LDO3 Regulator Output
D1	PVDD2	Analog Output	LDO4 Regulator Output
F6	PWGD	Digital I/O multiplexed	Power Good, SPDIF, PLL clock, PWM digital output. Configurable as open drain or push pull. Master CLK digital input (e.g. from CPU)
J6	PWRUP	Digital input with pull down	Power Up input
J4	Q24M	Digital output multiplexed	12-24MHz Clock output, PLL clock. Configurable as open drain or push pull.
J3	Q32K	Digital output multiplexed	32kHz Clock output, SPDIF, PLL clock, PWM. Configurable as open drain or push pull.
G2	RVDD	Analog Output	RTC Supply Regulator Output prog. to 1.0-2.5V
F4	SCLK	Digital I/O with pull down	I2S Shift Clock
H4	SDI	Digital input with pull down	I2S Data Input to DAC
G5	SDO	Digital output	I2S Data output from ADC
A1	SW15	Analog Output	DCDC15V switch terminal
D4	USBH_CSN	Analog Input	USB-Host Step Up neg. Current sense terminal to 100mΩ resistor
C4	USBH_CSP	Analog Input	USB-Host Step Up pos. Current sense term. to 100mΩ resistor (BVDD)
C5	USBH_PG	Digital output	Output to control USB-Host DCDC high Side P-Switch
G6	VPRG1	Analog Input	5 State Prog Input to define power up sequence
H6	VPRG2	Analog Input	5 State Prog Input to define default regulator voltages
H8	VREF	Analog I/O	Analog Reference (filtered AVDD) decoupling cap terminal
C3	VBUS	Analog I/O	USB supply terminal for supervision and charge pump or StepUp feedback
B9	VSSH	Supply	Headphone Amplifier Neg. Supply terminal
J7	XIN24	Analog I/O	24MHz Oscillator Crystal terminal
H1	XIN32	Analog I/O	32kHz RTC Oscillator Crystal terminal
H5	XIRQ	Digital output	Interrupt Request Output. Configurable as open drain or push pull, active high or active low
J8	XOUT24	Analog I/O	24MHz Oscillator Crystal terminal
J1	XOUT32	Analog I/O	32kHz RTC Oscillator Crystal terminal
J5	XRES	Digital output open drain	Reset Output

6.2 Ball Assignment

6.2.1 CTBGA81

Figure 2 Ball Assignment CTBGA81

	1	2	3	4	5	6	7	8	9	
A	SW15	CVSS3	LXC3	BVDDC2	LXC2	CVSS1	LXC1	BVDDC1	HPL	A
B	ISINK	CVSS15	CVDD3	BVDDC3	CVDD2	CVSS2	CVDD1	BVDDH	VSSH	B
C	CN_GEXT	CP_CP	VBUS	USBH_CSP	USBH_PG	LOUT1R	LOUT1L	HPCM	HPR	C
D	PVDD2	PVDD1	BVDD	USBH_CSN	nc	LIN1R	LIN1L	LOUT2L	HPGND	D
E	CHG_OUT	BATTEMP	BVDD	nc	nc	nc	LOUT2R	MIC2S	MIC2N	E
F	CHG_IN	BVDDR	HBT	SCLK	nc	PWGD	LIN2R	LIN2L	MIC2P	F
G	DVDD	RVDD	CSCL	LRCLK	SDO	VPRG1	AGND	MIC1S	MIC1P	G
H	XIN32	FVDD	CSDA	SDI	XIRQ	VPRG2	AVDD	VREF	MIC1N	H
J	XOUT32	DVSS	Q32K	Q24M	XRES	PWRUP	XIN24	XOUT24	AVSS	J
	1	2	3	4	5	6	7	8	9	

6.3 Package Drawings

6.3.1 CTBGA81

Marking

Figure 3 CTBGA81 Marking

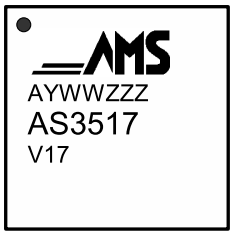
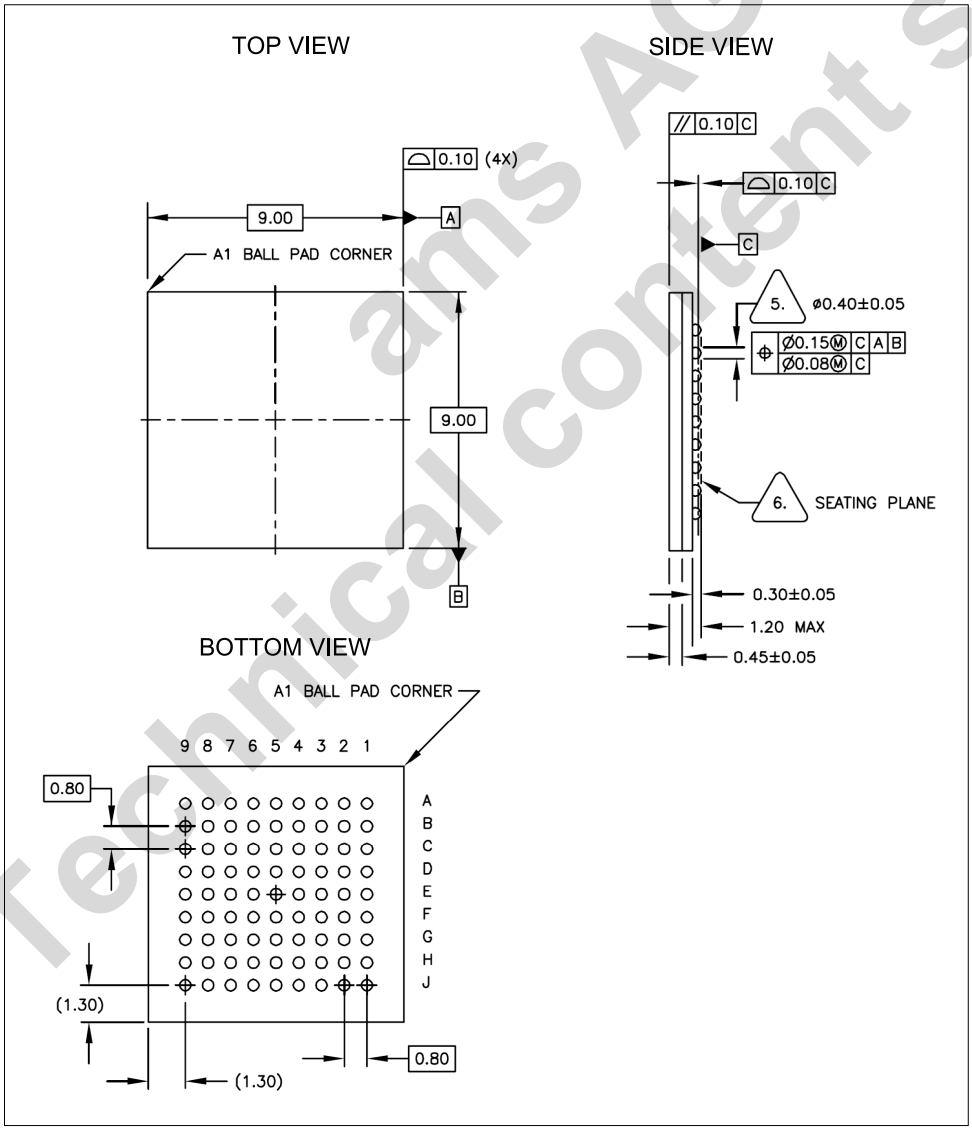


Table 2 Package Code AYWWZZZ

A	Y	WWW	ZZZ
A ... for PB free	Year	Working week assembly/packaging	Free choice

Dimensions

Figure 4 CTBGA81 9x9mm 0.8mm pitch



7 Ordering Information

Device ID	Version	Temperature Range	Package Type	Delivery Form
AS3517H-ECTP	V17	-20 to +85 °C	CTBGA81; 9x9mm package size, 0.8mm ball pitch	Tape & Reel DryPack
AS3517H-ECTS	V17	-20 to +85 °C	CTBGA81; 9x9mm package size, 0.8mm ball pitch	Tray DryPack

8 Absolute Maximum Ratings (Non-Operating)

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

Table 3 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{IN_5V}	5V pins	-0.5	7.0	V	Applicable for pins BVDD, BVDDH, BVDDC1, BVDDC2, BVDDC3, BVDDR, CHG_IN, VBUS
V_{IN_SW15}	15V pin	-0.5	17	V	Applicable for pin SW15
V_{IN_VSS}	Voltage difference at VSS terminals	-0.5	0.5	V	Applicable for pins CVSS3, CVSS15, CVSS1, CVSS2, VSSH, AVSS, DVSS
V_{IN_DVDD}	3.3V pins with diode to DVDD	-0.5	5.0 DVDD+0.5	V	Applicable for pins LRCK, SCLK, SDI, VPRG1, VPRG2, BATTEMP, ISINK, XIN32, XOUT32, XIN24, XOUT24, XIRQ, XRES, PWGD, Q32K, Q24M, HBT
V_{IN_xDVDD}	pins with no diode to DVDD	-0.5	7.0V	V	Applicable for pins CSCL, CSDA, PWRUP
V_{IN_AVDD}	3.3V pins with diode to AVDD	-0.5	5.0 AVDD+0.5	V	Applicable for pins HPCM, HPGND, LOUT1L/R, LOUT2L/R, VREF, AGND, LIN1L/R, LIN2L/R, MIC1P/N, MIC2P/N, MIC1S, MIC2S
V_{IN_REG}	voltage regulator pins with diodes to BVDD	-0.5	5.0 BVDD+0.5	V	Applicable for pins AVDD, DVDD, PVDD1/2, CVDD1/2/3, UVDD
V_{IN_RVDD}	voltage regulator pin with diode to BVDD	-0.5	3.6 BVDD+0.5	V	Applicable for pins RVDD
V_{IN_BVDD}	pins with diode to BVDD	-0.5	7.0 BVDD+0.5	V	Applicable for pins HPR/L, CHG_OUT
I_{scr}	Input Current (latchup immunity)	-100	100	mA	Norm: JEDEC 17
ESD	Electrostatic Discharge HBM		+/-1	kV	Norm: JEDEC JESD22-A114C
P_t	Total Power Dissipation (all supplies and outputs)		1000	mW	BGA81, T_{amb}=70°C
H	Humidity non-condensing	5	85	%	

Table 4 Soldering Conditions

Symbol	Parameter	Min	Max	Unit	Note
T_{body}	Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only
T_{peak}	Solder Profile*	235	245	°C	
D_{well}		30	45	s	above 217 °C

* austriamicrosystems AG strongly recommends to use underfill.

8.1 Operating Conditions

8.1.1 Supply Voltages

Table 5 Operating conditions for supply voltages

Symbol	Parameter	Min	Max	Unit	Note
BVDDx	Battery Supply Voltage BVDD, BVDDH, BVDDC1, BVDDC2, BVDDC3, BVDDR	3.0	5.5	V	
VBUS	USB VBUS Voltage	4.0	5.5	V	
CHG_IN	Charger Supply Voltage	4.5	5.5	V	
DVDD	Digital Supply Voltage	2.8	3.6	V	Digital Audio Supply Voltage (LDO2)
AVDD	Analogue Supply Voltage	2.8	3.6	V	Analog Audio Supply Voltage (LDO1)
AGND	Analogue Ground Voltage		AVDD/2		
V_{DELTA-}	Difference of Negative Supplies CVSS1, CVSS2, CVSS3, CVSS15, VSSH, AVSS, DVSS	-0.1	0.1	V	To achieve good performance, the negative supply terminals should be connected to low impedance ground plane.
V_{DELTA+}	Difference of Positive Supplies	-0.25	0.25	V	AVDD-DVDD

Table 6 Electrical Specification of other function blocks

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{POR_ON}	Power-on Reset Activation Level		2.15		V	Power-on Reset activation level when DVDD decreases
V_{POR_OFF}	Power-on Reset Release Level		2.0		V	Power-on Reset release when DVDD increases
V_{POR_HY}	Power-on Hysterisis		100		mV	
f_{LRCLK_WD}	LRCLK Frequency Watchdog	2	4.1	8	kHz	
t_{ON_DELAY}	Delay Time of pin PWRUP		10		ms	Minimum key press time
V_{DO_L}	Digital Output Driver Capability (drive LOW)			0.3	V	Pins XRES, XIRQ, PWGD @ 8mA, SDO
V_{DO_H}	Digital Output Driver Capability (drive HIGH)	2.6			V	Pins XRES, XIRQ @ 8mA, push/pull mode only, SDO
I_{PU}	Internal Pull-up Current Source		10		µA	Pins XRES, XIRQ, PWGD
V_{PWRUP_L}	Digital Input Level LOW, BVDD>3V			0.5	V	Pin PWRUP
V_{PWRUP_H}	Digital Input Level HIGH, BVDD>3V	BVVD/3			V	Pin PWRUP
V_{PWRUP_H}	Digital Input Level HIGH, BVDD<=3V	1			V	Pin PWRUP
R_{PWRUP}	Internal Pull-down resistor		360		kΩ	Pin PWRUP
V_{DI_L}	Digital Input Level LOW		DVDD/2 *0.3	0.42	V	Pin HBT, SDI, SCLK, MCLK, LRCK
V_{DI_H}	Digital Input Level HIGH	1.02	DVDD/2 *0.7		V	Pin HBT, SDI, SCLK, MCLK, LRCK
I_{PD}	Internal Pull-down current source		10		µA	Pin HBT
f_{CLK}	Audio Clock Frequency	8		48	kHz	LRCK according to streamed audio data

8.1.2 Operating Currents

Table 7 Supply currents

Symbol	Parameter	Typ	Max	Unit	Note
I_{HPH}	Headphone current from BVDDH	1		mA	quiescent current, no load
$I_{DAC->HP}$	DAC playback current	6.4		mA	no load, including PMU
$I_{Line->HP}$	Line Input playback current	1.9		mA	no load, including PMU

8.1.3 Temperature Range

Table 8 Temperature Range

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{amb}	Operating temperature range	-20	25	85	°C	
T_j	Junction temperature range	0		110	°C	
R_{th}	Thermal Resistance		39		°C/W	For CTBGA81 package

8.1.4 Audio Specification

Table 9 Audio Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
DAC Input to Line Output						
FS	Full Scale Output		0.97		V_{RMS}	1kHz FS input
SNR	Signal to Noise Ratio		91		dB	A-weighted, no load, silence input
DR	Dynamic Range		88		dB	A-weighted, no load, -60dB FS 1kHz input
THD	Total Harmonic Distortion		-90		dB	1kHz FS input
SINAD	Signal to Noise and Distortion		85		dB	A-weighted, 1kHz FS input
Line Input to Line Output						
FS	Full Scale Output		0.96		V_{RMS}	1kHz 1V_{RMS} (FS) input
SNR	Signal to Noise Ratio		92		dB	A-weighted, no load, silence input
THD	Total Harmonic Distortion		-90		dB	1kHz 1V_{RMS} (FS) input
SINAD	Signal to Noise and Distortion		86		dB	A-weighted, 1kHz FS input
CS	Channel Separation		89		dB	
DAC Input to HP Output						
FS	Full Scale Output		0.895		V_{RMS}	R_L= 32Ω
			0.89		V_{RMS}	R_L= 16Ω
SNR	Signal to Noise Ratio		94		dB	A-weighted, no load, silence input
DR	Dynamic Range		90		dB	A-weighted, no load, -60dB FS 1kHz input
THD	Total Harmonic Distortion		-95		dB	no load, 1kHz FS input
			-75		dB	Pout=20mW, R_L= 32Ω, f=1kHz FS input
			-69	-60	dB	Pout=40mW, R_L= 16Ω, f=1kHz FS input
SINAD	Signal to Noise and Distortion		91		dB	A-weighted, no load, 1kHz FS input
			73		dB	A-weighted,Pout=20mW, R_L= 32Ω, f=1kHz FS input
			68		dB	A-weighted,Pout=40mW, R_L= 16Ω, f=1kHz FS input
CS	Channel Separation		74		dB	R_L = 32Ω
			68		dB	R_L = 16Ω
Line Input to HP Output						
FS	Full Scale Output		0.875		V_{RMS}	R_L= 32Ω, 1kHz 1V_{RMS}(FS) input
			0.87		V_{RMS}	R_L= 16Ω, 1kHz 1V_{RMS} (FS) input
SNR	Signal to Noise Ratio		95		dB	A-weighted, no load, silence input
DR	Dynamic Range		95		dB	A-weighted, no load, -60dB FS 1kHz (FS) input
THD	Total Harmonic Distortion		-91		dB	no load, 1kHz 1$V_{RMS\ input}$
			-75		dB	Pout=20mW, R=32Ω, 1kHz 1V_{RMS} (FS) input
			-70	-60	dB	Pout=40mW, R=16Ω, 1kHz 1V_{RMS} (FS) input
SINAD	Signal to Noise and Distortion		87		dB	A-weighted, no load, 1kHz 1$V_{RMS\ input}$

Symbol	Parameter	Min	Typ	Max	Unit	Note
			74		dB	A-weighted, Pout=20mW, R=32Ω, 1kHz $1V_{RMS}$ (FS) input
			68		dB	A-weighted, Pout=40mW, R=16Ω, 1kHz $1V_{RMS}$ (FS) input
CS	Channel Separation		75		dB	R_L = 32Ω
			70		dB	R_L = 16Ω
MIC Input to Line Output						
FS	Full Scale Output		0.97		V_{RMS}	1kHz FS input
SNR	Signal to Noise Ratio		81		dB	A-weighted, no load, silence input
DR	Dynamic Range		83		dB	A-weighted, no load, -60dB FS 1kHz input
THD	Total Harmonic Distortion		-78		dB	1kHz $27mV_{RMS}$ (-3dB FS) input
SINAD	Signal to Noise and Distortion		75		dB	A-weighted, 1kHz $27mV_{RMS}$ (-3dB FS) input
Line Input to ADC Output						
SNR	Signal to Noise Ratio		90		dB	A-weighted, no load, silence input
DR	Dynamic Range		90		dB	A-weighted, no load, -60dB FS 1kHz input
THD	Total Harmonic Distortion		-78		dB	1kHz $1V_{RMS}$ (-3dB FS) input
SINAD	Signal to Noise and Distortion		78		dB	A-weighted, 1kHz $1V_{RMS}$ (-3dB FS) input

9 Detailed Functional Description

9.1 Audio Functions

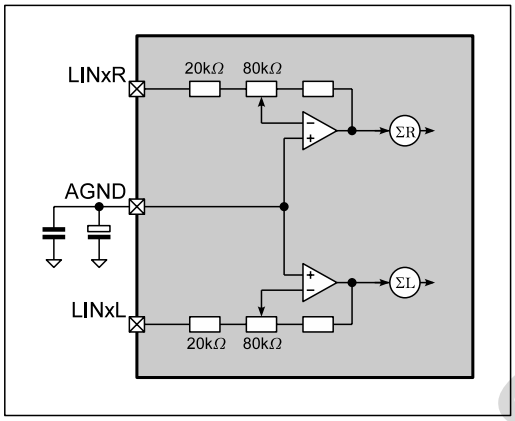
9.1.1 Audio Line Inputs (2x)

General

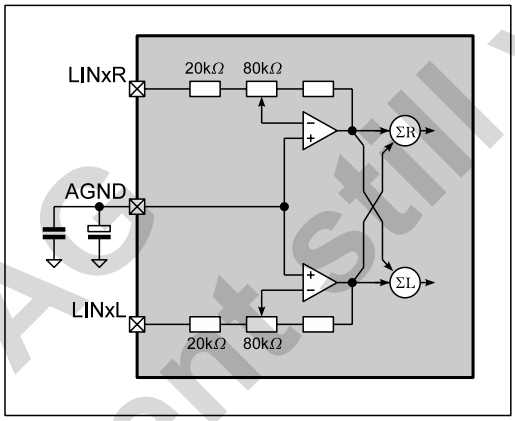
The chip features includes two identical line inputs. The blocks can work in mono differential, 2x mono single ended or in stereo single ended mode.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each and MUTE. The gain can be set from –34.5dB to +12dB. The stage is set to mute by default. If the line input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

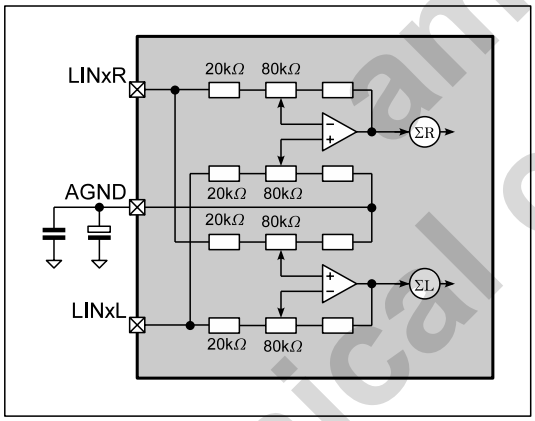
Figure 5 Line Inputs



Stereo Mode



Mono Single Ended Mode



Mono Differential Mode

Parameter

Table 10 Line Input Parameter

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{LIN}	Input Signal Level		1.0		V_{PEAK}	Pls observe gain settings. Max. peak levels at any node within the circuit shall not exceed AVDD
R_{LIN}	Input Impedance		20-100		kΩ	depending on gain setting
Δ_{RLIN}	Input Impedance Tolerance		±15		%	
C_{LIN}	Input Capacitance		5		pF	
A_{LIN}	Programmable Gain	-34.5		+12	dB	
	Gain Steps		1.5		dB	discrete logarithmic gain steps
	Gain Step Accuracy		±0.25		dB	
$A_{LINMUTE}$	Mute Attenuation		100		dB	

BVDD = 3.3V, T_A= 25°C, fs=48kHz unless otherwise mentioned

Register Description

Table 11 Line Input Related Register

Name	Base	Offset	Description
LINE_IN1_R	2-wire serial	0Ah	Right Line Input 1 settings
LINE_IN1_L	2-wire serial	0Bh	Left Line Input 1 settings
LINE_IN2_R	2-wire serial	0Ch	Right Line Input 2 settings
LINE_IN2_L	2-wire serial	0Dh	Left Line Input 2 settings
AudioSet_1	2-wire serial	14h	Enable/disable driver stage
AudioSet_3	2-wire serial	16h	Enable/disable mixer input

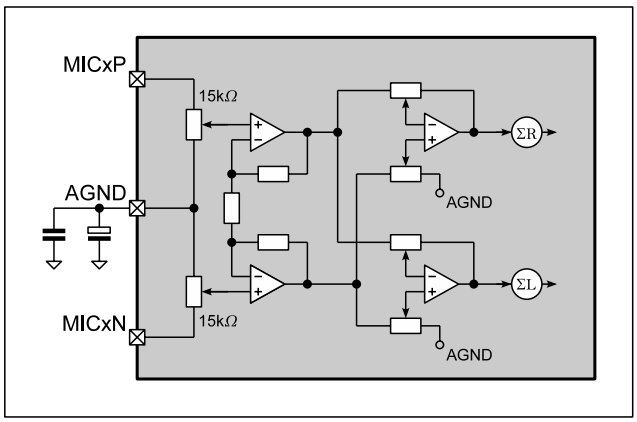
Line Inputs have to be enabled in register 14h first before other settings in register 0Ah to 0Dh can be programmed.

9.1.2 Microphone Inputs (2x)

General

The AFE offers two microphone inputs and 2 low noise microphone voltage supply (microphone bias), voice activation, microphone connect detection and push button remote control.

Figure 6 Microphone Input



Microphone Preamplifier and Gain Stage

Gain Stage & Limiter

The integrated pre-amplifier allows 3 preset gain settings. There is also a limiter which attenuates high input signals from e.g. electrete microphones signal to 1Vp. The AGC has 15 steps with a dynamic range of about 29dB. The AGC is ON by default but can be disabled by a microphone register bit.

Apart from the microphone pre-amplifier the microphone input signal can further be amplified with 32 @1.5dB programmable logarithmic gain steps and MUTE. All gains and MUTE are independently programmable. The gain can be set from –40.5dB to +6dB.

The stage is set to mute by default. If the microphone input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

Supply & Detection

Each microphone input generates a supply voltage of 1.5V above HPHCM. The supply is designed for ≤2mA and has a 10mA current limit. In OFF mode the MICS terminal is pulled to AVDD with 30kOhm. A current of typically 50uA generates an interrupt to inform the CPU, that a circuit is connected. When using HPCM as headset ground the HP–stage gives the interrupt. After enabling the HP-stage through the CPU the microphone detection interrupt will follow.

When using the MICxS terminals as ADC-10 input to monitor external voltages the 30kOhm pull-up can be disabled.

Remote Control

Fast changes of the supply current of typically 500uA are detected as a remote button press, and an interrupt is generated. Then the CPU can start the measurement of the microphone supply current with the internal 10-bit ADC to distinguish which button was pressed. As the current measurement is done via an internal resistor, only two buttons generating a current of about 0.5mA and 1mA can be detected. With this 1mA as microphone bias is still available.

Voice Activation

Further a built-in voice activation comparator can actuate an interrupt if microphone input voltage of about 5mVRMS is detected.

Parameter

Table 12 Microphone Inputs Parameter

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{MICIN}0$	Input Signal Level		40		mV_{PEAK}	A_{MICPRE} = 28dB; A_{MIC} = 0dB
$V_{MICIN}1$			20		mV_{PEAK}	A_{MICPRE} = 34dB; A_{MIC} = 0dB
$V_{MICIN}2$			10		mV_{PEAK}	A_{MICPRE} = 40dB; A_{MIC} = 0dB
R_{MICIN}	Input Impedance		15		kΩ	MICP, MICN to AGND
Δ_{MICIN}	Input Impedance Tolerance		±15		%	
C_{MICIN}	Input Capacitance		5		pF	
A_{MICPRE}	Microphone Preamplifier Gain		28 34 40		dB dB dB	Preamplifier has 3 selectable (fixed) gain settings
A_{MIC}	Programmable Gain	-40.5		+6	dB	
	Gain Steps		1.5		dB	discrete logarithmic gain steps
	Gain Step Precision		±0.25		dB	
$V_{MICLIMIT}$	Limiter Activation Level		1		V_{PEAK}	
$A_{MICLIMIT}$	Limiter Gain Overdrive		15*2		dB	
t_{ATTACK}	Limiter Attack Time		50		µs/6dB	
t_{DECAY}	Limiter Decay Time		120		ms/6dB	
$A_{MICMUTE}$	Mute Attenuation		100		dB	
V_{MICSUP}	Microphone Supply Voltage		2.9		V	
I_{MICMAX}	Max. Microphone Supply Current		10		mA	microphones nominally need a bias current of 0.5mA-1mA
V_{NOISE}	Microphone Supply Voltage Noise		5		µV	
I_{MICDET}	Microphone Detection Current		50		µA	
I_{REMDET}	Max. Remote Detection Current		500		µA	

BVDD = 3.3V, T_A= 25°C unless otherwise mentioned

Register Description

Table 13 Microphone Related Register

Name	Base	Offset	Description
MIC1_R	2-wire serial	06h	Right Microphone Input 1 volume settings, AGC control
MIC1_L	2-wire serial	07h	Left Microphone Input 1 volume settings, MIC 1 supply control
MIC2_R	2-wire serial	08h	Right Microphone Input 2 volume settings, AGC control
MIC2_L	2-wire serial	09h	Left Microphone Input 2 volume settings, MIC 2 supply control
AudioSet_1	2-wire serial	14h	Enable/disable driver stage
AudioSet_3	2-wire serial	16h	Enable/disable mixer input
IRQ_ENRD_1	2-wire serial	24h	Interrupt settings for microphone voice activation
IRQ_ENRD_3	2-wire serial	26h	Interrupt settings for microphone detection
IRQ_ENRD_4	2-wire serial	27h	Interrupt settings for remote button press detection

Microphone inputs have to be enabled in register 14h first before other settings in register 06h to 09h can be programmed.

9.1.3 Audio Line Outputs (2x)

General

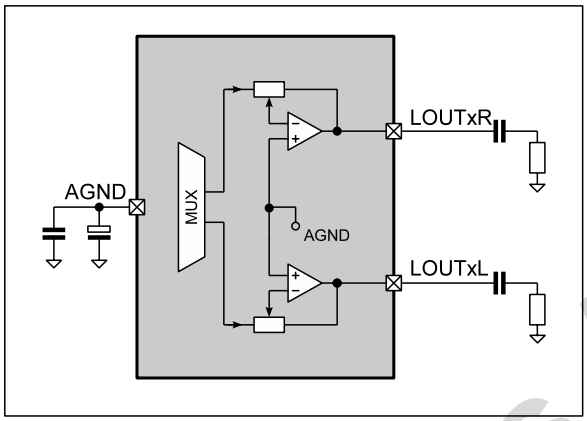
The line outputs are designed to provide the audio signal with typical $1V_{PEAK}$ at a load of minimum 10kΩ, which is a minimum value for line inputs. If the limiters (N20/N21) are deactivated the peak output voltage is $1.45V_{PEAK}$. The load however can decrease to 64Ohm. In addition these line output can be configured as mono differential to drive $1V_{PEAK}$ @ 32Ω load (e.g. an earpiece of a mobile phone).

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -40.5dB to +6dB. A zero cross detection allows to control the actual execution of new gain settings.

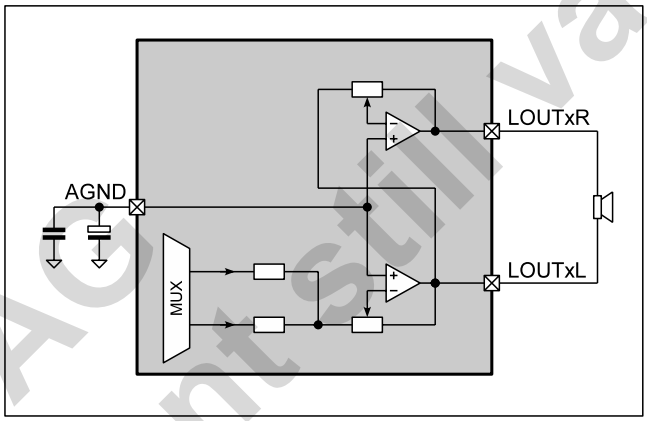
If the line output is not enabled, the volume settings are set to their default values. Changing of volume and mute control can only be done after enabling the output.

If using the output in mono differential mode, the volume setting for the right channel should be set to 0dB.

Figure 7 Line Output



Stereo Mode



Mono Differential Mode (please observe that gain of right channel amplifier has to best to 0dB)

Parameter

Table 14 Line Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
R_{L_LO}	Load Impedance (Stereo Mode)	64			Ω	line inputs nominally have 10kΩ
C_{L_LO}	Load Capacitance (Stereo Mode)			100	pF	
A_{LO}	Programmable Gain	-40.5		+6	dB	
	Gain Steps		1.5		dB	discrete logarithmic gain steps
	Gain Step Accuracy		±0.25		dB	
A_{LOMUTE}	Mute Attenuation		100		dB	

BVDD = 3.3V, T_A= 25ºC unless otherwise mentioned

Register Description

Table 15 Line Output Related Register

Name	Base	Offset	Description
LINE_OUT1_R	2-wire serial	00h	Right Line Output 1 volume settings, MUX control
LINE_OUT1_L	2-wire serial	01h	Left Line Output 1 volume settings
LINE_OUT2_R	2-wire serial	04h	Right Line Output 2 volume settings, MUX control
LINE_OUT2_L	2-wire serial	05h	Left Line Output 2 volume settings
AudioSet_1	2-wire serial	14h	Enable/disable driver stage
AudioSet_3	2-wire serial	16h	Enable/disable mixer input

Line output have to be enabled in register 14h first before other settings in register 00h and 01h can be programmed.

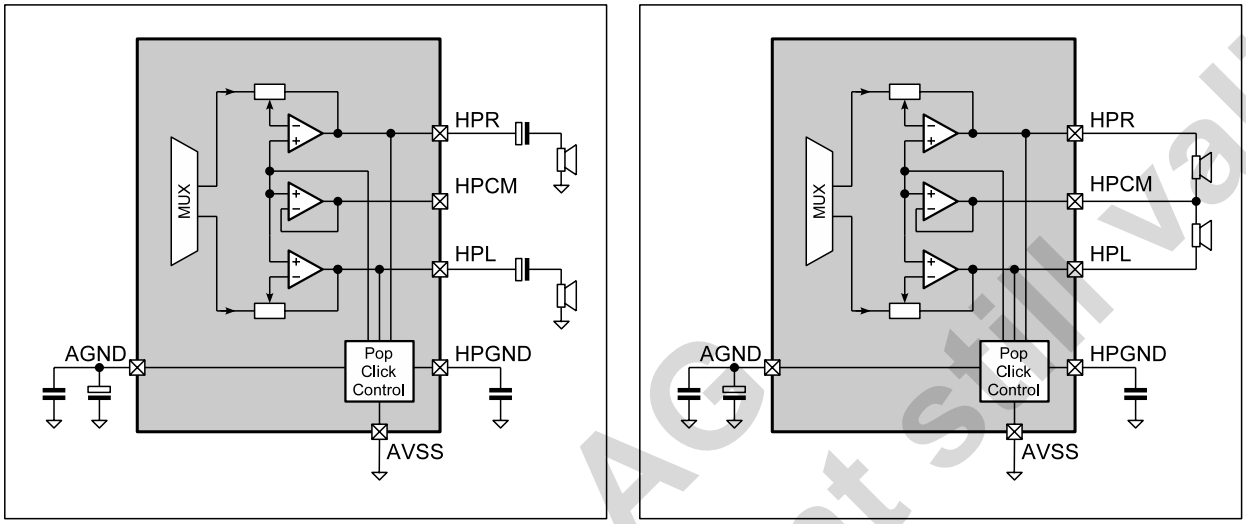
9.1.4 Headphone Output

General

The headphone output is designed to provide the audio signal with 2x40mW @ 16Ω or 2x20mW @32Ω, which are typical values for headphones. If the limiters (N20/N21) are disabled a maximum output of 2x60mW@16Ω or 2x30mW@32Ω can be achieved.

This output stage has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –43.43dB to +1.07dB. A zero cross detection allows to control the actual execution of new gain settings.

Figure 8 Headphone Output



Headphones connected via decoupling capacitors

Headphones connected to Phantom Ground (Common Mode)

Phantom Ground

There are 2 ways to connect a headphone to the AFE. In order to spare the bulky ac/dc decoupling capacitors at pins HPR/HPL a buffered ground (Phantom Ground) is provided. This Common Mode Buffer needs to be switched on if utilized. If form factor considerations are less stringent, the headphones can be conventionally connected via 2x100µF capacitors.

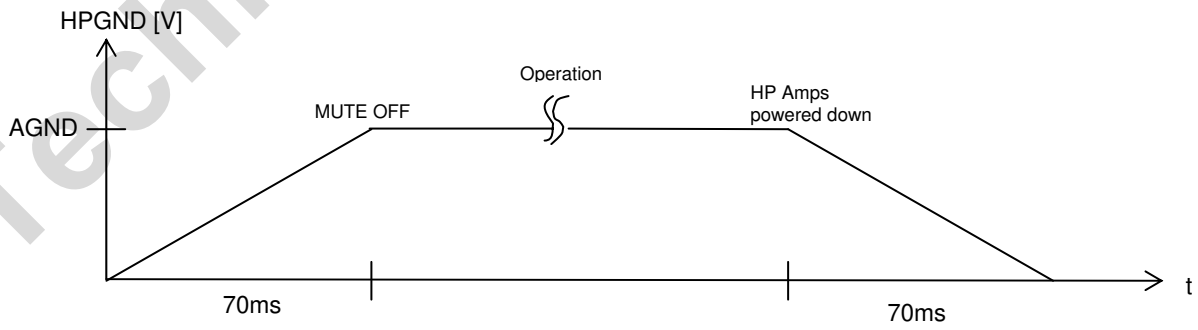
No-Pop Function

The output is automatically set to mute when the output stage is disabled.

To avoid Pop-Click noise during power-up and shut-down of the headphone amplifier, a charge/discharge control of HPGND (0V-1.45V-0V) at pins HPR/HPL is incorporated into the AFE. The 100nF capacitor at pin HPGND is used to form the charge/discharge slope. Pls observe that pin HPGND is a high impedance node which must not be connected to any other external device than the 100nF buffer capacitor. To avoid Pop-Click noise one has to wait for 150ms in between a power-down (switch-off) and a power-up (switch-on) of the headphone amplifier.

The output is automatically set to mute when the output stage is disabled.

Figure 9 HP POP-Click Suppression



Over-current Protection

The headphone amplifier has an over-current protection (e.g. HPR/HPL is shorted). This over-current protection will power the headphone amplifier down for a programmable timeout period (512ms, 256ms, 128ms). The current threshold is at 150mA for HPR/HPL and 300mA for HPCM. There is a corresponding interrupt available to be enabled.

Headphone Detection

When the headphone amplifier is powered down, one can detect the connection of a headset. It only work if the headset is connected between pins HPR/HPL and HPCM. As long as the headphone amplifier is powered down, HPCM is biased to 150mV and acting as the sense pin. There is a corresponding interrupt available to be enabled.

Power Save Options

To save power, especially when driving 32 Ohm loads, a reduction of the bias current can be selected. Together with switching off the phantom ground this gives 4 possible operating modes.

Table 16 Headphone Power-Save Options

HPCM_OFF	IBR_HPH	IDD_HPH (typ.)	Load
0	0	2.2mA	16 Ohm
1	0	1.5mA	16 Ohm
0	1	1.5mA	32 Ohm
1	1	1.0mA	32 Ohm

BVDD = 3.3V, T_A= 25ºC unless otherwise mentioned

Parameter

Table 17 Power Amplifier Block Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
R_{L_HP}	Load Impedance	16			Ω	stereo mode
C_{L_LO}	Load Capacitance			100	pF	stereo mode
P_{HP}	Nominal Output Power		40mW 20mW			RL=16Ω, limiter enabled RL=32Ω, limiter enabled
P_{HP_MAX}	Max. Output Power		60mW 30mW			RL=16Ω RL=32Ω
A_{LO}	Programmable Gain	-45.5		+1	dB	
	Gain Steps		1.5		dB	discrete logarithmic gain steps
	Gain Step Accuracy		±0.25		dB	
	Over current limit		150 300		mA mA	HPR/HPL pins HPCM pin
P_{SRRHP}	Power Supply Rejection Ratio		90		dB	200Hz-20kHz, 720mVpp, RL=16Ω
A_{LOMUTE}	Mute Attenuation		100		dB	

BVDD = 3.3V, T_A= 25ºC unless otherwise mentioned

Register Description

Table 18 Headphone Related Register

Name	Base	Offset	Description
HPH_OUT_R	2-wire serial	02h	Right HP Output volume and over-current settings
HPH_OUT_L	2-wire serial	03h	Left HP Output volume settings, enable and detection control
AudioSet_3	2-wire serial	16h	Power save options, common mode buffer
IRQ_ENRD_3	2-wire serial	26h	Interrupt settings for over current and HP detection

9.1.5 DAC, ADC and I2S Digital Audio Interface

Input

The AFE receives serialized audio data for the DAC via pin SDI. The output of the DAC is fed through a volume control to the mixer stage and to the multiplexers of line output and headphone amplifiers.

This serialized audio data is a digital audio data stream with the left and the right audio channels multiplexed into one bit-stream. Via pin LRCLK the alignment clock is input to the DAC digital filters. LRCLK (Left Right Clock) indicates whether the serial bit-stream received via pin SDI, represents right channel or left channel audio data. Via pin SCLK the bit clock for the serial bit-stream is signalled. SDI and LRCLK are synchronous with SCLK. SDI is an inputs; LRCLK and SCLK are either inputs or outputs depending on the master/slave operation mode. SDO is not used.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB. The stage is set to mute by default. If the DAC input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

Output

This block consists of an audio multiplexer where the signal, which should be recorded, can be selected. The output is then fed through a volume control to the 20 bit ADC. The digital output is done via an I2S interface.

The AFE sends serialized audio data from the ADC via pin SDO. This serialized audio data is a digital audio data stream with the left and the right audio channels multiplexed into one bit-stream. Via pin LRCLK the alignment clock is signalled to the connected devices (e.g. CPU). LRCLK (Left Right Clock) indicates whether the serial bit-stream sent via pin SDI, presents right channel or left channel audio data. Via pin SCLK the bit clock for the serial bit-stream is signalled. SDO and LRCLK are synchronous with SCLK. SDO is an output; LRCLK and SCLK are either inputs or outputs depending on the master/slave operation mode. SDI is not used.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –34.5dB to +12dB. The stage is set to mute by default. If the ADC output is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

The I2S output uses the same clocks as the I2S input. The sampling rate therefore depends also on the input sampling rate.

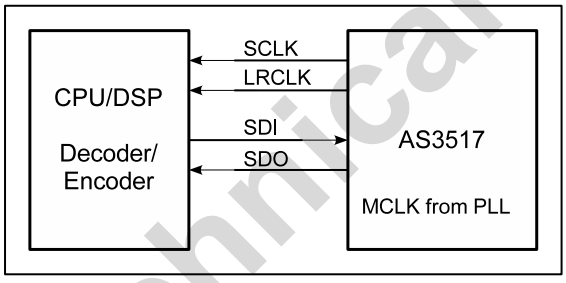
I2S Modes

The AFE can be operated either in Master Mode, Slave Mode or additionally in Slave Mode with the master clock directly signalled via pin PWGD (pin PWGD is multiplexed for I2S Direct Mode). The difference between Master and Slave Mode is whether the AFE or the externally attached decoder/encoder device is generating the interface clocks. The master clock (MCLK) is the necessary internal over-sampling clock for the DAC and ADC (e.g. 256*fs, fs=audio sampling frequency).

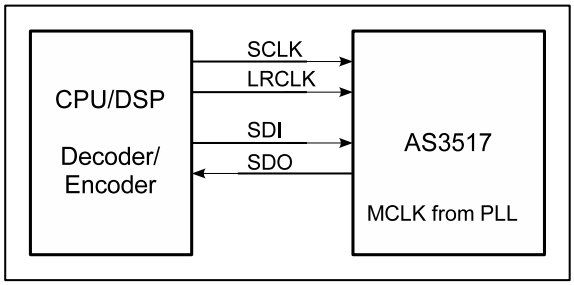
Due to the internal structure left and right audio samples are exchanged in I2S Direct Mode.

In Slave Mode the PLL generates the master clock based on LRCLK. Thus the PLL needs to be preset to the expected sampling frequency. The ranges are 8kS-12kS (8kHz-12kHz) and 16kS-48kS (16kHz-48kHz). Please refer to register 0x1Dh.

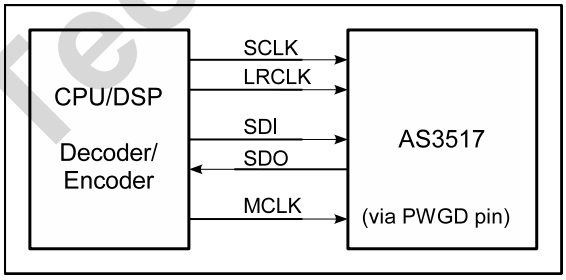
Table 19 I2S Modes



Master Mode



Slave Mode, internal PLL of the AFE generates MCLK



Slave Mode with I2S direct, the master clock is signalled

via pin PWGD

Power Save Options

The bias current of the DAC block can be reduced in three steps down to 50% to reduce the power consumption.

Clock Supervision

The digital audio interface automatically checks the LRCLK. An interrupt can be generated when the state of the LRCLK input changes. A bit in the interrupt register represents the actual state (present or not present) of the LRCLK.

Signal Description

The digital audio interface uses the standard I2S format:

- left justified
- MSB first
- one additional leading bit

The first 18 bits are taken for DAC conversion. The on-chip synchronization circuit allows any bit-count up 32bit. When there are less than 18 bits sampled, the data sample is completed with "0"s. In I2S direct mode the data length has to be minimum 18 bits.

The ADC output is always 20 bit. If more SCLK pulses are provided, only the first 20 will be significant. All following bits will be "0".

SCLK has not to be necessarily synchronous to LRCLK but the high going edge has to be separate from LRCLK edges. The LRCK signal has to be derived from a jitter-free clock source, because the on-chip PLL is generating a clock for the digital filter, which has to be always in correct phase lock condition to the external LRCLK.

Please observe that in slave mode LRCLK has to be activated before enabling the ADC.

In Master Mode operation SCLK has 32 clock cycles for each sample word.

$$SCLK = \frac{MCLK}{4} = \frac{LRCLK * 256}{4} = LRCK * 64$$

Sample Rates

In Master Mode AS3517 allows programming various sample rates. The master clock is generated by the 12-24MHz oscillator. Sampling frequencies from 8kHz to 48kHz can be selected. For certain division ratios between master clock and sample ratio a certain deviation is system inherent.

$$LRCLK = f_{osc} * \frac{1}{(PLLMode + 1) * 2} * \frac{1}{RD + 2}$$

f_{osc} ..... *Quarzoscillator frequency*

$PLLMode$ ..... *PLL factor* (1,2)

RD ..... *RateDivider* $(0 - 511)$