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AS3542

Data Sheet, Strictly Confidential

Ultra Low Power Stereo Audio Codec with System PMU

1 General Description

The AS3542 is an ultra low power stereo audio codec and is designed for Portable Digital Audio Applications.

It allows CD quality playback with up to 96dBA SNR and recording in FM quality. With one microphone (including pre-amplifier and supply for an electret microphone) and one line input, it allows connecting a variety of audio inputs. The different audio signals can be mixed via a 6-channel mixer and fed to either a headphone output for 16 /32 headsets or a line output. The audio outputs have also an auto fading implemented which performs the fade-in, fade-out as well as the transition between specific volume levels automatically with an selectable timing.

Further the device offers advanced power management functions. All necessary ICs and peripherals in a Digital Audio Player are supplied by the AS3542. It features 2 DCDC converters for core and memory/periphery supply as well as 4 LDOs. Both DCDC converter feature DVM (dynamic voltage management) with an selectable timing for the voltage stepping. The different regulated supply voltages are programmable via the serial control interface.

The step-up converter for the backlight can operate up to 15V (with an external transistor even higher) in voltage and current control mode. An internal voltage protection is limiting the output voltage in the case of external component failures. An automatic dimming function allows a logarithmic on/off of the backlight with selectable timing.

AS3542 also contains a Li-Ion battery charger with constant current, constant voltage and trickle charging. The maximum charging current is 460mA. An integrated battery switch is separating the battery during charging or whenever an external power supply is present. With this switch it is also possible to operate with no or deeply discharged batteries.

The AS3542 has an on-chip, phase locked loop (PLL) which generates the needed internal CODEC master clock. I2S Frame and shift-clock have to be applied from the processor for playback and recording.

The single supply voltage may vary from 2.7V to 5.5V.

2 Key Features

Audio

Audio power consumption:

- - 5mW: 95dB DAC to Headphone @ 1.8V, 32Ω

Sigma Delta Converters

- DAC
  - 96dB SNR ('A' weighted) @ 1.8V
- ADC
  - 85dB SNR ('A' weighted) @ 1.8V
- Sampling Frequency
  - DAC: 8-48kHz
  - ADC: 8-24kHz

High Efficiency Headphone Amplifier

- volume control via serial interface
- 32 steps @1.5dB and MUTE
- 2x12mW @16Ω driver capability@ 1.8V supply
- THD -74dB @16Ω; 1.8V
- 2x40mW @16Ω driver capability@ 2.9V supply
- THD -77dB @16Ω; 2.9V
- headphone and over-current detection

Line Output

- volume control via serial interface
- 32 steps @1.5dB and MUTE
- 0.6Vp @10kΩ

Microphone Input

- 3 gain pre-setting (30dB/36dB/42dB) and AGC
- 32 gain steps @1.5dB and MUTE
- supply for electret microphone
- microphone detection
- remote control by switch

Line Input

- volume control via serial interface
- 32 steps @1.5dB and MUTE
- stereo or 2x mono

Audio Mixer

- 6 channel input/output mixer with AGC
- mixes line input and microphone with DAC
- left and right channels independent

Power Management

Voltage Generation

- step down for CPU core (0.61V-3.35V, 250mA)
- step down for peripheral (0.61V-3.35V, 250mA)
- LDO1 for AFE supply (1.7V (1.65-3.2V), 50mA)
- LDO2 for AFE supply (2.7V (2.3-3.5V), 200mA)
- LDO3 for peripherals (1.2V-3.5V, 100mA)
- LDO4 for peripherals (1.2V-3.5V, 100mA)
- separate input for LDO3
- power supply supervision & hibernation modes
- 5sec and 10sec emergency shut-down

Backlight Driver

- step up for backlight (15V)
- current control mode (1.2-36mA)
- voltage control mode
- 1 HV current sink
- automatic dimming
- over-voltage protection

Battery Charger

- automatic trickle charge (55mA)
- prog. constant current charging (55-460mA)
- prog. constant voltage charging (3.9V-4.25V)
- current limitation for USB mode
- integrated battery switch

General

Supervisor

- automatic battery monitoring with interrupt generation and selectable warning level
- automatic temperature monitoring with interrupt generation and selectable warning and shutdown levels

General Purpose ADC

- 10bit resolution
- 19 inputs analog multiplexer

Interfaces

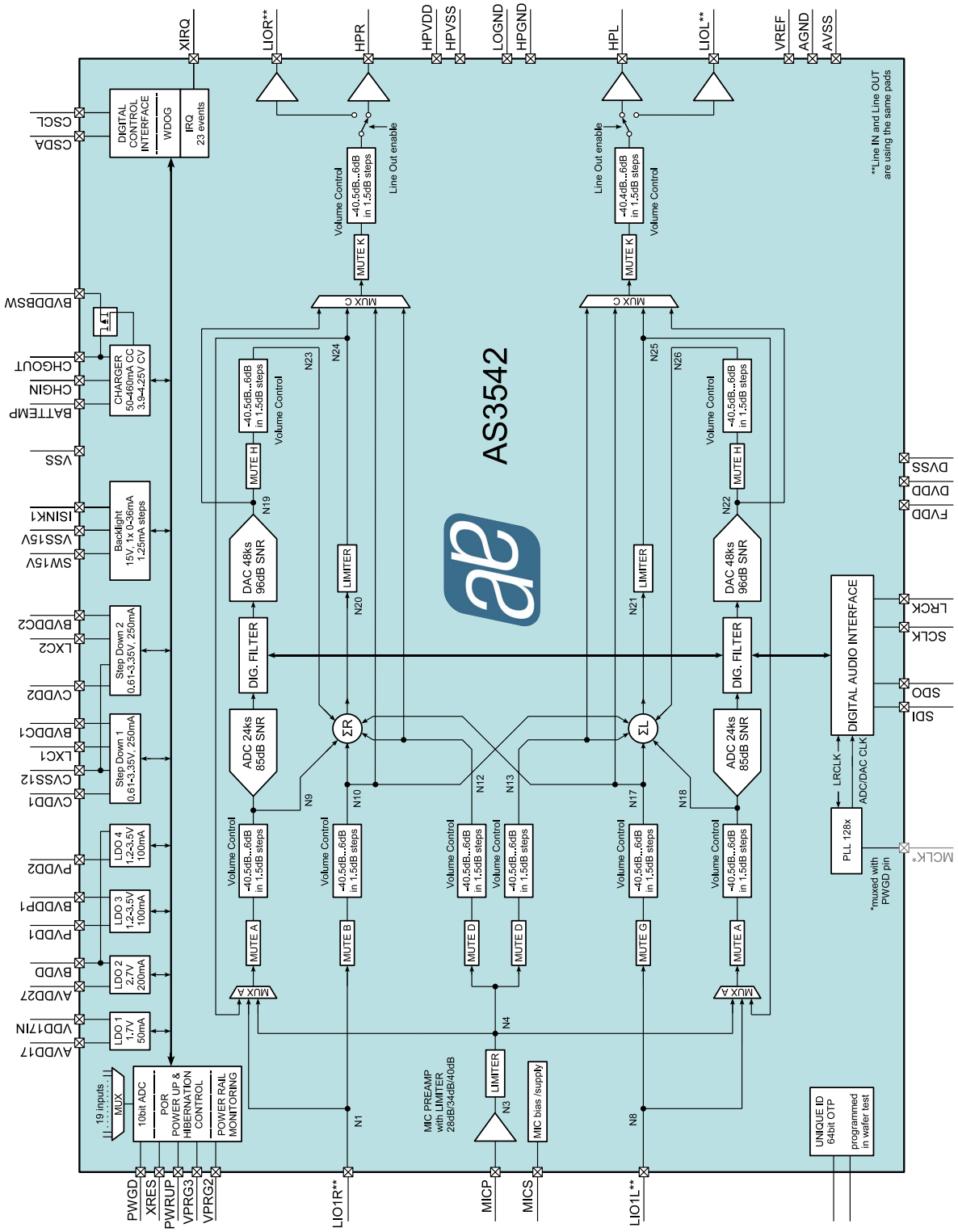
- 2 wire serial control interface
- reset pin with selectable delay, power good pin
- 64bit unique ID (OTP)
- 25 different interrupts
- Package MLF2 56 [7.0x7.0x0.85mm] 0.4mm pitch

3 Applications

Portable Digital Audio/Video Player and Recorder

PDA, Smartphone

Figure 1. Block Diagram



Contents

Revision History

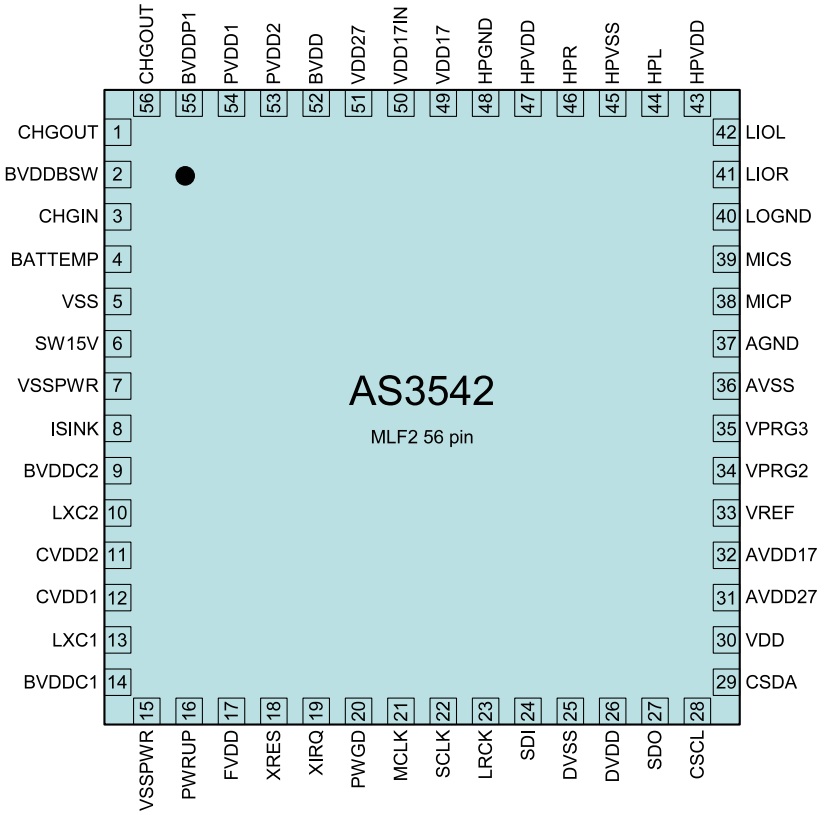
Table 1. Revision History

Revision	Date	Owner	Description
1.00	17.4.2009	pkm	official release
1.10	26.5.2009	pkm	added audio characterisation data

4 Pinout

4.1 Pin Assignment

Figure 2. Pin Assignments (Top View)



4.2 Pin Description

Table 2. Pin Description for AS3542

Pin Number	Pin Name	Type	Description
1	CHGOUT	SUP IO	Li-Ion Charger Output
2	BVDDBSW	SUP IO	Battery Switch output to be connected against BVDD
3	CHGIN	SUP IN	Li-Ion Charger Input
4	BATTEMP	ANA IO	Li-Ion Charger Battery Temp. Sensor Input
5	VSS	GND	Power Management Neg. Reference Supply
6	SW15V	DIG OUT	DCDC15V Switch Output to Coil
7	VSSPWR	GND	Power Management Neg. Supply Terminal
8	ISINK	ANA IO	DCDC15V Load Current Sink Terminal
9	BVDDC2	SUP IN	CVDD2 Step Down Pos. Supply Terminal
10	LXC2	DIG OUT	CVDD2 Step Down Switch Output to Coil
11	CVDD2	ANA IN	CVDD2 and Feedback Pin
12	CVDD1	ANA IN	CVDD1 and Feedback Pin
13	LXC1	DIG OUT	CVDD1 Step Down Switch Output to Coil
14	BVDDC1	SUP IN	CVDD1 Step Down Pos. Supply Terminal

Table 2. Pin Description for AS3542

Pin Number	Pin Name	Type	Description
15	VSSPWR	GND	Power Management Neg. Supply Terminal
16	PWRUP	DIG IN	Power Up Input
17	FVDD	SUP IN	Digital Pos. Supply (e.g. DAC, …)
18	XRES	DIG OUT	Reset Output
19	XIRQ	DIG OUT	Interrupt Request Output
20	PWGD	DIG IO	PowerUp Sequence Complete Output
21	MCLK	DIG IN	MCLK input
22	SCLK	DIG IN	I2S Shift Clock Input
23	LRCK	DIG IN	I2S Frame Clock Input
24	SDI	DIG IN	I2S Data Input to DAC
25	DVSS	GND	Digital Circuit Neg. Supply Terminal
26	DVDD	SUP IN	Digital Periphery Pos. Supply
27	SDO	DIG OUT	I2S Data Output from ADC
28	CSCL	DIG IN	2 wire SERIF Clock Input
29	CSDA	DIG IO	2 wire SERIF Data I/O
30	VDD	ANA IO	LDO output, supply input
31	AVDD27	SUP IN	Analog Pos. Supply
32	AVDD17	SUP IN	Audio Pos. Supply
33	VREF	ANA IO	DAC Reference Pin
34	VPRG2	ANA IN	Memory Supply Voltage Definition Pin
35	VPRG3	ANA IN	PowerUp Sequence Definition Pin
36	AVSS	GND	Ground (analog)
37	AGND	ANA IO	Analog Common Mode Voltage Pin
38	MICP	ANA IN	Microphone Input
39	MICS	ANA IO	Microphone Supply Output / Remote Control input
40	LOGND	ANA IO	Line Output Common Mode Voltage Pin
41	LIOR	ANA IO	Analog Line Input 1 Right Channel
42	LIOL	ANA IO	Analog Line Input 1 Right Channel
43	HPVDD	SUP IN	Headphone Supply default 1.8V (max. 3.6V)
44	HPL	ANA OUT	Headphone Output Left Channel
45	HPVSS	GND	Headphone Ground
46	HPR	ANA OUT	Headphone Output Right Channel
47	HPVDD	SUP IN	Headphone Supply default 1.8V (max. 3.6V)
48	HPGND	ANA IO	Headphone Common Mode Voltage Pin
49	VDD17	SUP IO	LDO1 Output default 1.7V
50	VDD17IN	SUP IN	LDO1 Pos. Supply Terminal
51	VDD27	SUP IO	LDO2 Output default 2.7V
52	BVDD	SUP IN	Main Battery Supply Input (2.7-5.5V)

Table 2. Pin Description for AS3542

Pin Number	Pin Name	Type	Description
53	PVDD2	ANA OUT	LDO4 Output (PVDD2)
54	PVDD1	ANA OUT	LDO3 Output (PVDD1)
55	BVDDP1	SUP IN	LDO3 Pos. Supply Terminal
56	CHGOUT	SUP IO	Li-Ion Charger Output (battery switch input)

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 11 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
5V pins	-0.5	7.0	V	Applicable for pins BVDD, BVDDC1, BVDDC2, BVDDP1, BVDDBSW, CHGIN, CHGOUT, VBUS, CSCL, CSDA, PWRUP
3V pins	-0.5	5.0	V	Applicable for pins DVDD, HPVDD, FVDD, VDD17IN, VDD, VPRG2, VPRG3
15V pins	-0.5	17	V	Applicable for pin SW15V, ISINK
Voltage difference at VSS terminals	-0.5	0.5	V	Applicable for pins VSS, VSS15V, CVSS12, HPVSS, AVSS, DVSS
3.3V pins with protection to AVDD27	-0.5	5.0 AVDD27	V	Applicable for pins BATTEMP, HPGND
3.3V pins with protection to DVDD	-0.5	5.0 DVDD+0.5	V	Applicable for pins MCLK, LRCK, SCLK, SDI, SDO, XIRQ, XRES, PWGD
3.3V pins with protection to AVDD17	-0.5	5.0 AVDD17+0.5	V	Applicable for pins LIOL/R, LOGND, VREF, AGND, MICP,MICS
3.3V pins with protection to HPVDD	-0.5	5.0 HPVDD+0.5	V	Applicable for pins HPCM, HPR/L
voltage regulator pins with protection to BVDD	-0.5	5.0 BVDD+0.5	V	Applicable for pins AVDD27, PVDD1/2, CVDD1, LXC1, CVDD2, LXC2
voltage regulator pins with protection to AVDD17IN	-0.5	5.0 AVDD17IN +0.5	V	Applicable for pins AVDD17
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 17
Continuous Power Dissipation (T_A = +70ºC)				
Continuous power dissipation		600	mW	P_T[1] for MLF56 package
Electrostatic Discharge				
Electrostatic Discharge HBM		+/-1	kV	Norm: JEDEC JESD22-A114C
Temperature Ranges and Storage Conditions				
Operating Temperature Range	-20	+85	ºC	
Junction Temperature		+110	ºC	
Storage Temperature Range	-50	+125	ºC	
Humidity non-condensing	5	85	%	

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Bump Temperature (soldering)				
Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only
Moisture Sensitive Level	3		1	Represents a max. floor live time of 168h

1. Depending on actual PCB layout and PCB used

6 Electrical Characteristics

BVDD=+2.7V...+5.5V, T_A =-20ºC...+85ºC. Typical values are at BVDD=+3.6V, T_A=+25ºC, unless otherwise specified.

Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Voltages						
BVDDx	Battery Supply Voltage BVDD, BVDDBSW, BVDDC1, BVDDC2, BVDDP1		2.7	3.6	5.5	V
VBUS	USB VBUS Voltage			5.0	5.5	V
CHGIN	Charger Supply Voltage		4.5		5.5	V
HPVDD	HP Supply Voltage		1.8		3.6	V
DVDD	Digital Periphery Supply Voltage		1.8	2.9	3.6	V
VDD17IN	LDO1 Input Voltage		1.8		3.6	V
FVDD	Digital Supply Voltage		1.75	1.8	2.0	V
AVDD27	Analogue Supply Voltage		2.6	2.7	3.5	V
AVDD17	Analogue Supply Voltage		1.7	1.7	3.5	V
AGND	Analog Ground Voltage	Internally generated		AVDD17 /2		V
V_{DELTA-}	Difference of Negative Supplies CVSS12, VSS15V, HPVSS, AVSS, DVSS, VSS	To achieve good performance, the negative supply terminals should be connected to low impedance ground plane.	-0.1		0.1	V
V_{DELTA+}	Difference of Positive Supplies	RVDD-AVDD27; AVDD17-AVDD27; FVDD-AVDD27			0	V
		HPVDD-AVDD27			0.3	V
		AVDD27-BVDD			0.1	V
POR & Watchdog						
V_{POR_ON}	Power-on Reset Activation Level	Power-on Reset activation level when DVDD decreases		2.15		V
V_{POR_OFF}	Power-on Reset Release Level	Power-on Reset release when DVDD increases		2.0		V
V_{POR_HY}	Power-on Hysteresis			100		mV
f_{LRCLK_WD}	LRCLK Watchdog		2	4.1	8	kHz
PWRUP						
t_{ON_DELAY}	Delay Time of pin PWRUP	Minimum key press time		30		ms
V_{PWRUP_L}	Input Level LOW,	Pin PWRUP, BVDD>3V			0.5	V
V_{PWRUP_H}	Input Level HIGH	Pin PWRUP, BVDD>3V	BVDD/ 3			V
		Pin PWRUP, BVDD<=3V	1			V
I_{PWRUP}	Internal Pull-down Current Source	Pin PWRUP; @2.9V	2.5	7	19	uA

Table 4. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Digital Inputs/Outputs						
V_{DO_DL}	Digital Output Driver Capability (drive LOW)	Pins XRES, XIRQ, PWGD @ 6mA, push/pull mode only, SDO			10% DVDD	V
V_{DO_DH}	Digital Output Driver Capability (drive HIGH)	Pins XRES, XIRQ PWGD @ 6mA, push/pull mode only, SDO	90% DVDD			V
I_{PU}	Internal Pull-up Current Source	Pins XRES, XIRQ, PWGD; @ 0V		10		µA
V_{DI_L}	Digital Input Level LOW	Pin SDI, SCLK, MCLK, LRCK		30% DVDD		V
V_{DI_H}	Digital Input Level HIGH	Pin SDI, SCLK, MCLK, LRCK		70% DVDD		V
f_{CLK}	Audio Clock Frequency	LRCK according to streamed audio data	8		48	kHz
Power Requirements						
I_{REF}	Reference supply current	all regulators off, only LDO2 on		210		uA
I_{BIAS}	Audio Bias current			32		uA
I_{SUM}	Summing stage current			174		uA
I_{LIN}	Line input stage current	no signal		146		uA
I_{MIC}	Mic input stage current	no signal		643		uA
I_{MICS}	Mic Supply stage current	no load		201		uA
I_{LOUT}	Line output stage current	no load		436		uA
I_{DAC_GS}	DAC gain stage current	no signal		214		uA
I_{ADC_GS}	ADC gain stage current	no signal		1,36		mA
I_{HPH}	Headphone stage current	1.8V, no load		0,95		mA
		1.8V, Bias on, no load		1,21		
		1.8V, CM buffer on, no load		1,37		
		1.8V, Bias on, CM buffer on, no load		1,77		
		1.8V, HQ on		1,24		
I_{DAC}	DAC supply current	LRCK=48kHz		1,48		mA
		LRCK=44.1kHz		1,41		
		LRCK=32kHz		1,19		
		LRCK=16kHz		0,91		
		LRCK=8kHz		0,76		
I_{ADC}	ADC supply current	LRCK=24kHz		1,7		mA
		LRCK=22.05kHz		1,69		
		LRCK=16kHz		1,64		
		LRCK=8kHz		1,58		
		LRCK=4kHz		1,55		
I_{RTC}	RTC supply current			600		nA

6.1 Audio Specification

BVDD=+3.6V, VDD27=+2.7V, HPVDD=FVDD=1.8V, VDD17=+1.7V, f_S=48kHz, T_A=+25ºC, unless otherwise specified.

Table 5. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DAC Input to Line Output						
FS	Full Scale Output	R_L= 10kΩ, f=1kHz, 1V_{RMS} input		0,568		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		96		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS, f=1kHz		95		dB
THD	Total Harmonic Distortion	1kHz -1dB FS input, R_L=10kΩ		-90		dB
CS	Channel Separation	R_L=10kΩ		62		dB
Line Input to Line Output						
FS	Full Scale Output	R_L= 10kΩ, f=1kHz, 545mV_{RMS} input		0,545		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		97		dB
THD	Total Harmonic Distortion	1kHz 1V_{RMS} (-1dB FS) input, R_L=10kΩ		-81		dB
CS	Channel Separation	R_L=10kΩ		100		dB
DAC Input to HP Output						
FS	Full Scale Output	R_L=32Ω		0,560		V_{RMS}
		R_L=16Ω		0,550		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		97		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS, f=1kHz		94		dB
THD	Total Harmonic Distortion	no load, f=1kHz, FS input		-87		dB
		P_{OUT}=6mW, R_L=32Ω, f=1kHz, -1dB FS		-81		dB
		P_{OUT}=12mW, R_L=16Ω, f=1kHz, -1dB FS		-78	-60	dB
CS	Channel Separation	R_L=32Ω		63		dB
		R_L= 16Ω		60		dB
Line Input to HP Output						
FS	Full Scale Output	R_L= 32Ω, f=1kHz, 545mV_{RMS}(FS) input		0,450		V_{RMS}
		R_L= 16Ω, f=1kHz, 545mV_{RMS}(FS) input		0,447		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		97		dB
THD	Total Harmonic Distortion	no load, f=1kHz, 545mV_{RMS}		-77		dB
		P_{OUT}=6mW, R_L=32Ω, f=1kHz, 545mV_{RMS}		-75		dB
		P_{OUT}=12mW, R_L=16Ω, f=1kHz, 545mV_{RMS}		-75	-60	dB
CS	Channel Separation	R_L = 32Ω		77		dB
		R_L = 16Ω		66		dB
Mic Input to Line Output						
FS	Full Scale Output	f=1kHz, 27mV_{RMS} FS input		0,512		V_{RMS}
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		75		dB
THD	Total Harmonic Distortion	1kHz 27mV_{RMS} FS input		77		dB
Mic Input to ADC Output						
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		80		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS, f=1kHz		77		dB
THD	Total Harmonic Distortion	1kHz 27mVV_{RMS} FS input		-64		dB

7 Typical Operating Characteristics

BVDD = +3.6V, T_A = +25ºC, unless otherwise specified.

8 Detailed Description - Audio Functions

8.1 Audio Line Input

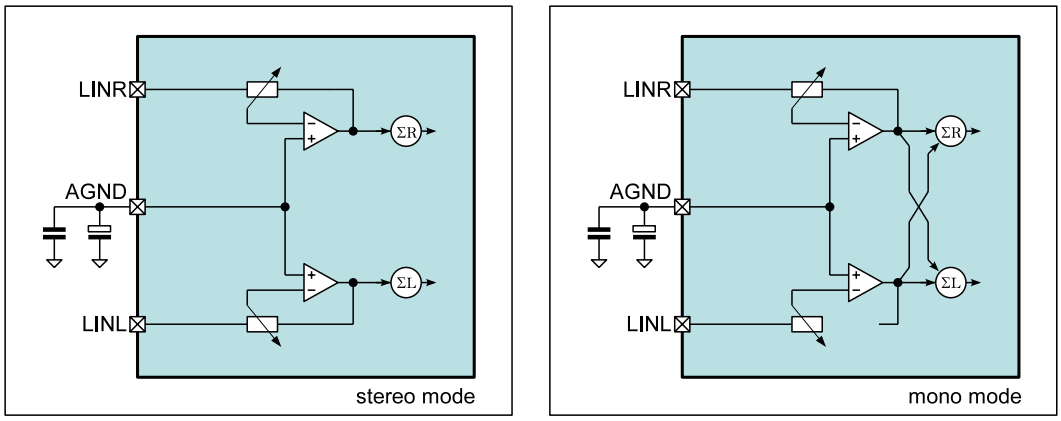
8.1.1 General

The chip features two identical line inputs. The blocks can work in 2x mono single ended or in stereo single ended mode.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each and MUTE. The gain can be set from –40.5dB to +6dB. The stage is set to mute by default. If the line input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

Line Input and Line Output are sharing the same pins. Please make sure to disable the line out discharge resistors when using line input (LO_DISCHG_OFF in reg. 0Bh).

Figure 3. Line Inputs



8.1.2 Parameter

AVDD17=1.7V, AVDD27=2.7V, T_A= 25°C, unless otherwise mentioned

Table 6. Line Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{LIN}	Input Signal Level	Pls observe gain settings. Max. peak levels at any node within the circuit shall not exceed AVDD		AVDD17 /3	AVDD17 /2	V_{PEAK}
R_{LIN}	Input Impedance	depending on gain setting		8-25		kΩ
Δ_{RLIN}	Input Impedance Tolerance			±30		%
C_{LIN}	Input Capacitance			5		pF
A_{LIN}	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Accuracy			±0.25		dB
$A_{LINMUTE}$	Mute Attenuation			100		dB

8.1.3 Register Description

Table 7. Line Input Related Register

Name	Base	Offset	Description
LINE_IN_R	2-wire serial	0Ah	Right Line Input settings
LINE_IN_L	2-wire serial	0Bh	Left Line Input settings
AudioSet1	2-wire serial	14h	Enable/disable driver stage
AudioSet3	2-wire serial	16h	Enable/disable mixer input

Line input has to be enabled in register 14h first before other settings in register 0Ah and 0Bh can be programmed.

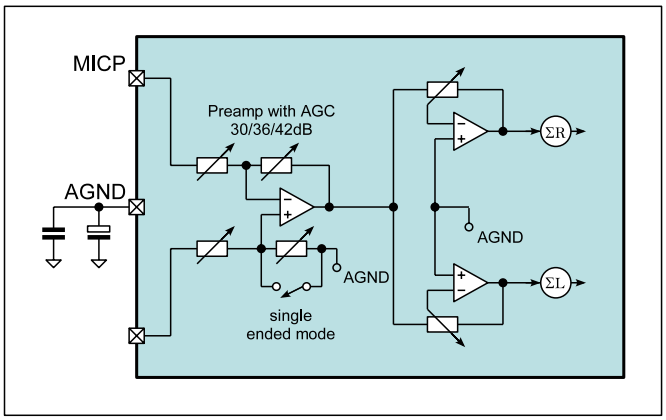
8.2 Microphone Input

8.2.1 General

The AFE offers one microphone input and one low noise microphone voltage supply (microphone bias), voice activation, microphone connect detection and push button remote control.

Please not that only single ended mode is possible for the microphone input, make sure that the MIC_MODE in reg. 06h is set for enalbing the single ended mode.

Figure 4. Microphone Input



8.2.2 Gain Stage & Limiter

The integrated pre-amplifier allows 3 preset gain settings. There is also a limiter which attenuates high input signals from e.g. electret microphones signal to 1Vp. The AGC has 128 steps with 0.375dB with a dynamic range of the full pre-amplifier level. The AGC is ON by default but can be disabled by a microphone register bit.

Apart from the microphone pre-amplifier the microphone input signal can further be amplified with 32 @1.5dB programmable logarithmic gain steps and MUTE. All gains and MUTE are independently programmable. The gain can be set from –40.5dB to +6dB.

The stage features a soft-start function. Pre-amplifier and gain-stage settings can be set before enabling the microphone stage. After enabling the stage to gain is automatically set to the defined value by using the 128 steps of the AGC.

8.2.3 Supply & Detection

Each microphone input generates a supply voltage of 1.5V above HPCM. The supply is designed for ≤2mA and has a 6.5mA current limit. In OFF mode the MICS terminal is pulled to AVDD with 20kOhm. A current of typically 50uA generates an interrupt to inform the CPU, that a circuit is connected. When using HPCM as headset ground the HP–stage gives the interrupt. After enabling the HP-stage through the CPU the microphone detection interrupt will follow.

When using the MICS terminal as ADC-10 input to monitor external voltages the 20kOhm pull-up has to be disabled by disabling the interrupt for microphone detection.

8.2.4 Remote Control

Fast changes of the supply current of typically 500uA are detected as a remote button press, and an interrupt is generated. Then the CPU can start the measurement of the microphone supply current with the internal 10-bit ADC to distinguish which button was pressed. As the current measurement is done via an internal resistor, only two buttons generating a current of about 0.5mA and 1mA can be detected. With this, 1mA as microphone bias is still available.

8.2.5 Voice Activation

Further a built-in voice activation comparator can actuate an interrupt if microphone input voltage of about 5mVRMS is detected.

8.2.6 Parameter

AVDD17=1.7V, AVDD27=2.7V, T_A= 25°C unless otherwise mentioned

Table 8. Microphone Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{MICIN}0$	Input Signal Level	A_{MICPRE} = 30dB; AMIC = 0dB		20		mV_P
$V_{MICIN}1$		A_{MICPRE} = 36dB; AMIC = 0dB		10		mV_P
$V_{MICIN}2$		A_{MICPRE} = 42dB; AMIC = 0dB		5		mV_P
R_{MICIN}	Input Impedance	MICP to AGND		7.5		kΩ
Δ_{MICIN}	Input Impedance Tolerance			-7 +33		%
C_{MICIN}	Input Capacitance			5		pF
A_{MICPRE}	Microphone Preamplifier Gain	Preamplifier has 3 selectable (fixed) gain settings		30 36 42		dB
A_{MIC}	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Precision			±0.25		dB
V_{ATTACK}	Limiter Activation Level			0.57		V_{PEAK}
V_{DECAY}	Limiter Release Level			0.47		V_{PEAK}
$A_{MICLIMIT}$	Limiter Gain Overdrive	128 @ 0.375dB		30 36 42		dB
t_{ATTACK}	Limiter Attack Time			50		µs/6dB
t_{DECAY}	Limiter Decay Time			120		ms/ 6dB
$A_{MICMUTE}$	Mute Attenuation			100		dB
V_{MICSUP}	Microphone Supply Voltage	depending on V_MICS setting		2 1.55 1.26 1.06		V
I_{MICMAX}	Max. Microphone Supply Current	microphones nominally need a bias current of 0.5mA-1mA		6.5		mA
V_{NOISE}	Microphone Supply Voltage Noise			5		µV
I_{MICDET}	Microphone Detection Current			50		µA
I_{REMDET}	Max. Remote Detection Current			500		µA

8.2.7 Register Description

Table 9. Microphone Input Related Register

Name	Base	Offset	Description
MIC_R	2-wire serial	06h	Right Microphone Input volume settings, AGC control
MIC_L	2-wire serial	07h	Left Microphone Input volume settings, MIC supply control
AudioSet1	2-wire serial	14h	Enable/disable driver stage
AudioSet3	2-wire serial	16h	Enable/disable mixer input
IRQENRD_1	2-wire serial	24h	Interrupt settings for microphone voice activation
IRQENRD_3	2-wire serial	26h	Interrupt settings for microphone detection
IRQENRD_4	2-wire serial	27h	Interrupt settings for remote button press detection

8.3 Line Output

8.3.1 General

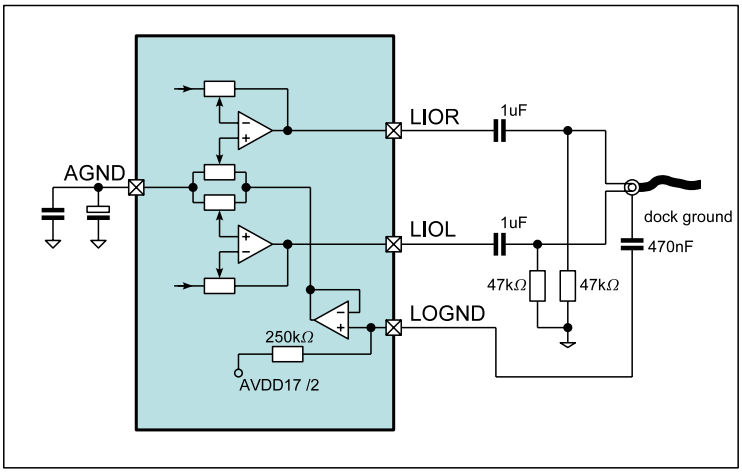
The line output is designed to provide the audio signal with a typical V_{PEAK} level at a load of minimum 10kΩ, which is a minimum value for line inputs. If the limiters (N20/N21) are deactivated the peak output voltage is AVDD17/2 Vp.

This AFE has a combined output stage for headphone and line output with an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -40.5dB to +6dB.

If the line output is not enabled, the volume settings are set to their default values. Changing of volume and mute control can only be done after enabling the output.

Line Output and Line Input are sharing the same pins.

Figure 5. Line Output



8.3.2 Auto Fading

By setting a new output volume level, the stage does a automatic fading from the current gain setting to the new target. Changing the input multiplexer from one source to another will be done by fadeing out to mute, source changing and fading in of the new source to the target volume. Change from HPH-out to LINE-out is done by fading out of HPH-out to mute and fading in of the LINE-out to the target volume.

The fading speed can be programmed to 3 different speed levels. The immediate response can be selected as 4th state.

8.3.3 Ground Noise Cancelation

A separate ground input allows to connect a ground sense line direct from the dock connector ground or line out jack shield to make the audio output independent from PCB ground noise.

8.3.4 Parameter

AVDD17=1.7, AVDD27=2.7, T_A= 25°C, unless otherwise mentioned

Table 10. Line Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{L_LO}	Load Impedance (Stereo Mode)	line inputs nominally have 10kΩ	5			kΩ
C_{L_LO}	Load Capacitance (Stereo Mode)				100	pF
A_{LO}	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Accuracy			±0.25		dB
A_{LOMUTE}	Mute Attenuation			100		dB

8.3.5 Register Description

Table 11. Line Output Related Register

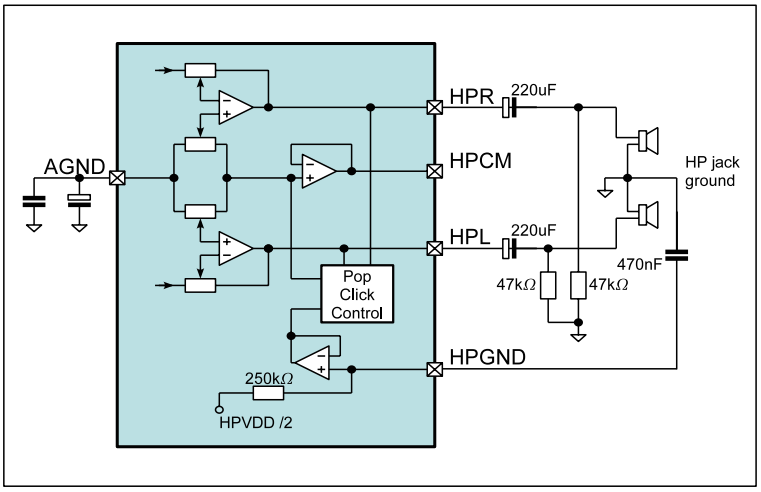
Name	Base	Offset	Description
OUT_R	2-wire serial	00h	Right Line Output volume settings, MUX control
OUT_L	2-wire serial	01h	Left Line Output volume settings
AudioSet2	2-wire serial	15h	Auto fading timing settings
AudioSet3	2-wire serial	16h	Enable/disable mixer input

8.4 Headphone Output

The headphone output is designed to provide the audio signal with 2x40mW @ 16Ω or 2x20mW @32Ω, which are typical values for headphones.

This AFE has a combined output stage for headphone and line output with an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -40.5dB to +6dB.

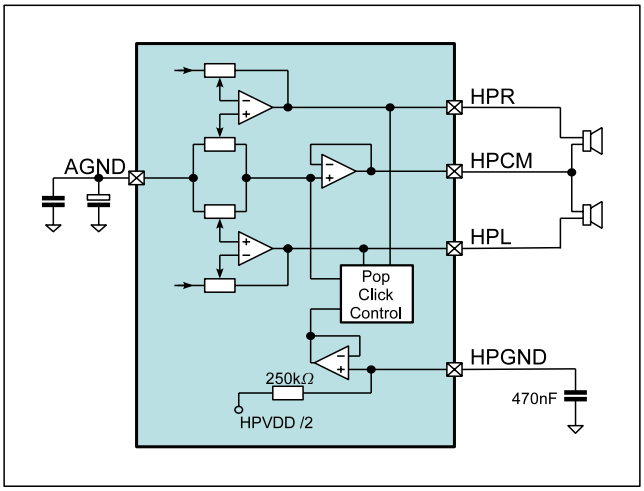
Figure 6. Headphone Output



8.4.1 Phantom Ground

There are 2 ways to connect a headphone to the AFE. In order to spare the bulky ac/dc de-coupling capacitors at pins HPR/HPL a buffered ground (Phantom Ground) is provided. This Common Mode Buffer needs to be switched on if utilized. If form factor considerations are less stringent, the headphones can be conventionally connected via 2x200µF capacitors.

Figure 7. Headphone Output using Common Mode Buffer



8.4.2 No-Pop Function

The output is automatically set to mute when the output stage is disabled.

To avoid Pop-Click noise during power-up and shut-down of the headphone amplifier, a charge/discharge control of HPGND (0V-HPVDD/2-0V) at pins HPR/HPL is incorporated into the AFE. The 470nF capacitor at pin HPGND is used to form the charge/discharge slope. Pls observe that pin HPGND is a high impedance node which must not be connected to any other external device than the 470nF buffer capacitor. To avoid Pop-Click noise one has to wait for 750ms in between a power-down (switch-off) and a power-up (switch-on) of the headphone amplifier.

8.4.3 Auto Fading

By setting a new output volume level, the stage does a automatic fading from the current gain setting to the new target. Changing the input multiplexer from one source to another will be done by fading out to mute, source changing and fading in of the new source to the target volume. Change from HPH-out to LINE-out is done by fading out of HPH-out to mute and fading in of the LINE-out to the target volume.

The fading speed can be programmed to 3 different speed levels. The immediate response can be selected as 4th state.

Figure 8. Headphone Startup with MaxGain Settings

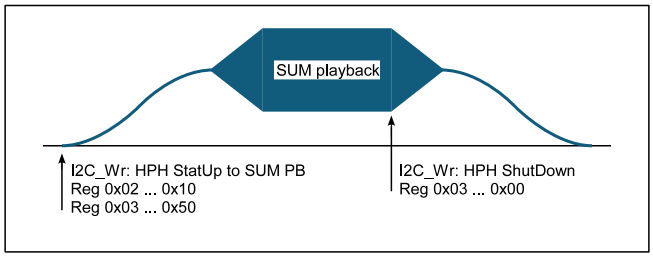
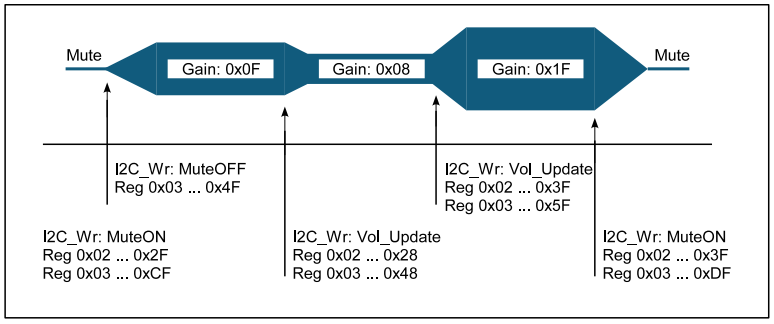


Figure 9. Headphone Change Gain Settings



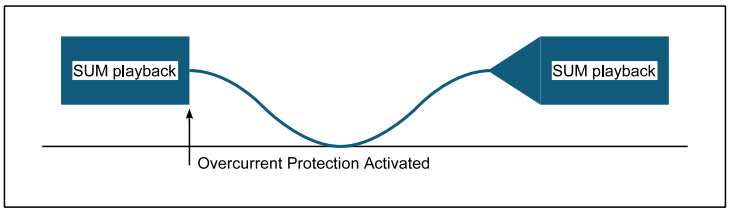
8.4.4 Headphone Detection

When the headphone amplifier is powered down, one can detect the connection of a headset. It only work if the headset is connected between pins HPR/HPL and HPCM. As long as the headphone amplifier is powered down, HPCM is biased to 150mV and acting as the sense pin. There is a corresponding interrupt available to be enabled.

8.4.5 Over-current Protection

The headphone amplifier has an over-current protection (e.g. HPR/HPL is shorted). This over-current protection will power down the headphone amplifier for a programmable time-out period (512ms, 0ms). There is a corresponding interrupt available to be enabled.

Figure 10. Headphone Overcurrent OFF-ON Sequence



8.4.6 Ground Noise Cancelation

As separate ground input allows to connect a ground sense line direct from the dock connector ground or headphone jack shield to make the audio output independent from PCB ground noise.

8.4.7 Power Options

To save power, especially when driving 32 Ohm loads, a reduction of the bias current is selected. For 16Ohm loads the bias current can be increased.

8.4.8 Parameter

AVDD17=1.7, AVDD27=2.7, HPVDD = 2.7V, T_A= 25°C, unless otherwise mentioned

Table 12. Headphone Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{L_HP}	Load Impedance	stereo mode	16			Ω
C_{L_HP}	Load Capacitance	stereo mode			100	pF
P_{HP}	Nominal Output Power	RL=16Ω, limiter enabled RL=32Ω, limiter enabled		40 20		mW
A_{HP}	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB

Table 12. Headphone Output Parameter (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Gain Step Accuracy			±0.25		dB
	Over current limit	HPR/HPL pins HPCM pin, @1.8V		70mA 140mA		mA mA
P_{SRRHP}	Power Supply Rejection Ratio	200Hz-20kHz, 720mVpp, RL=16Ω		90		dB
A_{HPMUTE}	Mute Attenuation			100		dB

8.4.9 Register Description

Table 13. Headphone Related Register

Name	Base	Offset	Description
OUT_R	2-wire serial	02h	Right HP Output volume and over-current settings
OUT_L	2-wire serial	03h	Left HP Output volume settings, enable and detection control
AudioSet2	2-wire serial	15h	Auto fading timing settings
AudioSet3	2-wire serial	16h	Power options, common mode buffer enable
IRQENRD_3	2-wire serial	26h	Interrupt settings for over current and HP detection

8.5 DAC, ADC and I2S Digital Audio Interface

8.5.1 Input

The AFE receives serialized audio data for the DAC via pin SDI. The output of the DAC is fed through a volume control to the mixer stage and to the multiplexers of line output and headphone amplifiers or direct to these output stages.

This serialized audio data is a digital audio data stream with the left and the right audio channels multiplexed into one bit-stream. Via pin LRCK the alignment clock is input to the DAC digital filters. LRCK (Left Right Clock) indicates whether the serial bit-stream received via pin SDI, represents right channel or left channel audio data. Via pin SCLK the bit clock for the serial bit-stream is signalled. SDI and LRCK are synchronous with SCLK. SDI, LRCK and SCLK are inputs; SDO is not used.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –40.5dB to +6dB. The stage is set to mute by default. If the DAC input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

8.5.2 Output

This block consists of an audio multiplexer where the signal, which should be recorded, can be selected. The output is then fed through a volume control to the audio ADC. The digital output is done via an I2S interface.

The AFE sends serialized audio data from the ADC via pin SDO. This serialized audio data is a digital audio data stream with the left and the right audio channels multiplexed into one bit-stream. Via pin LRCK the alignment clock is signalled to the connected devices (e.g. CPU). LRCLK (Left Right Clock) indicates whether the serial bit-stream sent via pin SDI, presents right channel or left channel audio data. Via pin SCLK the bit clock for the serial bit-stream is signalled. SDO and LRCK are synchronous with SCLK. SDO is an output; LRCK and SCK are inputs; SDI is not used.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from –34.5dB to +12dB. The stage is set to mute by default. If the ADC output is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

The I2S output uses the same clocks as the I2S input. The sampling rate therefore depends also on the input sampling rate. The exact ratio can be set in register 11h.

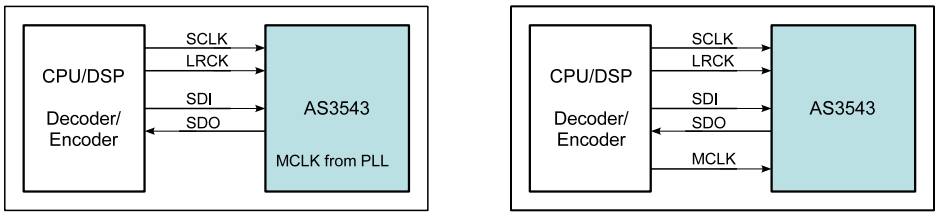
The SDO output can be configured to operate in push/pull (3 different driver strengths) or to be tri-state. For a more detailed description of the GPIO functionality of this pin please refer to chapter GPIO Pins on page 48.

8.5.3 I2S Modes

The AFE can be operated either in Slave Mode or in Slave Mode with the master clock directly signalled via pin MCLK. The master clock (MCLK) is the necessary internal over-sampling clock for the DAC and ADC (e.g. 128*fs, fs=audio sampling frequency)

In Slave Mode the PLL generates the master clock based on LRCK. Thus the PLL needs to be preset to the expected sampling frequency. The ranges are 8kS-23kS (8kHz-23kHz) and 24kS-48kS (24kHz-48kHz). Please refer to register 1A-7h.

Figure 11. I2S Modes



8.5.4 Clock Supervision

The digital audio interface automatically checks the LRCK. An interrupt can be generated when the state of the LRCK input changes. A bit in the interrupt register represents the actual state (present or not present) of the LRCK.

8.5.5 Signal Description

The digital audio interface uses the standard I2S format:

- left justified
- MSB first
- one additional leading bit

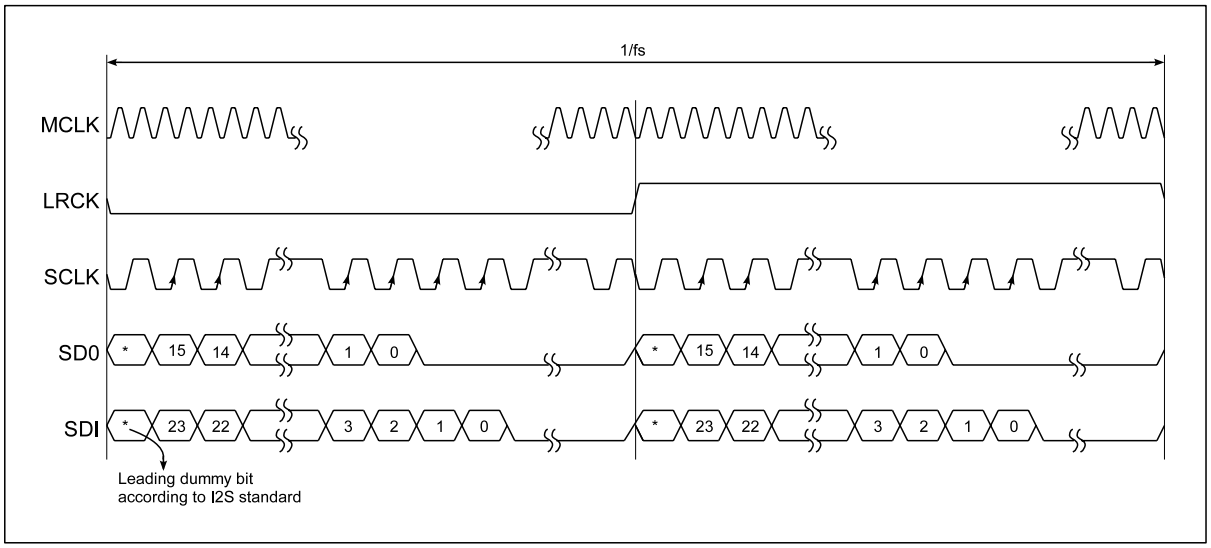
The on-chip synchronization circuit allows any bit-count up 32bit. When there are less than 18 bits sampled, the data sample is completed with “0”s. In I2S direct mode the data length has to be minimum 18 bits.

The ADC output is always 14 bit. If more SCLK pulses are provided, only the first 14 will be significant.

SCLK has not to be necessarily synchronous to LRCK but the high going edge has to be separate from LRCK edges. The LRCK signal has to be derived from a jitter-free clock source, because the on-chip PLL is generating a clock for the digital filter, which has to be always in correct phase lock condition to the external LRCK.

Please observe that LRCK has to be activated before enabling the ADC.

Figure 12. I2S left justified mode



8.5.6 Parameter

DVDD=2.9V, T_A=25°C, Slave Mode, f_S=48kHz, MCLK = 128*f_S, unless otherwise specified

Table 14. I2S Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SCLK}	SCLK Cycle Time		160			ns
t_{SCLKH}	SCLK Pulse Width High		80			ns
t_{SCLKL}	SCLK Pulse Width Low		80			ns
T_{LRSU}	LRCK Setup Time before SCLK rising edge		80			ns
T_{LRHD}	LRCK Hold Time after SCLK rising edge		80			ns
t_{SDSU}	SDI setup time before SCLK rising edge		25			ns
t_{SDHD}	SDI hold time after SCLK rising edge		25			ns
t_{SDOD}	SDO Delay from SCLK falling edge				25	ns
t_{JITTER}	Jitter of LRCK	internal PLL generates MCLK from LRCK	-20		20	ns
I2S direct mode						
T_{SCD}	SCLK delay after MCLK rising edge		0.5		1.5	ns
T_{LRD}	LRLCK delay after SCLK rising edge		0.5		1.5	ns
t_{SDSU}	SDI setup time before SCLK rising edge		5			ns
t_{SDHD}	SDI hold time after SCLK rising edge		5			ns
t_{SDOD}	SDO Delay from SCLK falling edge				15	ns

8.5.7 Register Description

Table 15. Audio Converter Related Register

Name	Base	Offset	Description
DAC_R	2-wire serial	0Eh	DAC input volume settings
DAC_L	2-wire serial	0Fh	DAC input volume settings
ADC_R	2-wire serial	10h	ADC output volume settings, source multiplexer settings
ADC_L	2-wire serial	11h	ADC output volume settings, sampling rate settings
DAC_IF	2-wire serial	11h	DAC input digital volume settings
AudioSet1	2-wire serial	14h	Enable/disable DAC, DAC gain stage & ADC
AudioSet3	2-wire serial	16h	Enable/disable mixer input
Out_Cntr3	2-wire serial	1A-3h	Control of SDO signal and drive
PLL	2-wire serial	1A-7h	PLL sample rate settings
PMU_Enable	2-wire serial	1Ch	Enables writings to extended registers 1Ah-3 and 1Ah-7
IRQENRD_1	2-wire serial	25h	Interrupt settings for LRCK changes

DAC and ADC have to be enabled in register 14h first before other settings in register 0Eh to 11h can be programmed.

8.6 Audio Output Mixer

8.6.1 General

The mixer stage sums up the audio signals of the following stages

- Microphone Input 1
- Line Input 1/2
- DAC Output
- ADC Input

The mixing ratios have to be set within the volume registers of the corresponding input stages. Please be sure that the peak voltage of input signals for the mixer stage is less than AVDD17/3. If summing up several signals, each individual signal has of course to be accordingly lower. This shall insure that the output signal is also not higher than AVDD17/3 peak to get a proper signal for the output amplifier.

This stage features an automatic gain control (AGC), which automatically avoids clipping.

8.6.2 Register Description

Table 16. Audio Mixer Related Register

Name	Base	Offset	Description
AudioSet2	2-wire serial	15h	Enable/disable mixer stage and AGC
AudioSet3	2-wire serial	16h	Enable/disable DAC, MIC or Line Inputs to mixer stage