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# AS3543

**DataSheet**

## High End Stereo Audio Codec with System PMU

### 1 General Description

The AS3543 is an ultra low power stereo audio codec and is designed for Portable Digital Audio Applications.

It allows high-end quality playback with up to 100dBa SNR and recording in FM quality. With one microphone (including pre-amplifier and supply for an electret microphone) and two line inputs, it allows connecting a variety of audio inputs. The different audio signals can be mixed via a 6-channel mixer and fed to either a headphone output for 16 /32 headsets or a line output. Both outputs have a ground noise cancellation to use it e.g. in car docking stations. The audio outputs have also an auto fading implemented which performs the fade-in, fade-out as well as the transition between specific volume levels automatically with an selectable timing.

Further the device offers advanced power management functions. All necessary ICs and peripherals in a Digital Audio Player are supplied by the AS3543. It features 2 DCDC converters for core and memory/periphery supply as well as 4 LDOs. Both DCDC converter feature DVM (dynamic voltage management) with an selectable timing for the voltage stepping. The different regulated supply voltages are programmable via the serial control interface.

The step-up converter for the backlight can operate up to 15V (with an external transistor even higher) in voltage and current control mode. An internal voltage protection is limiting the output voltage in the case of external component failures. 2 high voltage current sinks can be used to operate two, if needed also unbalanced, LED strings. An automatic dimming function allows a logarithmic on/off of the backlight with selectable timing.

AS3543 also contains a Li-Ion battery charger with constant current, constant voltage and trickle charging. The maximum charging current is 460mA. An integrated battery switch is separating the battery during charging or whenever an external power supply is present. With this switch it is also possible to operate with no or deeply discharged batteries.

The AS3543 has an on-chip, phase locked loop (PLL) which generates the needed internal CODEC master clock. I2S Frame and shift-clock have to be applied from the processor for playback and recording.

Further the AS3543 has an independent 32kHz real time clock (RTC) on chip which allows a complete power down of the system CPU while only consuming less than 1µA. An internal switch automatically switches between the RTC backup-battery and main battery supply.

The single supply voltage may vary from 2.7V to 5.5V.

### 2 Key Features

#### Audio

##### Audio power consumption:

- - 5mW: 96dB DAC to Headphone @ 1.8V, 32Ω
- - 7mW: 100dB DAC to Headphone @ 2.9V, 32Ω

##### Sigma Delta Converters

- DAC
  - 98dB SNR ('A' weighted) @ 1.7V
  - 102dB SNR ('A' weighted) @ 2.9V
- ADC
  - 85dB SNR ('A' weighted) @ 1.7V
- Sampling Frequency
  - DAC: 8-96kHz
  - ADC: 8-24kHz

##### High Efficiency Headphone Amplifier

- volume control via serial interface
- 32 steps @1.5dB and MUTE
- 2x12mW @16Ω driver capability@ 1.8V supply
- THD -74dB @16Ω; 1.8V
- 2x40mW @16Ω driver capability@ 3.6V supply
- THD -77dB @16Ω; 3.6V
- headphone and over-current detection
- phantom ground eliminates large capacitors
- ground noise cancellation

##### Line Output

- volume control via serial interface
- 32 steps @1.5dB and MUTE
- 0.6Vp @10kΩ, 1.8V
- ground noise cancellation



## Microphone Input

- 3 gain pre-setting (30dB/36dB/42dB) and AGC
- 32 gain steps @1.5dB and MUTE
- supply for electret microphone
- microphone detection
- remote control by switch

## 2 Line Inputs

- volume control via serial interface
- 32 steps @1.5dB and MUTE
- stereo or 2x mono

## Audio Mixer

- 8 channel input/output mixer with AGC
- mixes line inputs, microphone and ADC with DAC
- left and right channels independent

## Power Management

### Voltage Generation

- step down for CPU core (0.61V-3.35V, 250mA)
- step down for peripheral (0.61V-3.35V, 250mA)
- LDO1 for AFE supply (1.7V (1.65-3.2V), 50mA)
- LDO2 for AFE supply (2.7V (2.3-3.5V), 200mA)
- LDO3 for peripherals (1.2V-3.5V, 100/200mA)
- LDO4 for peripherals (1.2V-3.5V, 100/200mA)
- VBUS comparator
- separate input for LDO3
- power supply supervision & hibernation modes
- 5sec and 10sec emergency shut-down

### Backlight Driver

- step up for backlight (15V (25V))
- current control mode (1.2-37.2mA)
- voltage control mode
- 2 HV current sinks
- automatic dimming
- over-voltage protection

### Battery Charger

- automatic trickle charge (55mA)
- prog. constant current charging (55-460mA)
- prog. constant voltage charging (3.9V-4.25V)
- current limitation for USB mode
- integrated battery switch

## General

### Supervisor

- automatic battery monitoring with interrupt generation and selectable warning level
- automatic temperature monitoring with interrupt generation and selectable warning and shutdown levels

### Real Time Clock

- ultra low power 32kHz oscillator
- 32bit RTC sec counter, 96 days auto wake-up
- selectable interrupt (seconds or minutes)
- 128bit free SRAM for random settings
- 32kHz clock output to peripheral
- voltage generation
- trim able oscillator
- <1uA total power consumption

### Auxiliary Oscillator (system clock generation)

- low power 12-24MHz oscillator
- clock output

### General Purpose ADC

- 10bit resolution
- 22 inputs analog multiplexer

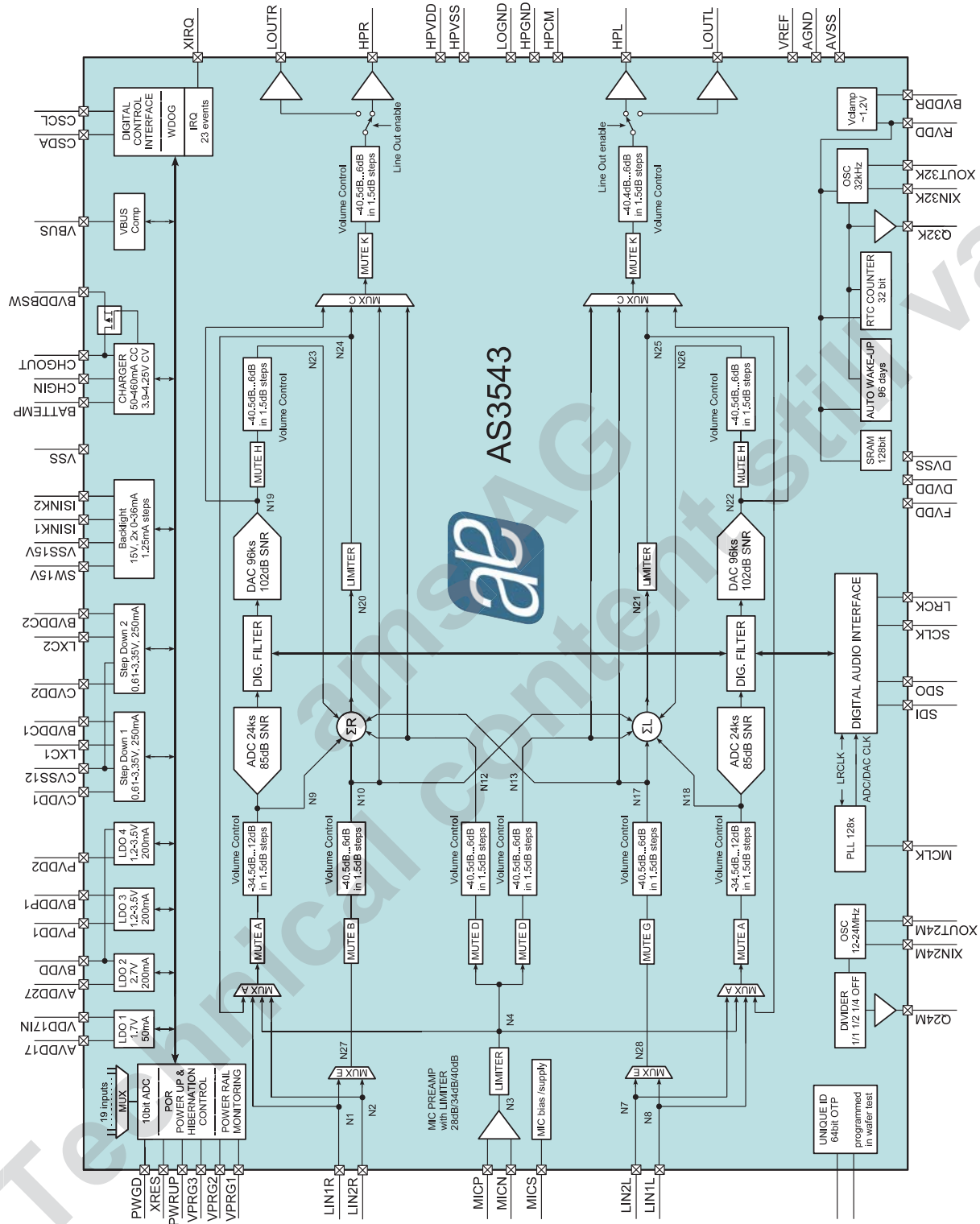
### Interfaces

- 2 wire serial control interface
- reset pin with selectable delay, power good pin
- 64bit unique ID (OTP)
- 26 different interrupts
- Package CTBGA68 [6.0x6.0x1.1mm] 0.5mm pitch

## 3 Applications

Portable Digital Audio/Video Player and Recorder  
PDA, Smartphone

Figure 1. Block Diagram



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## Revision History

Table 1. Revision History

Revision	Date	Owner	Description
1.01	17.4.2009	pkm	official release
1.10	5.2009	pkm	added audio characterisation data
1.11	12.2012	pkm	typo and register bit description corrections

ams AG  
Technical content still valid

## 4 Pinout

### 4.1 Pin Assignment

Figure 2. Pin Assignments (Top View)

	1	2	3	4	5	6	7	8	9	10
A	CHGOUT	BVDDBSW	PVDD1		PVDD2	HPCM		HPR	HPVSS	HPL
B	CHGIN	BATTEMP	BVDDP1	BVDD	VDD17IN	HPGND	HPVDD	LOGND	LOUTR	LOUTL
C	VSS15V	SW15V							LIN1R	LIN1L
D		ISINK2		VSS	VBUS	LIN2R	LIN2L		MICS	
E	BVDDC2	ISINK1		MCLK			VPROG3		MICN	MICP
F	LXC2	CVDD2		SCLK			VPROG2		AGND	AVSS
G		FVDD		LRCK	SDI	SDO	VPROG1		VREF	
H	CVSS12	CVDD1							AVDD27	AVDD17
J	LXC1	PWRUP	XRES	XIRQ	PWGD	Q24M	Q32K	CACL	RVDD	XIN32K
K	BVDDC1	XIN24M	XOUT24M		DVSS	DVDD		CSDA	BVDDR	XOUT32K

### 4.2 Pin Description

Table 2. Pin Description for AS3543

Pin Number	Pin Name	Type	Description
K2	XIN24M	ANA IO	24MHz Crystal Input (ext. 22pF C needed)
K3	XOUT24M	ANA IO	24MHz Crystal Output (ext. 22pF C needed)
J2	PWRUP	DIG IN	Power Up Input
G2	FVDD	SUP IN	Digital Pos. Supply (e.g. DAC, ...)
J3	XRES	DIG OUT	Reset Output
J4	XIRQ	DIG OUT	Interrupt Request Output
J5	PWGD	DIG IO	PowerUp Sequence Complete Output
E4	MCLK	DIG IN	MCLK input
F4	SCLK	DIG IN	I2S Shift Clock Input
G4	LRCK	DIG IN	I2S Frame Clock Input
G5	SDI	DIG IN	I2S Data Input to DAC



Table 2. Pin Description for AS3543

Pin Number	Pin Name	Type	Description
K5	DVSS	GND	Digital Circuit Neg. Supply Terminal
K6	DVDD	SUP IN	Digital Periphery Pos. Supply
G6	SDO	DIG OUT	I2S Data Output from ADC
J6	Q24M	DIG IO	24MHz clock digital output
J7	Q32K	DIG IO	32kHz clock digital output
J8	CSCL	DIG IN	2 wire SERIF Clock Input
K8	CSDA	DIG IO	2 wire SERIF Data I/O
K9	BVDDR	SUP IN	Secondary RTC Supply - Supercap
K10	XOUT32K	ANA IO	32KHz Crystal Output XIN
J10	XIN32K	ANA IO	32kHz Crystal Input XOUT
J9	RVDD	ANA IO	RTC LDO output, RTC supply input
G9	VREF	ANA IO	DAC Reference Pin
G7	VPRG1	ANA IN	Core Supply Voltage Definition Pin
F7	VPRG2	ANA IN	Memory Supply Voltage Definition Pin
E7	VPRG3	ANA IN	PowerUp Sequence Definition Pin
F10	AVSS	GND	Ground (analog)
F9	AGND	ANA IO	Analog Common Mode Voltage Pin
E10	MICP	ANA IN	Microphone Input P
E9	MICN	ANA IN	Microphone Input N
D9	MICS	ANA IO	Microphone Supply Output / Remote Control input
D6	LIN2R	ANA IN	Analog Line Input 2 Right Channel
D7	LIN2L	ANA IN	Analog Line Input 2 Left Channel
B8	LOGND	ANA IO	Line Output Common Mode Voltage Pin
C9	LIN1R	ANA IO	Analog Line Input 1 Right Channel
B9	LOUTR	ANA OUT	Analog Line Output Right Channel
B10	LOUTL	ANA OUT	Analog Line Output Left Channel
C10	LIN1L	ANA IO	Analog Line Input 1 Right Channel
B7	HPVDD	SUP IN	Headphone Supply default 1.8V (max. 3.6V)
A10	HPL	ANA OUT	Headphone Output Left Channel
A8	HPR	ANA OUT	Headphone Output Right Channel
A6	HPCM	ANA OUT	Headphone Common Mode Buffer Pin
A9	HPVSS	GND	Headphone Ground
B6	HPGND	ANA IO	Headphone Common Mode Voltage Pin
H10	AVDD17	SUP IO	LDO1 Output default 1.7V
B5	VDD17IN	SUP IN	LDO1 Pos. Supply Terminal
H9	AVDD27	SUP IO	LDO2 Output default 2.7V
B4	BVDD	SUP IN	Main Battery Supply Input (2.7-5.5V)
D5	VBUS	ANA IN	VBUS Detection Input
A5	PVDD2	ANA OUT	LDO4 Output (PVDD2)
A3	PVDD1	ANA OUT	LDO3 Output (PVDD1)

Table 2. Pin Description for AS3543

Pin Number	Pin Name	Type	Description
B3	BVDDP1	SUP IN	LDO3 Pos. Supply Terminal
A2	BVDDBSW	SUP IO	Battery Switch output to be connected against BVDD
A1	CHGOUT	SUP IO	Li-Ion Charger Output (battery switch input)
B1	CHGIN	SUP IN	Li-Ion Charger Input
B2	BATTEMP	ANA IO	Li-Ion Charger Battery Temp. Sensor Input
D4	VSS	GND	Power Management Neg. Reference Supply
C1	VSS15V	GND	DCDC15V & Current Sinks Neg. Supply Terminal
C2	SW15V	DIG OUT	DCDC15V Switch Output to Coil
D2	ISINK2	ANA IO	DCDC15V Load Current Sink2 Terminal
E2	ISINK1	ANA IO	DCDC15V Load Current Sink1 Terminal
E1	BVDDC2	SUP IN	CVDD2 Step Down Pos. Supply Terminal
F1	LXC2	DIG OUT	CVDD2 Step Down Switch Output to Coil
F2	CVDD2	ANA IN	CVDD2 and Feedback Pin
H1	CVSS12	GND	DCDC12 Substrate Pin
H2	CVDD1	ANA IN	CVDD1 and Feedback Pin
J1	LXC1	DIG OUT	CVDD1 Step Down Switch Output to Coil
K1	BVDDC1	SUP IN	CVDD1 Step Down Pos. Supply Terminal

## 5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics on page 11](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
5V pins	-0.5	7.0	V	Applicable for pins BVDD, BVDDC1, BVDDC2, BVDDR, BVDDP1, BVDDBSW, CHGIN, CHGOUT, VBUS, CSCL, CSDA, PWRUP
3V pins	-0.5	5.0	V	Applicable for pins DVDD, HPVDD, FVDD, VDD17IN, RVDD, VPRG1, VPRG2, VPRG3
15V pins	-0.5	17	V	Applicable for pin SW15V, ISINK1/2
Voltage difference at VSS terminals	-0.5	0.5	V	Applicable for pins VSS, VSS15V, CVSS12, HPVSS, AVSS, DVSS
3.3V pins with protection to AVDD27	-0.5	5.0 AVDD27	V	Applicable for pins BATTEMP, HPGND
3.3V pins with protection to DVDD	-0.5	5.0 DVDD+0.5	V	Applicable for pins MCLK, LRCK, SCLK, SDI, SDO, XIRQ, XRES, PWGD, Q32K, Q24M, XIN24M, XOUT24M
3.3V pins with protection to RVDD	-0.5	5.0 RVDD+0.5	V	Applicable for pins XIN32K, XOUT32K
3.3V pins with protection to AVDD17	-0.5	5.0 AVDD17+0.5	V	Applicable for pins LOU1L/R, LOGND, VREF, AGND, LIN1L/R, LIN2L/R, MICP/N, MICS
3.3V pins with protection to HPVDD	-0.5	5.0 HPVDD+0.5	V	Applicable for pins HPCM, HPR/L
voltage regulator pins with protection to BVDD	-0.5	5.0 BVDD+0.5	V	Applicable for pins AVDD27, PVDD1/2, CVDD1, LXC1, CVDD2, LXC2
voltage regulator pins with protection to AVDD17IN	-0.5	5.0 AVDD17IN +0.5	V	Applicable for pins AVDD17
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 17
<b>Continuous Power Dissipation (T<sub>A</sub> = +70°C)</b>				
Continuous power dissipation		500	mW	P <sub>T</sub> <sup>1</sup> for CTBGA68 package
<b>Electrostatic Discharge</b>				
Electrostatic Discharge HBM		+/-1	kV	Norm: JEDEC JESD22-A114C
<b>Temperature Ranges and Storage Conditions</b>				
Operating Temperature Range	-20	+85	°C	
Junction Temperature		+110	°C	
Storage Temperature Range	-50	+125	°C	
Humidity non-condensing	5	85	%	

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
<b>Bump Temperature (soldering)</b>				
Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only
Solder Profile	235	245	°C	peak temperature
	30	45	s	well time above 217 °C
Moisture Sensitive Level	3		1	Represents a max. floor live time of 168h

1. Depending on actual PCB layout and PCB used

## 6 Electrical Characteristics

BVDD=+2.7V...+5.5V,  $T_A$  =-20°C...+85°C. Typical values are at BVDD=+3.6V,  $T_A$ =+25°C, unless otherwise specified.

Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Supply Voltages</b>						
BVDDx	Battery Supply Voltage BVDD, BVDDBSW, BVDDC1, BVDDC2, BVDDP1		2.7	3.6	5.5	V
BVDDR	RTC secondary Supply Voltage		1.2		5.5	V
VBUS	USB VBUS Voltage			5.0	5.5	V
CHGIN	Charger Supply Voltage		4.5		5.5	V
HPVDD	HP Supply Voltage		1.8		3.6	V
DVDD	Digital Periphery Supply Voltage		1.8	2.9	3.6	V
VDD17IN	LDO1 Input Voltage		1.8		3.6	V
FVDD	Digital Supply Voltage		1.75	1.8	3.5	V
AVDD27	Analogue Supply Voltage		2.6	2.7	3.5	V
AVDD17	Analogue Supply Voltage		1.7	1.7	3.5	V
AGND	Analog Ground Voltage	Internally generated		AVDD17 /2		V
V <sub>DELTA-</sub>	Difference of Negative Supplies CVSS12, VSS15V, HPVSS, AVSS, DVSS, VSS	To achieve good performance, the negative supply terminals should be connected to low impedance ground plane.	-0.1		0.1	V
V <sub>DELTA+</sub>	Difference of Positive Supplies	RVDD-AVDD27; AVDD17-AVDD27; FVDD-AVDD27			0	V
		AVDD27-HPVDD			0.3	V
		BVDD-AVDD27			0.1	V
<b>POR &amp; Watchdog</b>						
V <sub>POR_ON</sub>	Power-on Reset Activation Level	Power-on Reset activation level when DVDD decreases		2.15		V
V <sub>POR_OFF</sub>	Power-on Reset Release Level	Power-on Reset release when DVDD increases		2.0		V
V <sub>POR_HY</sub>	Power-on Hysteresis			100		mV
f <sub>LRCLK_WD</sub>	LRCLK Watchdog		2	4.1	8	kHz
<b>PWRUP</b>						
t <sub>ON_DELAY</sub>	Delay Time of pin PWRUP	Minimum key press time		30		ms
V <sub>PWRUP_L</sub>	Input Level LOW,	Pin PWRUP, BVDD>3V			0.5	V
V <sub>PWRUP_H</sub>	Input Level HIGH	Pin PWRUP, BVDD>3V	BVDD/ 3			V
		Pin PWRUP, BVDD<=3V	1			V
I <sub>PWRUP</sub>	Internal Pull-down Current Source	Pin PWRUP; @2.9V	2.5	7	19	uA



Table 4. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Digital Inputs/Outputs</b>						
V <sub>DO_DL</sub>	Digital Output Driver Capability (drive LOW)	Pins XRES, XIRQ, PWGD @ 8mA, SDO			10% DVDD	V
V <sub>DO_DH</sub>	Digital Output Driver Capability (drive HIGH)	Pins XRES, XIRQ @ 8mA, push/pull mode only, SDO	90% DVDD			V
I <sub>PU</sub>	Internal Pull-up Current Source	Pins XRES, XIRQ, PWGD, Q32K, Q24M; @0V		10		μA
V <sub>DI_L</sub>	Digital Input Level LOW	Pin SDI, SCLK, MCLK, LRCK		30% DVDD		V
V <sub>DI_H</sub>	Digital Input Level HIGH	Pin SDI, SCLK, MCLK, LRCK		70% DVDD		V
f <sub>CLK</sub>	Audio Clock Frequency	LRCK according to streamed audio data	8		96	kHz
<b>Block Power Requirements</b>						
I <sub>REF</sub>	Reference supply current	all blocks off, only LDO2 on		330		μA
I <sub>BIAS</sub>	Audio Bias current			32		μA
I <sub>SUM</sub>	Summing stage current			174		μA
I <sub>LIN</sub>	Line input stage current	no signal		146		μA
I <sub>MIC</sub>	Mic input stage current	no signal		643		μA
I <sub>MICS</sub>	Mic Supply stage current	no load		201		μA
I <sub>LOUT</sub>	Line output stage current	no load		436		μA
I <sub>DAC_GS</sub>	DAC gain stage current	no signal		214		μA
I <sub>ADC_GS</sub>	ADC gain stage current	no signal		1,36		mA
I <sub>HPH</sub>	Headphone stage current	1.8V, no load		1,94		mA
		Bias reduction on, no load		1,48		
		CM buffer off, no load		1,47		
		Bias reduction on, CM buffer off, no load		0,94		
I <sub>DAC</sub>	DAC supply current	LRCK=48kHz		1,48		mA
		LRCK=44.1kHz		1,41		
		LRCK=32kHz		1,19		
		LRCK=16kHz		0,91		
		LRCK=8kHz		0,76		
I <sub>ADC</sub>	ADC supply current	LRCK=24kHz		1,7		mA
		LRCK=22.05kHz		1,69		
		LRCK=16kHz		1,64		
		LRCK=8kHz		1,58		
		LRCK=4kHz		1,55		
I <sub>DAC-&gt;HP</sub>	DAC playback current	no load, 44.1kHz, including PMU				mA
I <sub>Line-&gt;HP</sub>	Line Input playback current	no load, including PMU				mA
I <sub>RTC</sub>	RTC supply current			600		nA

## 6.1 Audio Specification

BVDD=+3.6V, VDD27=HPVDD=FVDD=+3V, VDD17=+2.9V,  $f_s=48\text{kHz}$ ,  $T_A=+25^\circ\text{C}$ , unless otherwise specified.

Table 5. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>DAC Input to Line Output</b>						
FS	Full Scale Output	$R_L=10\text{k}\Omega$ , $f=1\text{kHz}$ , $1V_{\text{RMS}}$ input		0,960		$V_{\text{RMS}}$
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		100		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS, $f=1\text{kHz}$		94		dB
THD	Total Harmonic Distortion	1kHz -1dB FS input, $R_L=10\text{k}\Omega$		-82		dB
CS	Channel Separation	$R_L=10\text{k}\Omega$		62		dB
<b>Line Input to Line Output</b>						
FS	Full Scale Output	$R_L=10\text{k}\Omega$ , $f=1\text{kHz}$ , $1V_{\text{RMS}}$ input		0,754		$V_{\text{RMS}}$
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		101		dB
THD	Total Harmonic Distortion	1kHz $1V_{\text{RMS}}$ (-1dB FS) input, $R_L=10\text{k}\Omega$		-72		dB
CS	Channel Separation	$R_L=10\text{k}\Omega$		100		dB
<b>DAC Input to HP Output</b>						
FS	Full Scale Output	$R_L=32\Omega$		0,800		$V_{\text{RMS}}$
		$R_L=16\Omega$		0,793		$V_{\text{RMS}}$
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		100		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS, $f=1\text{kHz}$		89		dB
THD	Total Harmonic Distortion	no load, $f=1\text{kHz}$ , -1dB FS input		-80		dB
		$P_{\text{OUT}}=20\text{mW}$ , $R_L=32\Omega$ , $f=1\text{kHz}$ , -1dB FS		-79		dB
		$P_{\text{OUT}}=40\text{mW}$ , $R_L=16\Omega$ , $f=1\text{kHz}$ , -1dB FS		-78	-60	dB
CS	Channel Separation	$R_L=32\Omega$		-61		dB
		$R_L=16\Omega$		-60		dB
<b>Line Input to HP Output</b>						
FS	Full Scale Output	$R_L=32\Omega$ , $f=1\text{kHz}$ , $1V_{\text{RMS}}$ (FS) input		0,834		$V_{\text{RMS}}$
		$R_L=16\Omega$ , $f=1\text{kHz}$ , $1V_{\text{RMS}}$ (FS) input		0,827		$V_{\text{RMS}}$
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		101		dB
THD	Total Harmonic Distortion	no load, $f=1\text{kHz}$ , $1V_{\text{RMS}}$		-72		dB
		$P_{\text{OUT}}=20\text{mW}$ , $R_L=32\Omega$ , $f=1\text{kHz}$ , $1V_{\text{RMS}}$		-72		dB
		$P_{\text{OUT}}=40\text{mW}$ , $R_L=16\Omega$ , $f=1\text{kHz}$ , $1V_{\text{RMS}}$		-72	-60	dB
CS	Channel Separation	$R_L=32\Omega$		84		dB
		$R_L=16\Omega$		72		dB
<b>Mic Input to Line Output</b>						
FS	Full Scale Output	$f=1\text{kHz}$ , $27\text{mV}_{\text{RMS}}$ FS input		0,950		$V_{\text{RMS}}$
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		80		dB
THD	Total Harmonic Distortion	1kHz $27\text{mV}_{\text{RMS}}$ FS input		-77		dB
<b>Mic Input to ADC Output</b>						
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		81		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS, $f=1\text{kHz}$		84		dB
THD	Total Harmonic Distortion	1kHz $27\text{mV}_{\text{RMS}}$ FS input		-65		dB

BVDD=+3.6V, VDD27=+2.7V, HPVDD=VDD=1.8V, VDD17=+1.7V,  $f_S=48\text{kHz}$ ,  $T_A=+25^\circ\text{C}$ , unless otherwise specified.

Table 6. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>DAC Input to Line Output</b>						
FS	Full Scale Output	$R_L = 10\text{k}\Omega$ , $f=1\text{kHz}$ , $1V_{\text{RMS}}$ input		0,568		$V_{\text{RMS}}$
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		96		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS, $f=1\text{kHz}$		95		dB
THD	Total Harmonic Distortion	1kHz -1dB FS input, $R_L=10\text{k}\Omega$		-90		dB
CS	Channel Separation	$R_L=10\text{k}\Omega$		62		dB
<b>Line Input to Line Output</b>						
FS	Full Scale Output	$R_L = 10\text{k}\Omega$ , $f=1\text{kHz}$ , $545mV_{\text{RMS}}$ input		0,545		$V_{\text{RMS}}$
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		97		dB
THD	Total Harmonic Distortion	1kHz $1V_{\text{RMS}}$ (-1dB FS) input, $R_L=10\text{k}\Omega$		-81		dB
CS	Channel Separation	$R_L=10\text{k}\Omega$		100		dB
<b>DAC Input to HP Output</b>						
FS	Full Scale Output	$R_L=32\Omega$		0,560		$V_{\text{RMS}}$
		$R_L=16\Omega$		0,550		$V_{\text{RMS}}$
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		97		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS, $f=1\text{kHz}$		88		dB
THD	Total Harmonic Distortion	no load, $f=1\text{kHz}$ , FS input		-87		dB
		$P_{\text{OUT}}=6\text{mW}$ , $R_L=32\Omega$ , $f=1\text{kHz}$ , -1dB FS		-81		dB
		$P_{\text{OUT}}=12\text{mW}$ , $R_L=16\Omega$ , $f=1\text{kHz}$ , -1dB FS		-78	-60	dB
CS	Channel Separation	$R_L=32\Omega$		63		dB
		$R_L=16\Omega$		60		dB
<b>Line Input to HP Output</b>						
FS	Full Scale Output	$R_L = 32\Omega$ , $f=1\text{kHz}$ , $545mV_{\text{RMS}}$ (FS) input		0,450		$V_{\text{RMS}}$
		$R_L = 16\Omega$ , $f=1\text{kHz}$ , $545mV_{\text{RMS}}$ (FS) input		0,447		$V_{\text{RMS}}$
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		97		dB
THD	Total Harmonic Distortion	no load, $f=1\text{kHz}$ , $545mV_{\text{RMS}}$		-77		dB
		$P_{\text{OUT}}=6\text{mW}$ , $R_L=32\Omega$ , $f=1\text{kHz}$ , $545mV_{\text{RMS}}$		-75		dB
		$P_{\text{OUT}}=12\text{mW}$ , $R_L=16\Omega$ , $f=1\text{kHz}$ , $545mV_{\text{RMS}}$		-75	-60	dB
CS	Channel Separation	$R_L = 32\Omega$		77		dB
		$R_L = 16\Omega$		66		dB
<b>Mic Input to Line Output</b>						
FS	Full Scale Output	$f=1\text{kHz}$ , $27mV_{\text{RMS}}$ FS input		0,512		$V_{\text{RMS}}$
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		75		dB
THD	Total Harmonic Distortion	1kHz $27mV_{\text{RMS}}$ FS input		77		dB
<b>Mic Input to ADC Output</b>						
SNR	Signal to Noise Ratio	A-weighted, no load, silence input		77		dB
DR	Dynamic Range	A-weighted, no load, -60dB FS, $f=1\text{kHz}$		84		dB
THD	Total Harmonic Distortion	1kHz $27mV_{\text{RMS}}$ FS input		-64		dB

## 7 Typical Operating Characteristics

BVDD = +3.6V, T<sub>A</sub> = +25°C, unless otherwise specified.

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## 8 Detailed Description - Audio Functions

### 8.1 Audio Line Inputs (2x)

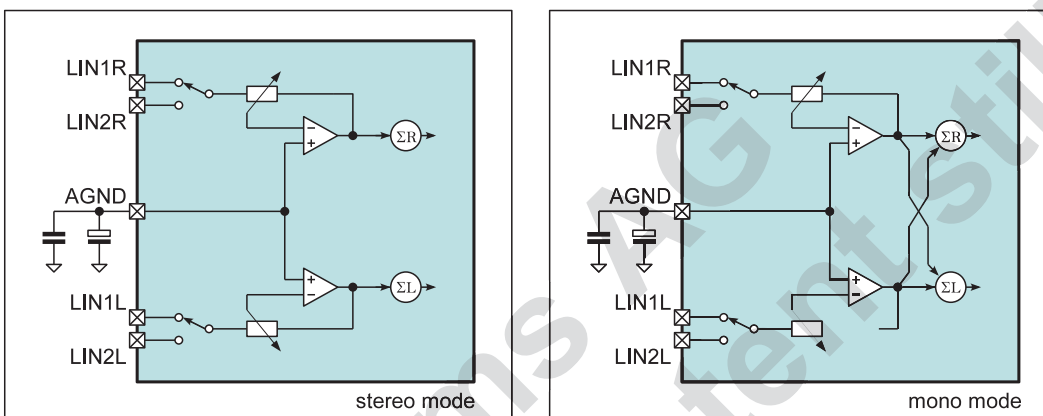
#### 8.1.1 General

The chip features two identical line inputs. The blocks can work in 2x mono single ended or in stereo single ended mode.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each and MUTE. The gain can be set from  $-40.5\text{dB}$  to  $+6\text{dB}$ . The stage is set to mute by default. If the line input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

Line Input 1 and 2 are sharing one gain stage.

Figure 3. Line Inputs



#### 8.1.2 Parameter

AVDD17=1.7V, AVDD27=2.7V,  $T_A=25^{\circ}\text{C}$ , unless otherwise mentioned

Table 7. Line Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{LIN}$	Input Signal Level	Pls observe gain settings. Max. peak levels at any node within the circuit shall not exceed AVDD		AVDD17 /3	AVDD17 /2	$V_{PEAK}$
$R_{LIN}$	Input Impedance	depending on gain setting		8-25		$k\Omega$
$\Delta R_{LIN}$	Input Impedance Tolerance			$\pm 30$		%
$C_{LIN}$	Input Capacitance			5		pF
$A_{LIN}$	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Accuracy			$\pm 0.25$		dB
$A_{LINMUTE}$	Mute Attenuation			100		dB



### 8.1.3 Register Description

Table 8. Line Input Related Register

Name	Base	Offset	Description
LINE_IN_R	2-wire serial	0Ah	Right Line Input 1/2 settings, Line Input 2 selection
LINE_IN_L	2-wire serial	0Bh	Left Line Input 1/2 settings
AudioSet1	2-wire serial	14h	Enable/disable driver stage
AudioSet3	2-wire serial	16h	Enable/disable mixer input

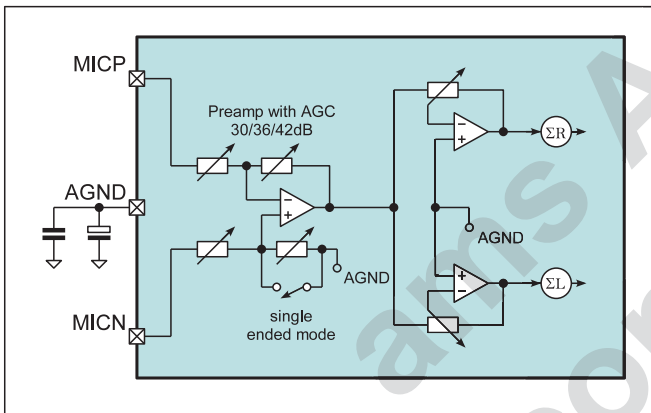
Line input has to be enabled in register 14h first before other settings in register 0Ah and 0Bh can be programmed.

## 8.2 Microphone Input

### 8.2.1 General

The AFE offers one microphone input and one low noise microphone voltage supply (microphone bias), voice activation, microphone connect detection and push button remote control.

Figure 4. Microphone Input



### 8.2.2 Gain Stage & Limiter

The integrated pre-amplifier allows 3 preset gain settings. There is also a limiter which attenuates high input signals from e.g. electret microphones signal to 1Vp. The AGC has 128 steps with 0.375dB with a dynamic range of the full pre-amplifier level. The AGC is ON by default but can be disabled by a microphone register bit.

Apart from the microphone pre-amplifier the microphone input signal can further be amplified with 32 @1.5dB programmable logarithmic gain steps and MUTE. All gains and MUTE are independently programmable. The gain can be set from -40.5dB to +6dB.

The stage features a soft-start function. Pre-amplifier and gain-stage settings can be set before enabling the microphone stage. After enabling the stage to gain is automatically set to the defined value by using the 128 steps of the AGC.

### 8.2.3 Supply & Detection

Each microphone input generates a supply voltage of 1.5V above HPCM. The supply is designed for  $\leq 2\text{mA}$  and has a 6.5mA current limit. In OFF mode the MICS terminal is pulled to AVDD with 20kOhm. A current of typically 50uA generates an interrupt to inform the CPU, that a circuit is connected. When using HPCM as headset ground the HP-stage gives the interrupt. After enabling the HP-stage through the CPU the microphone detection interrupt will follow.

When using the MICS terminal as ADC-10 input to monitor external voltages the 20kOhm pull-up has to be disabled by disabling the interrupt for microphone detection.

### 8.2.4 Remote Control

Fast changes of the supply current of typically 500uA are detected as a remote button press, and an interrupt is generated. Then the CPU can start the measurement of the microphone supply current with the internal 10-bit ADC to distinguish which button was pressed. As the current measurement is done via an internal resistor, only two buttons generating a current of about 0.5mA and 1mA can be detected. With this, 1mA as microphone bias is still available.

### 8.2.5 Voice Activation

Further a built-in voice activation comparator can actuate an interrupt if microphone input voltage of about 5mVRMS is detected.

### 8.2.6 Parameter

AVDD17=1.7V, AVDD27=2.7V, T<sub>A</sub>= 25°C unless otherwise mentioned

Table 9. Microphone Input Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>MICIN0</sub>	Input Signal Level	A <sub>MICPRE</sub> = 30dB; A <sub>MIC</sub> = 0dB		20		mV <sub>P</sub>
V <sub>MICIN1</sub>		A <sub>MICPRE</sub> = 36dB; A <sub>MIC</sub> = 0dB		10		mV <sub>P</sub>
V <sub>MICIN2</sub>		A <sub>MICPRE</sub> = 42dB; A <sub>MIC</sub> = 0dB		5		mV <sub>P</sub>
R <sub>MICIN</sub>	Input Impedance	MICP, MICN to AGND		7.5		kΩ
Δ <sub>MICIN</sub>	Input Impedance Tolerance			-7 +33		%
C <sub>MICIN</sub>	Input Capacitance			5		pF
A <sub>MICPRE</sub>	Microphone Preamplifier Gain	Preamplifier has 3 selectable (fixed) gain settings		30 36 42		dB
A <sub>MIC</sub>	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Precision			±0.25		dB
V <sub>ATTACK</sub>	Limiter Activation Level			0.57		V <sub>PEAK</sub>
V <sub>DECAY</sub>	Limiter Release Level			0.47		V <sub>PEAK</sub>
A <sub>MICLIMIT</sub>	Limiter Gain Overdrive	128 @ 0.375dB		30 36 42		dB
t <sub>ATTACK</sub>	Limiter Attack Time			50		μs/6dB
t <sub>DECAY</sub>	Limiter Decay Time			120		ms/ 6dB
A <sub>MICMUTE</sub>	Mute Attenuation			100		dB
V <sub>MICSUP</sub>	Microphone Supply Voltage	depending on V_MICS setting		2 1.55 1.26 1.06		V
I <sub>MICMAX</sub>	Max. Microphone Supply Current	microphones nominally need a bias current of 0.5mA-1mA		6.5		mA
V <sub>NOISE</sub>	Microphone Supply Voltage Noise			5		μV
I <sub>MICDET</sub>	Microphone Detection Current			50		μA
I <sub>REMDT</sub>	Max. Remote Detection Current			500		μA

## 8.2.7 Register Description

Table 10. Microphone Input Related Register

Name	Base	Offset	Description
MIC_R	2-wire serial	06h	Right Microphone Input volume settings, AGC control
MIC_L	2-wire serial	07h	Left Microphone Input volume settings, MIC supply control
AudioSet1	2-wire serial	14h	Enable/disable driver stage
AudioSet3	2-wire serial	16h	Enable/disable mixer input
IRQENRD_1	2-wire serial	24h	Interrupt settings for microphone voice activation
IRQENRD_3	2-wire serial	26h	Interrupt settings for microphone detection
IRQENRD_4	2-wire serial	27h	Interrupt settings for remote button press detection

## 8.3 Line Output

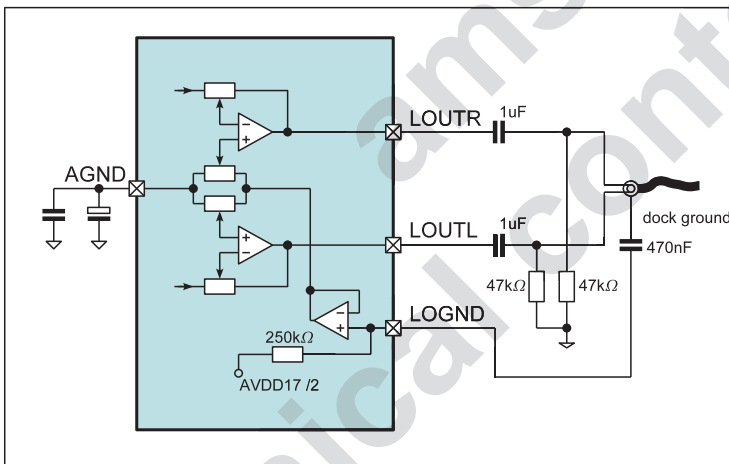
### 8.3.1 General

The line output is designed to provide the audio signal with a typical  $V_{PEAK}$  level at a load of minimum  $10k\Omega$ , which is a minimum value for line inputs. If the limiters (N20/N21) are deactivated the peak output voltage is  $AVDD17/2 V_p$ .

This AFE has a combined output stage for headphone and line output with an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -40.5dB to +6dB.

If the line output is not enabled, the volume settings are set to their default values. Changing of volume and mute control can only be done after enabling the output.

Figure 5. Line Output



### 8.3.2 Auto Fading

By setting a new output volume level, the stage does an automatic fading from the current gain setting to the new target. Changing the input multiplexer from one source to another will be done by fading out to mute, source changing and fading in of the new source to the target volume. Change from HPH-out to LINE-out is done by fading out of HPH-out to mute and fading in of the LINE-out to the target volume.

The fading speed can be programmed to 3 different speed levels. The immediate response can be selected as 4th state.

### 8.3.3 Ground Noise Cancellation

A separate ground input allows to connect a ground sense line direct from the dock connector ground or line out jack shield to make the audio output independent from PCB ground noise.

### 8.3.4 Parameter

AVDD17=1.7, AVDD27=2.7,  $T_A=25^{\circ}\text{C}$ , unless otherwise mentioned

Table 11. Line Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$R_{L\_LO}$	Load Impedance (Stereo Mode)	line inputs nominally have 10k $\Omega$	5			k $\Omega$
$C_{L\_LO}$	Load Capacitance (Stereo Mode)				100	pF
$A_{LO}$	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Accuracy			$\pm 0.25$		dB
$A_{LOMUTE}$	Mute Attenuation			100		dB

### 8.3.5 Register Description

Table 12. Line Output Related Register

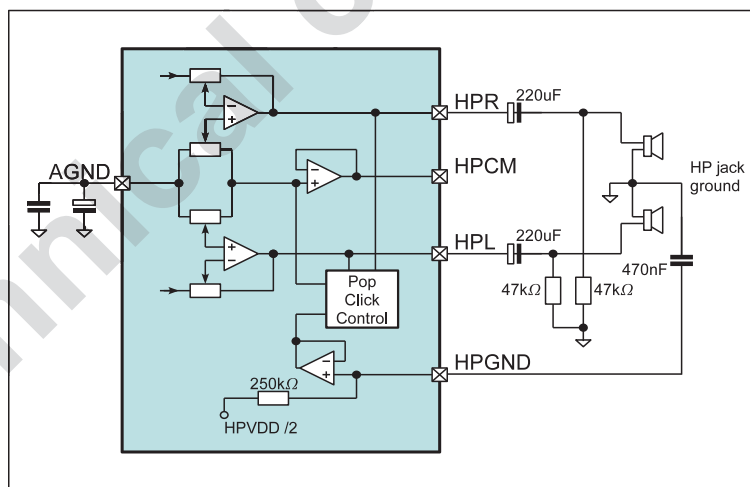
Name	Base	Offset	Description
<a href="#">OUT_R</a>	2-wire serial	00h	Right Line Output volume settings, MUX control
<a href="#">OUT_L</a>	2-wire serial	01h	Left Line Output volume settings
<a href="#">AudioSet2</a>	2-wire serial	15h	Auto fading timing settings
<a href="#">AudioSet3</a>	2-wire serial	16h	Enable/disable mixer input

## 8.4 Headphone Output

The headphone output is designed to provide the audio signal with 2x40mW @ 16 $\Omega$  or 2x20mW @32 $\Omega$ , which are typical values for headphones.

This AFE has a combined output stage for headphone and line output with an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -40.5dB to +6dB.

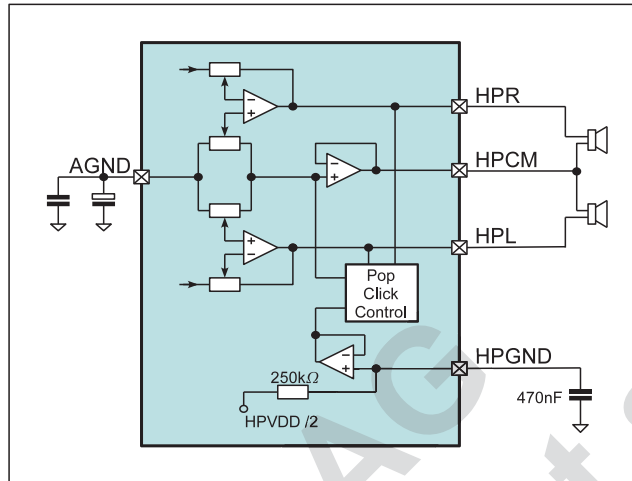
Figure 6. Headphone Output



### 8.4.1 Phantom Ground

There are 2 ways to connect a headphone to the AFE. In order to spare the bulky ac/dc de-coupling capacitors at pins HPR/HPL a buffered ground (Phantom Ground) is provided. This Common Mode Buffer needs to be switched on if utilized. If form factor considerations are less stringent, the headphones can be conventionally connected via 2x200 $\mu$ F capacitors.

Figure 7. Headphone Output using Common Mode Buffer



### 8.4.2 No-Pop Function

The output is automatically set to mute when the output stage is disabled.

To avoid Pop-Click noise during power-up and shut-down of the headphone amplifier, a charge/discharge control of HPGND (0V-HPVDD/2-0V) at pins HPR/HPL is incorporated into the AFE. The 470nF capacitor at pin HPGND is used to form the charge/discharge slope. Pls observe that pin HPGND is a high impedance node which must not be connected to any other external device than the 470nF buffer capacitor. To avoid Pop-Click noise one has to wait for 750ms in between a power-down (switch-off) and a power-up (switch-on) of the headphone amplifier.

### 8.4.3 Auto Fading

By setting a new output volume level, the stage does a automatic fading from the current gain setting to the new target. Changing the input multiplexer from one source to another will be done by fading out to mute, source changing and fading in of the new source to the target volume. Change from HPH-out to LINE-out is done by fading out of HPH-out to mute and fading in of the LINE-out to the target volume.

The fading speed can be programmed to 3 different speed levels. The immediate response can be selected as 4th state.

Figure 8. Headphone Startup with MaxGain Settings

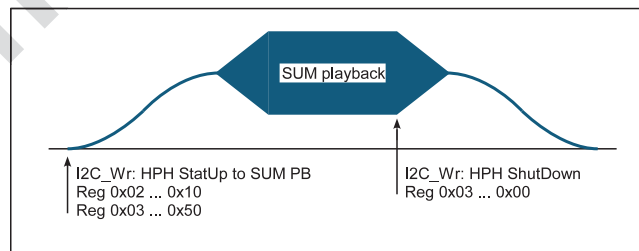
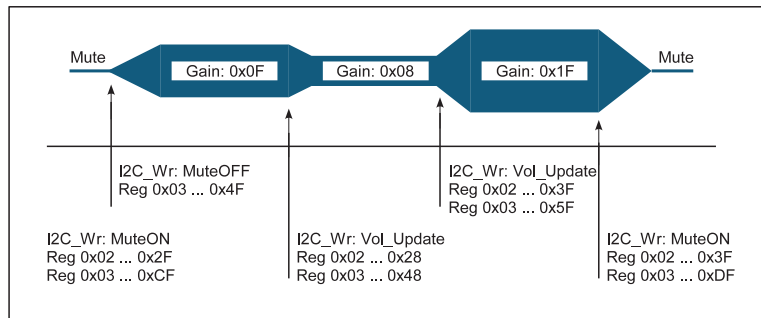




Figure 9. Headphone Change Gain Settings



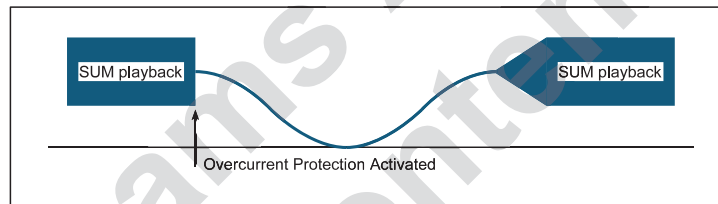
#### 8.4.4 Headphone Detection

When the headphone amplifier is powered down, one can detect the connection of a headset. It only work if the headset is connected between pins HPR/HPL and HPCM. As long as the headphone amplifier is powered down, HPCM is biased to 150mV and acting as the sense pin. There is a corresponding interrupt available to be enabled.

#### 8.4.5 Over-current Protection

The headphone amplifier has an over-current protection (e.g. HPR/HPL is shorted). This over-current protection will power down the headphone amplifier for a programmable time-out period (512ms, 0ms). There is a corresponding interrupt available to be enabled.

Figure 10. Headphone Overcurrent OFF-ON Sequence



#### 8.4.6 Ground Noise Cancellation

As separate ground input allows to connect a ground sense line direct from the dock connector ground or headphone jack shield to make the audio output independent from PCB ground noise.

#### 8.4.7 Power Options

To save power, especially when driving 32 Ohm loads, a reduction of the bias current is selected. For 16Ohm loads the bias current can be increased.

#### 8.4.8 Parameter

AVDD17=1.7, AVDD27=2.7, HPVDD = 2.7V,  $T_A = 25^{\circ}\text{C}$ , unless otherwise mentioned

Table 13. Headphone Output Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
RL_HP	Load Impedance	stereo mode	16			$\Omega$
CL_HP	Load Capacitance	stereo mode			100	pF
P_HP	Nominal Output Power	RL=16 $\Omega$ , limiter enabled RL=32 $\Omega$ , limiter enabled		40 20		mW
A_HP	Programmable Gain		-40.5		+6	dB
	Gain Steps	discrete logarithmic gain steps		1.5		dB
	Gain Step Accuracy			$\pm 0.25$		dB

Table 13. Headphone Output Parameter (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Over current limit	HPR/HPL pins HPCM pin, @1.8V		70mA 110mA		mA mA
	Over current limit	HPR/HPL pins HPCM pin, @2.7V		140mA 220mA		mA mA
P <sub>SRRHP</sub>	Power Supply Rejection Ratio	200Hz-20kHz, 720mVpp, RL=16Ω		90		dB
AHPMUTE	Mute Attenuation			100		dB

### 8.4.9 Register Description

Table 14. Headphone Related Register

Name	Base	Offset	Description
OUT_R	2-wire serial	02h	Right HP Output volume and over-current settings
OUT_L	2-wire serial	03h	Left HP Output volume settings, enable and detection control
AudioSet2	2-wire serial	15h	Auto fading timing settings
AudioSet3	2-wire serial	16h	Power options, common mode buffer enable
IRQENRD_3	2-wire serial	26h	Interrupt settings for over current and HP detection

## 8.5 DAC, ADC and I2S Digital Audio Interface

### 8.5.1 Input

The AFE receives serialized audio data for the DAC via pin SDI. The output of the DAC is fed through a volume control to the mixer stage and to the multiplexers of line output and headphone amplifiers or direct to these output stages.

This serialized audio data is a digital audio data stream with the left and the right audio channels multiplexed into one bit-stream. Via pin LRCK the alignment clock is input to the DAC digital filters. LRCK (Left Right Clock) indicates whether the serial bit-stream received via pin SDI, represents right channel or left channel audio data. Via pin SCLK the bit clock for the serial bit-stream is signalled. SDI and LRCK are synchronous with SCLK. SDI, LRCK and SCLK are inputs; SDO is not used.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -40.5dB to +6dB. The stage is set to mute by default. If the DAC input is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

### 8.5.2 Output

This block consists of an audio multiplexer where the signal, which should be recorded, can be selected. The output is then fed through a volume control to the audio ADC. The digital output is done via an I2S interface.

The AFE sends serialized audio data from the ADC via pin SDO. This serialized audio data is a digital audio data stream with the left and the right audio channels multiplexed into one bit-stream. Via pin LRCK the alignment clock is signalled to the connected devices (e.g. CPU). LRCLK (Left Right Clock) indicates whether the serial bit-stream sent via pin SDI, presents right channel or left channel audio data. Via pin SCLK the bit clock for the serial bit-stream is signalled. SDO and LRCK are synchronous with SCLK. SDO is an output; LRCK and SCK are inputs; SDI is not used.

The volume control has an independent gain regulation for left and right channel with 32 steps @ 1.5dB each. The gain can be set from -34.5dB to +12dB. The stage is set to mute by default. If the ADC output is not enabled, the volume settings are set to their default values. Changing the volume and mute control can only be done after enabling the input.

The I2S output uses the same clocks as the I2S input. The sampling rate therefore depends also on the input sampling rate. The exact ratio can be set in register 11h.

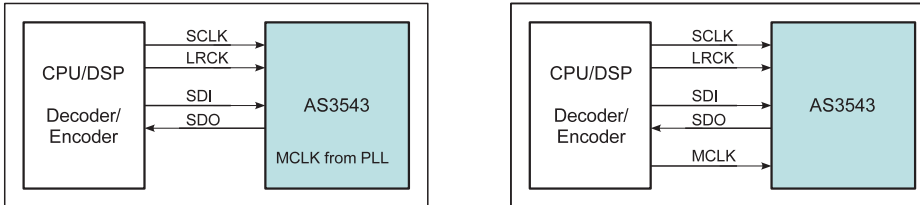
The SDO output can be configured to operate in push/pull (3 different driver strengths) or to be tri-state. For a more detailed description of the GPIO functionality of this pin please refer to chapter [GPIO Pins on page 50](#).

### 8.5.3 I2S Modes

The AFE can be operated either in Slave Mode or in Slave Mode with the master clock directly signalled via pin MCLK. The master clock (MCLK) is the necessary internal over-sampling clock for the DAC and ADC (e.g.  $128 \cdot f_s$ ,  $f_s$ =audio sampling frequency)

In Slave Mode the PLL generates the master clock based on LRCK. Thus the PLL needs to be preset to the expected sampling frequency. The ranges are 8kS-23kS (8kHz-23kHz) and 24kS-48kS (24kHz-48kHz). Please refer to register 1A-7h.

Figure 11. I2S Modes



### 8.5.4 Clock Supervision

The digital audio interface automatically checks the LRCK. An interrupt can be generated when the state of the LRCK input changes. A bit in the interrupt register represents the actual state (present or not present) of the LRCK.

### 8.5.5 Signal Description

The digital audio interface uses the standard I2S format:

- left justified
- MSB first
- one additional leading bit

The on-chip synchronization circuit allows any bit-count up to 32bit. When there are less than 18 bits sampled, the data sample is completed with "0"s. In I2S direct mode the data length has to be minimum 18 bits.

The ADC output is always 14 bit. If more SCLK pulses are provided, only the first 14 will be significant. All following bits will be "0".

SCLK has not to be necessarily synchronous to LRCK but the high going edge has to be separate from LRCK edges. The LRCK signal has to be derived from a jitter-free clock source, because the on-chip PLL is generating a clock for the digital filter, which has to be always in correct phase lock condition to the external LRCK.

Please observe that LRCK has to be activated before enabling the ADC.