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# AS3561

## Class-H Stereo Headphone Amplifier

## General Description

The AS3561 is a Class-H stereo headphone amplifier optimized for usage within portable devices. The Class-H supply rail adaptation is implemented by an integrated DCDC buck converter that takes its input directly from the battery. The continuous adoption of supply rails is done according to the input signal swing and load conditions. This architecture implements significant power savings compared to traditional Class-AB amplifiers.

An I²C control interface is implemented for a 32-step volume control including a mute function for each channel separately.

The integrated charge pump generates a symmetric negative supply for true ground output signal levels without the need of output coupling capacitors. In addition it helps to lower the overall pop noise of the amplifier.

A supervisory circuit is included for overtemperature and short-circuit protection.

Differential inputs together with output ground sensing guarantees very low noise sensitivity.

*Ordering Information* and *Content Guide* appear at end of datasheet.

### Key Benefits & Features

The benefits and features of the AS3561 Class-H stereo headphone amplifier, are listed below:

**Figure 1:**
**Added value of using AS3561**

| Benefits | Features |
|---|---|
| Highly optimized system power consumption | H-Class amplifier with integrated DCDC buck converter<br>• 2x30mW, 0.02% THD @ 16Ω<br>• 100dB SNR @ 0.9Vrms<br>• 1mA quiescent with both channels enabled |
| Popless startup and mute/unmute | Ultra low DC offset |
| Full digital system control | I²C control interface |
| Direct Li-Ion battery operation | Wide supply range 2.3V to 5.5V |
| No DC blocking capacitors | Charge pump for true ground headphone operation |
| Highest Noise Immunity | Two fully differential stereo inputs with ground sensing input |
| PCB area optimized | Package: 0.4mm Pitch WL-CSP (1.615 x 1.615mm) |

## Applications

The AS3561 applications include:

- Mobile Phones
- Portable Navigation Devices
- Media Devices

## Block Diagram

The functional blocks of this device for reference are shown below:

**Figure 2:**
**AS3561 Block Diagram**
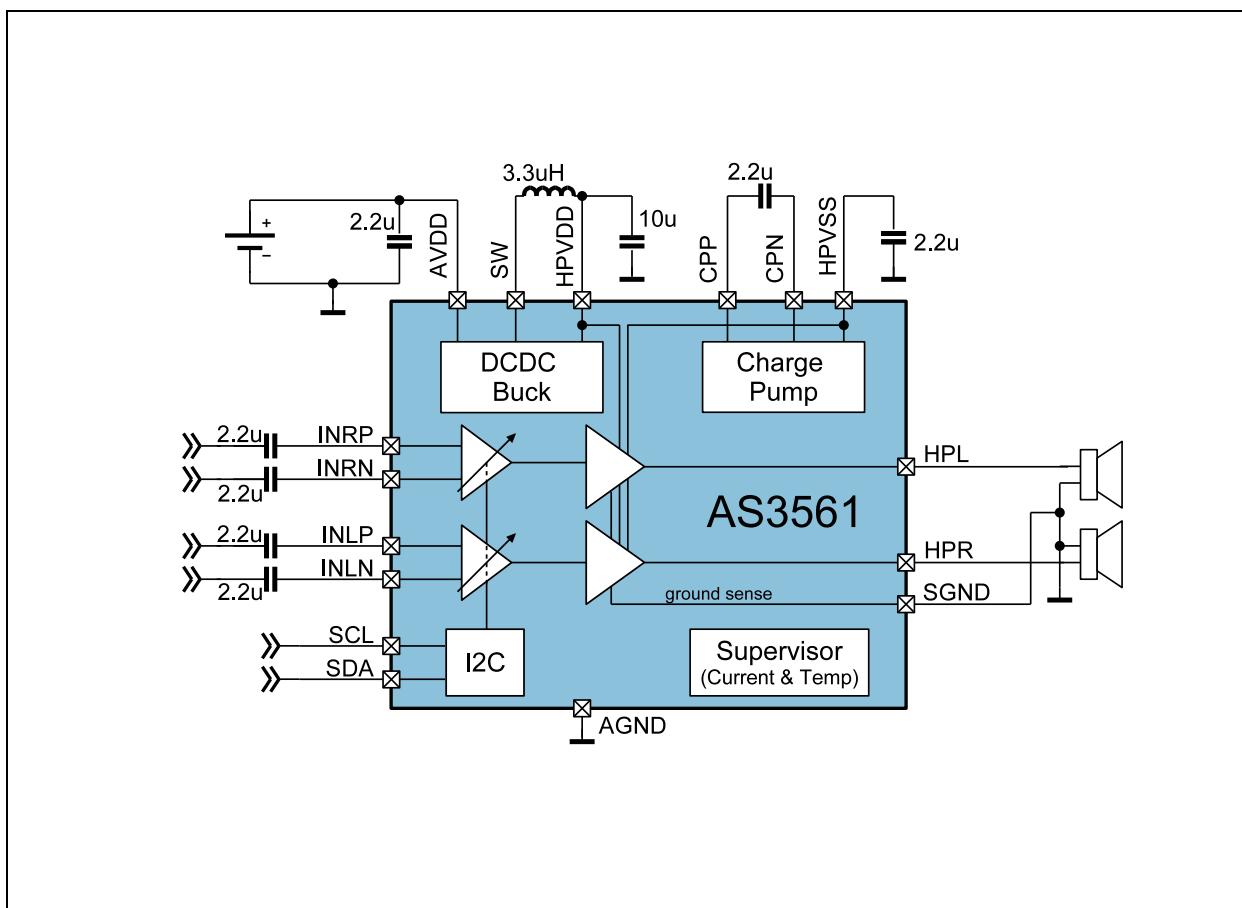
## Pin Assignments

The AS3561 pin assignments are described below:

**Figure 3:**
**Pin Assignments (Top View)**
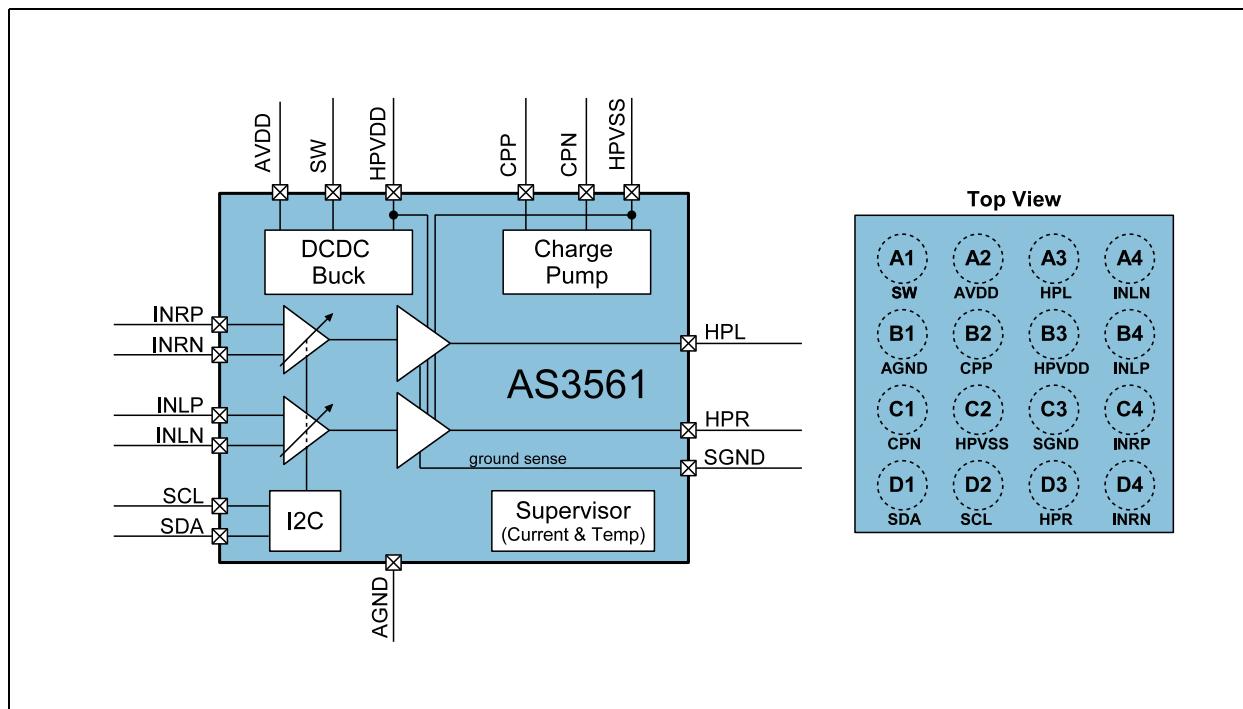


## Pin Descriptions

**Figure 4:**
**Pin Descriptions**

| Pin Name | Pin Number | Description |
|----------|------------|-------------|
| SW | A1 | Buck converter switching node |
| AVDD | A2 | Primary power supply for device |
| HPL | A3 | Left channel headphone amplifier output |
| INLN | A4 | Inverting left input for differential signals;<br>Connect to left input signal through 2.2µF capacitor for single-ended input applications |
| AGND | B1 | Main Ground for headphone amplifiers, DC/DC converter, and charge pump |
| CPP | B2 | Charge pump positive flying cap; connect to 2.2µF flying capacitor |
| HPVDD | B3 | Power supply for headphone amplifier (DC/DC output node) |
| INLP | B4 | Non-inverting left input for differential signals;<br>Connect to ground through 2.2µF capacitor for single-ended input applications |

| Pin Name | Pin Number | Description |
|----------|------------|-------------|
| CPN | C1 | Charge pump negative flying cap; connect to 2.2µF flying capacitor |
| HPVSS | C2 | Charge pump output; connect 2.2µF capacitor to GND |
| SGND | C3 | Ground sense; connect to headphone jack ground |
| INRP | C4 | Non-Inverting right input for differential signals; Connect to right input signal through 2.2µF capacitor for single-ended input applications |
| SDA | D1 | I²C Data; 1.8V logic compliant |
| SCL | D2 | I²C Clock; 1.8V logic compliant |
| HPR | D3 | Right channel headphone amplifier output |
| INRN | D4 | Inverting right input for differential signals; Connect to ground through 2.2µF capacitor for single-ended input applications |

## Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 5:**
**Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Unit | Comments |
|--------|-----------|-----|-----|------|----------|
| AVDD | Supply voltage | -0.3 | 7 | V | for 1ms peaks |
| HPVDD | Amplifier supply voltage | -0.3 | 2.0 | V | |
| SGND | | -0.3 | 0.3 | V | |
| | Differential Input voltage | HPVSS - 0.3V | HPVDD + 0.3V | V | |
| | Input voltage at SCL, SDA | -0.3 | 7.0 | V | |
| | Breakdown voltage at amplifier outputs | -0.5 | HPVDD + 0.5 | V | |
| | Input current (latchup immunity) | | ±200 | mA | Norm: JEDEC 78 |
| **Continuous Power Dissipation** | | | | | |
| | Continuous power dissipation | | TBD | mW | $P_T$ [1] |
| | Continuous power dissipation derating factor | | TBD | mW/°C | $P_{DERATE}$ [2] |
| **Electrostatic Discharge** | | | | | |
| ESD HBM | | | ±2 | kV | Norm: MIL 883 E Method 3015 |
| ESD MM | | | ±100 | V | Norm: JEDEC JESD 22-A115-A level A |
| ESD CDM | | | ±500 | V | Norm: JEDEC JESD 22-C101C |

| Symbol | Parameter | Min | Max | Unit | Comments |
|--------|-----------|-----|-----|------|----------|
| | **Temperature Range and Storage Conditions** | | | | |
| | Junction Temperature | | +150 | °C | internally limited (overtemperature protection) auto shutdown at 140°C |
| | Storage Temperature Range | -55 | +125 | °C | |
| | Humidity non-condensing | 5 | 85 | % | |
| | Moisture Sensitive Level | | 1 | | Represents a max. floor life time of unlimited |
| | Package Body Temperature | | +260 | | The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 *"Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*. |

**Note(s) and/or Footnote(s):**

1. Depending on actual PCB layout and PCB used

2. $P_{DERATE}$ derating factor changes the total continuous power dissipation ($P_T$) if the ambient temperature is not 70°C.
   Therefore for e.g. TAMB=85°C calculate $P_T$ at 85°C = $P_T$ - $P_{DERATE}$ * (85°C - 70°C)

**ams**

## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

AVDD=3.6V, $T_A$=25°C, Rload = 32Ω unless otherwise specified.

**Figure 6:**
**Operating Conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **General Operating Conditions** | | | | | | |
| AVDD | Supply Voltage | | 2.3 | | 5.5 | V |
| | Rail Voltages HPVDD, HPVSS (Buck and CP output) | | 0.8 | 0.9 | 1.0 | V |
| | | | 1.15 | 1.25 | 1.35 | V |
| | | | 1.7 | 1.8 | 1.9 | V |
| $I_{DD}$ | Quiescent Current | both channels enabled, no audio signal | | 0.9 | 1.5 | mA |
| $I_{SD}$ | Shutdown Current | SW shutdown | | 1.8 | 5 | µA |
| $I_S$ | | Output: 2 × 100µW @ 3dB Crest Factor | | 1.7 | 2.3 | mA |
| | Supply Current | Output: 2 × 500µW @ 3dB Crest Factor | | 2.85 | 3.6 | mA |
| | | Output: 2 × 1mW @ 3dB Crest Factor | | 3.7 | 4.6 | mA |
| $T_A$ | Operating Temperature Range | | -30 | 25 | +85 | °C |
| $t_{WAKEUP}$ | Wakeup Time | | | 10 | 15 | ms |
| **Input Interfaces** | | | | | | |
| $V_{IL}$ | Low-level input voltage (SCL, SDA) | AVDD 2.9V to 4.5V | | | 0.6 | V |
| $V_{IH}$ | High-level input voltage (SCL, SDA) | AVDD 2.9V to 4.5V | 1.2 | | | V |
| $V_{HYST}$ | Hysteresis (SCL, SDA) | | 50 | 100 | 200 | mV |
| $Z_{IN}$ | Input Impedance Line Inputs | Differential | 20 | | | kΩ |
| | | Single Ended | 10 | | | kΩ |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **HPA Output** | | | | | | |
| V$_{OUT}$ | Output Voltage | Rload=16Ω, THD + N=1%, L+R out of phase | 0.7 | | | V$_{rms}$ |
| | | Rload=32Ω, THD + N=1%, L+R in phase | 0.9 | | | V$_{rms}$ |
| | Output DC Offset | Both channels enabled | | | 500 | µV |
| Z$_{OUT}$ | Output Impedance | In HiZ mode < 40KHz | | 10 | | kΩ |
| | | In HiZ mode for 6MHz | | 500 | | Ω |
| | | In HiZ mode for 36MHz | | 75 | | Ω |
| | Voltage applied to Output; HPR, HPL | when SWS = 0, HiZ_L = HiZ_R = 1,device in HI-Z mode | -1.8 | | 1.8 | V |
| C$_{LOAD}$ | Capacitive Load | ext. cap, 15Ω series resistor | 0.8 | 5 | 100 | nF |
| | | ext cap, directly connected | | | 100 | pF |
| Z$_{OOT,SD}$ | Output impedance in shutdown | SWS = 1 | | 8 | | kΩ |
| | Voltage applied to Output; HPR, HPL | when SWS = 1, device disabled | -0.3 | | 3.6 | V |
| **Audio Parameters** | | | | | | |
| THD + N | Total Harmonic Distortion + Noise | 700mV$_{rms}$, 1KHz | | 0.02 | 0.04 | % |
| PSRR | Power Supply Rejection Ratio | Gain 0dB @ 217Hz | | 90 | | dB |
| SNR | Signal-to-Noise Ratio | 900mV$_{rms}$, 1KHz | | 104 | | dB |
| | Channel Separation | >16Ω (Headset) | | 60 | | dB |
| | | >10kΩ (Lineout) | | 80 | | dB |
| V$_N$ | Output Noise | Gain 0dB, A-weighted | | 5.3 | 9 | µV$_{rms}$ |
| **Other Parameters** | | | | | | |
| | Thermal Shutdown | Threshold | | 140 | | °C |
| | | Hysteresis | | 20 | | |

## Detailed Operating Characteristics

$T_A = 25°C$, AVDD (VDD) = 3.6V, GAIN = 0dB, $C_{HPVDD} = 10μF$, $C_{HPVSS} = 2.2μF$, $C_{INPUT} = C_{FLYING} = 2.2μF$. RL = 32Ω unless otherwise specified.

**Figure 7:**
**THD + N versus output power for AVDD = 2.5V,RL = 32Ω**
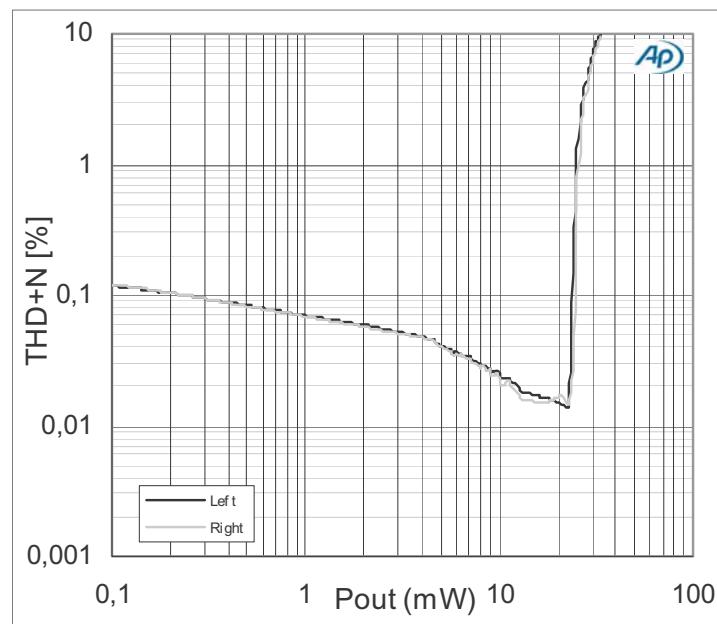


**Figure 8:**
**THD + N versus output power for AVDD = 2.5V,RL = 16Ω**
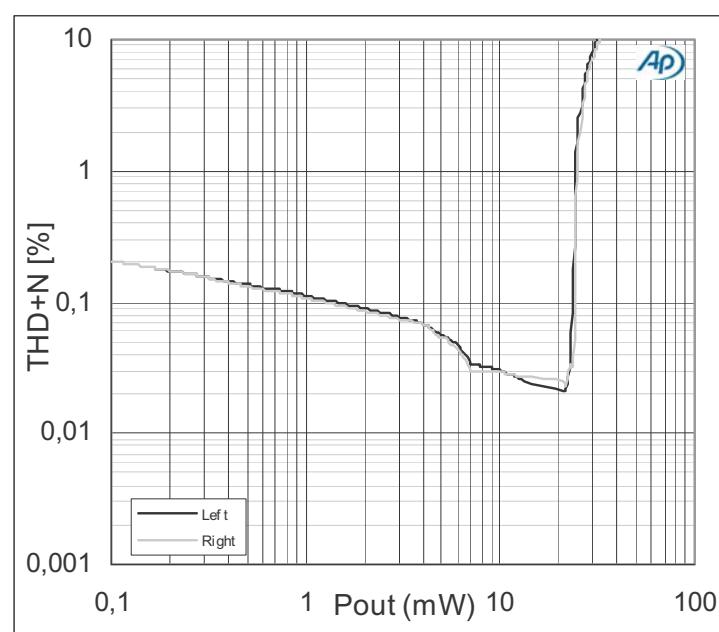
**Figure 9:**
**THD + N versus output power for AVDD = 3.6V, RL = 32Ω**
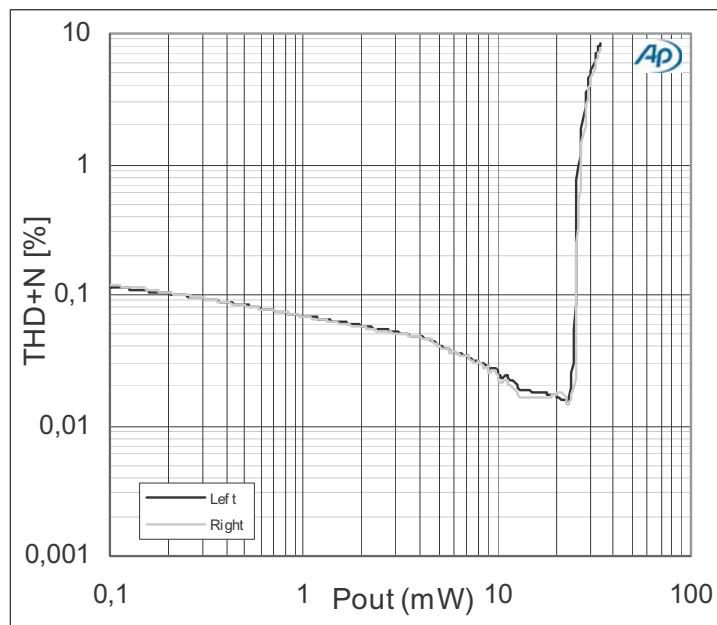


**Figure 10:**
**THD+ N versus output power for AVDD = 3.6V, RL = 16Ω**
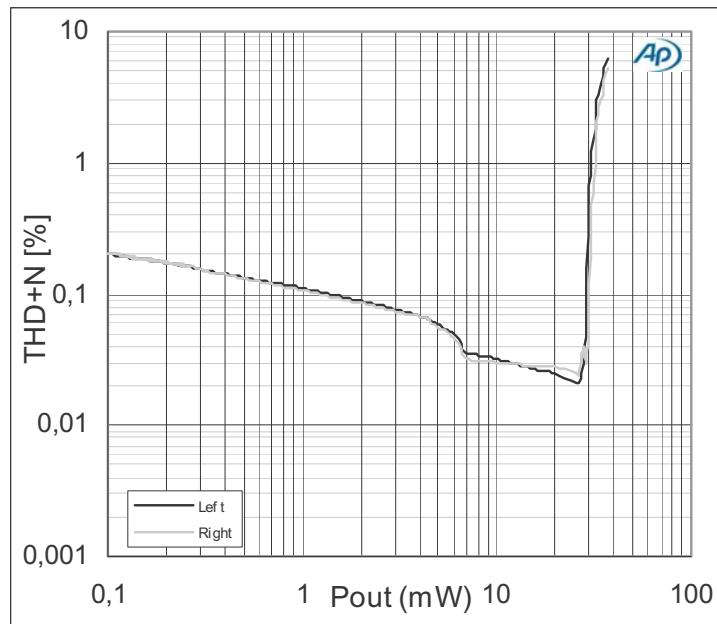
**Figure 11:**
**THD + N versus output power for AVDD = 5.5V,RL = 32Ω**
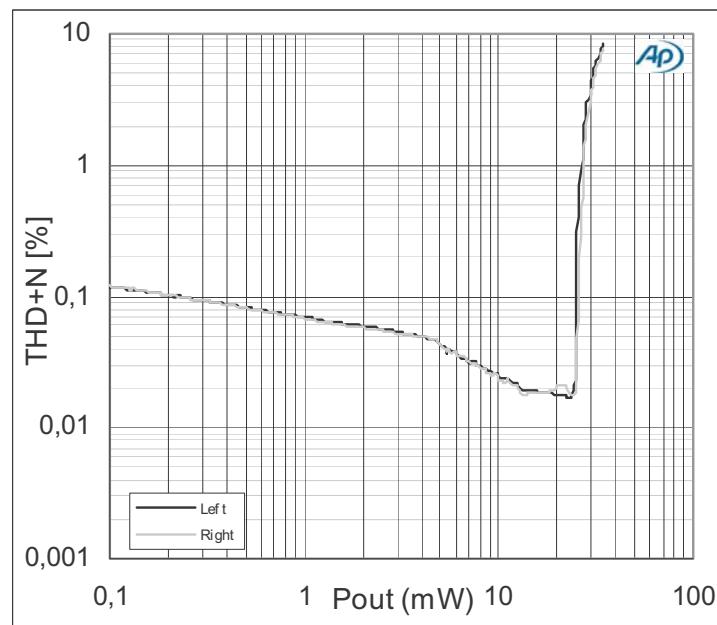


**Figure 12:**
**THD + N versus output power for AVDD = 5.5V,RL = 16Ω**
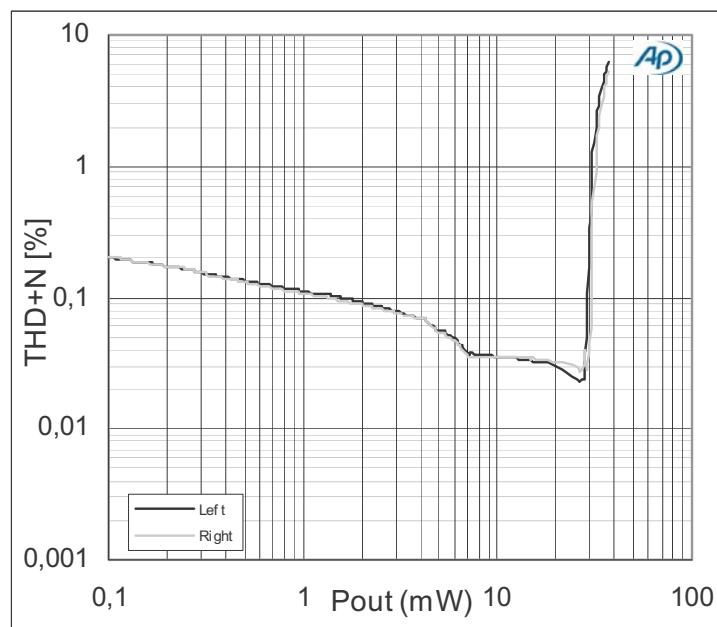
**Figure 13:**
**THD + N versus Frequency for AVDD = 2.5V,RL = 32Ω**
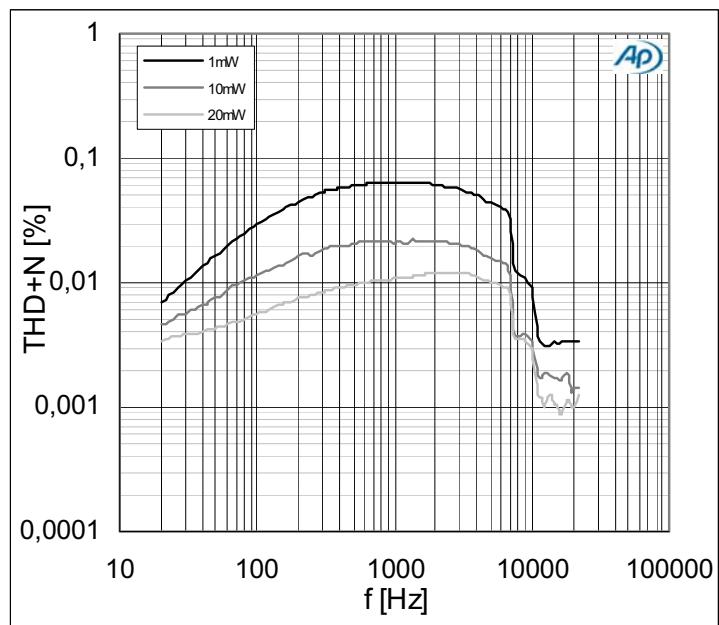


**Figure 14:**
**THD + N versus Frequency for AVDD = 2.5V,RL = 16Ω**
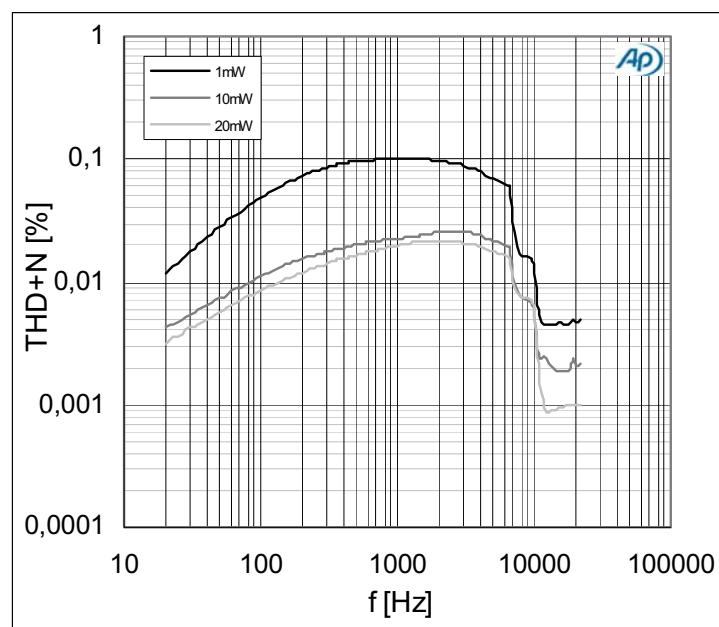
**Figure 15:**
**THD + N versus Frequency for AVDD = 3.6V,RL = 32Ω**
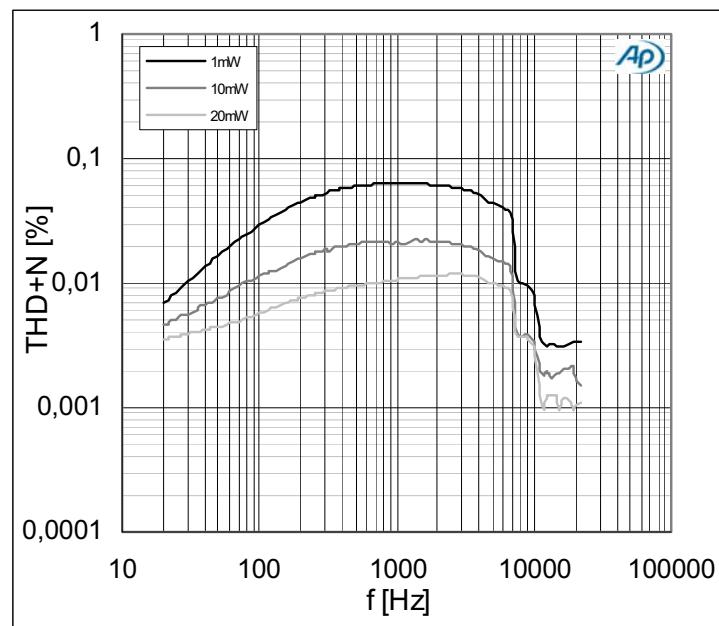


**Figure 16:**
**THD + N versus Frequency for AVDD = 3.6V,RL = 16Ω**
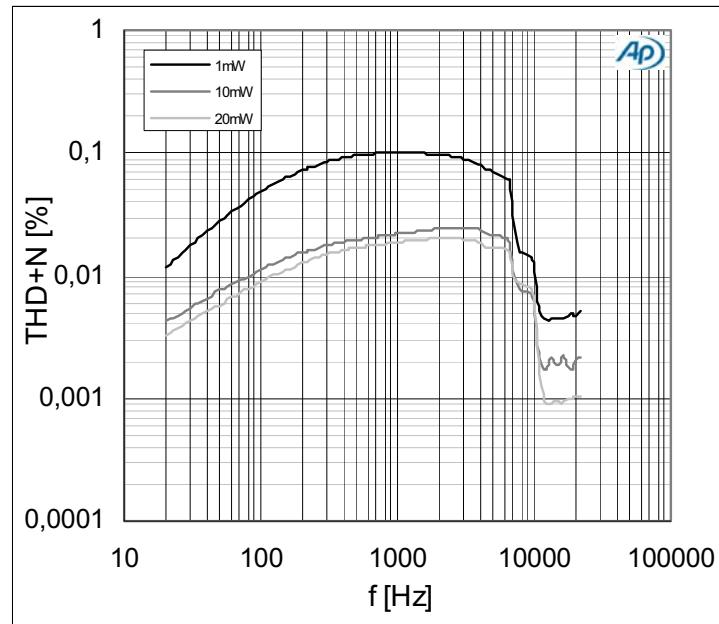
**Figure 17:**
**THD + N versus Frequency for AVDD = 5.5V,RL = 32Ω**
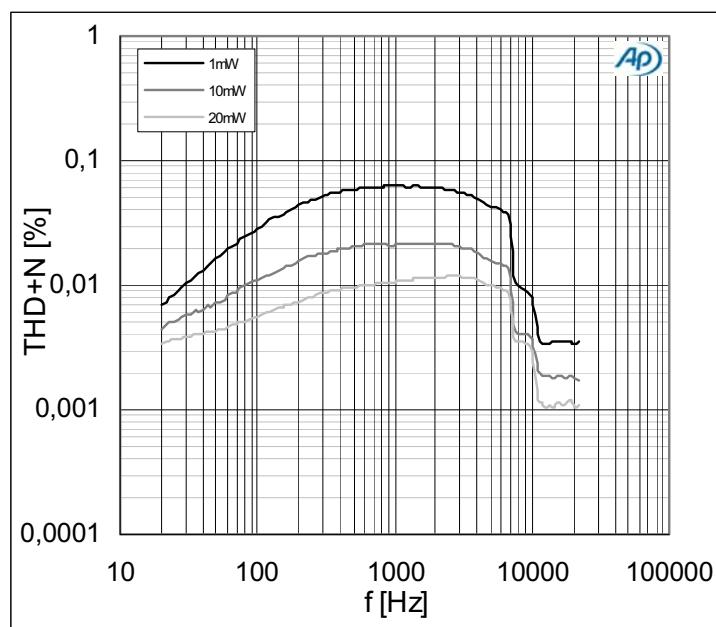


**Figure 18:**
**THD + N versus Frequency for AVDD = 5.5V,RL = 16Ω**
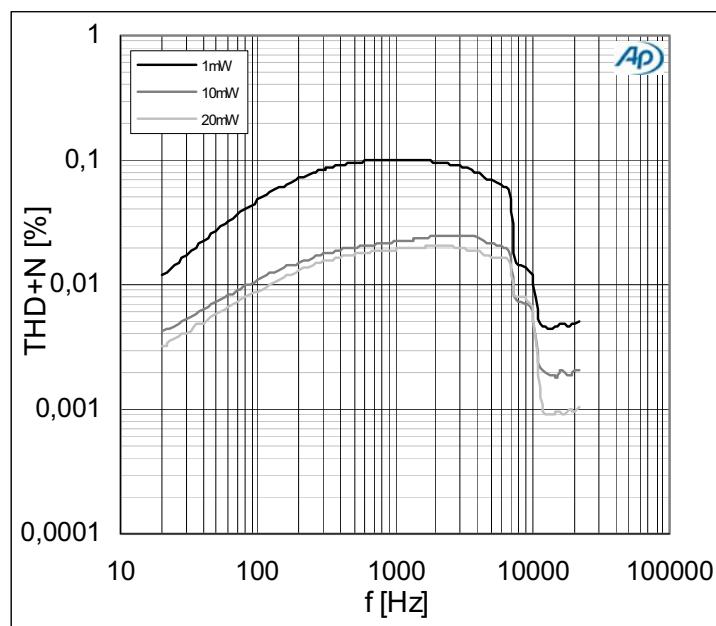
**Figure 19:**
**Supply Current vs. POUT for AVDD=2.5V**
**(Pout is the output power per channel)**
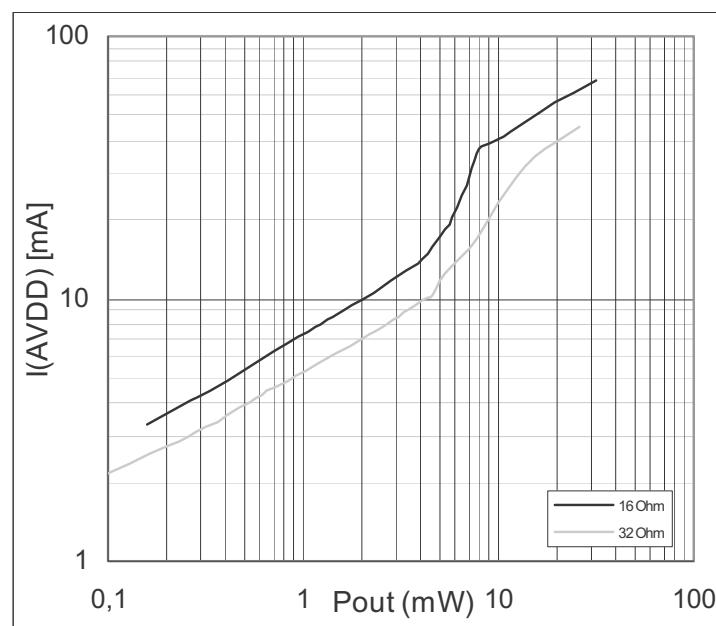


**Figure 20:**
**Ptotal vs. POUT for AVDD = 2.5V**
**(Pout is the output power per channel)**
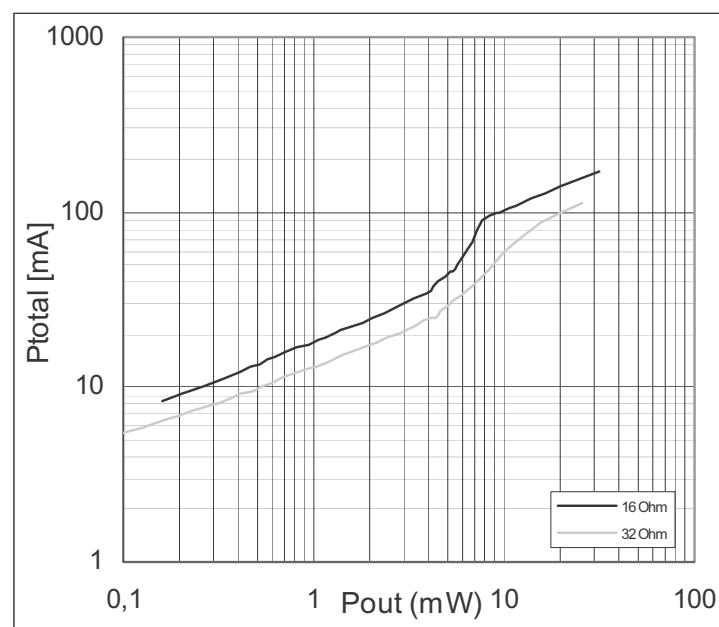
**Figure 21:**
**Supply Current vs. POUT for AVDD=3.6V**
**(Pout is the output power per channel)**
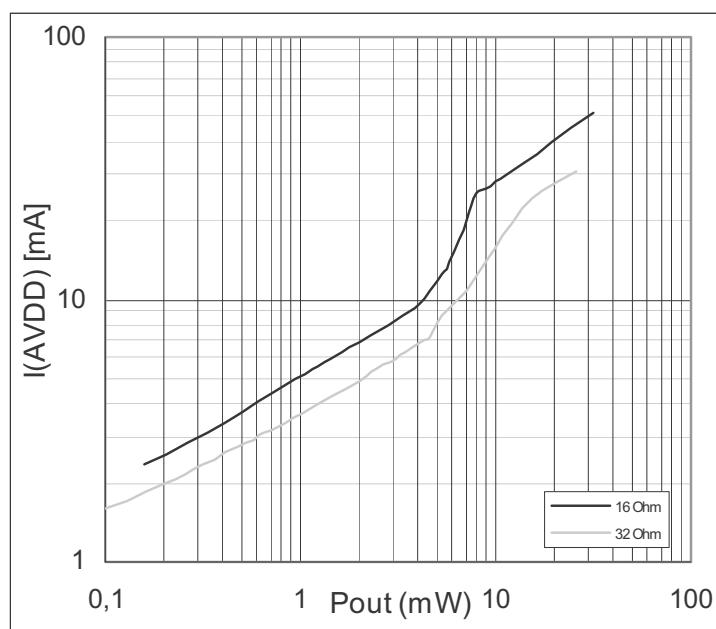


**Figure 22:**
**Ptotal vs. POUT for AVDD = 3.6V**
**(Pout is the output power per channel)**
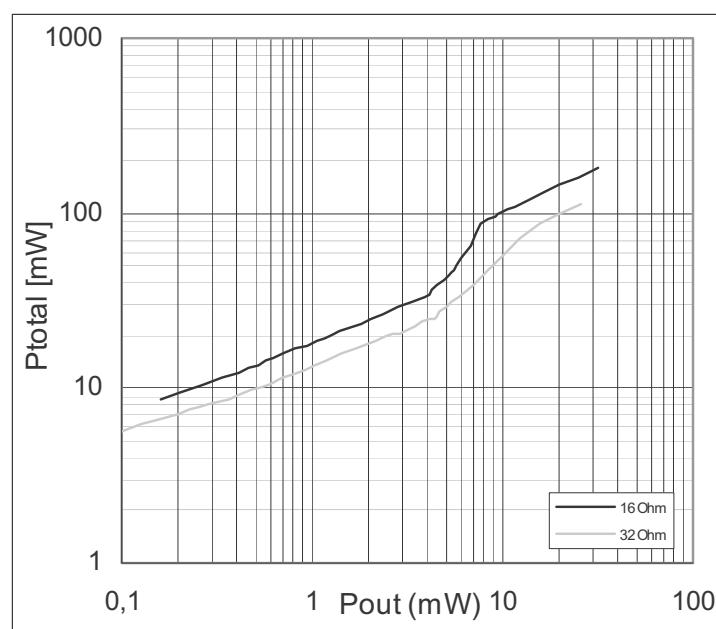
**Figure 23:**
**Supply Current vs. POUT for AVDD=5.5V**
**(Pout is the output power per channel)**
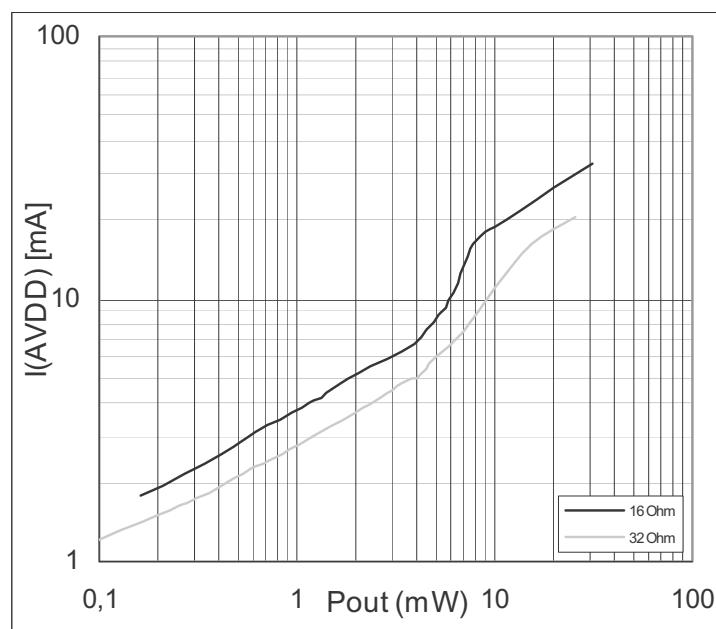


**Figure 24:**
**Ptotal vs. POUT for AVDD = 5.5V**
**(Pout is the output power per channel)**
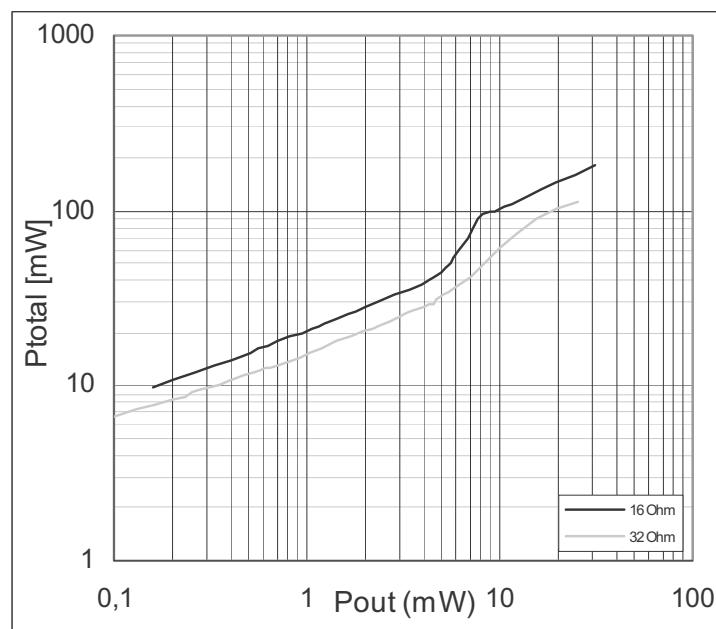
**Figure 25:**
**Quiescent Current Consumption vs. AVDDI**
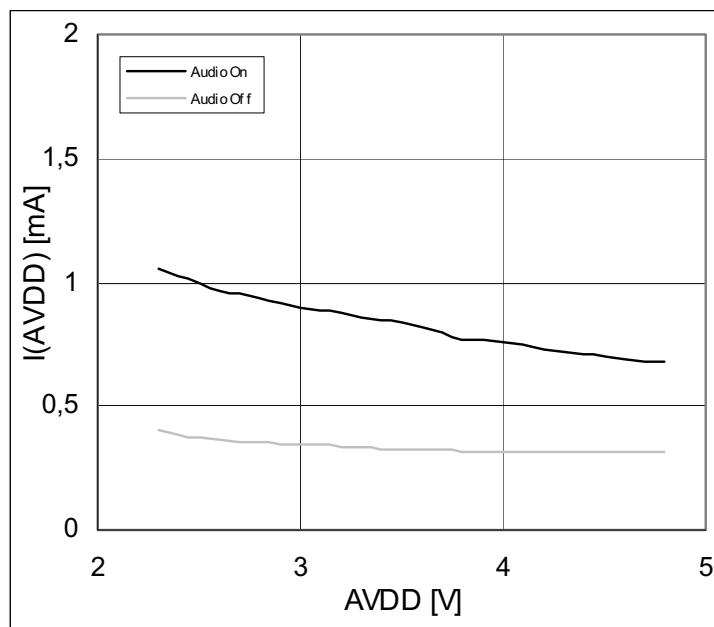


**Figure 26:**
**PSRR vs. Frequency (200mVpkpk supply ripple)**
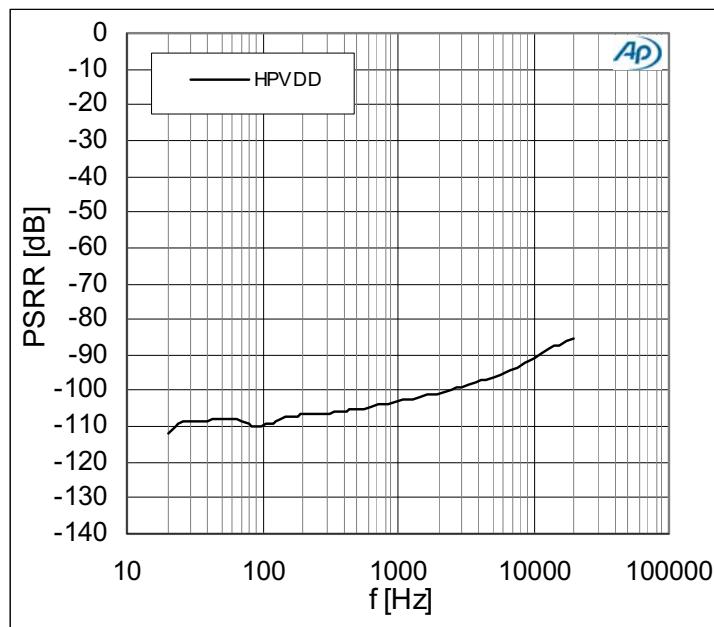
**Figure 27:**
**Crosstalk vs. Frequency (700mVrms, RL = 32Ω)**
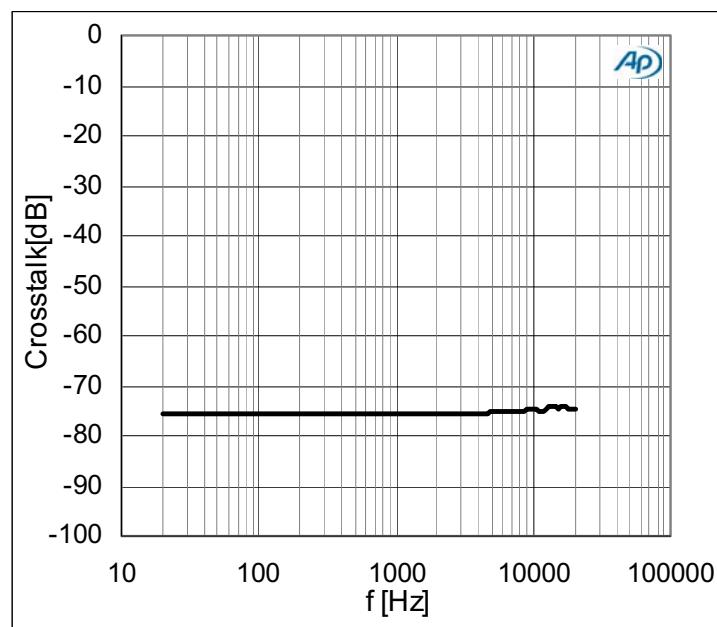


**Figure 28:**
**Startup Pop Noise for AVDD = 3.6V and RL=16Ω**
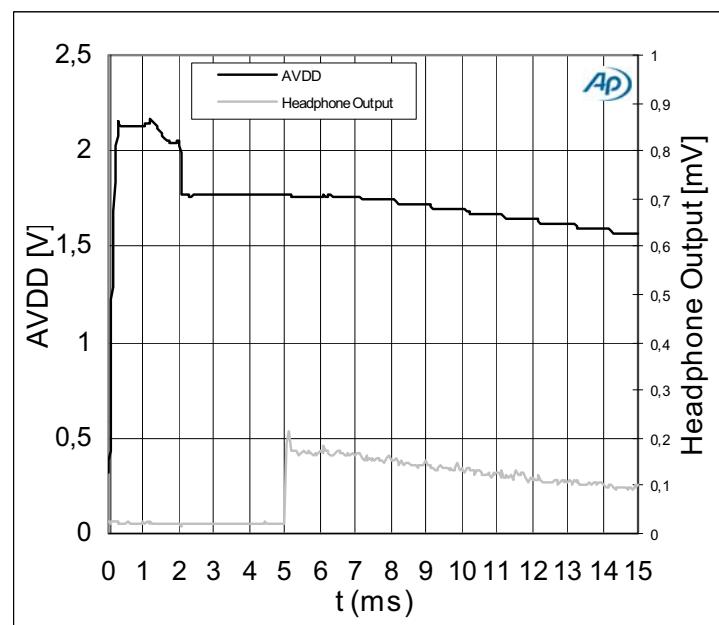
**Figure 29:**
**Startup Pop Noise for AVDD = 3.6V and RL=32Ω**
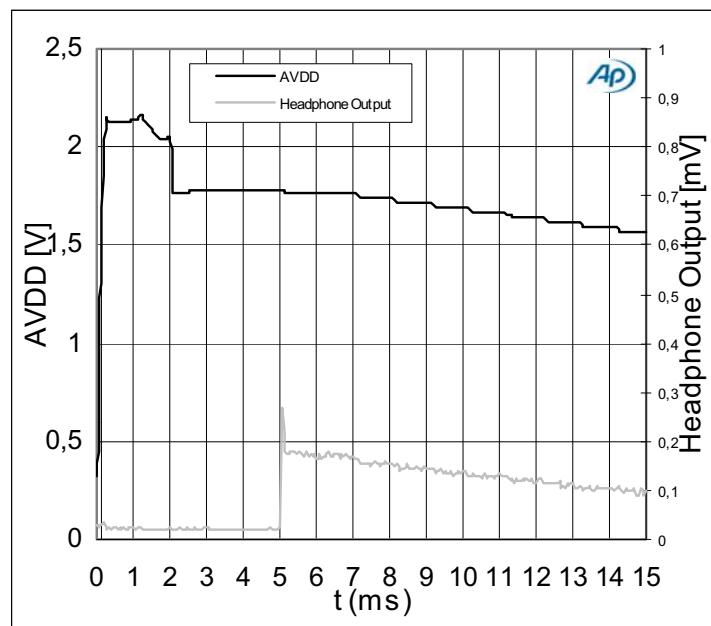
## Detailed Description

### I²C Control Interface

An I²C slave interface is implemented for read/write access of the internal registers. SCL is the corresponding clock input pin and SDA the data input pin.

Access is done in 7-bit addressing mode, addresses for read and write are defined by

C0h = 11000000b … write

C1h = 11000001b … read

**Figure 30:**
**I²C Block Diagram**
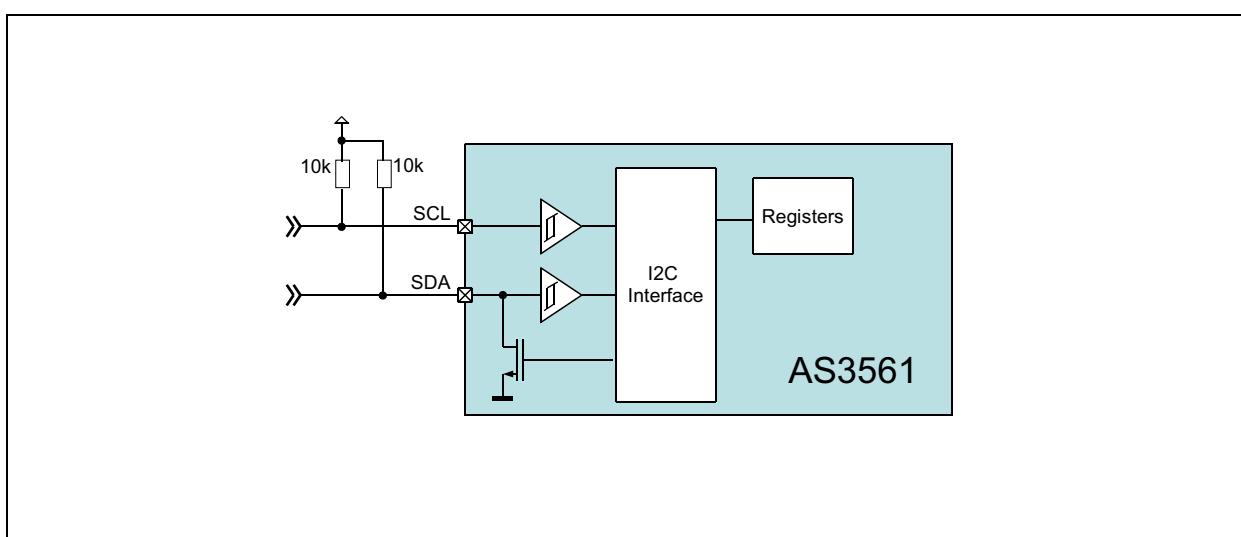


**Figure 31:**
**I²C Timing Definition**
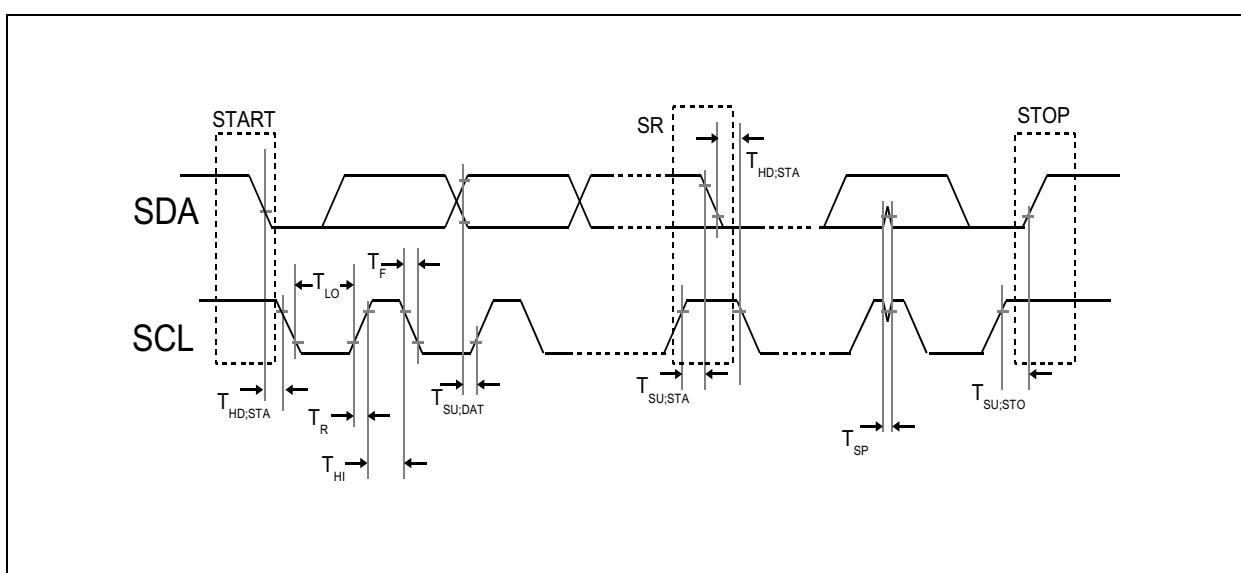
**Figure 32:**
**I²C Timing Parameters**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
| $T_{SP}$ | Spike Insensitivity | | 50 | 100 | | ns |
| $T_{HI}$ | High Clock Time | 400KHz clock speed | 330 | | | ns |
| $T_{LO}$ | Low Clock Time | | 660 | | | ns |
| $T_{SU}$ | | SDA has to change $T_{setup}$ before rising edge of SCLK | 30 | | | ns |
| $T_{HD}$ | | no hold time needed for SDA relative to rising edge of CSCL | -40 | | | ns |
| $T_{HD;STA}$ | Within start condition, after low going SDA, SCL has to stay constant for the specified hold time | | 300 | | | ns |
| $T_{ST;SUO}$ | After high going edge of SCL, SDA has to stay constant for the specified setup time before STOP or repeated start condition is applied | | 100 | | | ns |
| $T_{ST;STA}$ | | | 100 | | | ns |

## Register Definition

### Register Overview

**Figure 33:**
**Register Overview**

| Register | Description |
|---|---|
| Enable Register (1h) | General control register to switch on/off the device and enable the headphone amplifier stages. |
| Volume Register (2h) | Allows the use to configure the output volume of the headphone amplifier from -59dB up to +4dB. |
| HiZ Register (3h) | Configures the headphone amplifier for a high impedance output for power optimization. |
| Info Register (4h) | This register contains general information like IC version number and supplier information. |

### Detailed Register Descriptions

**Figure 34:**
**Enable Register (1h)**

| Bit | Bit Name | Default | Access | Bit Description |
|---|---|---|---|---|
| Bit 7 | HP_EN_L | 0 | RW | 0 … Disable Headphone Left; 1 … Enable Headphone Left Channel |
| Bit 6 | HP_EN_R | 0 | RW | 0 … Disable Headphone Right;1 … Enable Headphone Right Channel |
| Bit 5 | - | - | - | - |
| Bit 4 | - | - | - | - |
| Bit 3 | - | - | - | - |
| Bit 2 | - | - | - | - |
| Bit 1 | Thermal | 0 | S_RC | 0 … Normal Operation;1 … Thermal Shutdown |
| Bit 0 | SWS | 1 | RW | 0 … Normal Operation;1 … Software Shutdown |

**Figure 35:**
**Volume Register (2h)**

| Bit | Bit Name | Default | Access | Bit Description | |
|-----|----------|---------|--------|-----------------|--|
| Bit 7 | Mute_L | 1 | RW | 0 … Unmuted Left Channel; 1 … Mute Left Channel | |
| Bit 6 | Mute_R | 1 | RW | 0 … Unmuted Right Channel; 1 … Mute Right Channel | |
| Bit[5:1] | Vol[4:0] | 0 | RW | 0d … -55 dB; 1d … -52 dB; 2d … -49 dB; 3d … -46 dB; 4d … -43 dB; 5d … -39 dB; 6d … -35 dB; 7d … -31 dB; 8d … -27 dB; 9d … -25 dB; 10d … -23 dB; 11d … -21 dB; 12d … -19 dB; 13d … -17 dB; 14d … -15 dB; 15d … -13 dB; | 16d … -11 dB; 17d … -10 dB; 18d … -9 dB; 19d … -8 dB; 20d … -7 dB; 21d … -6 dB; 22d … -5 dB; 23d … -4 dB; 24d … -3 dB; 25d … -2 dB; 26d … -1 dB; 27d … 0 dB; 28d … 1 dB; 29d … 2 dB; 30d … 3 dB; 31d … 4 dB |
| Bit 0 | - | - | - | - | - |

**Figure 36:**
**HiZ Register (3h)**

| Bit | Bit Name | Default | Access | Bit Description |
|-----|----------|---------|--------|-----------------|
| Bit 7 | - | - | - | - |
| Bit 6 | - | - | - | - |
| Bit 5 | - | - | - | - |
| Bit 4 | - | - | - | - |
| Bit 3 | - | - | - | - |
| Bit 2 | - | - | - | - |
| Bit 1 | HiZ_L | 0 | RW | 0 … Normal Operation;1 … High Impedance on HPH_Output Left |
| Bit 0 | HiZ_R | 0 | RW | 0 … Normal Operation;1 … High Impedance on HPH_Output Right |

**Figure 37:**
**Info Register (4h)**

| Bit | Bit Name | Default | Access | Bit Description |
|---|---|---|---|---|
| Bit 7 | Supplier Bit [1:0] | RO | 1 | 11b … Default Supplier ID; else … unused |
| Bit 6 | | | 1 | |
| Bit 5 | - | - | - | - |
| Bit 4 | - | - | - | - |
| Bit 3 | Version Bit [3:0] | | 0 | 0 … First Version; else … unused |
| Bit 2 | | | 0 | |
| Bit 1 | | | 0 | |
| Bit 0 | | | 0 | |