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AS3605

Multi-Standard Power Management Unit

1 General Description

The AS3605 is a highly-integrated CMOS power management device designed specifically for portable devices such as mobile phones, PDAs, CD players, digital cameras and other devices powered by 1-cell Li-Ion battery. It can be used for any mobile phone handset standards such as CDMA, WCDMA, GSM, GPRS, EDGE, UTMS and other Japanese or American standards.

The device incorporates low dropout regulators (LDOs), a DC/DC converter, a complete battery charger, and an audio power amplifier on one die.

The linear analog LDOs feature extremely high performance regarding:

- Noise – typ 30µ V_{RMS} from 100Hz to 100kHz
- Line/Load Regulation – < 1mV static, < 10mV transient
- Power Supply Rejection – > 70dB @ 1kHz

The integrated Step Down DC/DC Converter does not require an external Schottky diode yet provides very high efficiency (up to 95%) throughout the whole operating range.

5 programmable current sources are included to control LED brightness.

A low-distortion audio power amplifier (1 Watt @ 8Ω) supports handsfree operation and HiFi ring-tones.

The device also features a battery charger including automatic trickle charging, and programmable constant voltage and current charging.

The AS3605 is controlled via a serial interface and integrates all necessary system specific functions such as Reset, Watchdog, and Power-On Detection.

Output voltages and start-up timings can be programmed via the internal OTP.

2 Key Features

- 8 Programmable High Performance LDOs
  - Four RF Low-Noise LDOs (1.8 to 3.35V, 150mA)
  - Two Analog Low-Noise LDOs (1.8 to 3.35V, 250mA)
  - One SIM Low-Power LDO (1.8 or 3.0V, 20mA)
  - One Low-Power LDO (2.5V, 10mA)
- Programmable High Efficiency DC/DC Converter
  - Step Down: 0.6 to 3.4V, up to 500mA with 2.2MHz
- Stereo Audio Power Amplifier
  - 0.5W @ 4Ω – Stereo; 1W @ 8Ω – Bridged
  - Digital Volume Control, 3dB Steps
  - Click- and Pop-Less Start-Up and Power-Down
- Battery Charger
  - Automatic Trickle Charging
  - Programmable Constant Current Charging
  - Programmable Constant Voltage Charging
  - Safety Functions (Low Battery Shutdown)
  - Over- and Under-Temperature Charge Disable
  - Operation without Battery
  - Can Regulate the Current Through the Battery or from the Charger
  - Charger Input Overvoltage Protection (6V)
  - Shutdown even with Connected Charger
  - Charger Resume Operation
  - Charger Interrupts (Inserted, Removed, Overvoltage, Resume)
  - No-Battery Detection
- Momentary Power Loss Detection
  - Battery Supply Short-Interruption Detection (<200ms); (e.g., due to a dropped phone)
- Five Programmable Current Sources (3x40mA, 2x160mA)
  - 8-Bit (0.625 to 160mA)
  - Buzzer, Vibrator, LEDs
- Charge Pump (1:1 and 1:2 mode) 60mA @3.3V VBAT
- OTP programmable boot sequence
- Wide Battery Supply Range 3.0 to 5.5V
- Three Programmable General Purpose I/O Pins
- On-Chip Bandgap Tuning for High Accuracy (±1%)
- Integrated Programmable Watchdog (16 to 4080ms)
- Programmable Reset (0 to 70ms)
- Shutdown Current typ <10µ A (2.5V Always On)
- Overcurrent and Thermal Protection
- 1.5 Watt Power Dissipation @T_A = 70ºC

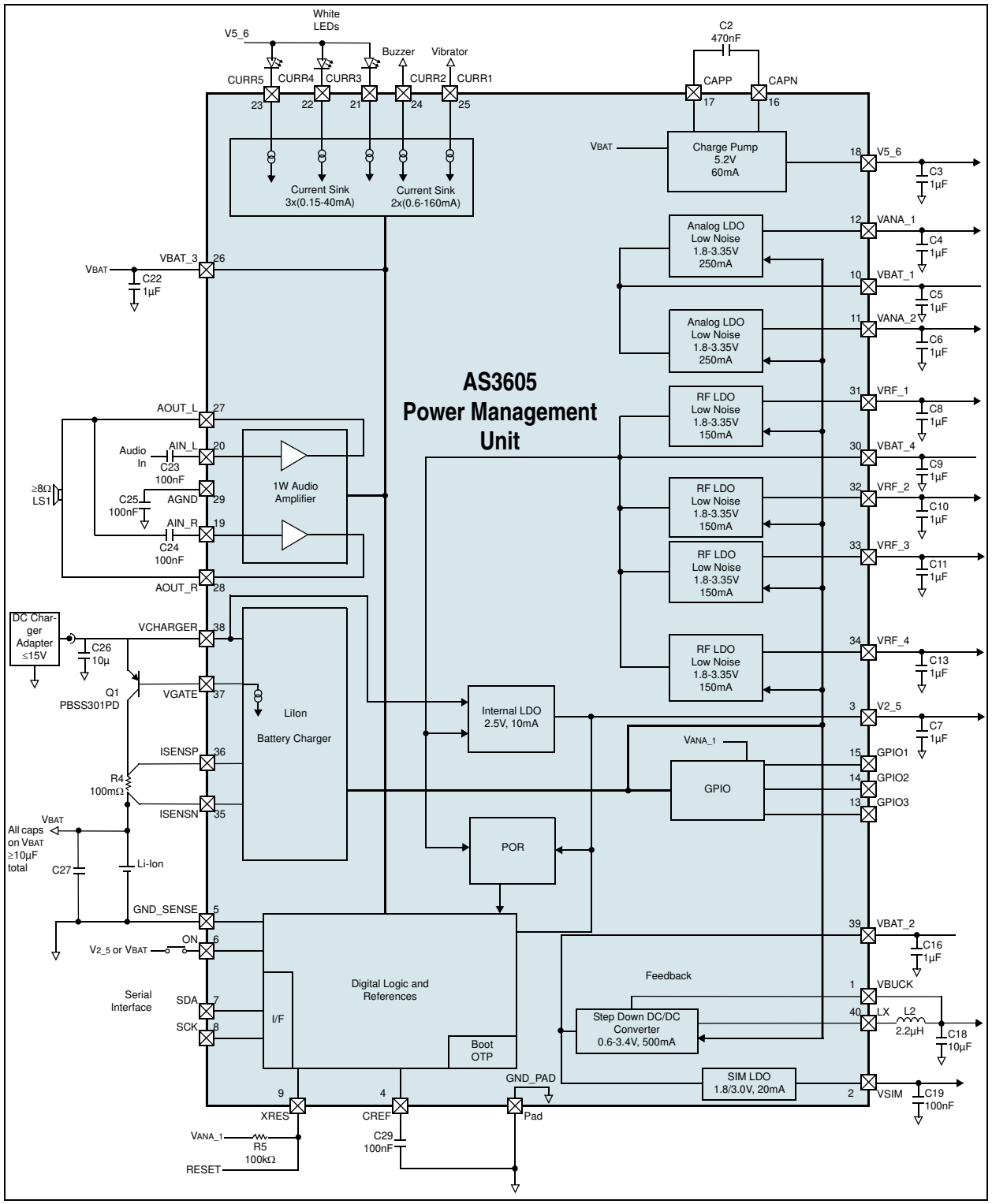
Packaging

QFN40 5x5mm, 0.4mm pitch

3 Application

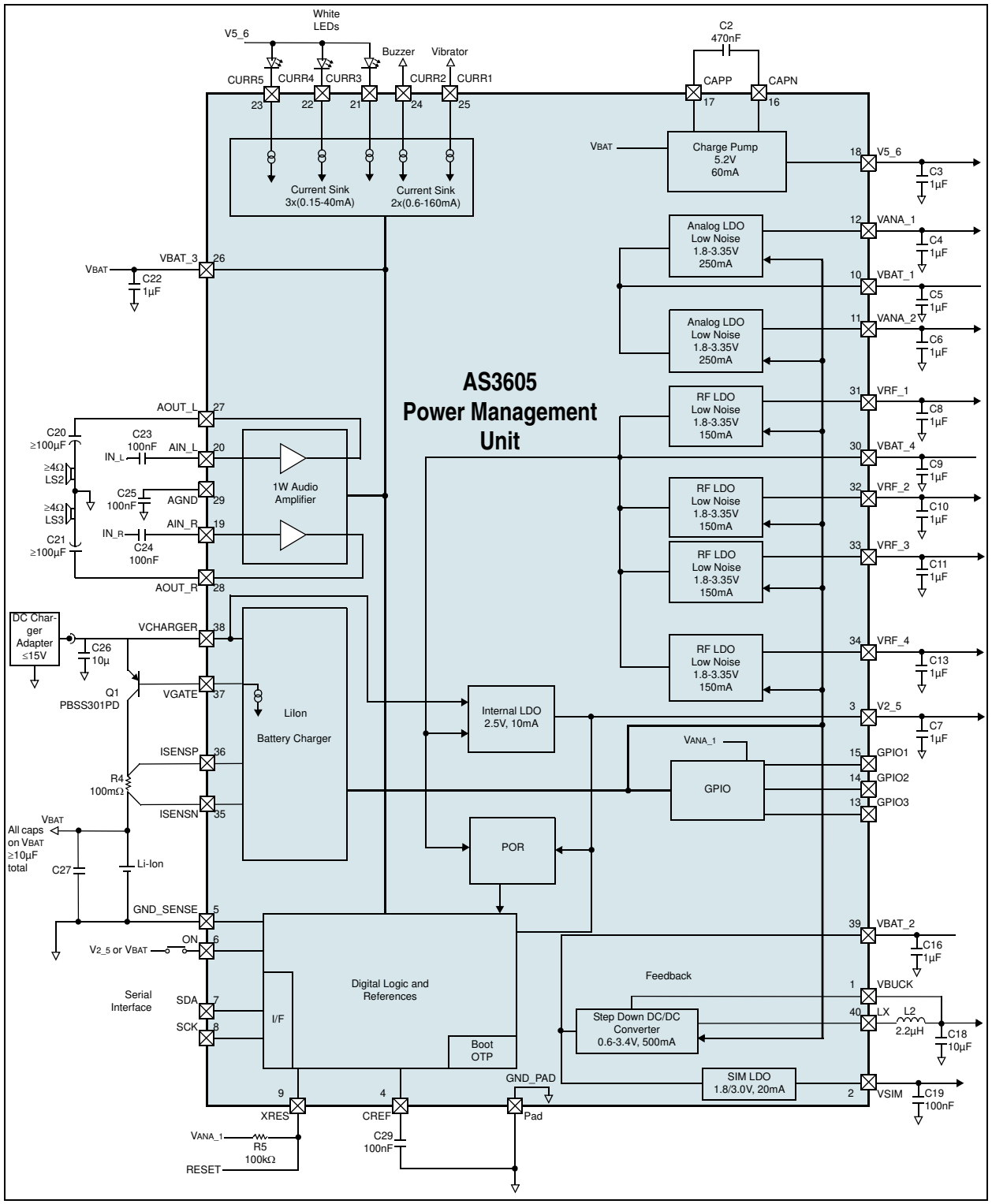
Multi-standard power management for mobile phones, PDAs, and any other 1-cell Li+ powered devices.

Figure 1. AS3605 Block Diagram. Option: Audio Amplifier In Differential Mode, Step Down DC/DC Converter as Pre-Regulator for Digital LDOs



Note: Refer to Table 33 for specifications of external components.

Figure 2. AS3605 Block Diagram. Option: Audio Amplifier in Stereo Single-Ended Mode, Digital LDOs Separated from Step Down DC/DC Converter

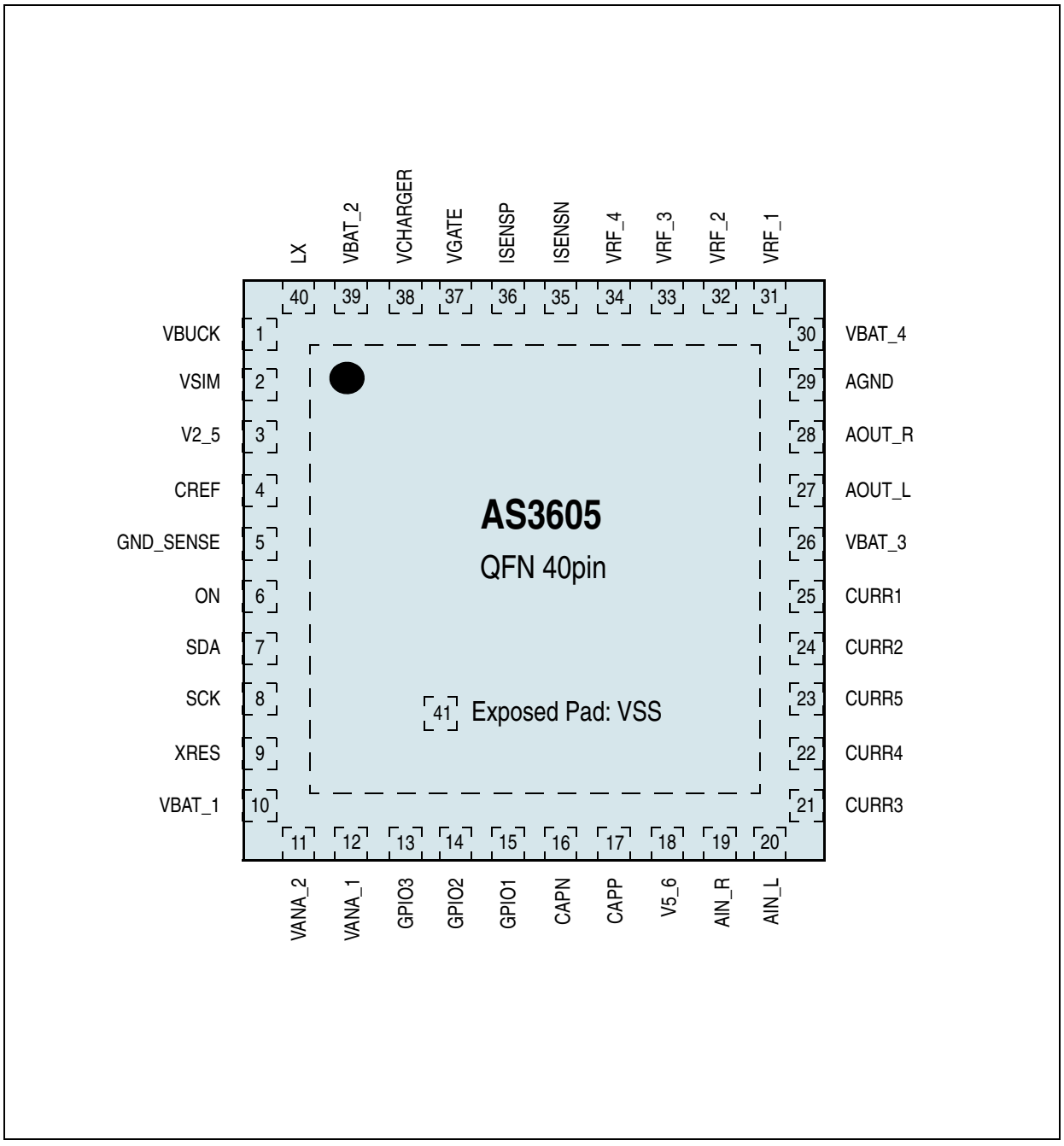


Note: Refer to Table 33 for specifications of external components.

Contents

4 Pin Assignments

Figure 3. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
VBUCK	1	Analog Input	Sense input of the DC/DC converter.
VSIM	2	Analog Output	Output voltage of LDO VSIM; if used, connect a ceramic capacitor of 100nF (±20%).
V2_5	3	Analog Output	Output voltage of low power LDO V2_5; always connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100% / -50%); do not load this pin during startup.
CREF	4	Analog Pin	Bypass capacitor for the internal voltage reference; always connect a capacitor of 100nF. **Caution:** Do not load this pin.
GND_SENSE	5	Analog Pin	Sensitive GND for Bandgap Voltage Reference.
ON	6	Digital Input	Input pin to startup the AS3605 (power on); internal pulldown; sense output in test mode.
SDA	7	Digital Input	SDA input/output in I^2C mode.
SCK	8	Digital Input	SCK input in I^2C mode.
XRES	9	Digital Input/Output / Open Drain (device can only pulldown this pin)	Bidirectional active low RESET pin; add an external pullup resistor.
VBAT_1	10	Supply Pin	Supply pin for Analog LDOs VANA_1 and VANA_2 as well as the charge pump; can be connected to VBAT or separate supply (3.0-5.5V).
VANA_2	11	Analog Output	Output voltage of one of Analog LDO VANA_2; if used as LDO, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100% / -50%).
VANA_1	12	Analog Pin	Output voltage of Analog LDO VANA_1; if used as LDO, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100% / -50%).
GPIO3	13	Digital Input/Output	General purpose switchable 5V input/output.
GPIO2	14	Digital Input/Output	General purpose switchable 5V input/output.
GPIO1	15	Digital Input/Output	General purpose switchable 5V input/output.
CAPN	16	Analog Pin	Flying capacitor of the Charge Pump; if used connect a ceramic capacitor of 470nF (±20%) to this pin.
CAPP	17	Analog Pin	Flying capacitor of the Charge Pump; if used, connect a ceramic capacitor of 470nF (±20%) to this pin.
V5_6	18	Analog Pin	Output voltage of the Charge Pump; if used, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100% / -50%).
AIN_R	19	Analog Input	Audio Amplifier right-channel input.
AIN_L	20	Analog Input	Audio Amplifier left-channel input; sense output in test mode.
CURR3	21	Analog Input	Analog current sink input.
CURR4	22	Analog Input	Analog current sink input.
CURR5	23	Analog Input	Analog current sink input.
CURR2	24	Analog Input	Analog current sink input.
CURR1	25	Analog Input	Analog current sink input.
VBAT_3	26	Supply Pin	Supply pin for Current Sinks, and Audio Amplifier; always connect to VBAT.
AOUT_L	27	Analog Output	Audio Amplifier left-channel output.
AOUT_R	28	Analog Output	Audio Amplifier right-channel output.

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
AGND	29	Analog Pin	Audio Amplifier reference GND; if the Audio Amplifier is used, connect a capacitor of 100nF (±10%) to this pin. **Caution:** Do not connect directly to VSS.
VBAT_4	30	Supply Pin	Supply pad for RF-LDOs VRF_1, VRF_2, VRF_3 and VRF_4; can be connected to VBAT or separate supply (3.0-5.5V).
VRF_1	31	Analog Output	Output voltage of RF LDO VRF_1; if used, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100% / -50%).
VRF_2	32	Analog Output	Output voltage of RF LDO VRF_2; if used, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100% / -50%).
VRF_3	33	Analog Output	Output voltage of RF LDO VRF_3; if used, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100% / -50%).
VRF_4	34	Analog Output	Output voltage of RF LDO VRF_4; if used, connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100% / -50%).
ISENSN	35	Analog Input	Negative sensing input voltage for the external charging current shunt resistor.
ISENSP	36	Analog Input	Positive sensing input voltage for the external charging current shunt resistor.
VGATE	37	Analog Output	Control pin for the external battery charger MOSFET transistor.
VCHARGER	38	Analog Input	High voltage input coming from the Battery Charger; if the Battery Charger is used, connect a ceramic capacitor of 1µF.
VBAT_2	39	Supply Pin	Supply pin for the Step Down DC/DC Converter and LDO VSIM; always connect to VBAT.
LX	40	Analog Output	Step Down DC/DC Converter switch output to coil
VSS	41	VSS	Ground pad (QFN40: exposed paddle).

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Operating Conditions on page 10 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comments
V_{IN_HV}	High Voltage Pins	-0.3	18.0	V	Applicable for high voltage pins: VCHARGER, VGATE
V_{IN_MV}	5V Pins	-0.3	7.0	V	Applicable for pins 5V pins: VBAT_1 - VBAT_4, V5_6, VBUCK, GPIO1 - GPIO3, CURR1 - CURR5, VANA_1, VANA_2, AIN_L, AIN_R, AOUT_L, AOUT_R, XRES, SCK, SDA, ON, and LX
V_{IN_LV}	3.3V Pins	-0.3	5.0	V	Applicable for 3.3V pins: VRF_1 - VRF_4, VSIM, CAPN, AGND, ISENSP, ISENSN, V2_5, CREF
I_{IN}	Input Pin Current	-25	+25	mA	At 25ºC Norm: JEDEC JESD78C
	Humidity	5	85	%	Non-condensing
Continuous Power Dissipation (T_A = +70ºC)					
P_T	Continuous power dissipation		1.5	W	P_T[1] for QFN40 package
Electrostatic Discharge					
V_{ESD}	Electrostatic Discharge HBM		±1.5	kV	Norm: JEDEC JESD22-A114F
Temperature Ranges and Storage Conditions					
T_j	Junction Temperature		+110	ºC	
T_{strg}	Storage Temperature Range	-55	+125	ºC	
	Humidity non-condensing	5	85	%	
Temperature (soldering)					
	Package Body Temperature		260	ºC	Norm IPC/JEDEC J-STD-020[2], reflects moisture sensitivity level only
	Moisture Sensitive Level	3			Represents a maximum floor live time of 168h

1. Depending on actual PCB layout and PCB used.
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

6 Electrical Characteristics

Table 3. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_{AMB}	Ambient Temperature	-40	25	85	ºC	
V_{HV}	High Voltage	0.0		15.0	V	Pins VCHARGER, VGATE
V_{BAT}	Battery Voltage	3.0	3.6	5.5	V	For pins VBAT_1 - VBAT_4. During startup from external battery charger adapter, the battery voltage can be below 3.0V.
V_{ANA_1}	Periphery Supply Voltage for GPIO pins	1.8	OTP	3.35	V	Internally generated from V_{ANA_1}
V_{ON}	Activation voltage for ON pin	1.75	V_{2_5}	V_{BAT}	V	
V_{2_5}	Voltage on Pin V2_5	2.4	2.5	2.6	V	Internally generated
V_{5_6}	Output Voltage of Charge Pump	4.9	5.2	5.6	V	2 x VBAT_1
I_{BAT}	Operating Current		195	260	µA	Normal operating current. With bit **low_power_on** = 0; only V_{ANA_1} active, no additional external loads.
$I_{LOWPOWER}$	Low-Power Mode Current Consumption		110		µA	With bit **low_power_on** = 1; only V_{ANA_1} active, no additional external loads.
$I_{POWEROFF}$	Power-Off Mode Current Consumption		10	20	µA	With bit **power_off** = 1; only V2_5 is active in power OFF mode. Not tested, guaranteed by design

7 Detailed Description

7.1 Battery Charge Controller

The AS3605 device serves as a standalone battery charge controller supporting rechargeable lithium ion (Li+) and) batteries. Requiring only a few external components, a full-featured battery charger with a high degree of flexibility can easily be realized. The main features of the controller are:

- Charge adapter detection
- Internal voltage regulator
- Low current (trickle) charging
- Constant current charging
- Constant voltage charging
- Overvoltage protection
- Battery presence indication
- Operation without battery

Figure 4. Charger Application Block Diagram

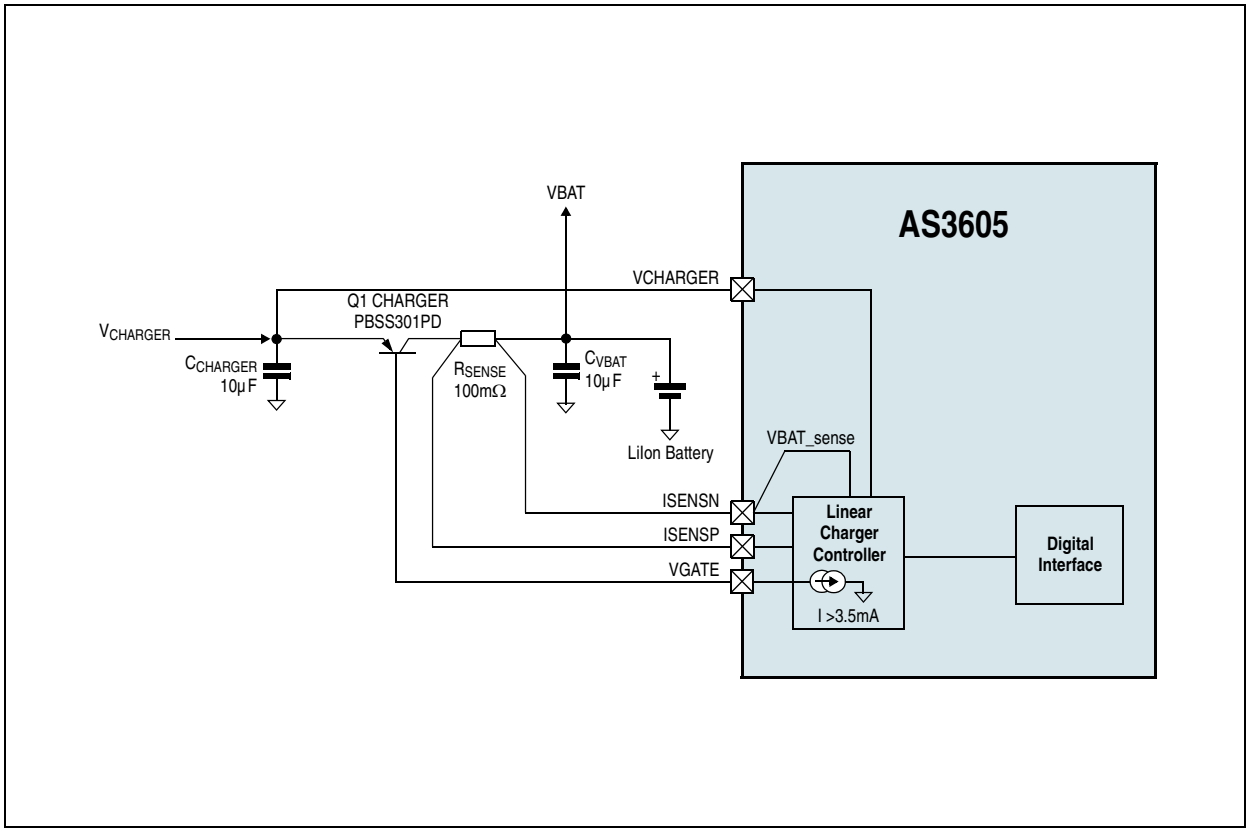


Table 4. Charger External Components

Symbol	Component	Value	Note
Q_1	PNP power transistor	PBSS301PD or similar	h_{FE} > 200 @ 0.8A
R_{SENSE}	Current sense resistor	100mΩ ±1%, 125mW for I_{CHG} < 1.5A	e.g. Vishay Dale WSL0805
C_{CHRG}	Bypass capacitor on charger pin	10µF ±20%, X5R or X7R dielectric	
C_{BAT}	Minimum total capacitance parallel to battery	10µF, X5R or X7R dielectric	

7.1.1 Charge Controller Operating Modes and Building Blocks

Charge Adapter Detection. The charge controller uses an integrated detection circuit to determine if an external charge adapter has been applied to the VCHARGER pin. If the adapter voltage exceeds the battery voltage at pin VBAT by V_{CHDET} the **ChDet** bit in the **ChargerStatus** register will be set. The detection circuit will reset the charge controller (bit **ChDet** is cleared) as soon as the voltage at the VCHARGER pin drops to only V_{CHMIN} above the battery voltage. In case the AS3605 device is reset the charge controller will also be reset, even if a charge adapter is applied to the VCHARGER pin.

Low Current (trickle) Charging. Trickle charge mode is started when an external charge adapter has been detected and the battery voltage at pin VBAT is below the V_{UVLO} threshold; bits **ChAct** and **Trickle** will be set in the **ChargerStatus** register. In this mode the charge current will be limited to **TrickleCurrent[1:0]** (set in the **ChargerControl1** register) to prevent undue stress on either the battery or any of the charger components in case of deeply discharged batteries. Once VUVLO has been exceeded, the charger will change over to constant current charging (**Trickle** is cleared) and switch on the device.

Constant Current Charging. Constant current charging is initiated by setting **ChEn** in the **ChargerControl1** register. Note that **ChEn** is set by default to enable operation of the device without a battery connected to the system. The **ChAct** bit is set when the charger has started, and the charge current will be limited to **ConstantCurrent[3:0]** (set in the **ChargerControl1** register) by the battery charge controller. When the battery approaches full charge, its voltage will exceed the charge termination threshold V_{CHOFF}. V_{CHOFF} depends on the **Li4v2** bit in the **ChargerControl2** register. The charging action will either be terminated (**EOC** bit will be set) or a top-off charge will be started (**CVM** will be set).

Constant Voltage Charging. Constant voltage charge mode is initiated and the **CVM** bit will be set when the V_{CHOFF} threshold has been reached.
The charge current is monitored during constant voltage charging. It will be decreasing from its initial value during constant current charging and eventually drop below the value set by **TrickleCurrent[1:0]** in the **ChargerControl1** register. If the measured charge current is less than or equal to **TrickleCurrent[1:0]**, the charging cycle is terminated and **EOC** is set.

Battery Presence Indication and Operation Without Battery. After EOC state is reached a timer for NOBAT detection is started. If there is no battery present, the voltage will drop to V_{NOBAT_REG}. Depending on the load on VBAT and the capacitor on VBAT this might take some mseconds to 1 second. If the RESUME mode is enabled (Bit **resume_disable**=0), the charger will restart charging (ConstantCurrent charging) after 100msec.
The 100msec dead time is necessary to get a battery oscillation frequency of below 10Hz, if there is no battery present.
If the NOBAT detection timer is below 2 seconds after reaching EOC state, and this happens 2 times in serial, the NOBAT bit in **ChargerStatus** register is set. If a battery is inserted, then the bit will be reset after the timer exceeds the 2 seconds.

Charger Overvoltage Protection. This blocks checks if the charger voltage is above 6.05V or 6.45V if **ChOvH** is 1. If the status bit **ChOv** is 1 when **ChOvEn** is 1, the charger will shut down by clearing the **ChEn** bit and an interrupt will be generated.

Table 5. Charger Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CHDET}	Charger detection threshold	50	75	105	mV	Hysteresis is > 40mV
V_{CHMIN}		0	20	35		
V_{CHOVH}	VCHARGER overvoltage detection	6.2	6.45	6.71	V	**ChOvH** = 1
		5.81	6.05	6.29		**ChOvH** = 0
V_{UVLO}	Undervoltage lockout threshold		3.1		V	V_{BAT} rising
			2.8			V_{BAT} falling
V_{CHOFF}	Charge termination threshold	4.158	4.20	4.242	V	Li+ Battery: **Li4v2** = 1
			4.10			Li+ Battery: **Li4v2** = 0
$V_{NOBATREG}$	"No battery" regulation voltage		3.85		V	Li+ Battery: **Li4v2** = 1
			3.75			Li+ Battery: **Li4v2** = 0
V_{RESUME_ON}	Charger resume on threshold		3.85		V	**Li4v2** = 1
			3.75			**Li4v2** = 0

Table 5. Charger Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VRESUME_OFF	Charger resume off threshold		4.02		V	**Li4v2** = 1
			3.92			**Li4v2** = 0
IGATE_OFF	Current into pin GATE, if charger disabled	0		0.4	µA	VCHARGER=5V
IGATE_ON	Current into pin GATE, if charger enabled and operation in low dropout mode (low VCE)	3.5	5		mA	VCHARGER=5V

7.1.2 Charger Registers

Table 6. Charger Register Summary

Name	Addr.	b7	b6	b5	b4	b3	b2	b1	b0	Page
LDO_CHG	10h					EOCCurrent[1:0]				14
ChargerControl1	14h	ChOvEn	TrickleCurrent[1:0]		ConstantCurrent[3:0]				ChEn	13
ChargerControl2	16h	ChOv	ChOvH	NA	Li4v2	resume_disable				14
ChargerStatus	35h	NA	NoBat	EOC	CVM	Trickle	NA	ChAct	ChDet	15

ChargerControl1 Register (Address 14h).

Addr: 14h		ChargerControl1			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
0	ChEn	1b	R/W	0	Disable charging
				1	Enable charging
4:1	ConstantCurrent[3:0]	OTP	R/W	0	0mA + Trickle_current
				1	50mA + Trickle_current
				2	100mA + Trickle_current
				3	150mA + Trickle_current
				4	200mA + Trickle_current
				5	250mA + Trickle_current
				6	300mA + Trickle_current
				7	350mA + Trickle_current
				8	400mA + Trickle_current
				9	450mA + Trickle_current
				A	500mA + Trickle_current
				B	550mA + Trickle_current
				C	600mA + Trickle_current
				D	650mA + Trickle_current
				E	700mA + Trickle_current
				F	750mA + Trickle_current

Addr: 14h		ChargerControl1			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:5	TrickleCurrent[1:0]	OPT	R/W	0	50mA
				1	100mA
				2	150mA
				3	200 mA
7	ChOvEn	1	R/W	0	Disable the Charger Overvoltage protection
				1	Enable the Charger Overvoltage protection

LDO_CHG Register (Address 10h).

Addr: 10h		LDO_CHG			
		Adjusts EOC current of Charger.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
3:2	EOCCurrent[1:0]	00	R/W	00	EOC Current = Trickle Current
				01	EOC Current = Trickle Current + 18mA
				10	do not use
				11	EOC Current = Trickle Current + 33mA

ChargerControl2 Register (Address 16h).

Addr: 16h		ChargerControl2			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
2:0	-	NA	NA		
3	resume_disable	0	R/W	0	Enable Resume in **EOC** state
				1	Disable Resume in **EOC** state
4	Li4v2	1	R/W	0	V_{CHOFF} = 4.1V for Li+ battery cells with coke anode
				1	V_{CHOFF} = 4.2V for Li+ battery cells with graphite anode
5	-	NA	NA		
6	ChOvH	1	R/W	0	Sets low threshold for Over voltage protection (typ. 6.05V)
				1	Sets high threshold for Over voltage protection (typ. 6.45V)
7	ChOv	NA	R	Indicates Charger overvoltage condition	

ChargerStatus Register (Address 35h).

Addr: 35h		**ChargerStatus**		
		Read only		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	ChDet	NA	R	Bit is set when external charge adapter has been detected
1	ChAct	NA	R	Bit is set when charger is operating
2	-	NA		
3	Trickle	NA	R	Bit is set when charger is in trickle charge mode
4	CVM	NA	R	Bit is set when charger is in top-off charge mode
5	EOC	NA	R	Bit is set when charging has been terminated. Bit is cleared automatically when **ChEn** is cleared.
6	NoBat	NA	R	Bit is set when battery detection circuit indicates that no battery is connected to the system. Bit is cleared automatically when a battery is connected or when **ChEn** is cleared.
7	-	NA	NA	

7.2 Step Down DC/DC Converter

The step-down converter is a high-efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches, efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 500mA, with an output capacitor of only 10µF. The implemented current limitation protects the DC/DC Converter and the coil during overload condition.

Figure 5. Step Down DC/DC Converter Block Diagram

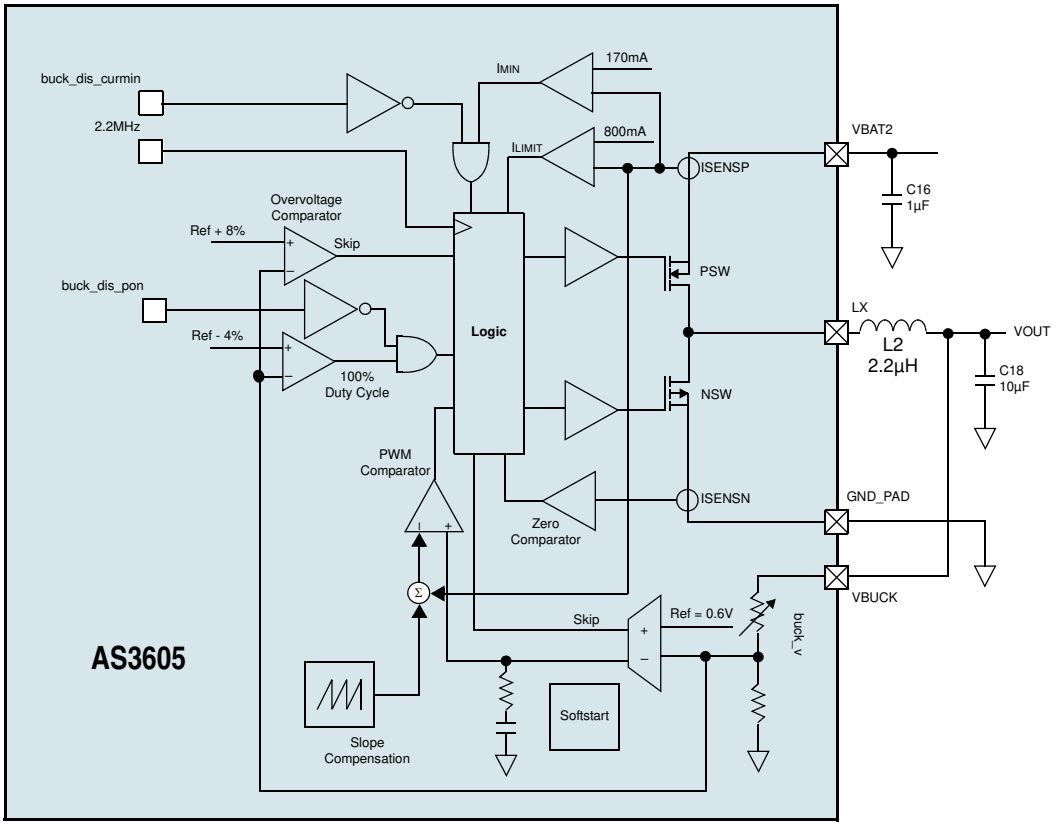


Table 7. Step Down DC/DC Converter Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VIN	Input Voltage	3.0		5.5	V	Pin VBAT_2
VOUT	Regulated Output Voltage	0.6		3.4	V	Sense pin VBUCK
VOUT_TOL	Output Voltage Tolerance	-50		50	mV	Sense pin VBUCK; Output Voltage < 1.6V
		-3%		3%		Sense pin VBUCK; Output Voltage > 1.6V
ILIMIT	Current Limit		900		mA	Supply current into PMOS transistor
RPSW	PSW On-Resistance			0.5	Ω	
RNSW	NSW On-Resistance			0.5	Ω	
ILOAD	Load Current	0		500	mA	
fSW	Switching Frequency		2.2		MHz	
COUT	Output Capacitor		10		µF	Ceramic
Lx	Inductor		2.2		µH	
h	Efficiency		90		%	ILOAD = 100mA, VOUT = 2.3V, VBAT = 3V
IVDD_DCDC	Current Consumption		250		µA	Operating Current; No Load
			100			Quiescent Current; Low-Power Mode
			0.1			Shutdown Current
tMIN_ON	Minimum ON Time		80		ns	
tMIN_OFF	Minimum OFF Time		40		ns	

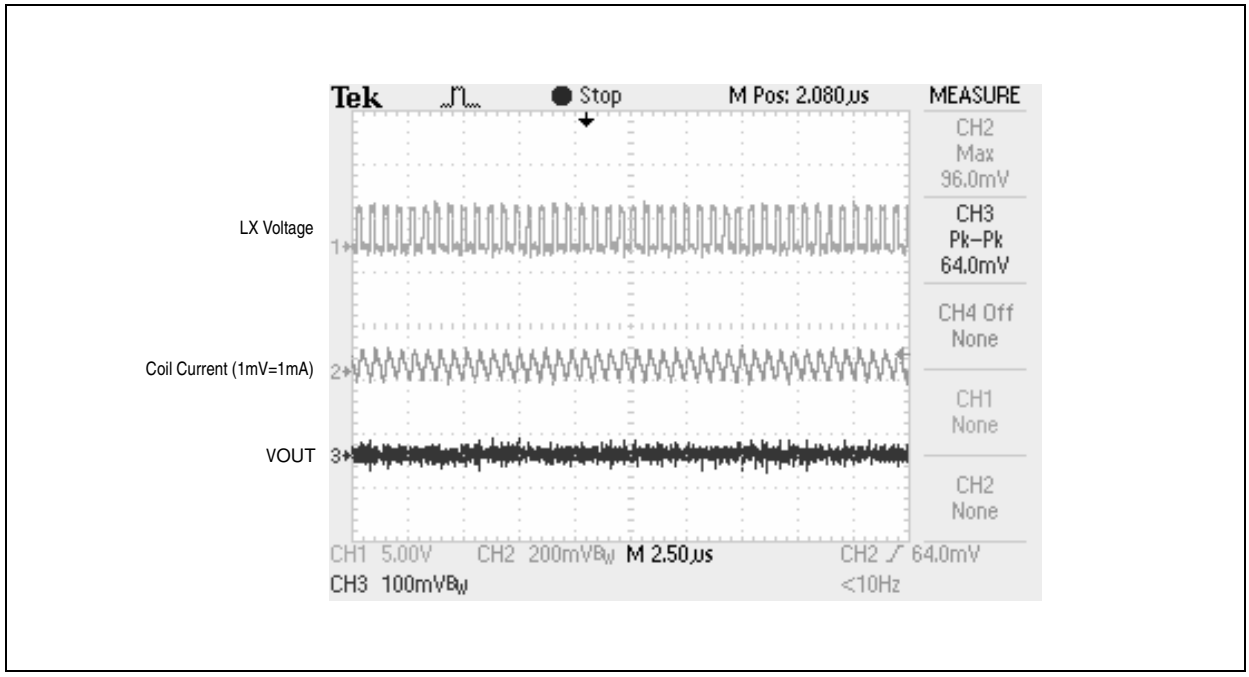
To allow optimized performance in different applications, there are bit settings possible, to get the best compromise between high efficiency and low input/output ripple.

7.2.1 Low-Ripple, Low-Noise Operation

Low-ripple, low-noise operation can be enabled by setting bit **buck_dis_curmin** = 1. In this mode there is no minimum coil current necessary before switching OFF the PMOS. As result, the ON time of the PMOS will be reduced down to tMIN_ON at no or light load conditions, even if the coil current is very small or the coil current is inverted. This results in a very low ripple and noise (but decreased efficiency) at light loads, especially at low input-to-output voltage differences.

Note: Because of the inverted coil current in that case the regulator will not operate in pulse skip mode.

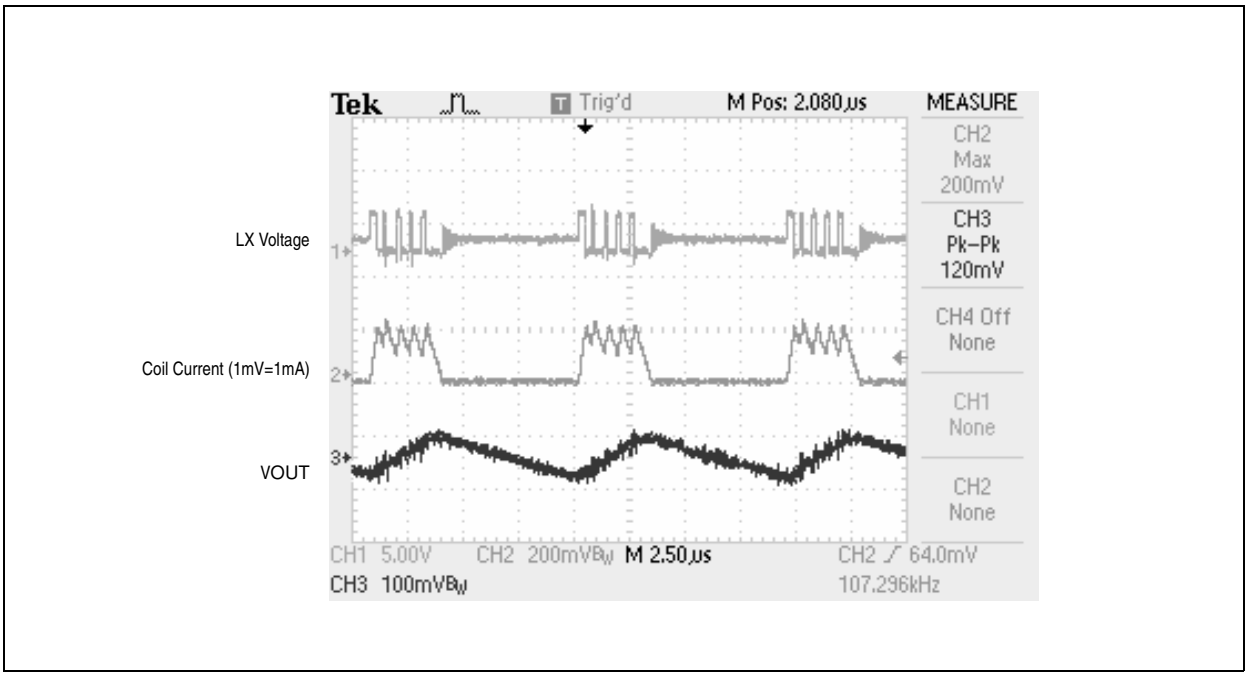
Figure 6. Bit buck_dis_curmin = 1 Operation



7.2.2 High-Efficiency Operation (Default Setting)

High-efficiency operation is enabled by setting bit **buck_dis_curmin** = 0. In this mode there is a minimum coil current necessary before switching OFF the PMOS. As result there are less pulses at low output load necessary, and therefore the efficiency at low output load is increased. This results in higher ripple, and noisy pulse skip operation up to a higher output current.

Figure 7. Bit buck_dis_curmin = 0 Operation



Note: It is possible to switch between these two modes during operation, i.e.:

Bit **buck_dis_curmin** = 0: System is in idle state. No audio or RF signal. Decreased supply current preferred. Increase ripple doesn't effect system performance.

Bit **buck_dis_curmin** = 1: System is operating. Audio signal on and/or RF signal used. Decreased ripple and noise preferred. Increased power supply current can be tolerated.

7.2.3 100% PMOS ON Mode for Low Dropout Regulation

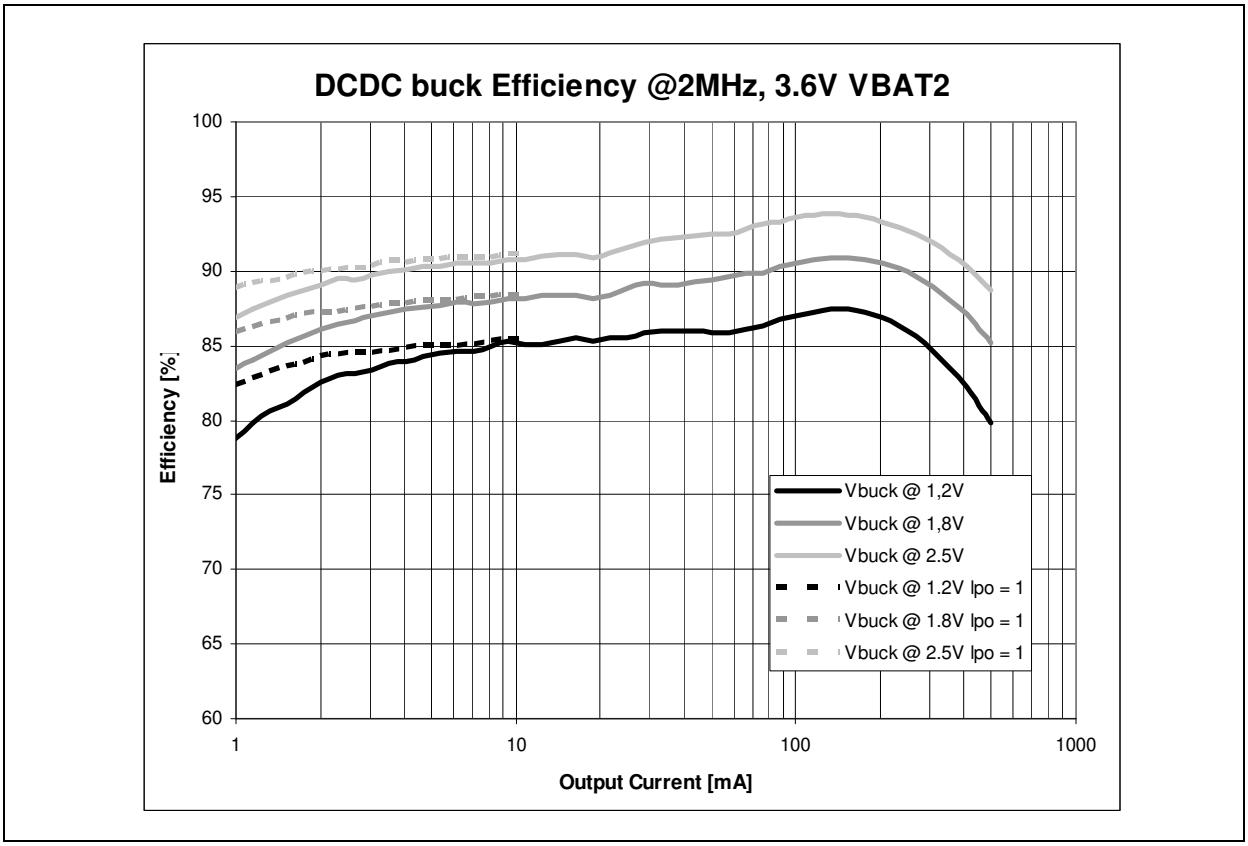
For low input-to-output voltage difference bit **buck_dis_pon** can be set to allow 100% duty cycle of the PMOS transistor, if the output voltage drops by more than 4% below regulation.

7.2.4 Low Power Mode

Bit **buck_lpo** can be set all the time. This mode allows internal power down, of not used blocks during pulseskip mode, which results in a better efficiency at light output loads.

7.2.5 Typical Performance Characteristics

Figure 8. DC/DC Step-Down Efficiency vs. Output Current (buck_dis_cfm = 0)



7.2.6 Step Down DC/DC Converter Registers

The Step Down DC/DC Converter is controlled by the registers listed in Table 8.

Table 8. Step Down DC/DC Converter Register Summary

Name	Addr.	b7	b6	b5	b4	b3	b2	b1	b0	Page
Step Down Voltage/Test Modes	01h	-		buck_v						20
Reg Power	09h	-		buck_on	ldo_sim_on			ldo_ana2_on	ldo_ana1_on	20
Step Down Configuration	17h	buck_dis_curmin	buck_dis_pon	buck_lpo	-	-	buck_dis_n	buck_nsw_on	buck_psw_on	20

Step Down Voltage Register (Address 01h).

Addr: 01h		**Step Down Voltage/Test Modes**		
		Sets the output voltage of the Step Down DC/DC Converter.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5:0	buck_v	Boot ROM	R/W	Controls the voltage selection for the Step Down DC/DC Converter. 000000: 0.6V …: (LSB = 50mV) 111000-111111: 3.4V
7:6	-	NA	NA	

Reg Power Register (Address 09h).

Addr: 09h		**Reg Power**		
		Enables/disables voltage regulators.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	ldo_ana1_on	Boot ROM	RW	Refer to page 28
1	ldo_ana2_on	Boot ROM	RW	Refer to page 28
3:2	-	NA	NA	
4	ldo_sim_on	Boot ROM	RW	Refer to page 28
5	buck_on	Boot ROM	R/W	Enables the Step Down DC/DC Converter. 0: Step Down DC/DC Converter is OFF. 1: Step Down DC/DC Converter is ON.
7:6	-	NA	NA	

Step Down Configuration Register (Address 17h).

Addr: 17h		**Step Down Configuration**			
		Configures the operation mode of the Step Down DC/DC Converter.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
0	buck_psw_on	0	R/W	Activate PSW (0.5Ω PMOS) only if **buck_on** and **buck_nsw_on** = 0.	
				0	Default setting. P-Channel switching transistor is controlled by the DC/DC Converter.
				1	Turns on P-Channel switching transistor. Bits **buck_on** and **buck_nsw_on** must both = 0.
1	buck_nsw_on	0	R/W	Activates NSW (0.5Ω NMOS) only if **buck_on** = 0 and **buck_psw_on** = 0.	
				0	Default setting. N-Channel switching transistor is controlled by the DC/DC Converter.
				1	Turns on N-Channel switching transistor. Bits **buck_on** and **buck_psw_on** must both = 0.
2	buck_dis_n	0	R/W	0	Default setting. Normal operation of The synchronous rectifier.
				1	The synchronous rectifier is disabled (NSW is always OFF).
3	-	0	RW	0	
				1	

Addr: 17h		Step Down Configuration			
		Configures the operation mode of the Step Down DC/DC Converter.			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
4	-	0	R/W		
				0	
				1	
5	buck_lpo	0	R/W	0	Low-power mode disabled.
				1	Low-power mode enabled.
6	buck_dis_pon	0	R/W	Step down PON feature control.	
				0	PON feature enabled. 100% duty cycle (PMOS always on) if output voltage drops more than 4%. Increased output ripple in that operation.
				1	PON feature disabled. Maximum duty cycle = 1 - (tmin_off*fsw)
7	buck_dis_curmin	0	R/W	Step down current force mode	
				0	current force mode enabled. Inductor current regulated to min 170mA. Higher efficiency in low dropout and low output current operation. Higher output ripple and noise.
				1	current force mode disabled. Decreased efficiency in low dropout mode and at low output current. Small output ripple and noise.

7.3 Low Dropout Regulators

The Low Dropout Regulators (LDOs) are linear high performance regulators with programmable output voltages. The LDOs can be controlled by either software (voltage, ON/OFF) or hardware (ON/OFF) using highly configurable GPIO1 to GPIO3 pins.

The Low Dropout Regulators include the following:

- RF and Analog Low Dropout Regulators – Described on page 22
- Analog LDO Block Diagram – Described on page 22
- SIMCard Low Dropout Regulator – Described on page 23
- Low Power Low Dropout Regulator – Described on page 24

7.3.1 RF and Analog Low Dropout Regulators

The RF LDOs (VRF_1 - VRF_4) and Analog LDOs (VANA_1 and VANA_2) are designed to supply power to sensitive analog circuits like LNAs, Transceivers, VCOs and other critical RF components of cellular radios. Additionally, these LDOs are suitable for supplying power to audio devices or as a reference for A/D and D/A converters.

The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices. Stability is guaranteed with ceramic output capacitors (see Figure) of 1µF ±20% (X5R) or 2.2µF +100 / -50% (Z5U).

The low ESR of these capacitors ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress ripple on the battery caused by the PA in TDMA systems. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power transistor enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease of performance.

The LDOs have a built-in discharge function when switched off.

Figure 9. Analog LDO Block Diagram

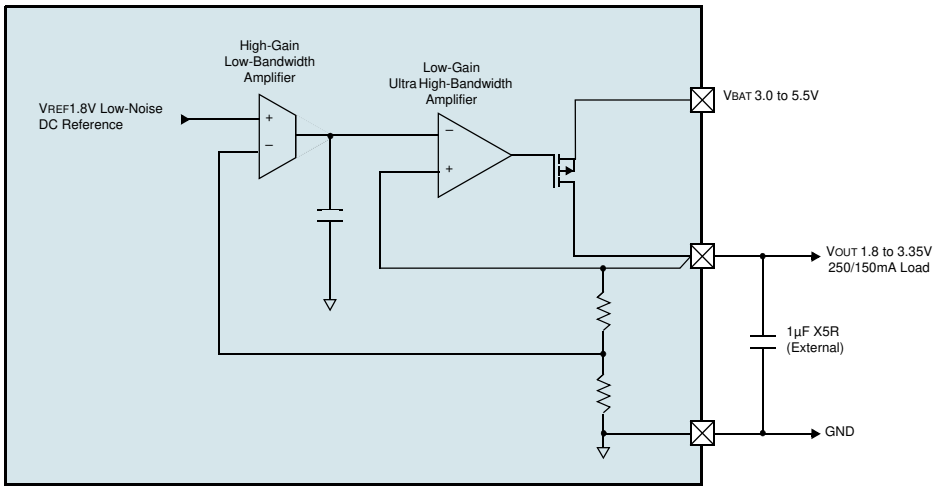


Table 9. RF and Analog LDO Characteristics
V_{BAT} = 3.6V; I_{LOAD} = 150mA; T_A = 25ºC; C_{LOAD} = 2.2µF (Ceramic); unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VBAT	Supply Voltage Range	3		5.5	V	
RON	On-Resistance			1	Ω	VANA_1, VANA_2
				2		VRF_1, VRF_2, VRF_3, VRF_4
PSRR	Power Supply Rejection Ratio	70			dB	f = 1kHz
		40				f = 100kHz
IOFF	Shut Down Current			100	nA	
IVDD_LDO	Supply Current			50	µA	Without load
Noise	Output Noise		30	50	µVrms	10Hz < f < 100kHz
tSTART	Startup Time			200	µs	
VOUT	Output Voltage	1.8		2.85	V	VBAT > 3.0V
		1.8		3.35		Full programmable range
VOUT_TOL	Output Voltage Tolerance	-50		50	mV	
VLINEREG	Line Regulation	-1		1	mV	Static
		-10		10		Transient; Slope: t_r = 10µs
VLOADREG	Load Regulation	-1		1	mV	Static
		-10		10		Transient; Slope: t_r = 10µs
ILIMIT	Current Limitation	250	400		mA	VANA_1, VANA_2
		150	180		mA	VRF_1, VRF_2, VRF_3, VRF_4

7.3.2 SIMCard Low Dropout Regulator

The SIMCard LDO (VSIM) is optimized for SIMCard supply. It is designed to achieve the lowest possible power consumption and still provide reasonable regulation characteristics. To ensure high PSRR and stability, a low-ESR ceramic capacitor of 100nF (min.) must be connected to the output. The LDO has a built-in discharge function when switched off.

Table 10. LDO VSIM Characteristics
V_{BAT} = 3.6V; I_{LOAD} = 20mA; T_A = 25ºC; C_{LOAD} = 100nF (Ceramic); unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VBAT	Supply Voltage Range	3		5.5	V	
RON	On-Resistance			50	Ω	
PSRR	Power Supply Rejection Ratio	40			dB	f = 1kHz
		20				f = 100kHz
IOFF	Shut Down Current			100	nA	
IVDD_SIMCARD	Supply Current		40		µA	
tSTART	Startup Time			200	µs	
VOUT	Output Voltage	1.8		3.0	V	VBAT > 3.2V
VOUT_TOL	Output Voltage Tolerance	-50		50	mV	
VLINEREG	Line Regulation	-10		10	mV	Static
		-100		100		Transient; Slope: t_r = 10µs

Table 10. LDO VSIM Characteristics (Continued)
V_{BAT} = 3.6V; I_{LOAD} = 20mA; T_A = 25ºC; C_{LOAD} = 100nF (Ceramic); unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{LOADREG}$	Load Regulation	-10		10	mV	Static
		-100		100		Transient; Slope: t_r = 10µs

7.3.3 Low Power Low Dropout Regulator

The low-power bootstrap LDO (V2_5) is needed to supply power to the core (analog and digital) of the AS3605. LDO V2_5 is designed to achieve the lowest possible power consumption, and still provide reasonable regulation characteristics. LDO V2_5 has two supply inputs selecting automatically the higher one. This gives the possibility to supply the AS3605 core either with the battery or with the Battery Charger, depending on the conditions.

To ensure high PSRR and stability, a low-ESR ceramic capacitor of 1µF (min.) must be connected to the output.

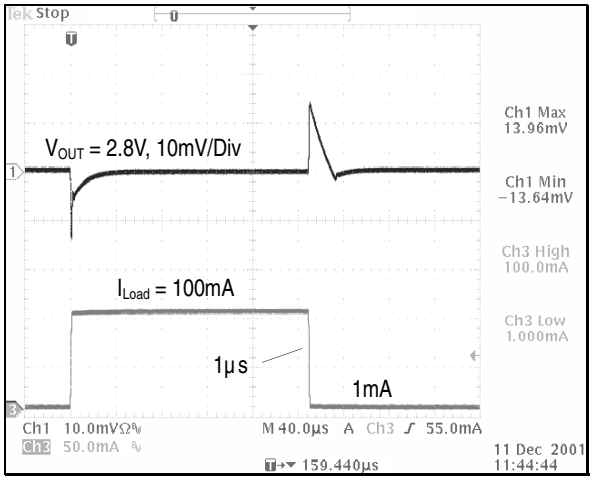
Note: Levelshifters in both directions (input and output) are placed between digital pins (VANA_1) and the digital core (V2_5) of the device, because of the different power supplies.

Table 11. LDO V2_5 Characteristics
V_{BAT} = 3.6V; C_{LOAD_EXT} = 0; T_A = 25ºC; C_{LOAD} = 2.2µF (Ceramic); unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{BAT}	Supply Voltage Range	2.8		5.5	V	
$V_{CHARGER}$	External Charger Adapter voltage	4		15	V	
R_{ON}	On-Resistance		50		Ω	Guaranteed per design
I_{OFF}	Shut Down Current			100	nA	
I_{VDD_LPLDO}	Supply Current			3	µA	Guaranteed per design; consider device internal load for measurement
t_{START}	Startup Time			200	µs	
V_{OUT}	Output Voltage	2.4	2.5	2.6	V	

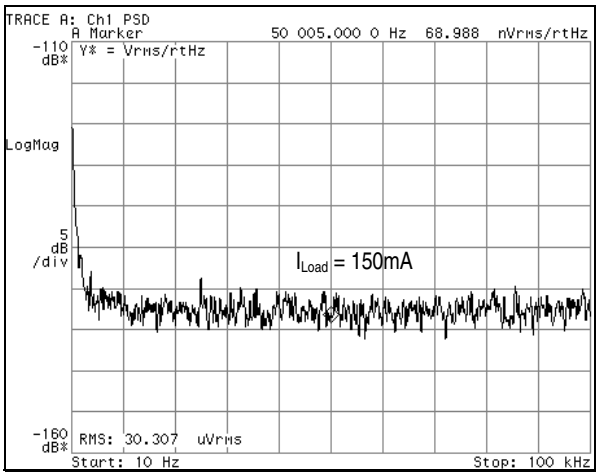
7.3.4 Typical Performance Characteristics

Figure 10. Load Regulation of LDOs VANA_1, VANA_2



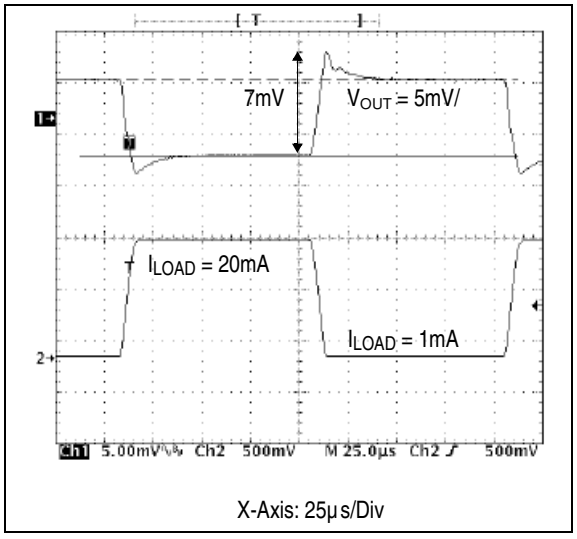
X-Axis: 40µs/Div

Figure 11. Output Noise of LDOs VANA_1, VANA_2



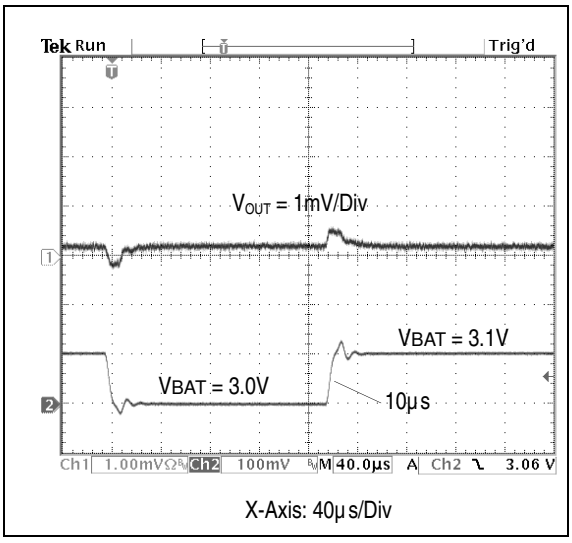
Spectral Distribution at 150mA Output Load

Figure 12. Load Regulation of LDO V2_5



X-Axis: 25µs/Div

Figure 13. Line Regulation of LDO V2_5



X-Axis: 40µs/Div