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AS3608

System PMU with HV Back Light Driver

1 General Description

The AS3608 is an ultra compact System PMU with integrated battery charger and HV back light driver.

The device offers advanced power management functions. All necessary ICs and peripherals in a battery powered mobile device are supplied by the AS3608. It features 3 DCDC converters as well as 5 low noise LDOs. The different regulated supply voltages are programmable via the serial control interface.

The step-up converter for the backlight can operate up to 30V. Both constant voltage (OLED supply) as well as constant current (white LED backlight) operations with 2 current sinks are possible. An internal voltage protection is limiting the output voltage in the case of external component failures.

AS3608 also contains a Li-Ion battery charger with constant current and constant voltage. The maximum charging current is 1A. An integrated battery switch and an optional external switch are separating the battery during charging or whenever an external power supply is present. With this switch it is also possible to operate with no or deeply discharged batteries. A programmable current limit can be used to control the maximum current used from a USB supply.

The single supply voltage may vary from 2.7V to 5.5V.

2 Key Features

Power Management

Voltage Generation

- 3 DCDC step down regulators
  - DVM (0.61V-3.3V, 1A@1.2V, 900mA@1.8V 800mA@2.5V)
  - 50µA quiescent current
  - Selectable switching frequency (2 or 1MHz)
  - 2A@1.2V with combined DCDC 2 & 3
- 1 LDO low noise 2.7V (2.3-3.5V), 100mA
- 3 or 4 LDOs low noise
  - 1.2-3.5V; 160/270mA
  - 30µA quiescent current (low power mode)
- Power supply supervision (LDO5)
- 4sec and 8sec emergency shut-down
- Hibernation function

HV Backlight Driver

- Step up for 30V backlight with internal transistor
- Voltage control mode and over-voltage protection
- 2 programmable current sink (max. 38mA)
- Max. 20mA@50V (with ext. transistor) or 500mA@5V
- Possible external PWM dimming input

Battery Charger

- Prog. trickle charging (25-265mA)
- Prog. constant current charging (94-1060mA)
- Prog. constant voltage charging (3.9V-4.25V)
- Charger time-out and temperature supervision
- Selectable current limitation for USB mode
- Integrated battery switch & ideal diode
- External battery switch control output

General

Battery and Temperature Supervisor

4 General Purpose IOs

- 10bit general purpose ADC input
- PWM dimming input or wake-up input
- Status output for: charger, low battery, power good and power-up key

OTP Programmable BOOT Sequence

- Programmable regulator default voltages
- Programmable start-up sequence
- Applicable for LDO 1-4 and DCDC 1-3

Control Interface

- I2C control lines, including watchdog
- Power-Up input
- Interrupt output
- Bidirectional reset, with selectable delay
- Low power standby mode, 180µA with LDO5 on

Power-On Reset Circuit

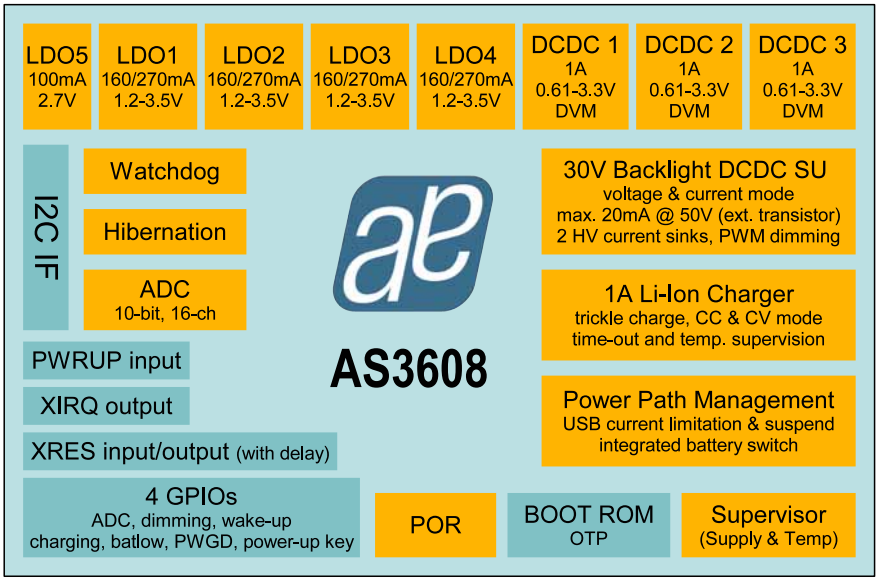
Packaging

QFN36 6x6mm, 0.5mm pitch

3 Application

The devices are ideal for Portable Media Players and Portable Navigation Devices, e-Books, Tablet PCs, etc

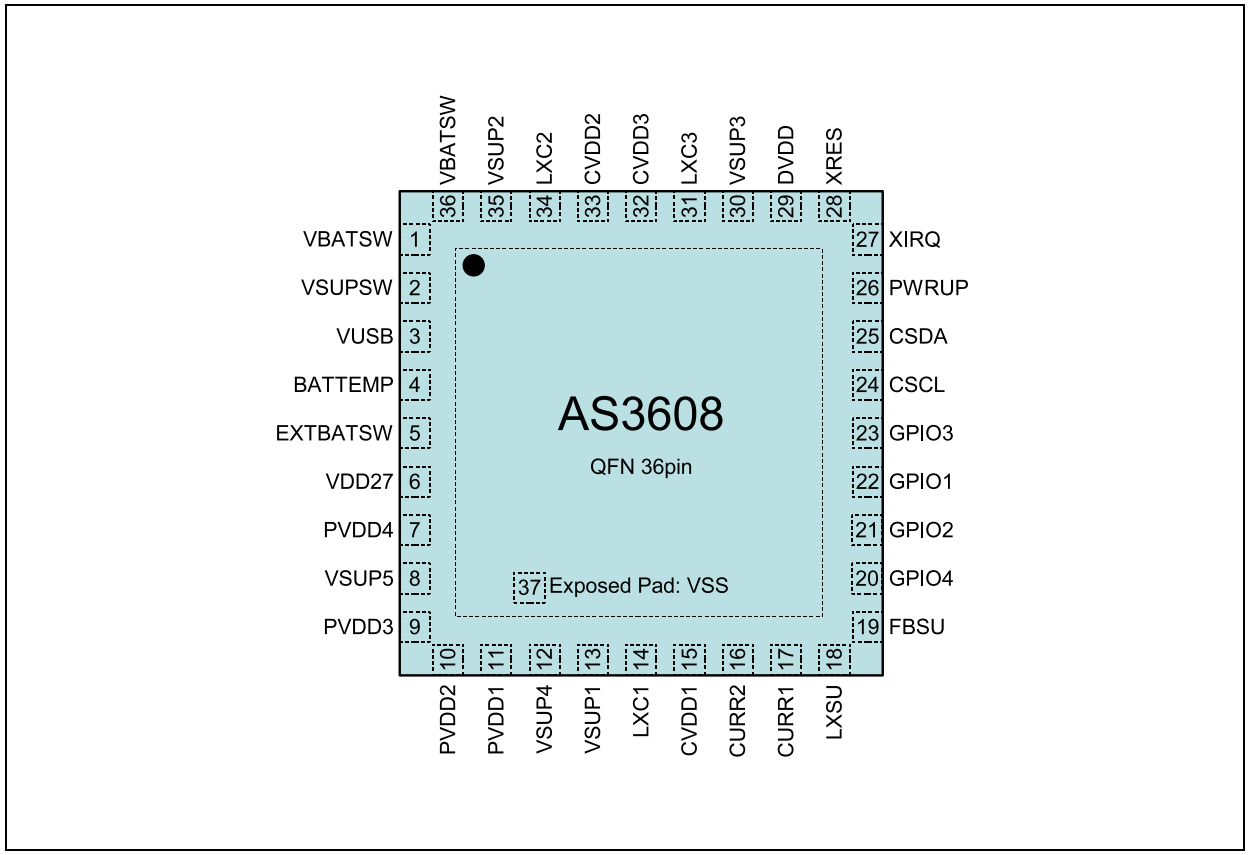
Figure 1. AS3608 Block Diagram



Contents

4 Pin Assignments

Figure 2. Pin Assignments (TopView)



4.1 Pin Descriptions

Note: Pin description may change in preliminary data sheets.

Table 1. Pin Description for AS3608

Pin Name	Pin Number	Type	Description	if not used
	AS3608			
VBATSW	1	SUP IO	Battery Switch Terminal to be connected to the Li-Ion battery	open
VSUPSW	2	SUP IO	Battery Switch Terminal to be connected to system supplies VSUPx	always needed
VUSB	3	SUP IN	Charger or USB Bus Power Input	open
BATTEMP	4	ANA IO	Li-Ion Charger Battery Temp. Sensor Input	open
EXTBATSW	5	ANA OUT	External Battery Switch Gate Driver Output	open
VDD27	6	SUP IO	LDO5 Output default 2.7V	always needed
PVDD4	7	ANA OUT	LDO4 Output	open
VSUP5	8	SUP IN	LDO3/4 & LDO5 Pos. Supply Terminal, connect to VSUPSW	always needed
PVDD3	9	ANA OUT	LDO3 Output	open
PVDD2	10	ANA OUT	LDO2 Output	open
PVDD1	11	ANA OUT	LDO1 Output	open
VSUP4	12	SUP IN	LDO1/2 Pos. Supply Terminal	always needed

Table 1. Pin Description for AS3608

Pin Name	Pin Number AS3608	Type	Description	if not used
VSUP1	13	SUP IN	CVDD1 Step Down Pos. Supply Terminal	always needed
LXC1	14	DIG OUT	CVDD1 Step Down Switch Output to Coil	open
CVDD1	15	ANA IN	CVDD1 and Feedback Pin	open
CURR2	16	ANA IO	Load Current Sink2 Terminal	open
CURR1	17	ANA IO	Load Current Sink1 Terminal	open
LXSU	18	DIG OUT	DCDC Step-Up Switch Output to Coil	open
FBSU	19	ANA IN	DCDC Step-Up Feed-Back	open
GPIO4	20	ANA IO	General Purpose IO 4	open
GPIO2	21	ANA IO	General Purpose IO 2	open
GPIO1	22	ANA IO	General Purpose IO 1	open
GPIO3	23	ANA IO	General Purpose IO 3	open
CSCL	24	DIG IN	2-wire SERIF Clock Input	open
CSDA	25	DIG IO	2-wire SERIF Data I/O	open
PWRUP	26	DIG IN	Power Up Input	open
XIRQ	27	DIG OUT	Interrupt Request Output	open
XRES	28	DIG IO	Reset Output	open
DVDD	29	SUP IN	Digital Periphery Pos. Supply Terminal	always needed
VSUP3	30	SUP IN	CVDD3 Step Down Pos. Supply Terminal	VSUPx
LXC3	31	DIG OUT	CVDD3 Step Down Switch Output to Coil	open
CVDD3	32	ANA IN	CVDD3 and Feedback Pin	open
CVDD2	33	ANA IN	CVDD2 and Feedback Pin	open
LXC2	34	DIG OUT	CVDD2 Step Down Switch Output to Coil	open
VSUP2	35	SUP IN	CVDD2 Step Down Pos. Supply Terminal	always needed
VBATSW	36	SUP IO	Battery Switch Terminal to be connected to the Li-Ion battery	open
VSS	37	SUP IO	Exposed Pad: Neg. Supply Terminal for all blocks	always needed

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 8 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated under recommended operating conditions.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
5V pins	-0.5	7.0	V	Applicable for pins VBATSW, VSUPSW, VSUP1/2/3/4/5, PWRUP, GPIO1/2/3/4, VBUS
3V pins	-0.5	5.0	V	Applicable for pins DVDD
30V pins	-0.5	32	V	Applicable for pin LXSU, CURR1/2
5V pins with protection to VSUPx	-0.5	7.0 VSUPx+0.5	V	Applicable for pins EXTBATSW, FBSU
3V pins with protection to VDD27	-0.5	5.0 VDD27	V	Applicable for pins BATTEMP
3V pins with protection to DVDD	-0.5	5.0 DVDD+0.5	V	Applicable for pins XIRQ, XRES, CSCL, CSDA
3V pins with protection to VSUPx	-0.5	5.0 VSUPx+0.5	V	Applicable for pins PVDD1/2/3/4, VDD27, CVDD1/2/3, LXC1,/2/3
Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC 78
Continuous Power Dissipation (T_A = +85ºC)				
Continuous power dissipation		1	W	P_T[1] for QFN36 package (R_{TH} ~ 30K/W)
Electrostatic Discharge				
Electrostatic Discharge HBM		±1.5	kV	Norm: JEDEC JESD22-A114C
Temperature Ranges and Storage Conditions				
Junction Temperature		+110	ºC	
Storage Temperature Range	-55	+125	ºC	
Humidity non-condensing	5	85	%	
Temperature (soldering)				
Package Body Temperature		260	ºC	Norm IPC/JEDEC J-STD-020[2] The lead finish for Pb-free leaded packages is matte tin (100% Sn)
Moisture Sensitive Level	3			Represents a max. floor live time of 168h

1. Depending on actual PCB layout and PCB used
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

6 Electrical Characteristics

VSUPx=+2.7V...+5.5V, T_A =-40ºC...+85ºC. Typical values are at VSUPx=+3.6V, T_A=+25ºC, unless otherwise specified.

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VBATSW	Battery Supply Voltage	operation, VBUS > 2.7V	0	3.6	5.5	V
		operation from battery	2.7	3.6	5.5	V
VSUPx	Supply Voltage VSUPSW, VSUP1/2/3/4/5		2.7	3.6	5.5	V
VBUS	USB VBUS Voltage	operating, VSUP5 > 2.7V	0	5.0	5.5	V
		charging	4.5	5.0	5.5	V
DVDD	Digital Periphery Supply Voltage		1.8		3.6	V
VDD27	Analog Supply Voltage		2.6	2.7	3.5	V
V_{DELTA+}	Difference of Positive Supplies	VDD27-VSUPx			0	V
T_{AMB}	Operating Temperature Range		-40		+85	ºC
I_{SD}	Shut-down current	@ VBATSW = 4.2V		600		nA
I_q	Quiescent current	All regulators off reference & LDO5 on		180		µA
IO Pins						
VID_{3V}	3V digital input pins XRES, CSCL, CSDA		0		3.6V or DVDD +0.5	V
VIA_{3V}	3V input pin BATTEMP		0		3.6V or VDD27 +0.5	V
VI_{5V}	5V input pins GPIO1/2/3/4		0		5.5V	V
VI_{5V}	5V input pin FBSU		0		5.5V or VSUP5 +0.5	V
VI_{30V}	20V analiog input pins LXSU, CURR1/2		0		30	V
POR & Watchdog						
V_{POR_ON}	Power-on Reset Activation Level	Power-on Reset activation level when VDD27 decreases		2.15		V
V_{POR_OFF}	Power-on Reset Release Level	Power-on Reset release when VDD27 increases		2.0		V
V_{POR_HY}	Power-on Hysteresis			100		mV
PWRUP						
t_{ON_DELAY}	Delay Time of pin PWRUP	Minimum key press time	60			ms
V_{PWRUP_L}	Input Level LOW	Pin PWRUP, VSUP5>3V			0.5	V
V_{PWRUP_H}	Input Level HIGH	Pin PWRUP, VSUP5>3V	VSUP5/3			V
		Pin PWRUP, VSUP5<=3V	1			V
I_{PWRUP}	Internal Pull-down Current Source	Pin PWRUP; @2.7V	10	20	30	µA

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Digital Inputs/Outputs						
V_{DO_DL}	Digital Output Driver Capability (drive LOW)	Pins XRES, XIRQ, GPIOx @ 6mA, open drain mode			20% DVDD	V
I_{PU}	Internal Pull-up Current Source	Pins XIRQ, XRES @ 0V		13		µA
		Pins CSDA, CSCL @ 0V		100		µA
I_{PD}	Internal Pull-down Current Source	Pins GPIOx @ 2.7V	8	13	20	µA
V_{DI_L}	Digital Input Level LOW	Pin GPIOx		30% DVDD		V
V_{DI_H}	Digital Input Level HIGH	Pin GPIOx		70% DVDD		V

7 Typical Operating Characteristics

VSUPx = +3.6V, T_A = +25ºC, unless otherwise specified.

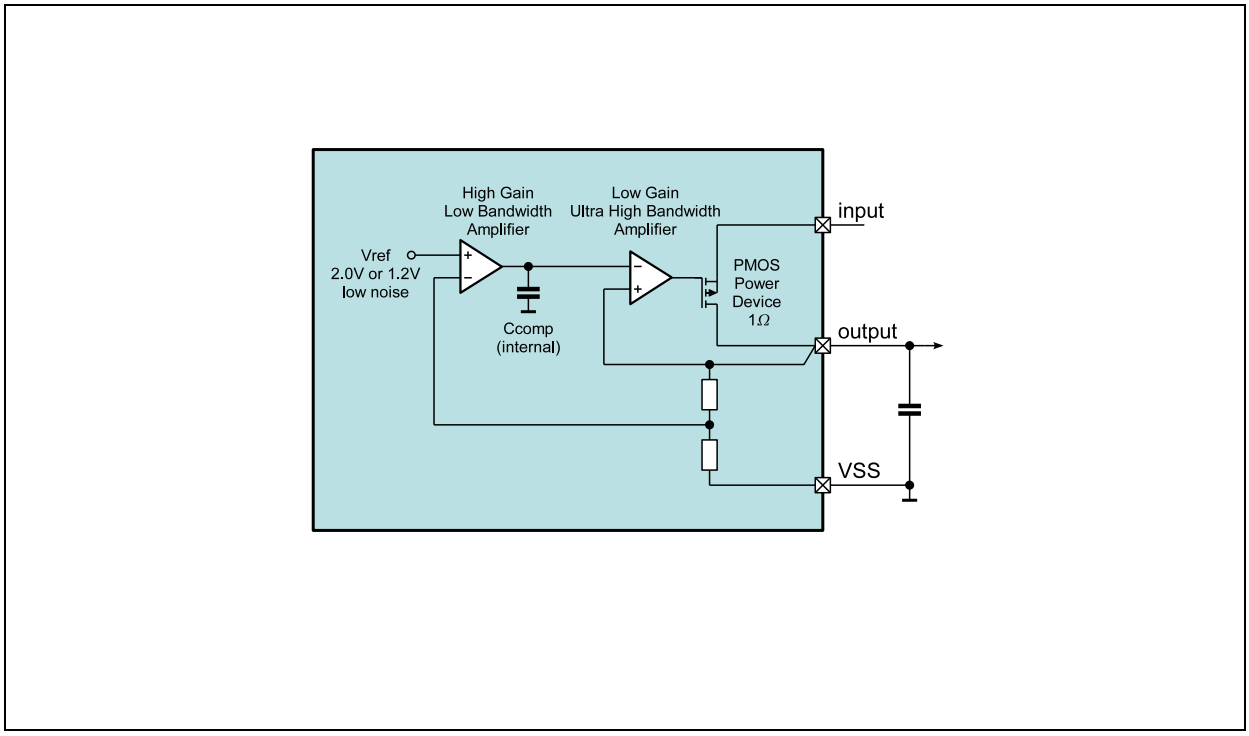
8 Detailed Description - Power Management Functions

8.1 Low Drop Out Regulators

These LDOs are designed to supply sensitive analog circuits, audio devices, AD and DA converters, micro-controller and other peripheral devices. The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of 1µF ±20% (X5R) or 2.2µF +100/-50% (Z5U). The low ESR of these caps ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress high ripple on the battery at the output. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power device enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease of performance.

Figure 3. LDO Block Diagram



8.1.1 LDO5

This LDO generates the digital supply voltage used for the PMU itself.

- Input Voltage is VSUP5
- Output Voltage is VDD27 (typ. 2.7V), this LDO always starts at the beginning of the start-up sequence as it is needed for all further operation. The default voltage cannot be changed in the boot ROM.
- Driver strength: 100mA, can be programmed to 200mA

It is set to a default output voltage of 2.7V, 100mA$_{max}$. It supplies the analog and digital part of the PMU. Additional external loads are possible but must not exceed the supply ratings in total together with the operating internal blocks. Further, the external load must not induce noise to the VDD27.

8.1.2 LDO 1, LDO2, LDO3 & LDO4

These LDOs can be used to generate the periphery voltage for the digital processor or other external components (e.g. ext. DAC, USB-PHY, SD-Cards, NAND-Flashes, FM-Tuner …). LDO4 is only available on AS3608.

- Input Voltage VSUP5 for LDO3 and LDO4, and VSUP4 for LDO2 and LDO1
- Output Voltage is PVDD1, PVDD2, PVDD3 & PVDD4 (1.2V to 3.5V)
- Default value at start-up is defined by the boot ROM, when the boot ROM is not programmed the LDOs will not start-up
- Driver strength: 160mA, can be programmed to 270mA

8.1.3 Parameter

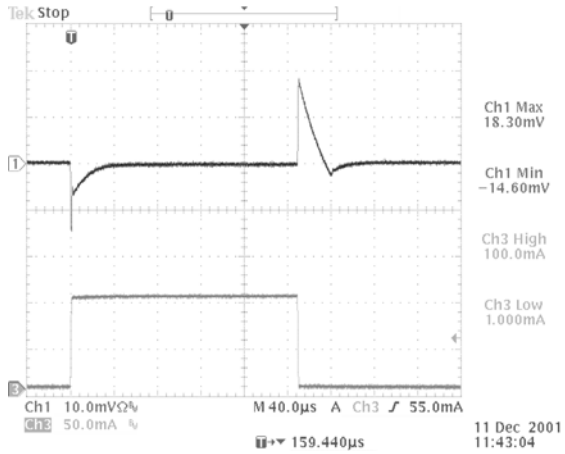
VSUPx=3.6V, T_A= 25ºC, unless otherwise specified.

Table 4. LDO Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{ON}	On resistance				1	Ω
PSRR	Power supply rejection ratio	f=1kHz		70		dB
		f=100kHz		40		
I_{OFF}	Shut down current			100		nA
I_{VDD}	Supply current	without load		50		µA
		low power enabled, without load		32		µA
Noise	Output noise	10Hz < f < 100kHz		50		μV_{rms}
t_{start}	Startup time			200		µs
V_{out_tol}	Output voltage tolerance	minimum ±50mV	-2.5%		2.5%	mV
$V_{LineReg}$	Line regulation	Static		<1		mV
		Transient; Slope: t_r=10µs		<10		
$V_{LoadReg}$	Load regulation	Static		<1		mV
		Transient; Slope: t_r=10µs		<10		
I_{LIMIT}	Current limitation	default		200		mA
		has to be enabled via register		370		

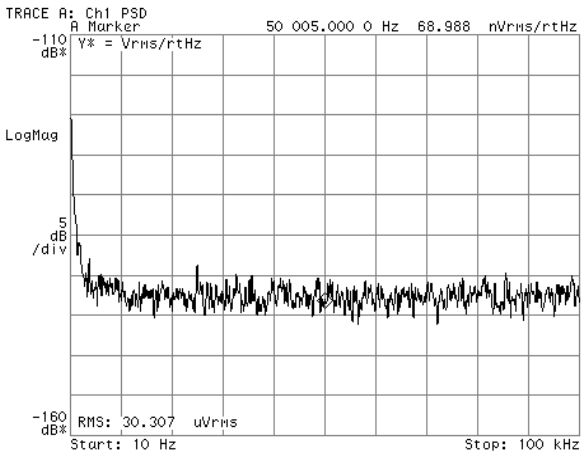
Figure 4. LDO Characteristics

Load Regulation



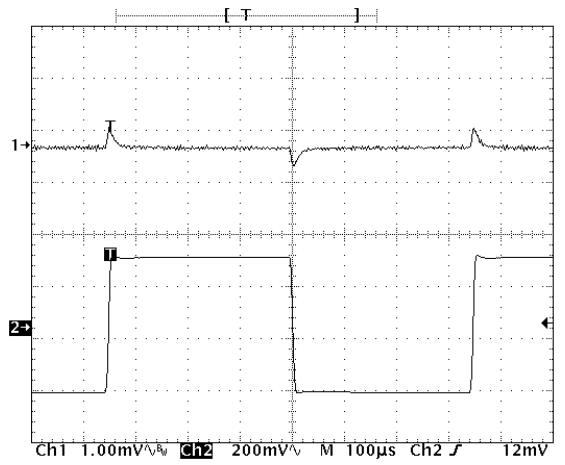
transient load: 1mA – 100mAslope: 1µs

Output Noise



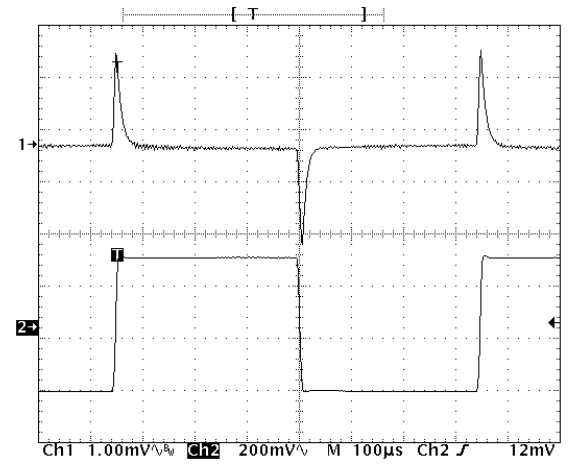
Output load: 150mA

Load Regulation



output load: 10mA
transient input voltage ripple: 500mV

Load Regulation



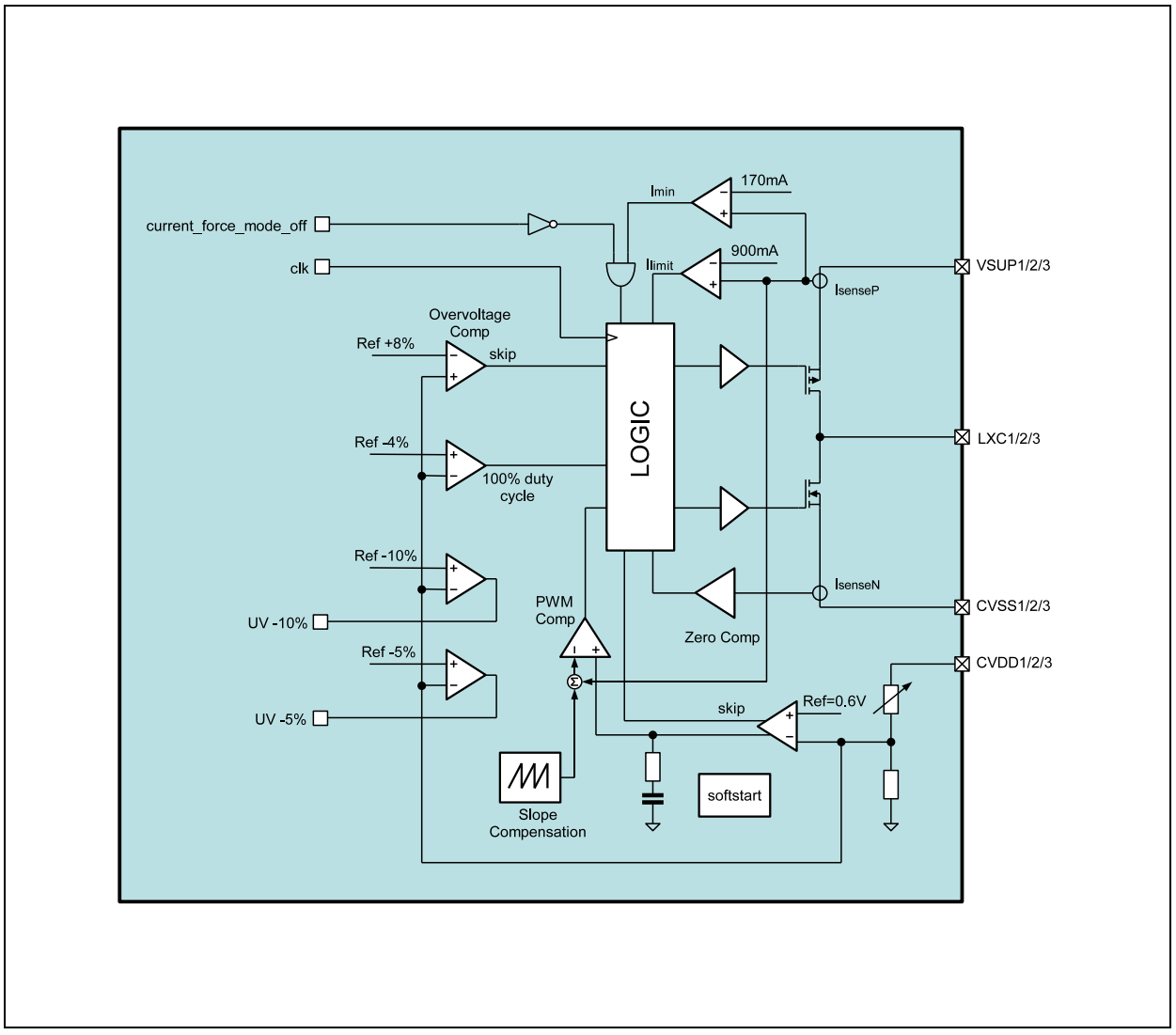
output load: 150mA
transient input voltage ripple: 500mV

8.2 DCDC Step-Down Converter

These converters are meant to convert the battery voltage down to voltages which fit to the core and peripheral supply voltage requirements for microprocessors.

- Input Voltage VSUP1/2/3 (usually connected to VSUPSW)
- Output Voltage CVDD1 & CVDD2 & CVDD3
- Output voltage levels can be programmed independently form 0.61V to 3.35V
- The default value at start-up is defined by the boot ROM
- DVM for all three outputs with selectable timings
- Driver strength 1A@1.2V, DCDC2 & 3 can be combined together to double the output current
- Under- and over-voltage detection
- High efficiency current force mode
- 1MHz or 2MHz switching frequency
- Fast regulation mode

Figure 5. DCDC Step-Down Block Diagram



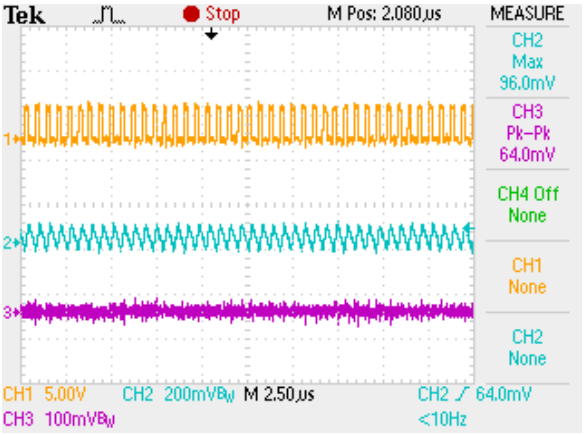
8.2.1 Functional Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 97% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 700mA, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC and the coil during overload condition.

To achieve optimized performance in different applications, adjustable settings allow to compromise between high efficiency and low input, output ripple:

Low Ripple, Low Noise Operation (current force mode = OFF). In this mode there is no minimum coil current necessary before switching off the PMOS. As result, the ON time of the PMOS will be reduced down to tmin_on at no or light load conditions, even if the coil current is very small or the coil current is inverted. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences. In the case of an inverted coil current the regulator will not operate in pulse skip mode.

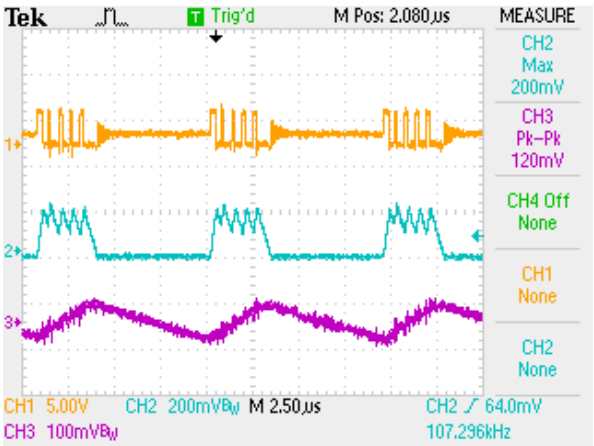
Figure 6. DCDC Buck with Disabled Current Force / Pulse Skip Mode



1: LXC1 voltage
2: Coil current (1mV=1mA)
3: Output voltage

High Efficiency Operation (current force mode = ON). In this mode, there is a minimum coil current necessary before switching off the PMOS. As result, fewer pulses at low output loads are necessary, and therefore the efficiency at low output load is increased. On the other hand the output voltage ripple increases, and the noisy pulse skip operation is on up to a higher output current.

Figure 7. DCDC Buck with Enabled Current Force / Pulse Skip Mode



1: LXC1 voltage
2: Coil current (1mV=1mA)
3: Output voltage

It's also possible to switch between these two modes dynamically during operation.

DVM (Dynamic Voltage Management). To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

Fast Regulation Mode. This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. FRM needs an 22uF output capacitor instead the 10uF one to guarantee the stability of the regulator.

Low Frequency Operation. Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency.

100% PMOS ON Mode for Low Dropout Regulation. For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is than in LDO mode.

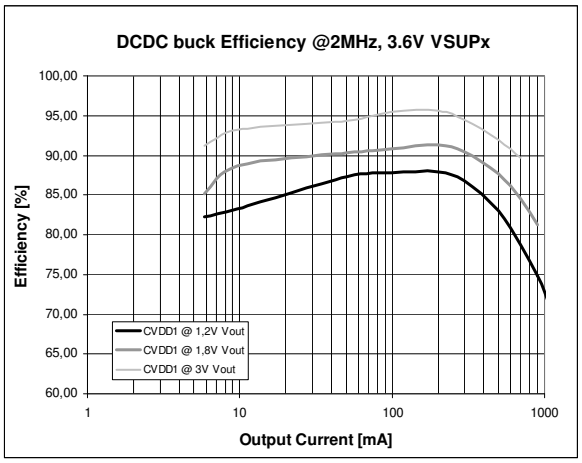
8.2.2 Parameter

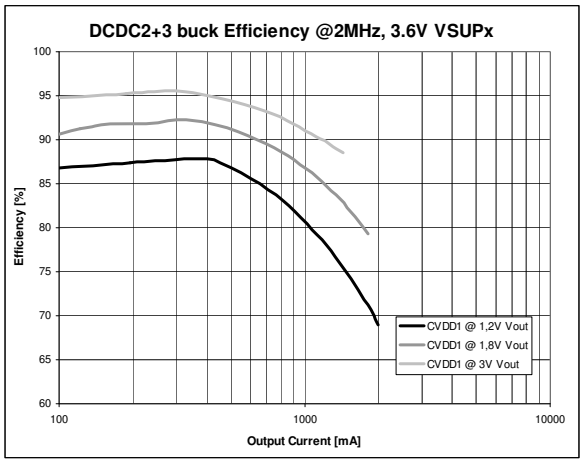
VSUP=3.6, T_A= 25ºC, unless otherwise specified.

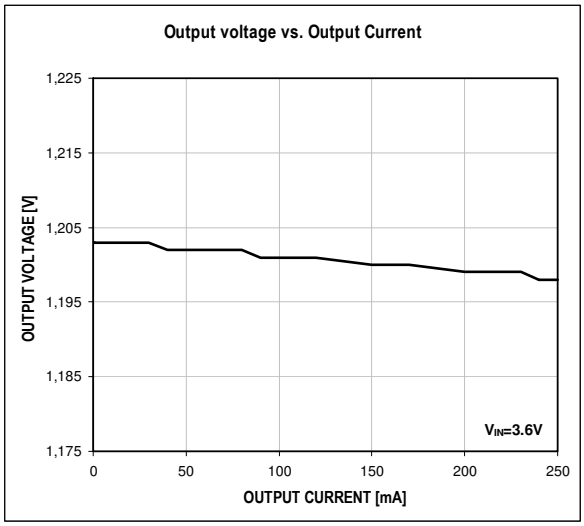
Table 5. DCDC Parameter

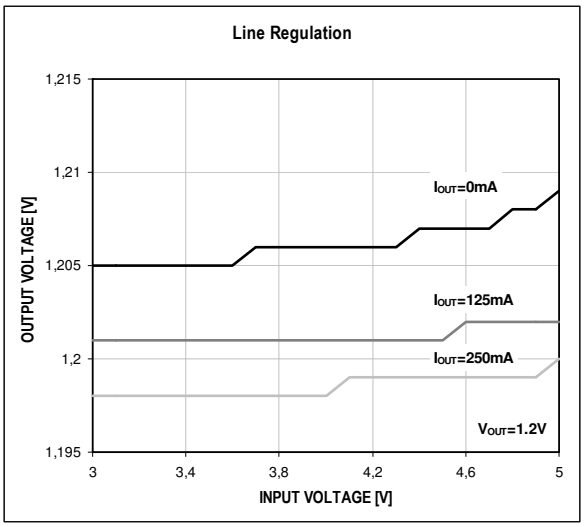
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input voltage	VSUPx	2.7		5.5	V
V_{OUT}	Regulated output voltage		0.6125		3.35	V
V_{OUT_tol}	Output voltage tolerance	minimum ±50mV	-3%		3%	mV
I_{load}	Maximum Load current				700	mA
		Vout=2.5V			800	mA
		Vout=1.8V			900	mA
		Vout=1.2V			1000	mA
I_{load}	Maximum Load current DCDC2+DCDC3				1400	mA
		Vout=2.5V			1600	mA
		Vout=1.8V			1800	mA
		Vout=1.2V			2000	mA
I_{LIMIT}	Current limit			1200		mA
R_{PSW}	P-Switch ON resistance	VSUPx=3.0V		0.5	0.7	Ω
R_{NSW}	N-Switch ON resistance	VSUPx=3.0V		0.5	0.7	Ω
f_{SW}	Switching frequency	depending on DCDC_Cntr settings		1/2		MHz
f_{SWsc}	Switching frequency	in shortcut case		0.6		MHz
C_{out}	Output capacitor	Ceramic, ±10% tolerance		10		µF
Lx	Inductor	±10% tolerance		2.2		µH
η_{eff}	Efficiency	Iout=150mA, Vout=3.0V		97		%
I_{VDD}	Current consumption	Operating current without load Shutdown current		65 0.1		µA
t_{MIN_ON}	Minimum on time			80		ns
t_{MIN_OFF}	Minimum off time			40		ns
$V_{LineReg}$	Line regulation	Static		2		mV
		Transient; Slope: t_r=10µs, 100mV step, 200mA load		10		
$V_{LoadReg}$	Load regulation	Static		5		mV
		Transient; Slope: t_r=10µs, 100mA step		50		

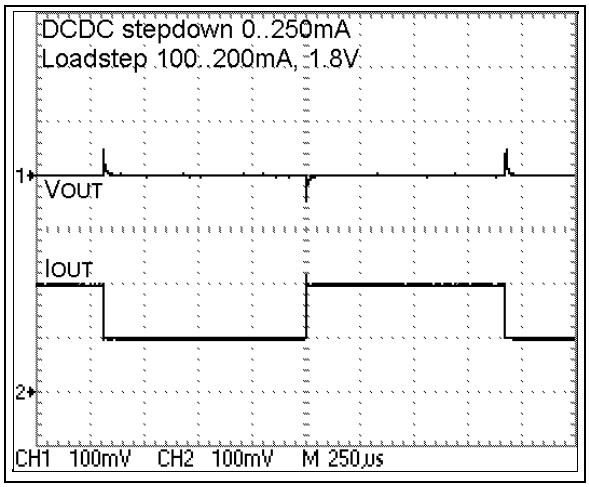
Figure 8. DCDC Step-down Performance Characteristics

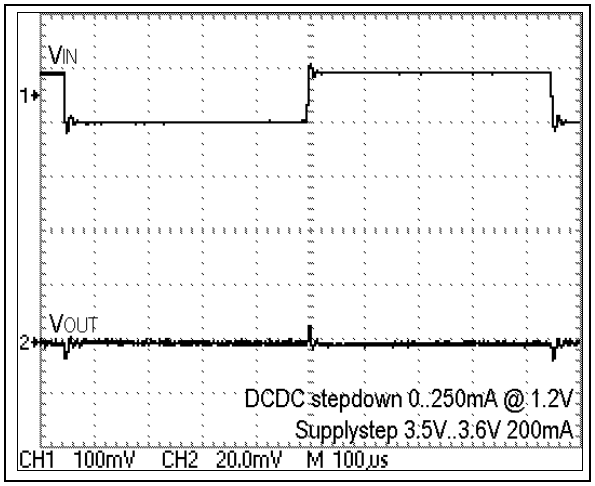












8.3 30V Step-Up DCDC Converter

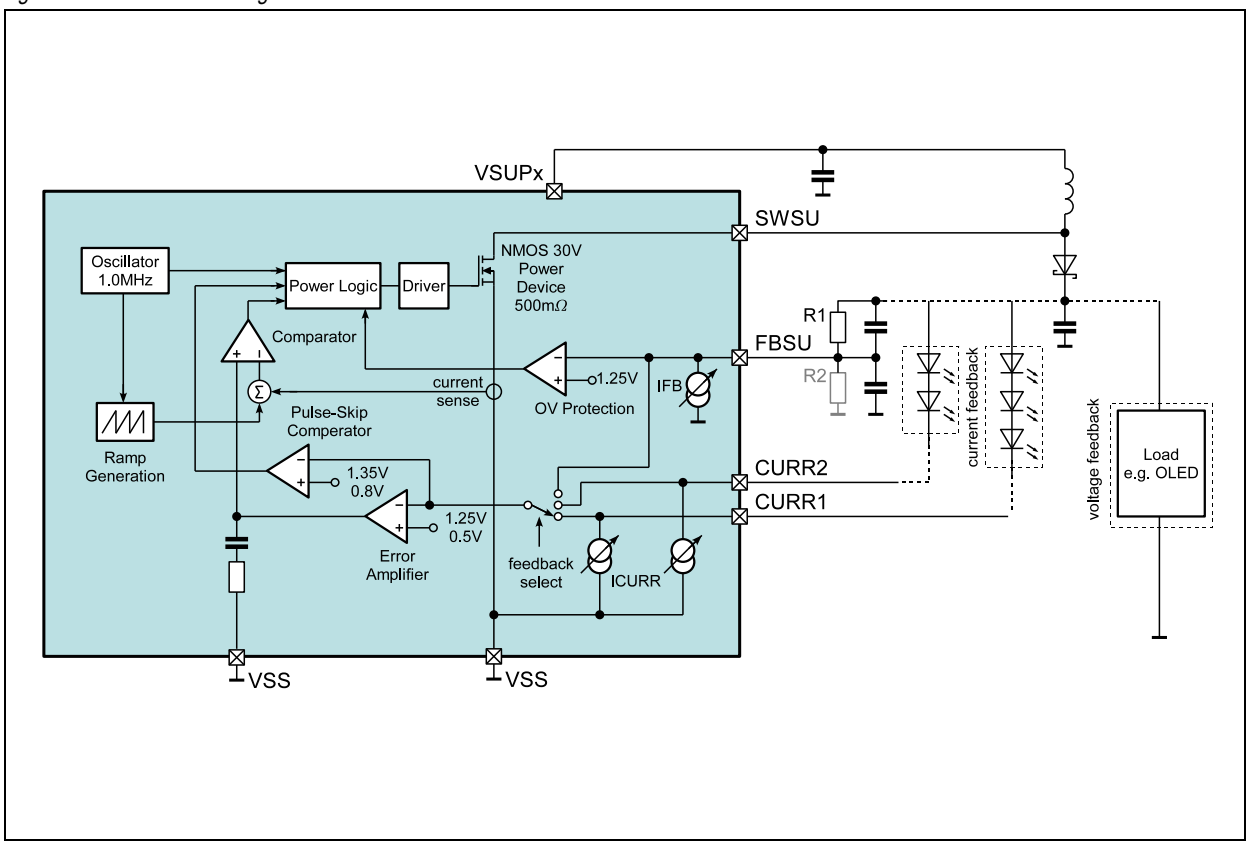
The integrated Step-Up DC/DC Converter is a high efficiency current-mode PWM regulator, providing an output voltage up to 30V. A constant switching-frequency results in a low noise on supply and output voltages.

It has two programmable high voltage current sinks (0 to 38.25mA) for driving e.g. white LEDs as back-light. It can drive also unbalanced strings due to the internal automatic feedback selection.

A voltage feedback mode allows generating constant supply voltages for e.g. OLEDs. The output voltage is set by an external resistor divider and an internal current sink.

An internal protection circuit will shut down the regulator if the voltage on FBSU exceeds the over voltage threshold. No more external protection has to be used to avoid an exceeding of the operation conditions in a no load situation.

Figure 9. DCDC15 Block Diagram



8.3.1 Voltage Feedback and OV Protection

8.3.2 Voltage Feedback

Setting bit **SU_CURR_FB** = 0 enables voltage feedback at pin FBSU.

The output voltage is regulated to a constant value, given by (Bit **SU_GAIN** should be set to 1 in this configuration)

$$U_{Step\ up\_out} = (R1+R2)/R2 * 1.25 + I_{FB} * R1 \qquad (EQ\ 1)$$

If R2 is not used, the output voltage is by (Bit **SU_GAIN** should be set to 0 in this configuration)

$$U_{Step\ up\_out} = 1.25 + I_{FB} * R1 \qquad (EQ\ 2)$$

Where:

$U_{Step\ up\_out}$ = Step Up DC/DC Converter output voltage

$R1$ = Feedback resistor R1

$R2$ = Feedback resistor R2

I_{FB} = Tuning current at pin FBSU; 0 to 31µA

Table 6. Voltage Feedback Example Values

IDCDC_FB	$U_{Step\ up\_out}$	$U_{Step\ up\_out}$
µA	R1 = 1MΩ, R2 not used	R1 = 500kΩ, R2 = 50kΩ
0	-	13.75
1	-	14.25
2	-	14.75
3	-	15.25
4	-	15.75
5	6.25	16.25
6	7.25	16.75
7	8.25	17.25
8	9.25	17.75
9	10.25	18.25
10	11.25	18.75
11	12.25	19.25
12	13.25	19.75
13	14.25	20.25
14	15.25	20.75
15	16.25	21.25
…	…	…
30	31.25	28.75
31	32.25	29.25

Note: The voltage on CURR1 and CURR2 must not exceed 30V.

8.3.3 Over Voltage Protection (OVP)

Setting bit **SU_CURR_FB** = 1 enables feedback via the current sink pins. The voltage on the current sink pin is regulated to **VCURR**. The selection of the current sink with the larger load is done automatically. The pin FBSU acts as an overvoltage protection in this mode. Please be sure to set the voltage to a higher level than needed to drive the longer LED string. The calculation of the resistor can be done the same as described in the chapter above.

8.3.4 DLS & Dimming

AS3608 feature external dimming inputs via CURR1, CURR2, GPIO1 or GPIO2 by directly connecting a PWM output of e.g. the display controller for DLS (dynamic luminance scaling). Manual dimming can be done at any time by setting the sink current via I2C commands.

8.3.5 Current Sinks

The current sinks work independent from each other and can also be used without the booster, or can act as a dimming input if they are not needed as a sink.

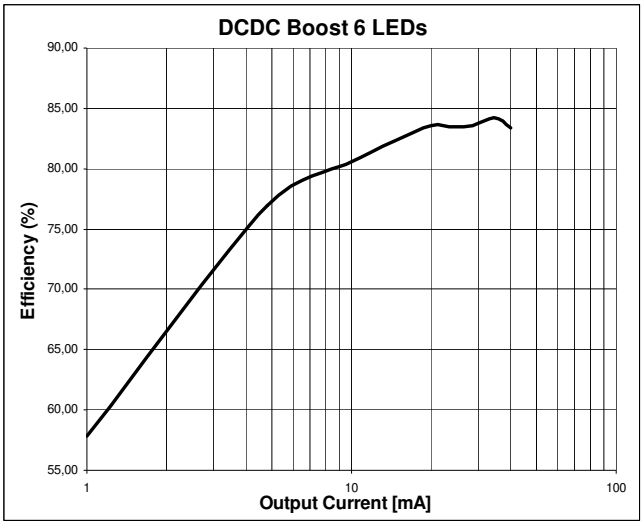
8.3.6 Parameter

VSUPx=3.6V, T_A= 25ºC, unless otherwise specified.

Table 7. DCDC Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{SW}	High Voltage Pin	Pin FBSU	0		30	V
I_{VDD}	Quiescent Current	Pulse Skipping mode		140		µA
V_{FB}	Feedback Voltage, Transientt	Pin CURR1 or CURR2	0		30	V
		Pin FBSU	0		5	V
V_{FBSU}	Feedback Voltage, for voltage regulation	Pin FBSU	1.2	1.25	1.3	V
V_{CURR}	Feedback Voltage, for current sink regulation	Pin CURR1 or CURR2	0.4	0.5	0.6	V
I_{DCDC_FB}	Additional Tuning Current at Pin DCDC_FB and over voltage protection	Adjustable by software using Register DCDC control1 1µA step size (0-31µA) $V_{PROTECT}$ = 1.25V + IDCDC_FB * R_1	0		31	µA
	Accuracy of Feedback Current at full scale		-6		6	%
R_{SW}	Switch Resistance				1	Ω
I_{LOAD}	Load Current	@ 30V output voltage	0		50	mA
F_{SW}	Fixed Switching Frequency	SU_FREQU = 0		1		MHz
C_{OUT}	Output Capacitor	Ceramic, ±20%. Use nominal 4.7µF capacitors to obtain at least 0.7µF under all conditions (voltage dependence of capacitors)	0.7	4.7		µF
L	Inductor	Use inductors with small $C_{PARASITIC}$ (<100pF) for high efficiency	7	10	13	µH
t_{MIN_ON}	Minimum On-Time	Guaranteed per design		100	190	ns
MDC	Maximum Duty Cycle	Guaranteed per design	84	90		%

Figure 10. 30V Step-Up Performance Characteristics



8.4 Charger

This block can be used to charge a 4V Li-Ion accumulator. It supports constant current and constant voltage charging modes with adjustable charging currents (94 to 1000mA) and maximum charging voltage (3.9 to 4.25V).

The charger consists basically of a pre-regulator, which limits the current from e.g. the USB input and provides a constant VSUP after reaching EOC (end of charge) and the battery switch, which is controlling the current into the battery.

- Input Voltage of the pre-regulator: VUSB
- Output of the pre-regulator and input for the battery switch and system supply: VSUPSW
- Output of the battery switch and battery terminal: VBATSW
- CVM (constant voltage), CCM (constant current) and trickle charging
- Adjustable EOC voltage and EOC current limit
- Selectable input -, trickle- and charging-current limit
- Auto-resume with selectable resume voltage level
- Charger time-out supervision with selectable time-out setting
- Battery temperature supervision supporting two levels (45 or 50ºC) and 100k or 10k NTC types
- No battery detection
- Status register and interrupt generation

Per default the USB current limit is set to 470mA and the charger is switched off.

The current battery and charger input voltage can be measured with the general purpose ADC.

Figure 11. Charger Block Diagram

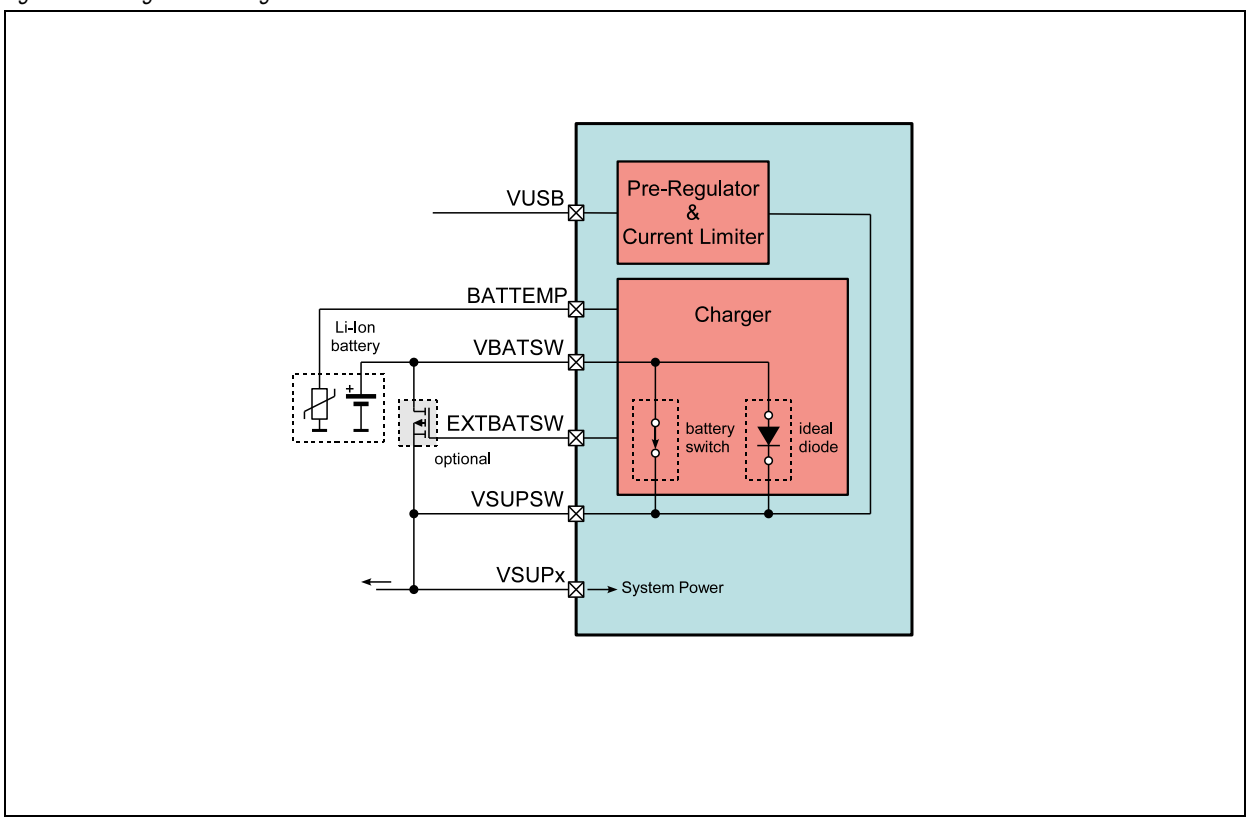
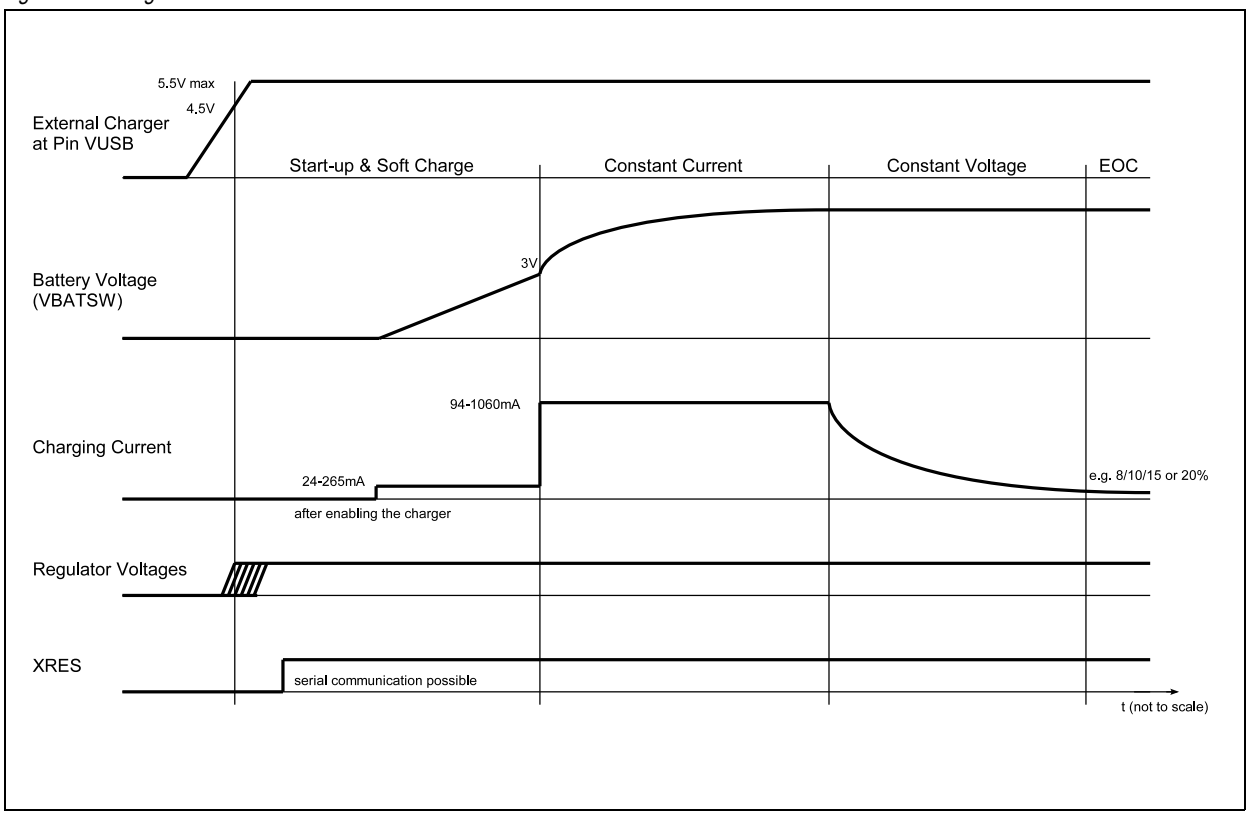


Figure 12. Charger States



8.4.1 Soft Charge/Trickle Charge

If the battery and therefore VBATSW is below 3V the charger is working in a fixed soft charge mode with a smaller trickle charging current of 24-265mA. After reaching the 3V level the charger switches to the constant current mode with the programmed charging current.

8.4.2 End of Charge Detection

For the EOC level 4 presets can be selected. This makes it possible to monitor the charging progress also during constant voltage mode. If the EOC level is reached an interrupt can be generated, but it is also possible to poll the charger status bits at any time.

8.4.3 VSUPSW and Temperature Supervision

The charger will automatically reduce the charging current if VSUPSW drops below the selected level. It will automatically stop charging when the chip temperature gets too to hot. The charger will return to normal operation as defined in the charger registers if VSUPSW and the chip temperature return to their normal operating range.

8.4.4 Battery Temperature Supervision

This charger block also features a supply for an external NTC resistor to measure the battery temperature while charging. If the temperature is too high (voltage on BATTEMP pin is below **VBATTEMP_ON**) the charger will stop operation. If needed an interrupt can be generated based on this event. When the battery temperature drops the charger the voltage on BATTEMP pin will rise above **VBATTEMP_OFF** and the charger will start charging again. This is forming a temperature hysteresis of about 3 to 5°C to avoid an oscillation of the charger.

The levels for switching off the charger (45ºC or 55ºC) as well as the type of NTC (10k or 100k) can be selected via register settings. The battery temperature supervision via the NTC can be switched off (**NTC_ON** = 0).

The supply for the NTC will be only on when a charger is detected and **NTC_ON** bit is set.

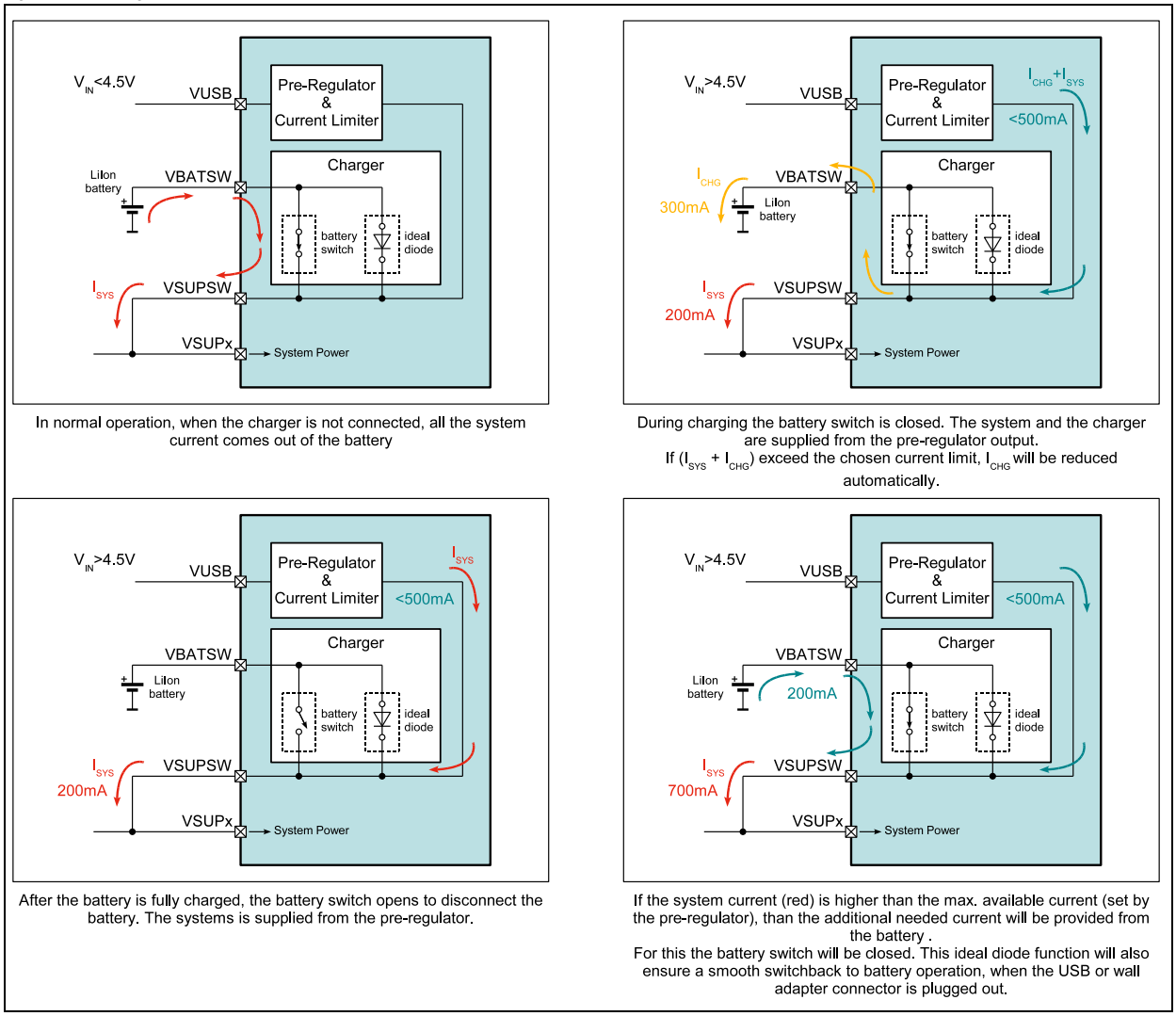
8.4.5 No Battery Detection

If the charger state machine reaches EOC 2 times within a very short period it assumes that there is no battery connected to the VBATSW terminal.

After this a sensing current of 1uA is applied to the BATTEMP pin to detect if a battery is reconnected.

8.4.6 Charger Modes

Figure 13. Charger Modes



In normal operation, when the charger is not connected, all the system current comes out of the battery

During charging the battery switch is closed. The system and the charger are supplied from the pre-regulator output.
If (I_{SYS} + I_{CHG}) exceed the chosen current limit, I_{CHG} will be reduced automatically.

After the battery is fully charged, the battery switch opens to disconnect the battery. The systems is supplied from the pre-regulator.

If the system current (red) is higher than the max. available current (set by the pre-regulator), than the additional needed current will be provided from the battery .
For this the battery switch will be closed. This ideal diode function will also ensure a smooth switchback to battery operation, when the USB or wall adapter connector is plugged out.

8.4.7 Parameter

VDD27=2.7, T_A= 25°C, unless otherwise specified.

Table 8. Charger Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{CHG} (0-7)	Charging Current	@ 470mA	I_{NOM} -8%	I_{NOM}	I_{NOM} +8%	mA
V_{CHG} (0-7)	Charging Voltage	end of charge is true	V_{NOM} -50mV	V_{NOM}	V_{NOM} +33mV	V
V_{ON_ABS}	Charger On Voltage Detection	rising edge on VUSB start			0.8	V
		rising edge on VUSB end	3.5V			V
V_{ON_REL}		VUSB-VBATSW		170	240	mV
V_{OFF_REL}		VUSB-VBATSW		50		mV
$V_{BATTEMP\_ON}$	Battery Temp. high level (45 or 55°C)	VSUP >3V NTC_{beta}=4200		610 or 400		mV

Table 8. Charger Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BATTEMP\_OFF}$	Battery Temp. low level (42 or 50ºC)	VSUP >3V NTC_{beta}=4200		700 or 500		mV
$I_{BATTEMP}$	NTC Bias Current	100k 10k		16 160		µA
I_{CHG_OFF}	End Of Charge current level	VSUP >3V		8% 10% 15% 20% I_{NOM}		mA
I_{REV_OFF}	Reverse current shut down	VSUPSW = 5V, VUSB open		<1		µA
R_{ON_BATSW}	Battery Switch On-resistance			0.15		Ω

9 Detailed Description - SYSTEM Functions

9.1 SYSTEM

The system block handles the power up, power down and regulator voltage settings of the PMU.

9.1.1 Power Up/Down Conditions

The chip powers up when one of the following conditions is true:

Table 9. Power UP Conditions

#	Source	Description
1	PWRUP PwUp	ON_KEY High Level at PWRUP pin of >= 1/3 VBATSW
2	VBUS PwUp	USB Plug-In …. High level at VBUS pin of >= 4.5V and > 2.7V on VSUP5

The chip automatically shuts off if one of the following conditions arises:

Table 10. Power DOWN Conditions

#	Source	Description
1	SERIF MAJOR PwDn	**Power-Down** by SERIF writing 0h to register 20h
2	Emergency PwDn	**Power-Down** if PWRUP pin is HIGH for 8sec. This has to be enabled in register 21h, per default a reset cycle is initiated. It can also be changed to 4s.
3	SERIF Watch-Dog PwDn	write 3h to reg. 20h … enable SERIF watch-dog **Power-Down** if no SERIF read is seen for 500ms.
4	Junction-Temp PwDn	**Power-Down** if junction temperature rises up to 140degC. This threshold can be lowered with bits <4:0> in reg 21h. This supervisor can be disabled with bit 2 in reg. 20h.
5	VDD27 LOW PwDn	**Power-Down** if VDD27 LDO5 has 10% under-voltage for more than 680µs. This supervisor can get disabled with bit 6 in reg. 21h.
6	CVDD1 LOW PwDn	**Power-Down** if enabled with bit 7 in reg. 23h and CVDD1 DCDC has 10% under-voltage for more than 680µs.
7	CVDD2 LOW PwDn	**Power-Down** if enabled with bit 5 in reg. 23h and CVDD2 DCDC has 10% under-voltage for more than 680µs.
8	CVDD3 LOW PwDn	**Power-Down** if enabled with bit 3 in reg. 23h and CVDD3 DCDC has 10% under-voltage for more than 680µs.
9	VSUP LOW PwDn	**Power-Down** if VSUPx goes below the defined level in Reg22h (bits <3:1>) This supervisor has to be enabled with bit 4 in reg. 22h.

9.1.2 Start-up Sequence

The start-up sequence is defined in the boot ROM and will be fixed during the production test.

The sequence and voltage of the regulators can be freely chosen for the start-up sequence with the following limitations:

- VDD27 will always start-up, after a ~5ms delay the sequencer will start-up the other chosen regulators with either 0, 1 or 4ms delay each.
- A maximum of 6 regulators (no matter of DCDC or LDO) or 5 regulators and a changed GPIO configuration can be chosen for the start-up.
- On a 7th time-slot PVDD2 can be started-up, but has reduced setting on the output voltage

PWRGOOD will be activated ~3ms after the last regulator.

XRES will be released 10ms to 110ms (set in the boot ROM) after the last regulator started up.