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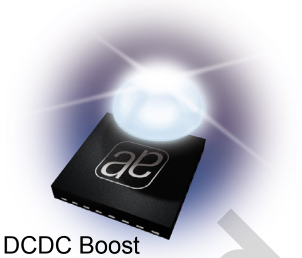
AS3647/47B

1600mA High Current LED Flash Driver



1 General Description

The AS3647/47B is an inductive high efficient DCDC step up converter with two current sinks. The DCDC step up converter operates at a fixed frequency of 4MHz and includes soft startup to allow easy integration into noise sensitive RF systems. The two current sinks can operate in flash / torch / assist (=video) light modes.

The AS3647/47B includes flash timeout, overvoltage, overtemperature, undervoltage and LED short circuit protection functions. A TXMASK/TORCH function reduces the flash current in case of parallel operation to the RF power amplifier and avoids a system shutdown. Alternatively this pin can be used to directly operate the torch light directly.

The AS3647/47B is controlled by an I²C interface and has a hardware automatic shutdown if SCL=0 for 100ms. Therefore no additional enable input is required for shutting down of the device once the system shuts down.

The AS3647/47B is available in a space-saving WL-CSP package measuring only 2.25x1.5x0.6mm (AS3647B: 2.25x1.5x0.5mm) and operates over the -30ºC to +85ºC temperature range.

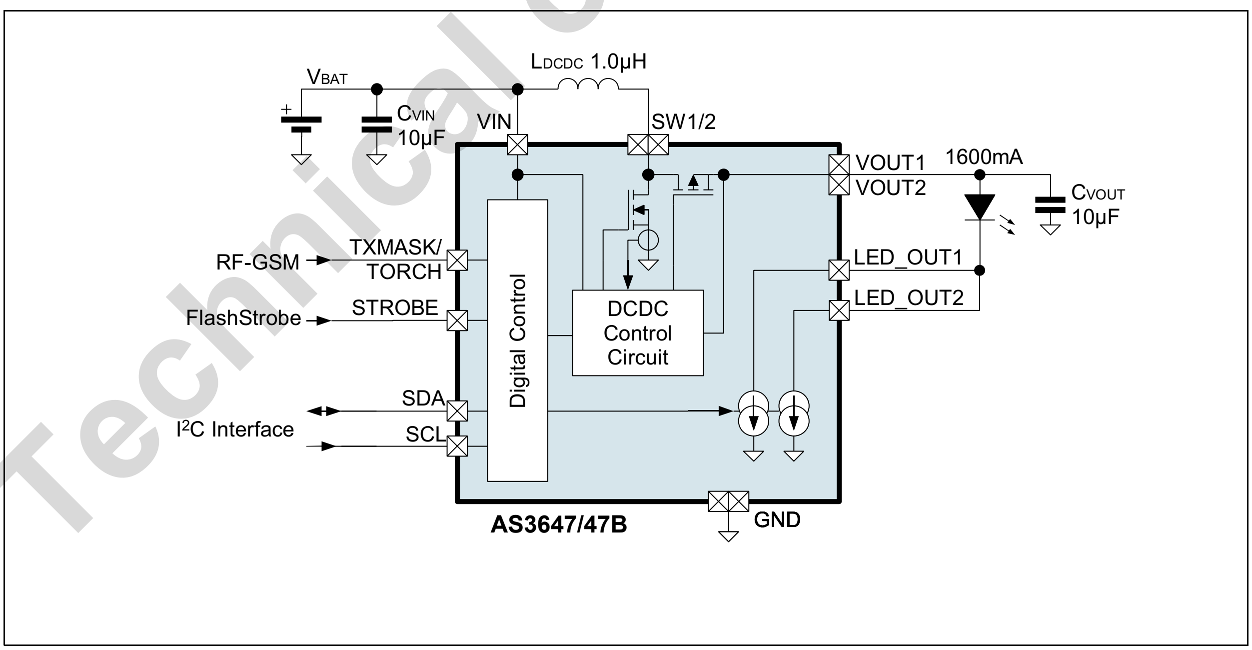
2 Key Features

- High efficiency 4MHz fixed frequency DCDC Boost converter with soft start allows small coils
  - Stable even in coil current limit
- LED current adjustable up to 1600mA
- Automatic current adjustment for low battery voltage
- PWM operation for lower output current for reliable light output of the LED; running at 31.25kHz to avoid audible noise
- Protection functions:
  Automatic Flash Timeout timer to protect the LED(s)
  Overvoltage and undervoltage Protection
  Overtemperature Protection
  LED short/open circuit protection
- I²C Interface with automatic shutdown
- 5V constant voltage mode operation
- Available in tiny WL-CSP Packages, 13 balls 0.5mm pitch 2.25x1.5x0.6mm, 15 balls 0.4mm pitch 2.25x1.5x0.5mm package size

3 Applications

Flash/torch/videolight for smartphones, feature-phones, tablets, DSCs, DVCs

Figure 1. Typical Operating Circuit



4 Pinout

Pin Assignment

Figure 2. Pin Assignments (Top View) AS3647

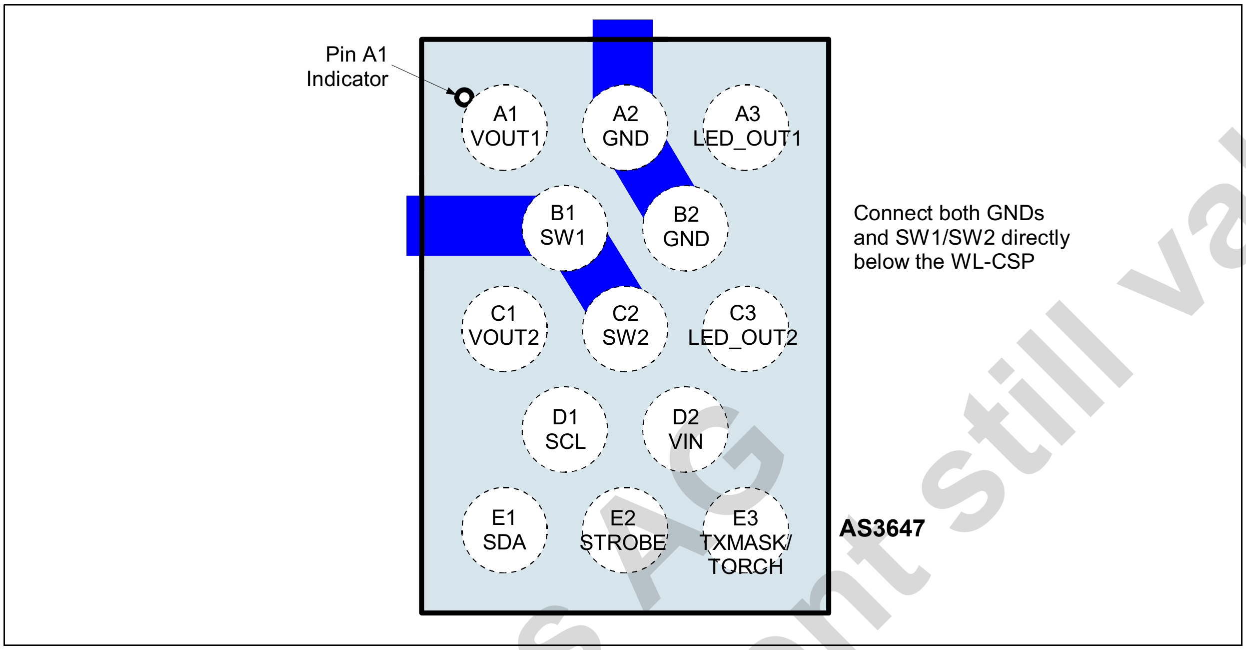
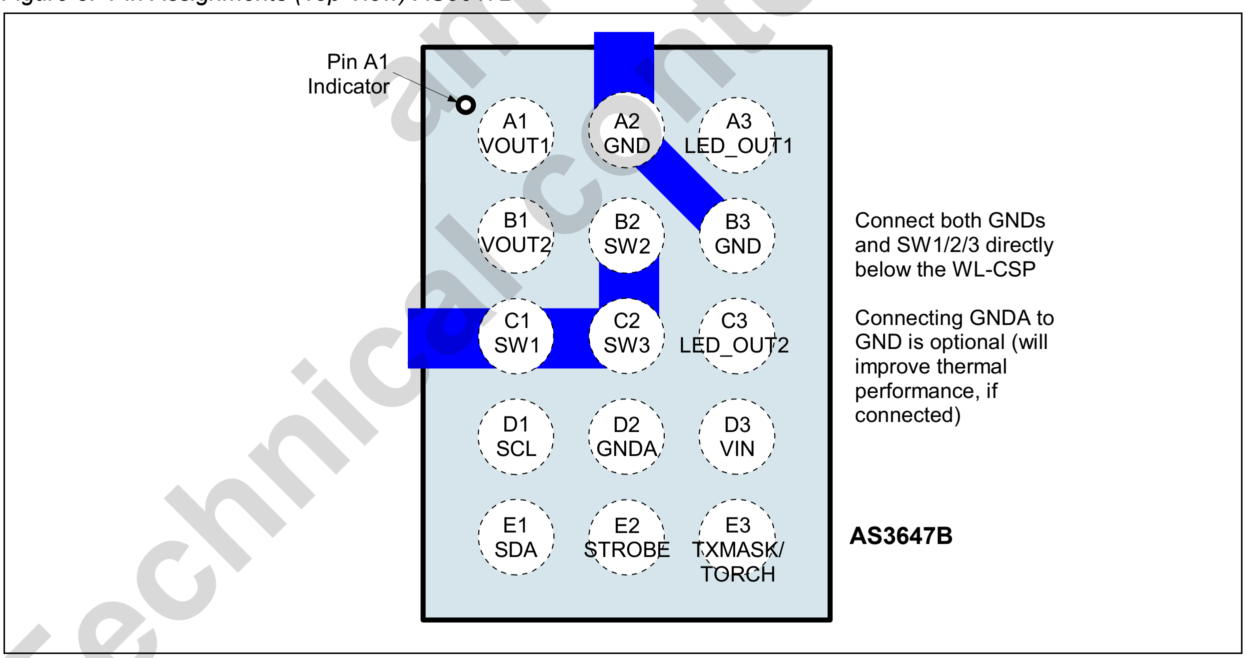


Figure 3. Pin Assignments (Top View) AS3647B



Pin Description

Table 1. Pin Description for AS3647

Pin Number	Pin Name	Description
A1	VOUT1	DCDC converter output capacitor - make a short connection to C_{VOUT} / VOUT2
A2	GND	Power and analog ground; make a short connection between both balls
A3	LED_OUT1	Flash LED current sink
B1	SW1	DCDC converter switching node - make a short connection to SW2 / coil L_{DCDC}
B2	GND	Power and analog ground; make a short connection between both balls
C1	VOUT2	DCDC converter output capacitor - make a short connection to C_{VOUT} / VOUT1
C2	SW2	DCDC converter switching node - make a short connection to SW1 /coil L_{DCDC}
C3	LED_OUT2	Flash LED current sink
D1	SCL	serial clock input for I^2C interface
D2	VIN	Positive supply voltage input - connect to supply and make a short connection to input capacitor C_{VIN} and to coil L_{DCDC}
E1	SDA	serial data input/output for I^2C interface (needs external pullup resistor)
E2	STROBE	Digital input with pulldown to control strobe time for flash function
E3	TXMASK/ TORCH	Function 1: Connect to RF power amplifier enable signal - reduces currents during flash to avoid a system shutdown due to parallel operation of the RF PA and the flash driver Function 2: Operate torch current level without using the I^2C interface to operate the torch without need to start a camera processor (if the I^2C is connected to the camera processor

Table 2. Pin Description for AS3647B

Pin Number	Pin Name	Description
A1	VOUT1	DCDC converter output capacitor - make a short connection to C_{VOUT} / VOUT2
A2	GND	Power ground; make a short connection between both balls
A3	LED_OUT1	Flash LED current sink
B1	VOUT2	DCDC converter output capacitor - make a short connection to C_{VOUT} / VOUT1
B2	SW2	DCDC converter switching node - make a short connection to SW1 /coil L_{DCDC}
B3	GND	Power ground; make a short connection between both balls
C1	SW1	DCDC converter switching node - make a short connection to SW2 / coil L_{DCDC}
C2	SW3	DCDC converter switching node - make a short connection to SW3 /coil L_{DCDC}
C3	LED_OUT2	Flash LED current sink
D1	SCL	serial clock input for I^2C interface
D2	GNDA	Analog ground - internally connected to GND ball A2; for improving thermal performance connect to ground plane (optional)
D3	VIN	Positive supply voltage input - connect to supply and make a short connection to input capacitor C_{VIN} and to coil L_{DCDC}
E1	SDA	serial data input/output for I^2C interface (needs external pullup resistor)

Table 2. Pin Description for AS3647B

Pin Number	Pin Name	Description
E2	STROBE	Digital input with pulldown to control strobe time for flash function
E3	TXMASK/ TORCH	Function 1: Connect to RF power amplifier enable signal - reduces currents during flash to avoid a system shutdown due to parallel operation of the RF PA and the flash driver Function 2: Operate torch current level without using the I^2C interface to operate the torch without need to start a camera processor (if the I^2C is connected to the camera processor

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 4, "Electrical Characteristics," on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VIN to GND	-0.3	+7.0	V	
STROBE, TXMASK/TORCH, SCL, SDA to GND	-0.3	VIN + 0.3	V	max. +7V
SW1/2/3, VOUT1/2, LED_OUT1/2 to GND	-0.3	+7.0	V	
VOUT1/2 to SW1/2/3	-0.3		V	**Note:** Diode between VOUT1/2 and SW1/2/3
voltage between 2xGND, GNDA pins	0.0	0.0	V	short connection recommended
Input Pin Current without causing latchup	-100	+100 $+I_{IN}$	mA	Norm: EIA/JESD78
Continuous Power Dissipation (T_A = +70ºC)				
Continuous power dissipation		1230	mW	P_T at 70ºC[1]
Continuous power dissipation derating factor		16.7	mW/ºC	P_{DERATE}[2]
Electrostatic Discharge				
ESD HBM pins LED_OUT1/2[3]		±8000	V	Norm: JEDEC JESD22-A114F
ESD HBM		±2000	V	
ESD CDM		±500	V	Norm: JEDEC JESD 22-C101E
ESD MM		±100	V	Norm: JEDEC JESD 22-A115-B
Temperature Ranges and Storage Conditions				
Junction to ambient thermal resistance		60[4]	ºC/W	For more information about thermal metrics, see application note AN01 Thermal Characteristics
Junction Temperature		+150	ºC	Internally limited (overtemperature protection), max. 20000s
Storage Temperature Range	-55	+125	ºC	
Humidity	5	85	%	Non condensing
Body Temperature during Soldering		+260	ºC	according to IPC/JEDEC J-STD-020
Moisture Sensitivity Level (MSL)	MSL 1			Represents a max. floor life time of unlimited

1. Depending on actual PCB layout and PCB used measured on demoboard; for peak power dissipation during flashing see document 'AS3647/47B Thermal Measurements'
2. P_{DERATE} derating factor changes the total continuous power dissipation (P_T) if the ambient temperature is not 70ºC. Therefore for e.g. T_{AMB}=85ºC calculate P_T at 85ºC = P_T - P_{DERATE} * (85ºC - 70ºC)
3. Pins LED_OUT1 connected to LED_OUT2 and capacitor C_{VOUT} connected to VOUT1/2 and GND; both GND pins connected together
4. Measured on AS3647/47B Demoboard.

6 Electrical Characteristics

V_{VIN} = +2.7V to +4.4V, T_{AMB} = -30ºC to +85ºC, unless otherwise specified. Typical values are at V_{VIN} = +3.7V, T_{AMB} = +25ºC, unless otherwise specified.

Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
General Operating Conditions						
V_{VIN}	Supply Voltage	pin VIN	2.7	3.7	4.4	V
$V_{VINREDUCED\_FUNC}$	Supply Voltage	AS3647/47B functionally working, but not all parameters fulfilled	2.5		2.7	V
			4.4		5.5	
$I_{SHUTDOWN}$	Shutdown Current	TXMASK/TORCH=L, SCL=SDA=0V, V_{VIN}<3.7V		0.6	2.0	µA
I_{STANBY}	Standby Current	interface active, TXMASK/TORCH=L, V_{VIN}<3.7V[1]		1.0	10	µA
T_{AMB}	Operating Temperature		-30	25	85	ºC
Eta	Application Efficiency (DCDC and current sink)	L_{COIL}=0.6µH@3A, L_{ESR}=60mΩ, LED_OUT1,2=1300mA[2], t_{FLASH}<300ms		84		%
DCDC Step Up Converter						
V_{VOUT}	DCDC Boost output Voltage (pin VOUT1/2)		2.8		5.5	V
V_{VOUT5V}	DCDC Boost output Voltage (pin VOUT1/2)	constant voltage mode operation const_v_mode (see page 25)=1		5.0		V
R_{PMOS}	On-resistance	DCDC internal PMOS switch		70		mΩ
R_{NMOS}	On-resistance	DCDC internal NMOS switch		70		mΩ
f_{CLK}	Operating Frequency	All internal timings are derived from this oscillator	-7.5%	4.0	+7.5%	MHz
Current Sinks						
V_{LED}	LED forward voltage	single LED at 1600mA	2.8	3.5	4.2	V
I_{LED_OUT}	LED_OUT1/2 current sinks output combined	single LED	0		1600	mA
$I_{LED\_OUT\Delta}$	LED_OUT1/2 current sink accuracy	I_{LED_OUT}>=800mA or I_{LED_OUT}<500mA 0ºC < T_J < 100ºC	-7		+7	%
		500mA<I_{LED_OUT}<800mA, 0ºC < T_J < 100ºC	-5		+5	%
$I_{LED\_OUT\ RAMP}$	LED_OUT1/2 ramp time	Ramp-up During startup		250	1000	µs
		Ramp-down		500	1000	µs
$I_{LED\_OUT\ RIPPLE}$	LED_OUT current ripple	I_{LED_OUT} = 1000mA, BW=20MHz		20		mA_{PP}
V_{ILED_COMP}	LED_OUT current sink voltage compliance	Minimum voltage between pin LED_OUT1/2 and GND for operation of the current sink		325		mV
V_{HIGH_VDS}	Comparator High VDS	low vds and high vds comparator - see 4MHz/ 1MHz Operating Mode Switching on page 13		900		mV
V_{LOW_VDS}	Comparator Low VDS			320		
$I_{LEAK\_LED\_OUT}$	LED_OUT1/2 Leakage Current	Pins LED_OUT1 and LED_OUT2	-1.0	0.0	+1.0	µA
Protection and Fault Detection Functions (see page 13)						

Table 4. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{VOUTMAX}$	V_{VOUT} overvoltage protection	DCDC Converter Overvoltage Protection	5.0	5.3	5.6	V
I_{LIMIT}	Current Limit for coil L_{DCDC} (Pin SW) measured at 40% PWM duty cycle[3] maximum 40000s lifetime operation in overcurrent limit	coil_peak=00b	1.8	2.0	2.23	A
		coil_peak=01b	2.25	2.5	2.78	
		default value; coil_peak (see page 24)=10b	2.7	3.0	3.34	
		coil_peak=11b	3.15	3.5	3.9	
$V_{LEDSHORT}$	Flash LED short circuit detection voltage	Voltage measured between pins VOUT1,2 and LED_OUT1,2		1.0		V
T_{OVTEMP}	Overtemperature Protection	Junction temperature		144		ºC
$T_{OVTEMPHYST}$	Overtemperature Hysteresis			5		ºC
$t_{FLASHTIMEOUT}$	Flash Timeout Timer	Can be adjusted with register flash_timeout (page 26)	2		1280	ms
		accuracy	-7.5		+7.5	%
V_{UVLO}	Undervoltage Lockout	Falling V_{VIN}	2.25	2.4	2.5	V
		Rising V_{VIN}	V_{UVLO} +0.05	V_{UVLO} +0.1	V_{UVLO} +0.15	V
Digital Interface						
V_{IH}	High Level Input Voltage	Pins SCL, SDA. Pin TXMASK/TORCH in external torch mode (ext_torch_on=10)	1.26		V_{VIN}	V
V_{IL}	Low Level Input Voltage		0.0		0.54	V
$V_{IHFLASH}$	High Level Input Voltage	Pin STROBE. Pin TXMASK/TORCH for TxMask mode (ext_torch_on=01)[4]	0.7		V_{VIN}	V
$V_{ILFLASH}$	Low Level Input Voltage		0.0		0.54	V
V_{OL}	Low Level Output Voltage	pin SDA, I_{OL}=3mA			0.3	V
I_{LEAK}	Leakage current	Pins SCL, SDA	-1.0	0.0	+1.0	µA
I_{PD}	Pulldown current to GND[5]	Pins TORCH, STROBE and TXMASK/TORCH		36		µA
$t_{DEBTORCH}$	TORCH debounce time		6.3	9	11.7	ms
$t_{TIMEOUT}$	SCL timeout	In indicator, assist or flash mode, if SCL is low longer than this timeout, the AS3647/47B automatically enters shutdown mode	35		100	ms
I^2C mode timings - see Figure 4 on page 9						
f_{SCLK}	SCL Clock Frequency		1/ $t_{TIMEOUT}$		400	kHz
t_{BUF}	Bus Free Time Between a STOP and START Condition		1.3			µs

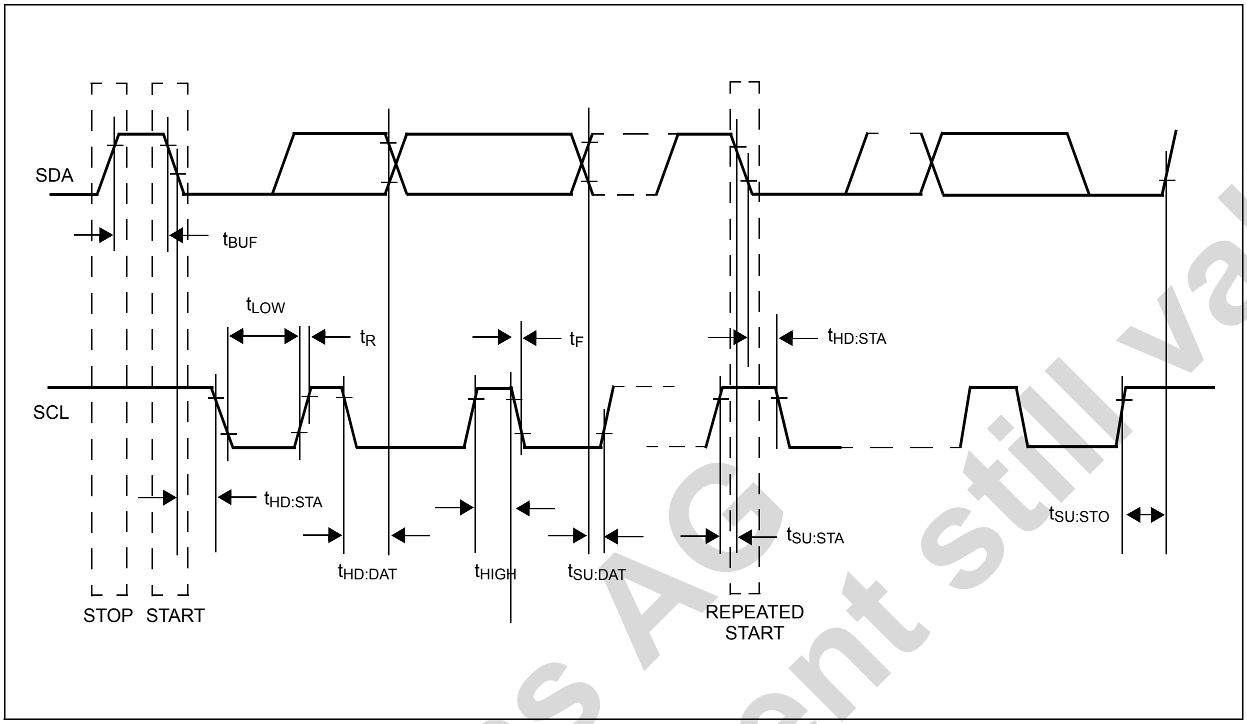
Table 4. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{HD:STA}$	Hold Time (Repeated) START Condition[6]		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time[7]		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time[8]		100			ns
t_R	Rise Time of Both SDA and SCL Signals		20 + $0.1C_B$		300	ns
t_F	Fall Time of Both SDA and SCL Signals		20 + $0.1C_B$		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	C_B — total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

1. For VBAT=4.5V, SCL=1.8V, SDA=1.8V maximum I_{STANBY} is <16µA.
2. To improve efficiency at low output currents, the active part of the internal switching transistor PMOS is reduced in size to 1/5 its original size. This reduces the current required to drive the PMOS transistor and therefore improves overall efficiency at low output currents.
3. Due to slope compensation of the current limit, I_{LIMIT} changes with duty cycle - see Figure 17 on page 12.
4. The logic input levels V_{IH} and V_{IL} allow for 1.2V or 1.8V supplied driving circuit
5. A pulldown current of 36µA is equal to a pulldown resistor of 42kΩ at 1.5V
6. After this period, the first clock pulse is generated.
7. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
8. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ = to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max + $t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

Timing Diagrams

Figure 4. I^2C mode Timing Diagram



7 Typical Operating Characteristics

VVIN = 3.7V, T_A = +25ºC (unless otherwise specified), LED: Osram Phaser 2 (VFLED=3.8V at 1A)

Figure 5. DCDC Efficiency vs. VVIN

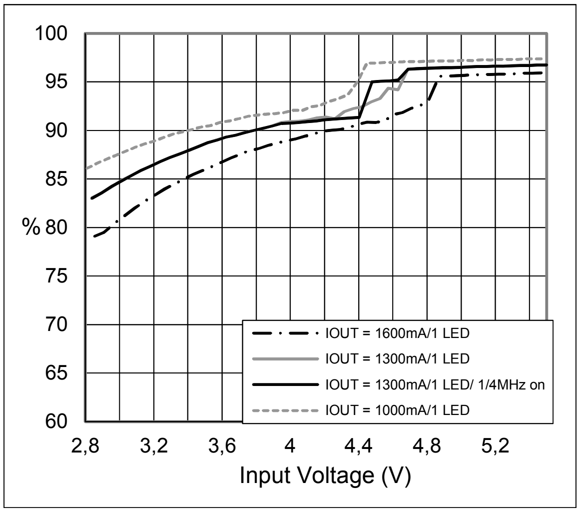


Figure 6. Application Efficiency (PLED/PVIN) vs. VVIN

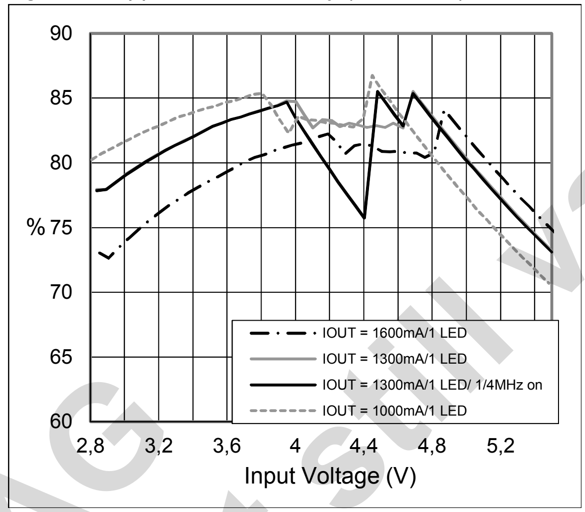


Figure 7. Battery Current vs. VVIN

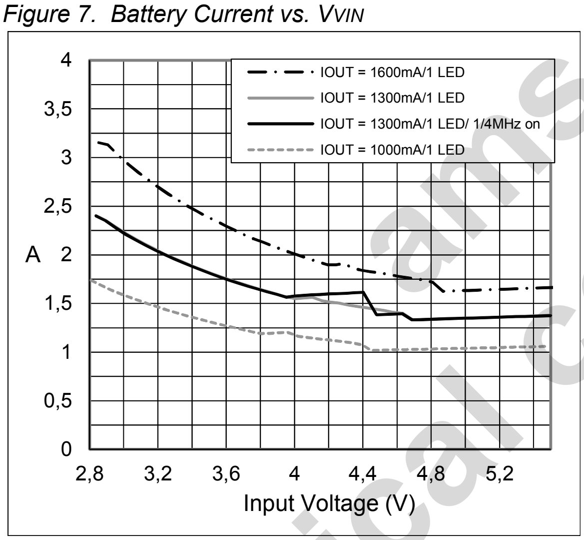


Figure 8. Efficiency at low currents (300mA)

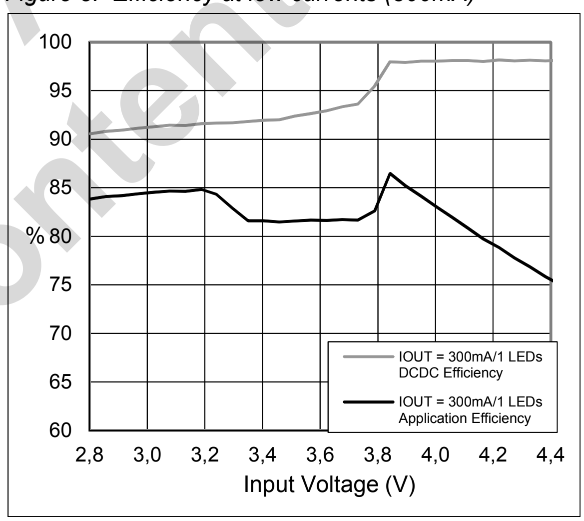


Figure 9. ILED Startup (ILED_OUT=1.0A)

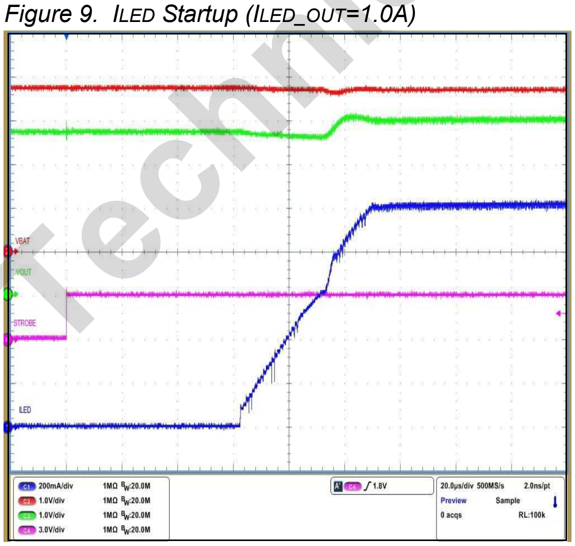


Figure 10. IVIN, ILED Startup (ILED_OUT=800mA)

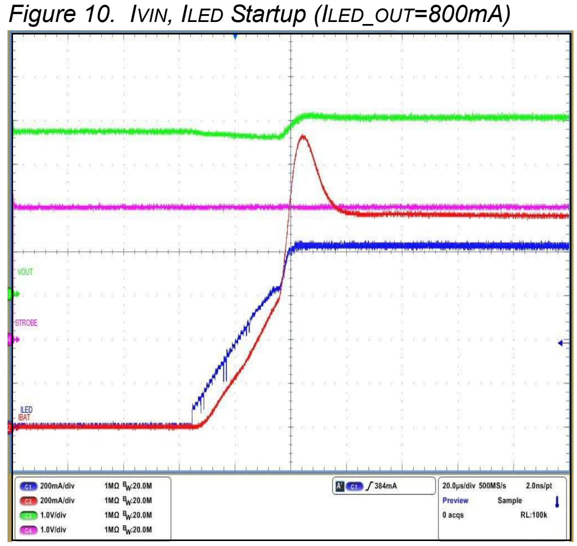


Figure 11. ILED Startup (ILED_OUT=60mA)

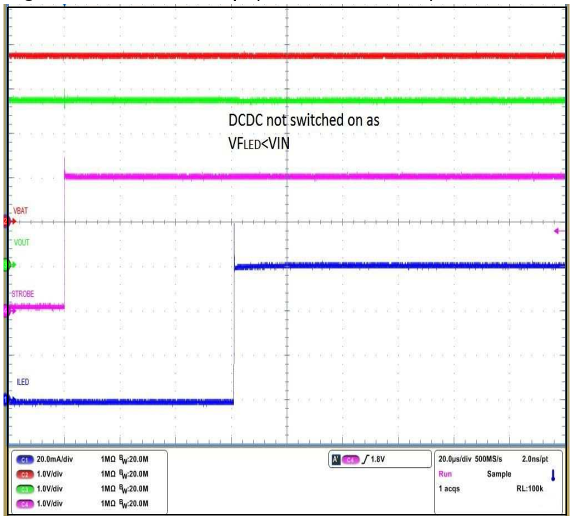


Figure 12. VOUT / ILED_OUT ripple, ILED_OUT = 1.0A

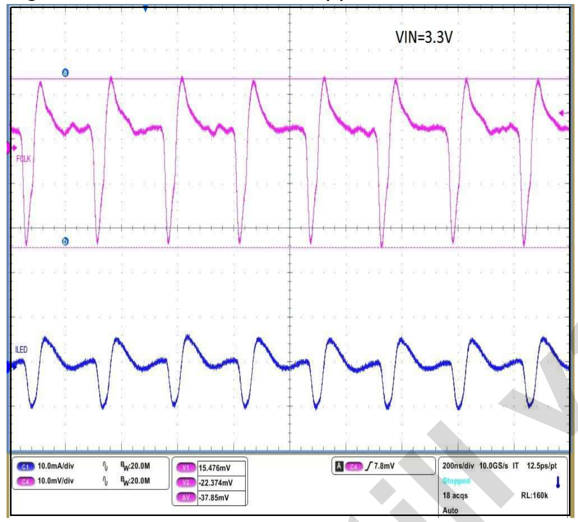


Figure 13. ILED Rampdown (ILED_OUT=1.0A)

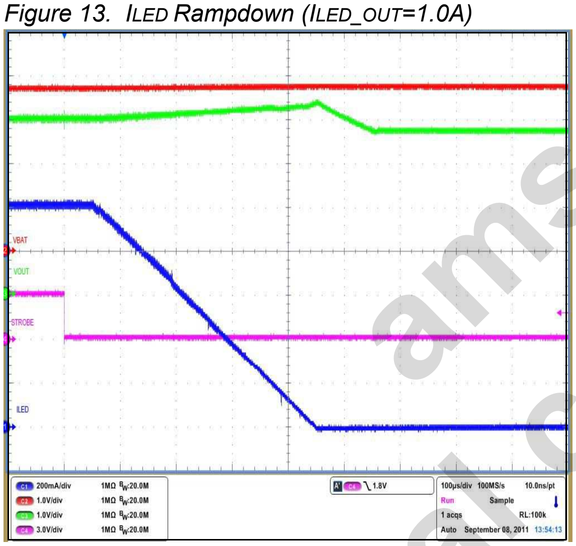


Figure 14. ILED_OUT vs. TAMB

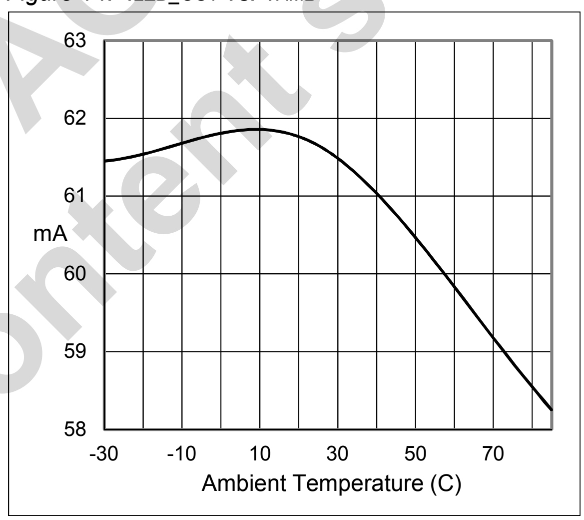


Figure 15. Oscillator frequency fCLK vs. TAMB

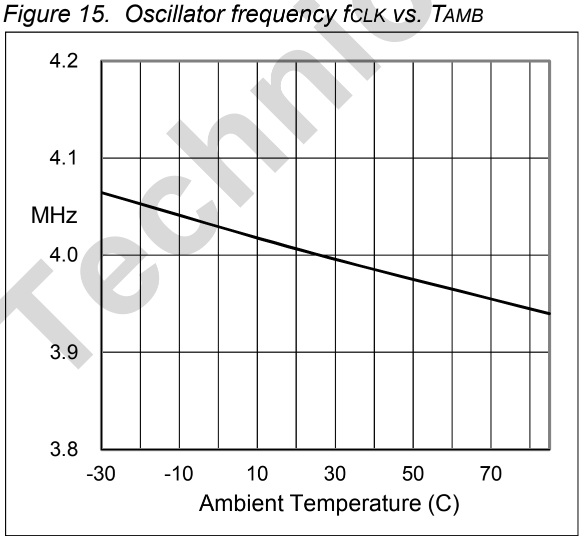
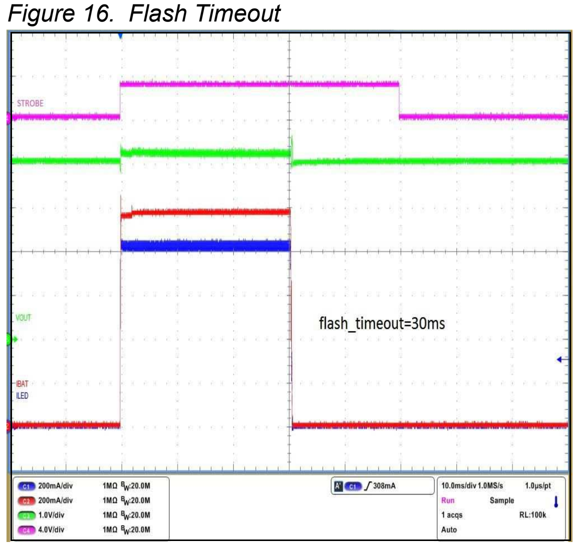


Figure 16. Flash Timeout



8 Detailed Description

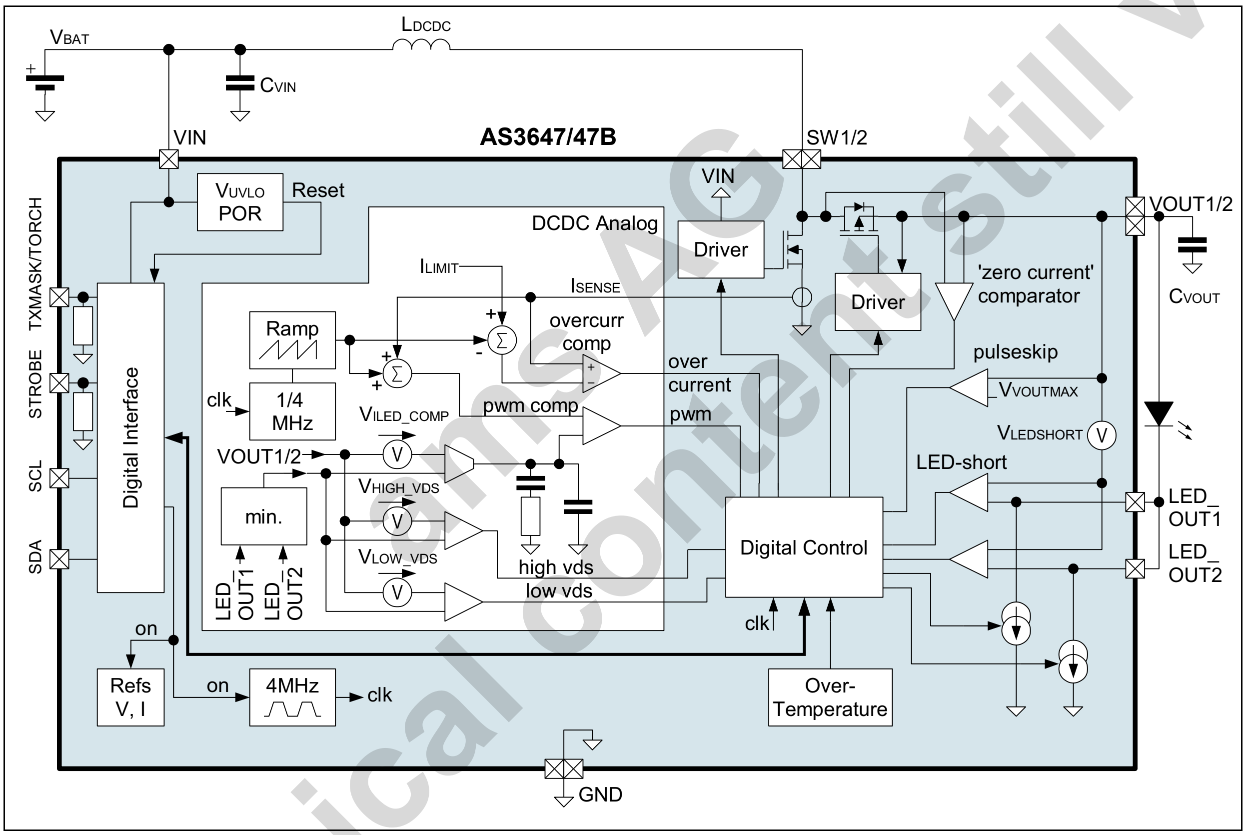
The AS3647/47B is a high performance DCDC step up converter with internal PMOS and NMOS switches. Its output is connected to one flash LED with an internal current sink. The device is controlled by the pins SDA and SCL in I^2C mode.

The actual operating mode like standby, assist light, indicator or flash mode, can then be chosen by the interface. If not in standby mode, the device automatically enters shutdown mode by keeping SCL low for more than $t_{TIMEOUT}$[1].

The AS3647/47B includes a fixed frequency DCDC step-up with accurate startup control. Together with the current sink (on LED_OUT1/2) it includes several protection and safety functions.

Internal Circuit Diagram

Figure 17. Internal circuit Diagram



Softstart / Soft ramp down

During startup and ramp down the LED current is smoothly ramped up and ramped down. If the DCDC converter goes out of regulation (measured by monitoring the voltage across the current sinks), the ramp up is temporarily stopped in order for the DCDC to return to regulation[2].

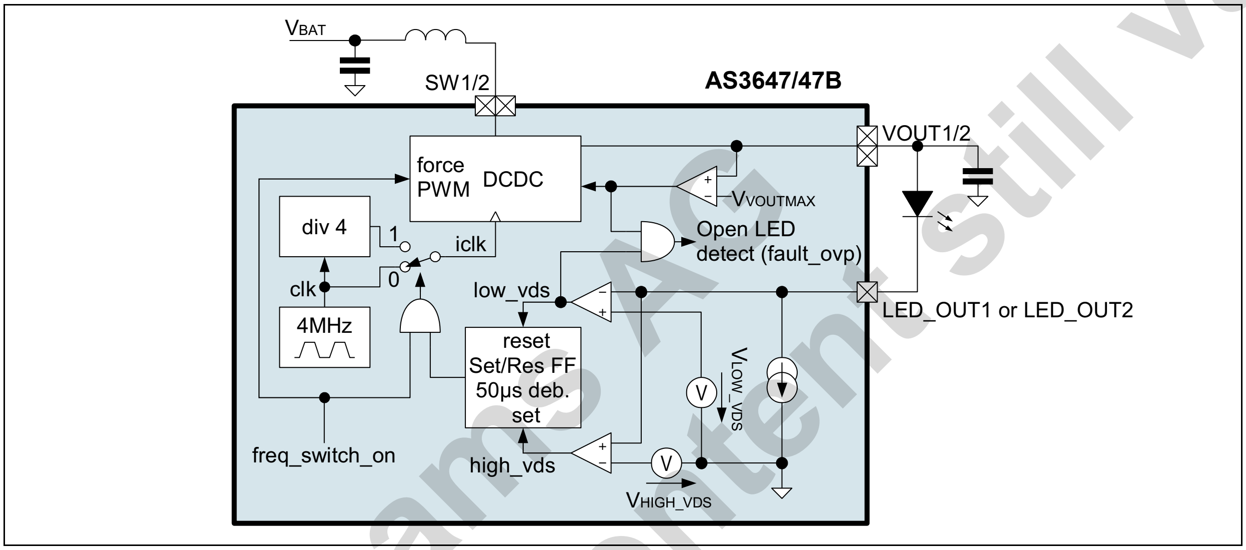
1. Following registers are reset to their default value if the timeout expires: out_on=0, ext_torch_on=00, mode_setting=00, const_v_mode=0.
2. The actual value of the LED current setting can be readout by the register led_current_actual (see page 28) to allow the camera processor to adopt to the actual operating conditions.

4MHz/1MHz Operating Mode Switching

If freq_switch_on (see page 28)=1 and in flash and assist light mode (indicator mode or low current mode using PWM mode -see mode_setting (page 26) - always will use pulseskip) if led_current>=40h , the DCDC converter always operates in PWM mode (exception: PFM mode is allowed during startup) to reduce EMI in EMI sensitive systems. For flash and assist light mode and high duty cycles close to 100% on-time (maximum duty cycle) of the PMOS, the DCDC converter can switch into a 1MHz operating mode and maximum duty cycle to improve efficiency for this load condition[3]. The DCDC converter returns back to its normal 4MHz operating frequency when load or supply conditions change. Due to this switching between two fixed frequencies the noise spectrum of the system is exactly defined and predictable. If improved efficiency is required, the fixed switching between 1MHz / 4MHz can be disabled by freq_switch_on (see page 28)=0. In this case pulseskip will be used.

The internal circuit for switching between these two frequencies is shown in Figure 18:

Figure 18. Internal circuit of 4MHz/1Mhz selection



Note: For simplicity Figure 18 shows only a single current sink.

Protection and Fault Detection Functions

The protection functions protect the AS3647/47B and the LED(s) against physical damage. In most cases a Fault register bit is set, which can be readout by the I^2C interface. The fault bits are automatically cleared by a I^2C readout of the fault register. Additionally the DCDC is stopped and the current sinks are disabled[4] by resetting out_on=0, mode_setting=00 and ext_torch_on=00.

Overvoltage Protection

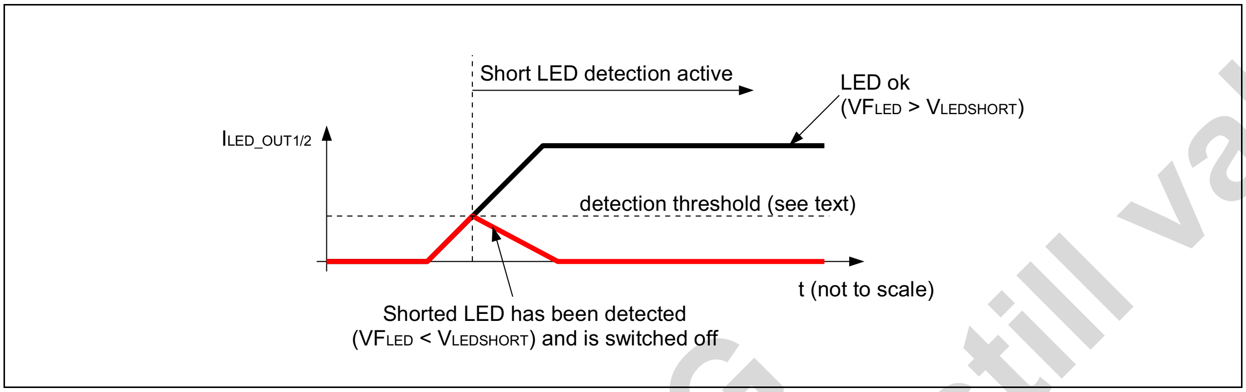
In case of no or a broken LED(s) at the pin LED_OUT1/2 and an enabled DCDC converter, the voltage on VOUT1/2 rises until it reaches $V_{VOUTMAX}$ (overvoltage condition) and the voltage across the current source is below low_vds[5]., the DCDC converter is stopped, the current sources are disabled and the bit fault_ovp (see page 27) is set[6].

3. Efficiency compared to a 4MHz only DCDC converter forced to operate with minimum duty cycle.
4. Applies for all faults except TXMASK event occurred
5. If overvoltage is reached, but none of the low_vds comparator(s) triggers, VOUT1/2 is still regulated below $V_{VOUTMAX}$.
6. In constant voltage mode (5V generation, register bit const_v_mode=1) this fault is disabled.

Short Circuit Protection

After the startup of the DCDC converter, the voltage on LED_OUT1/2 is continuously monitored and compared against $V_{LEDSHORT}$ if the LED current is above 25mA[7](see Figure 19). If the voltage across the LED (VF_{LED} = VOUT1/2-LED_OUT1/2) stays below $V_{LEDSHORT}$, the DCDC is stopped (as a shorted LED is assumed), the current sinks are disabled and the bit fault_led_short (see page 27) is set.

Figure 19. Short LED detection



Overtemperature Protection

The junction temperature of the AS3647/47B is continuously monitored. If the temperature exceeds T_{OVTEMP}, the DCDC is stopped, the current sinks are disabled (instantaneous) and the bit fault_overtemp (see page 27) is set. The driver is automatically re-enabled[8] once the junction temperature drops below T_{OVTEMP}-$T_{OVTEMPHYST}$.

TXMASK event occurred

If during flash, TXMASK current reduction is enabled (see TXMASK on page 16, configured by ext_torch_on=01) and a TXMASK event happened (pin TXMASK/TORCH=1), the fault register bit fault_txmask (see page 27) is set.

Flash Timeout

If the flash is started a timeout timer is started in parallel. If the flash duration defined by the STROBE input (strobe_on = 1 and strobe_type = 1, see Figure 26 on page 19) exceeds $t_{FLASHTIMEOUT}$ (adjustable by register flash_timeout (see page 26)), the DCDC is stopped and the flash current sinks (on pin LED_OUT1/2) are disabled and fault_timeout is set.

If the flash duration is defined by the timeout timer itself (strobe_on = 0, see Figure 24 on page 19), the register fault_timeout is set after the flash has been finished.

Supply undervoltage Protection

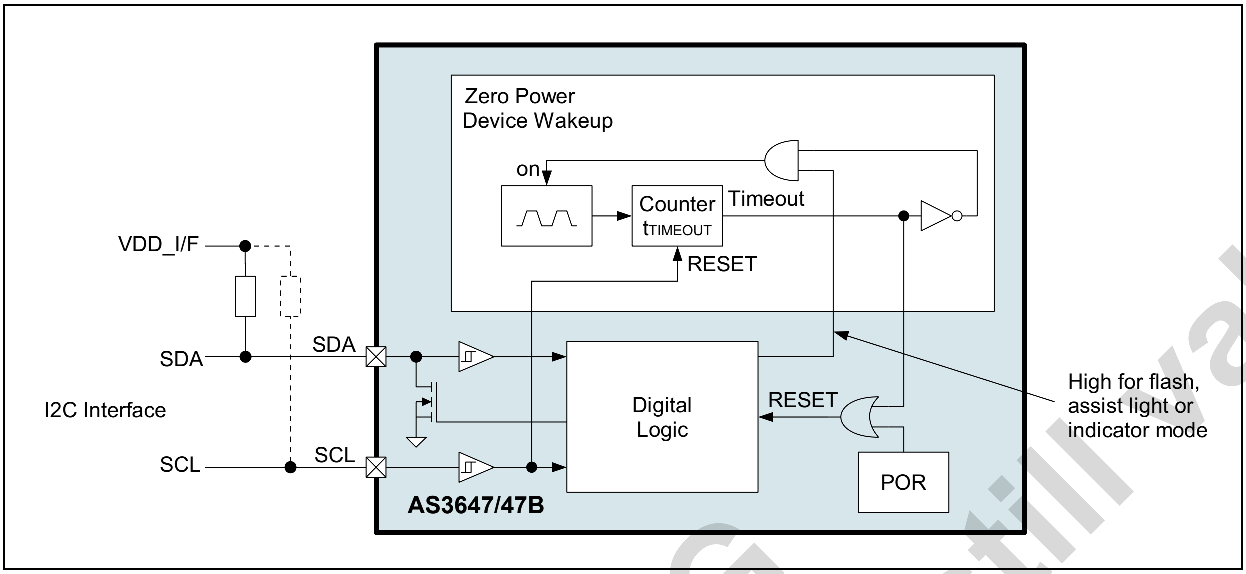
If the voltage on the pin VIN (=battery voltage) is or falls below V_{UVLO}, the AS3647/47B is kept in shutdown state and all registers are set to their default state.

Wakeup Circuit - Power off detection

In flash, assist light and indicator mode (register mode_setting (page 26)=01, 10 or 11) and out_on (page 26)=1, if SCL is L for more than $t_{TIMEOUT}$, shutdown mode is automatically entered. This feature automatically detects a power-off of the controlling circuit driving SCL and SDA (VDD_I/F goes to 0V e.g. due to a low power condition of the driving circuit) - the internal circuit is shown in Figure 20:

7. To avoid errors in short LED detection for LEDs with a high leakage current
8. In constant voltage mode (const_v_mode=1) the DCDC will not be automatically re-enabled.

Figure 20. Device Shutdown and Wakeup



In shutdown mode once pin SCL goes high for the first time, the internal counter shown in Figure 20 is immediately reset thus releasing the internal RESET (assuming VIN is above V_{UVLO}) signal and allows instant communication on the I^2C bus. Therefore no additional action is required to leave the shutdown mode and start I^2C communication.

Purpose of this circuit

The purpose of this circuit is an additional security mechanism.

Assume the user programmed torch or indicator operation (there is no timeout for these operating modes) and the battery slowly drops below the undervoltage limit of the system. The processor would get an reset by the PMIC and the LDO operating VDD_I/F is switched off, but the processor might not have been able to switch-off the torch/indicator operation of the AS3647/47B. Due to the implemented security mechanism the AS3647/47B detects a power off of VDD_I/F and automatically enters shutdown.

Current consumption in standby/shutdown mode

The AS3647/47B is designed to draw minimum current in standby and shutdown mode. There is a small difference in current consumption between these two operating modes (typ. 300nA) only due to the internal level shifters (see the schmitt trigger input buffers connected to SCL and SDA in Figure 20) for shifting up the voltage on SCL/SDA (VDD_I/F e.g. 1.8V) to the supply voltage on VIN (e.g. 3.7V). If the AS3647/47B is driven with digital levels close to 0V/VIN, the current consumption for standby mode is identical to shutdown mode.

Operating Mode and Currents

The output currents and operating mode are selected according to the following table:

Table 5. Operating Mode and current settings

AS3647/47B configuration						operating mode and currents	
SCL and SDA	**TORCH**	**STROBE**	**mode_setting (see page 26)**	**out_on (see page 26)**	**Condition**	**Mode**	**LED_OUT1/2 output current**
SCL low for $t_{TIMEOUT}$[1]	X	X	X	X	if previous operating mode was indicator, assist light or flash mode	shutdown all registers are reset to their default values	0

Table 5. Operating Mode and current settings (Continued)

AS3647/47B configuration						operating mode and currents	
SCL and SDA	**TORCH**	**STROBE**	**mode_ setting (see page 26)**	**out_on (see page 26)**	**Condition**	**Mode**	**LED_OUT1/2 output current**
I^{2}C commands are accepted	X	X	10, 01 or 11	0		standby	0
	X	X	00	X	ext_torch_on (see page 24) not 10		
	0	X			ext_torch_on =10		
	1	X			ext_torch_on =10	external torch mode	LED current is defined by the 7LSB[2] bits of led_current
	X	X	01	1		indicator mode or low current pwm mode[3]	LED current is defined by the 6LSB bits (bits 5...0) of led_current pwm modulated with 31.25kHz defined by register inct_pwm (1/16...4/16)
	X	X	10	1		assist light mode	LED current is defined by the 7LSB[2] bits (6...0) of led_current
	X	X	11	1	strobe_on (see page 27) = 0	flash mode; flash duration defined by flash_timeout (see page 26)	LED current is defined by led_current - the current can be reduced during flash, see Flash Current Reductions below
	X	0->1			strobe_on = 1 and strobe_type (see page 27) = 0		
	X	1			strobe_on = 1 and strobe_type = 1	flash mode; flash duration defined by STROBE input; timeout defined by flash_timeout	

1. SCL low for $t_{TIMEOUT}$ and operating mode is indicator, assist or flash mode then shutdown mode is entered.
2. The MSB bit of this register not used to protect the LED; therefore the maximum assist / torch light current = half the maximum flash current
3. The low current mode is a general purpose PWM mode to drive less current through the LED in average, but keep the actual pulsed current in a range where the light output from the LED is still specified. As only the 6 LSBs of led_current are used the maximum current is limited to 1/4 of the maximum flash current.

Flash Current Reductions

TXMASK

Usually the flash current is defined by the register led_current . If the TXMASK/TORCH input is used and (configured by ext_torch_on=01), the flash current is reduced to flash_txmask_current if TXMASK/TORCH=1.

Current Reduction by VIN measurements in Flash Mode

Due to the high load of the flash driver and the ESR of the battery (especially critical at low temperatures), the voltage on the battery drops. If the voltage drops below the reset threshold of the system would reset. To prevent this condition the AS3647/47B monitors the battery voltage and keeps it above vin_low_v_run as follows:

Before a flash is started the voltage on VIN is measured. If the voltage is below the setting of vin_low_v the fault_uvlo (see page 27) is set and the flash is disabled (driver stays in shutdown) if vin_low_v_shutdown=1. The flash current is reduced to flash_txmask_current if vin_low_v_shutdown=0.

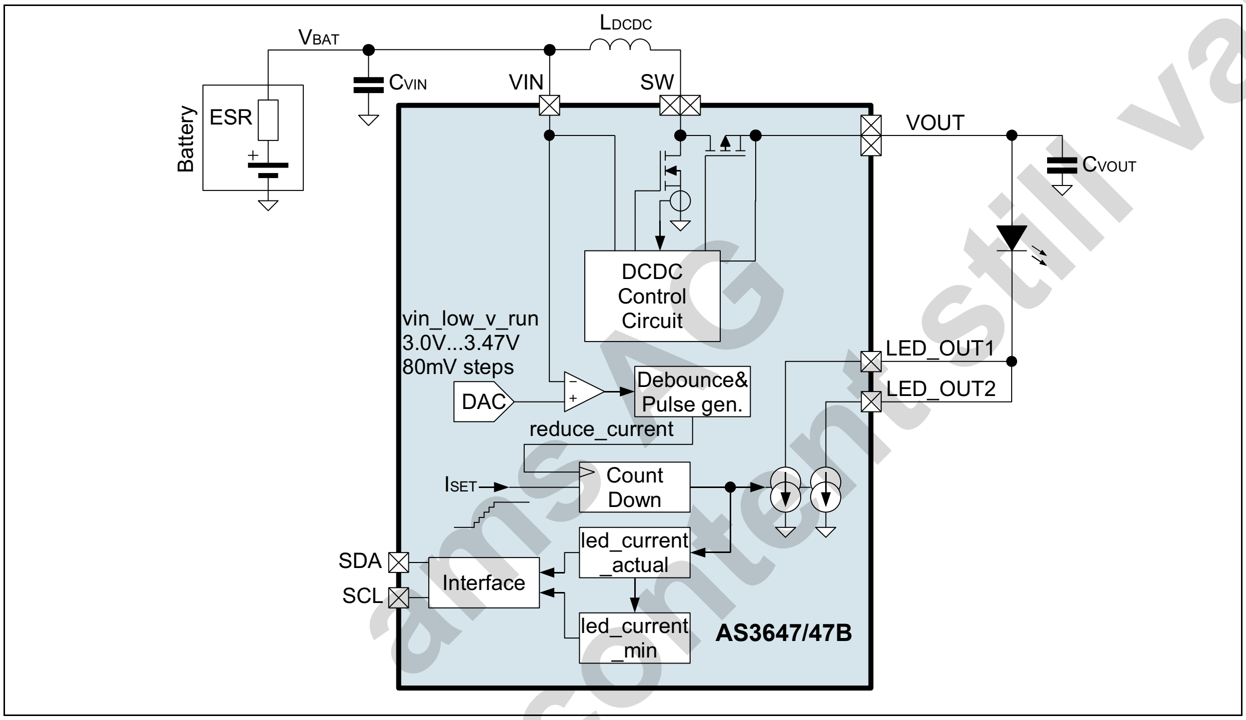
During flash, if the voltage on VIN drops below the threshold defined by vin_low_v_run, the flash current is reduced (or ramping of the current is stopped during flash current startup) and fault_uvlo is set. The timing for the reduction of the current is 8µs/LSB current change.

During the flash pulse the actual used current can be readout by the register led_current_actual.

After the flash pulse the minimum current can be readout by the register led_current_min - this allows to adjust the camera sensitivity (gain or iso-settings) for the subsequent flash pulse (e.g. when using a pre-flash and a main flash pulse).

The internal circuit for low voltage current reductions are shown in Figure 21:

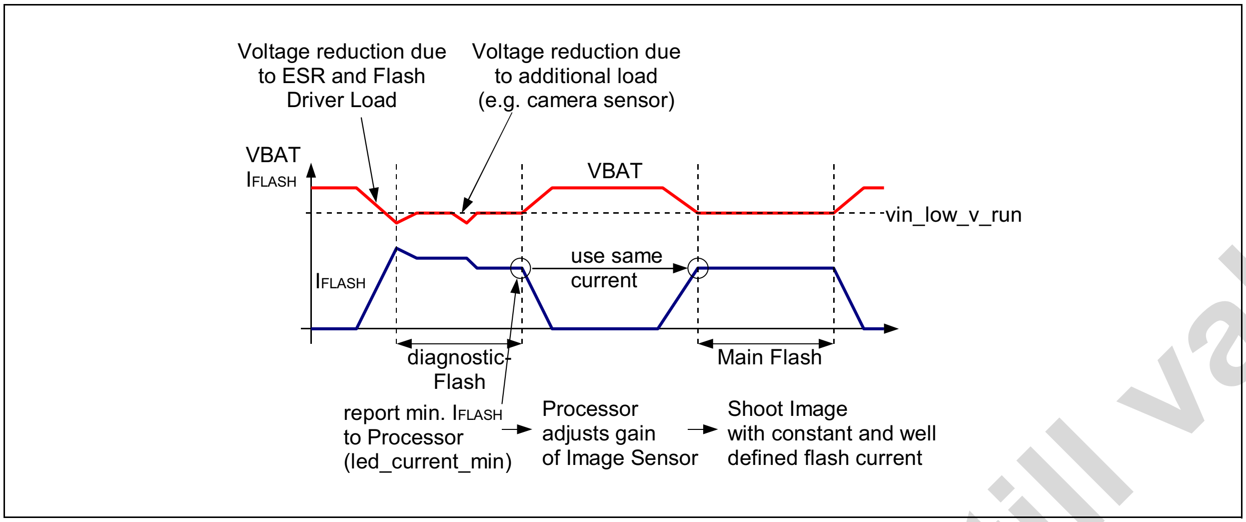
Figure 21. Low Voltage current Reduction Internal Circuit



A mobile phone camera flash system can trigger a diagnostic flash and a main-flash:

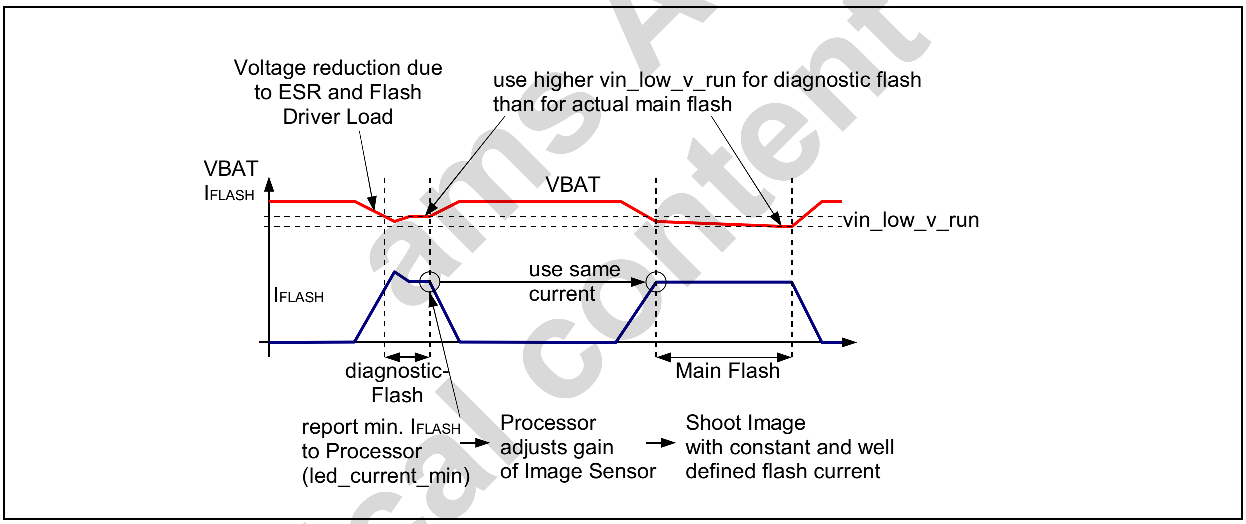
The diagnostic flash is initiated by the processor. After this diagnostic flash, the determined maximum flash current can be read back through the I²C interface from register led_current_min (see page 28) and used for the setting for the main flash. Therefore the current in the main-flash is constant and additionally the camera system can use this current for picture quality adjustments - the waveforms for this concept are shown in Figure 22:

Figure 22. Low Voltage current Reduction Waveform with diagnostic-Flash and Main-Flash Phase



If the diagnostic flash should be short (e.g. 10ms) it is recommended to operate this diagnostic flash at slightly higher vin_low_v_run setting compared to the main flash as shown in Figure 23:

Figure 23. Low Voltage current Reduction Waveform with short diagnostic-Flash and Main-Flash Phase



The different settings for vin_low_v_run allow a constant main flash current without dropping VIN below vin_low_v_run.

Flash Strobe Timings

The flash timing are defined as follows:

1. Flash duration defined by register flash_timeout and flash is started immediately when this mode is selected by the I^2C command (see Figure 24):
   set strobe_on = 0, start the flash by setting out_on = 1
2. Flash duration defined by register flash_timeout and flash started with a rising edge on pin STROBE (see Figure 25):
   set strobe_on = 1 and strobe_type = 0
3. Flash start and timing defined by the pin STROBE; the flash duration is limited by the timeout timer defined by flash_timeout (see Figure 26 and Figure 34):
   set strobe_on = 1 and strobe_type = 1

Figure 24. AS3647/47B flash duration defined by flash_timeout without using STROBE input

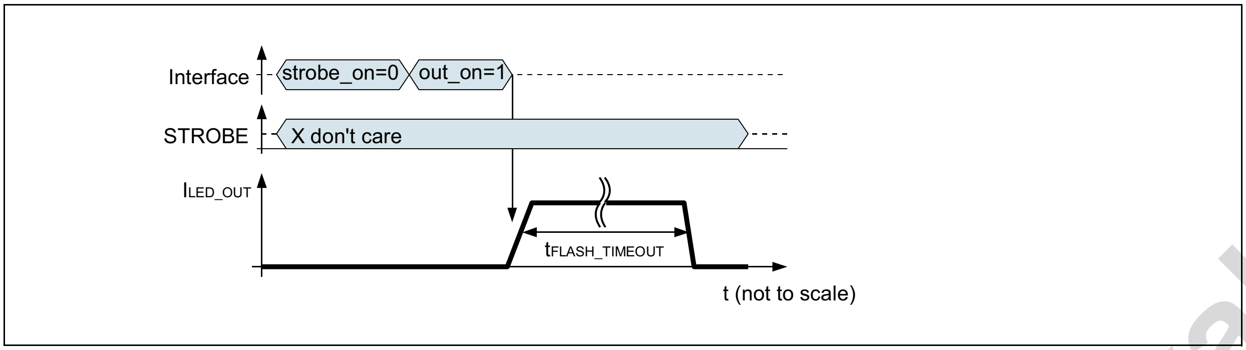


Figure 25. AS3647/47B flash duration defined by flash_timeout, starting flash with STROBE rising edge

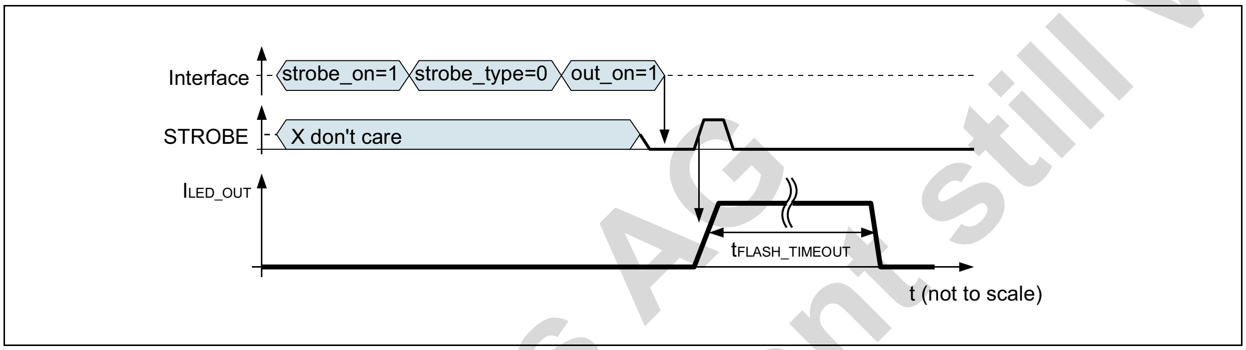


Figure 26. AS3647/47B flash duration and start defined by STROBE, limited by flash_timeout; timer not expired

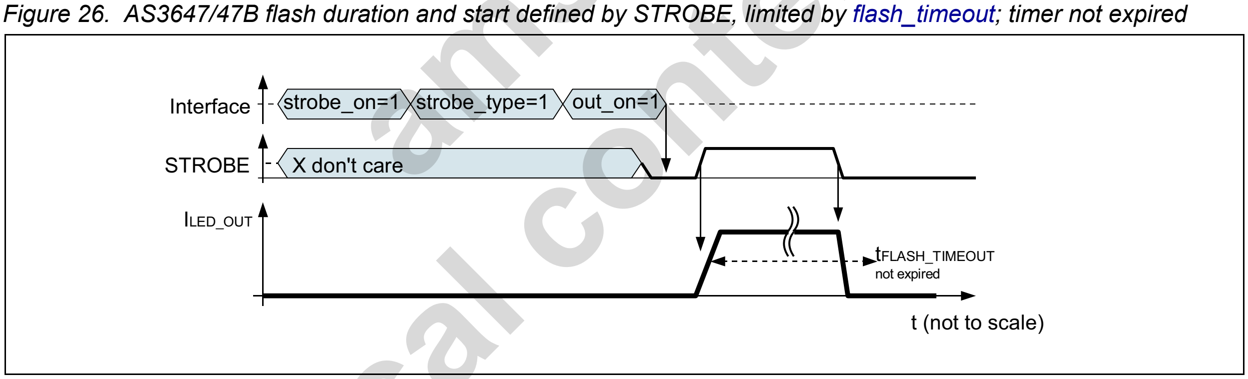
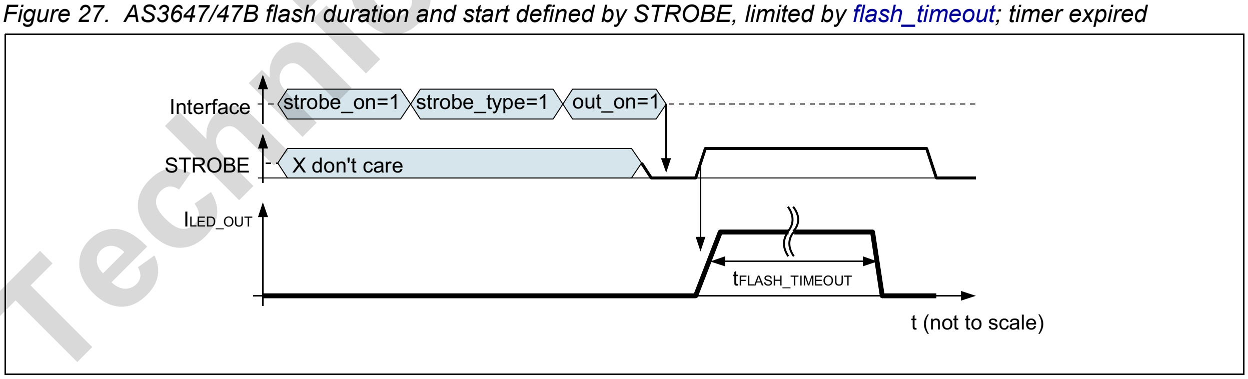


Figure 27. AS3647/47B flash duration and start defined by STROBE, limited by flash_timeout; timer expired



I²C Serial Data Bus

The AS3647/47B supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The AS3647/47B operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The AS3647/47B works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 28):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both data and clock lines remain HIGH.

Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

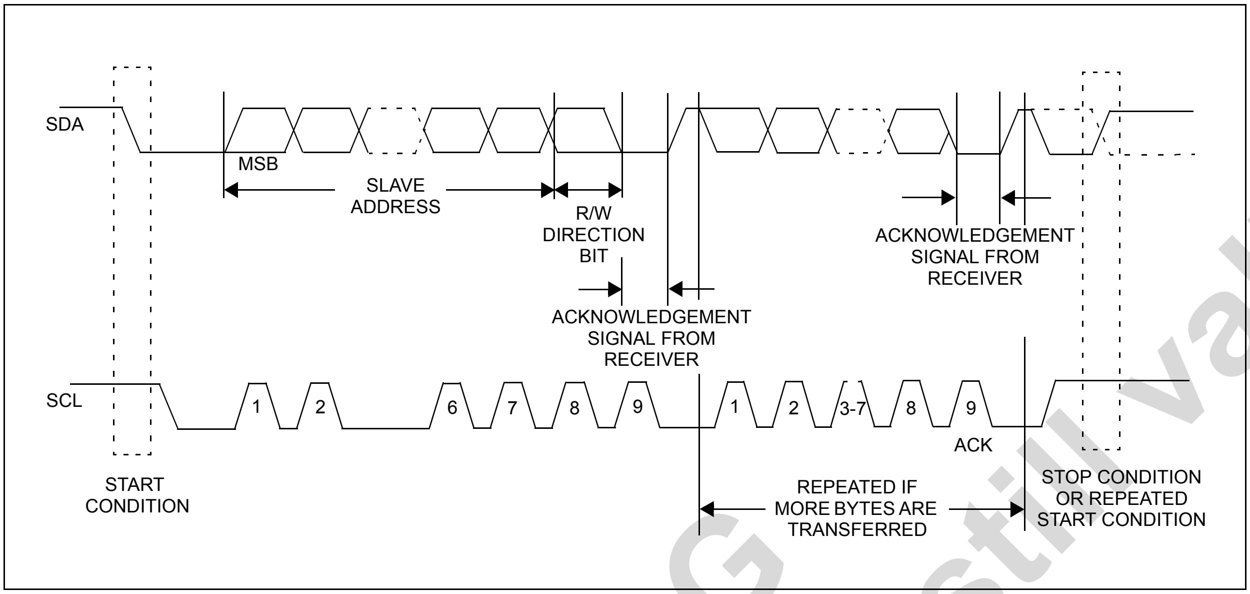
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 28. Data Transfer on I^2C Serial Bus



Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.
2. **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The AS3647/47B can operate in the following two modes:

1. **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 29). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit AS3647/47B address, which is 0110000, followed by the direction bit (R/W), which, for a write, is 0.[9] After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the AS3647/47B acknowledges the slave address + write bit, the master transmits a register address to the AS3647/47B. This sets the register pointer on the AS3647/47B. The master may then transmit zero or more bytes of data, with the AS3647/47B acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.
2. **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the AS3647/47B while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 30 and Figure 31). The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit AS3647/47B address, which is 0110000, followed by the direction bit (R/W), which, for a read, is 1.[10] After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The AS3647/47B then begins to transmit data starting with the register address pointed to by the register pointer. If

9. The address for writing to the AS3647/47B is 60h = 01100000b
10. The address for read mode from the AS3647/47B is 61h = 01100001b

the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The AS3647/47B must receive a “not acknowledge” to end a read.

Figure 29. Data Write - Slave Receiver Mode

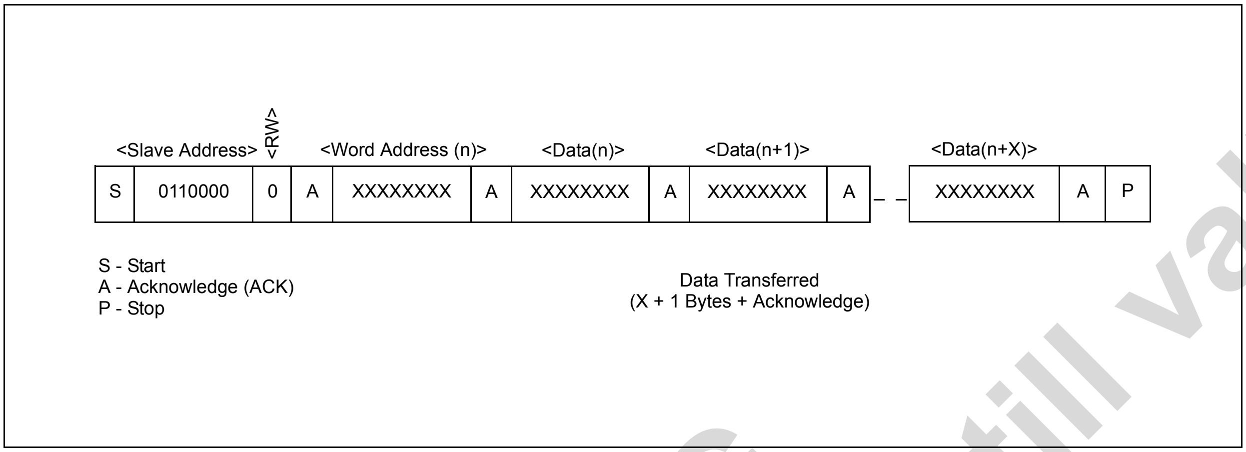


Figure 30. Data Read (from Current Pointer Location) - Slave Transmitter Mode

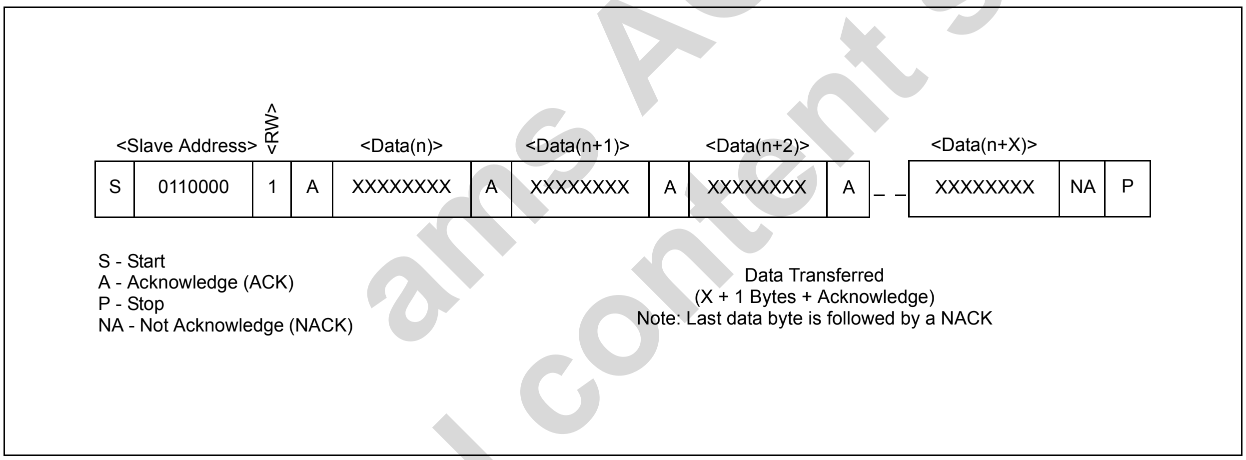
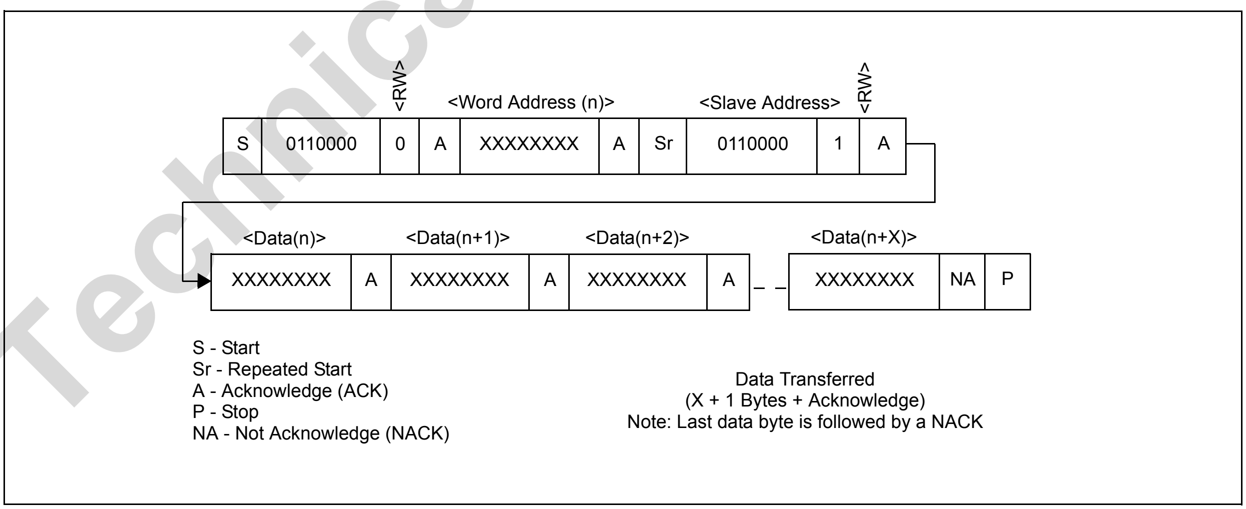


Figure 31. Data Read (Write Pointer, Then Read) - Slave Receive and Transmit



Register Description

Table 6. ChipID Register

Addr: 0		ChipID Register		
		This register has a fixed ID		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2:0	version	Xh	R	AS3647/47B chip version number
7:3	fixed_id	10110b	R	This is a fixed identification (e.g. to verify the I^2C communication)

Table 7. Current Set Register

Addr: 1		Current Set Register			
		This register defines design versions			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	led_current	9Ch	R/W	Define the current on pin LED_OUT1/2 (combined; each current sink has identical currents) **Caution:** assist mode uses bits 6:0 of this current setting (max. half of full current setting) indicator or low current pwm mode uses only 5:0 of this current setting (max. 1/4 of full current setting)	
				0h	0mA
				1h	6.3mA
				2h	12.5mA
				...	...
				3Fh	393.3mA (maximum current for indicator or low current pwm mode, mode_setting=01)
				...	...
				7Fh	796.9mA (maximum current for assist light mode, mode_setting=10)
				...	...
				9Ch	979mA - default setting
				...	...
				FEh	1593.7mA
				FFh	1600mA

Table 9. TXMask Register

Addr: 3		TXMask Register This register defines the TXMask settings and coil peak current			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	ext_torch_on	00	R/W	Defines operating mode for input pin TXMASK/TORCH	
				00	pin has no effect
				01	txmask-mode; during flash if TXMASK/TORCH=1, the LED current is set to flash_txmask_current - (see TXMASK on page 16)
				10	external torch mode: if TXMASK/TORCH=1 and mode_setting=00, the AS3647/47B is set into external torch mode (LED current is defined by the 7LSB[1] bits of led_current)
				11	don't use
3:2	coil_peak	10	R/W	Defines the maximum coil current (parameter ILIMIT)	
				00	ILIMIT = 2.0A
				01	ILIMIT = 2.5A
				10	ILIMIT = 3.0A
				11	ILIMIT = 3.5A
7:4	flash_txmask_current[2]	6h	R/W	Define the current on pin LED_OUT1/2 in flash mode if ext_torch_on=01 and TXMASK/TORCH=1	
				0h	0mA
				1h	100mA
				2h	201mA
				3h	301mA
				4h	402mA
				5h	502mA
				6h	602mA - default
				7h	703mA
				8h	803mA
				9h	904mA
				Ah	1004mA
				Bh	1104mA
				Ch	1205mA
				Dh	1305mA
				Eh	1405mA
				Fh	1506mA

1. The MSB bit of this register not used to protect the LED; therefore the maximum current = half the maximum flash current
2.