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1 General Description

The AS3654 is a highly integrated solution for power supply generation and monitoring, battery management including charging. It is controlled via a serial control interface and integrates all necessary system specific functions such as clock, reset and interrupt generation, voltage and temperature monitoring.

2 Key Features

System Control
- Serial Control Interface
- On/Off Control Module
- Reset Generation for system controller
- Programmable Interrupt Controller
- Low power off mode (9µA; 2.5V LDO on)

Supply Voltage Generation
- 1 RF Programmable Low Noise LDOs (400mA)
- 1 RF Programmable Low Noise LDOs (150mA)
- 2 Programmable Digital Low Power LDOs (200mA)
- 2 General Purpose PWM DC/DC step up converter with two programmable current sinks (e.g. for white led)
- 3 General Purpose high efficiency DC/DC step down converter
- 1 Low noise charge pump with 5V output voltage
- 1 Ultra Low Power 2.5V LDO (always on)

Current sinks
- 4 programmable(6-bit) from 0.625 to 40mA optional useable as GPIOs
- 3 programmable high voltage (15V) (6-bit) from 0.625 to 40mA

10-bit Successive Approximation ADC
- 40µs conversation time

Battery Management
- Full featured chemistry independent step down charger with included Gas Gauge and Current limitation.
- 0.15 Ω Battery switch for start-up during trickle charging
- Integrated USB charger up to 400mA

Power Management Features
- Wide Battery Supply Range 3.0...5.5V
- On-Chip Bandgap Tuning for High Accuracy (±1%)
- Current protection
- Thermal Protection with internal temperature sensor
- 0.35µm CMOS Solution

Audio
- Two Digital Audio Inputs (I2S interface)
- 18 Bit Audio DAC
- 2.9V low Noise LDO for Audio DAC
- Headphone Amplifier Output with GND separation
- GND Buffer for Headphone Amplifier
- Line/ Headphone output with GND separation

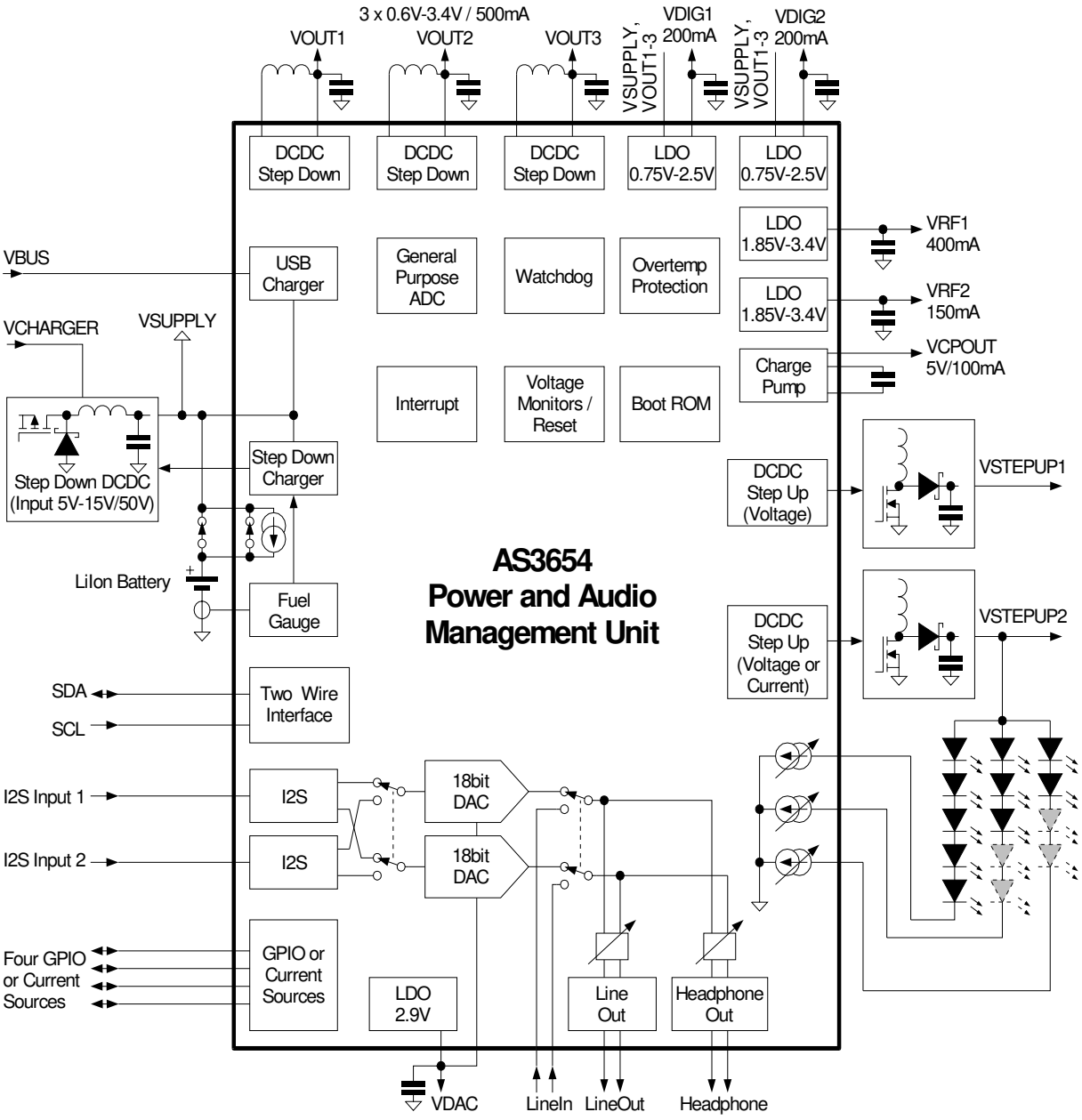
Programmable System clock
- 1.6 MHz to 2.3 MHz with 100 kHz steps

3 Applications

- Power and Audio Management Unit
- 1 Cell Li+ or 3 Cell NiMH powered devices
- Car Battery powered systems with and without internal battery

4 Block Diagram

Figure 1 – AS3654 Application Diagram



Document Revision History

Chapter	REV	Description of Change	Date	Author
all	0V19	- Additional descriptions and updates - Removed duplicated hp_det bit (register 58, b3)	21.3.2006	TJE/PTR
all	0V20	Typical XON pull up current updated = 5uA, Charger external components Qpu=BSS84 Added applicationdiagramm, reformatted headings	24.11.2006	TJE/PTR
all	0V21	- Changed V_{DETECT} minimum value to 2mV (dcdc stepup1 load detection) - Updated soldering conditions	12.1.2007	TJE/PTR
all	0V22	- Updated pwm_high_time and pwm_low_time settings - Updated package thickness tolerance from +/-0.1mm to +0.1/-0.15	17.12.2007	TJE/PTR

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5 Characteristics

5.1 Absolute Maximum ratings (non operating)

Stressed beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or beyond those under 'Operating conditions' is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 1 – Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{IN_HV}	High voltage pins	-0.3	17.0	V	Applicable for high voltage pins (1)
V_{IN_MV}	5V pins	-0.3	7.0	V	Applicable for pins 5V-pins (2)
V_{IN_LV}	3.3V pins	-0.3	5.0	V	Applicable for 3.3V-Pins (3)
I_{IN}	Input pin current	-25	+25	mA	At 25 °C, Norm: Jedec 78
T_{strg}	Storage Temperature Range	-55	125	°C	
	Humidity	5	85	%	Noncondens.
V_{ESD05}	Electrostatic discharge 0.5kV	-500	500	V	Norm: MIL 883 E Method 3015 Applicable for pins: LX1, LX2, LX3, VSUPPLY_1…VSUPPLY_6
V_{ESD1}	Electrostatic discharge 1kV	-1000	1000	V	Norm: MIL 883 E Method 3015 Applicable for pins: all, except the pins listed at V_{ESD05} Setup: Note(4)
P_t	Total Power Dissipation		1 0.72	W W	T_A = 70 degrees T_A = 85 degrees
Soldering Conditions					
TBODY	Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only
TPEAK	Solder Profile(5)	235	245	°C	
Dwell		30	45	s	above 217 °C

Notes

(1) HV pins are VCHARGER, VGATE, VOFF_B, DCDC_CURR1,DCDC_CURR2

(2) 5V pins are V_USB, CH_SENSE_N, CH_SENSE_P, VSUP_SW1, VSUP_SW2, VBAT_SW1, VBAT_SW2, V_BAT, SCL, SDA, XRESET, XINT, VSUPPLY_3, CURR1..6, DCDC_GATE1, DCDC_GATE2, DCDC_SENSE_P1, DCDCSENSE_P2, DCDC_SENSE_N1, DCDC_SENSE_N2, DCDC_FB1, DCDC_FB2, VCL, VCP_OUT, VCP_N, VCP_P, VCP_IN, VCP_IN, VRF1, VREF1_IN, VRF2, VRF2_IN, VDIG1, VDIG1_IN, VDIG2, VDIG2_IN, VSUPPLY_1, VSUPPLY_2, LX1, LX2, GND_SW, VSUPPLY_4, LINE_CM, HP_CM_PWR, HP_CM, LOUT_R, LOUT_L, ALVDD, AVDD, LSP_R, BVSS, LSP_L, AVDD, VSUPPLY_4

(3) 3.3V pins are ISENSEP, ISENSEN, ADC_IN, RPROGRAM, V2_5, CREF, ON, VI2S, SDI, SCLK, MCLK, LRCLK,AGND, VREF, LINL,LINR, VDAC

(4) ESD setup Following pins connected:
VSUPPLY_1...VSUPPLY_6, VCP_IN, VRF1_IN, VRF2_IN, VCURR connected together
VDIG1_IN,VDIG2_IN connected together
AVDD, ALVDD connected together

VBAT_SW1 and VBAT_SW2 connected together
VSUP_SW1 and VSUP_SW2 connected together
All VSS connected together

(5) Soldering austriamicrosystems strongly recommends to use underfill

5.2 Operating Conditions

Table 2 – Operating conditions

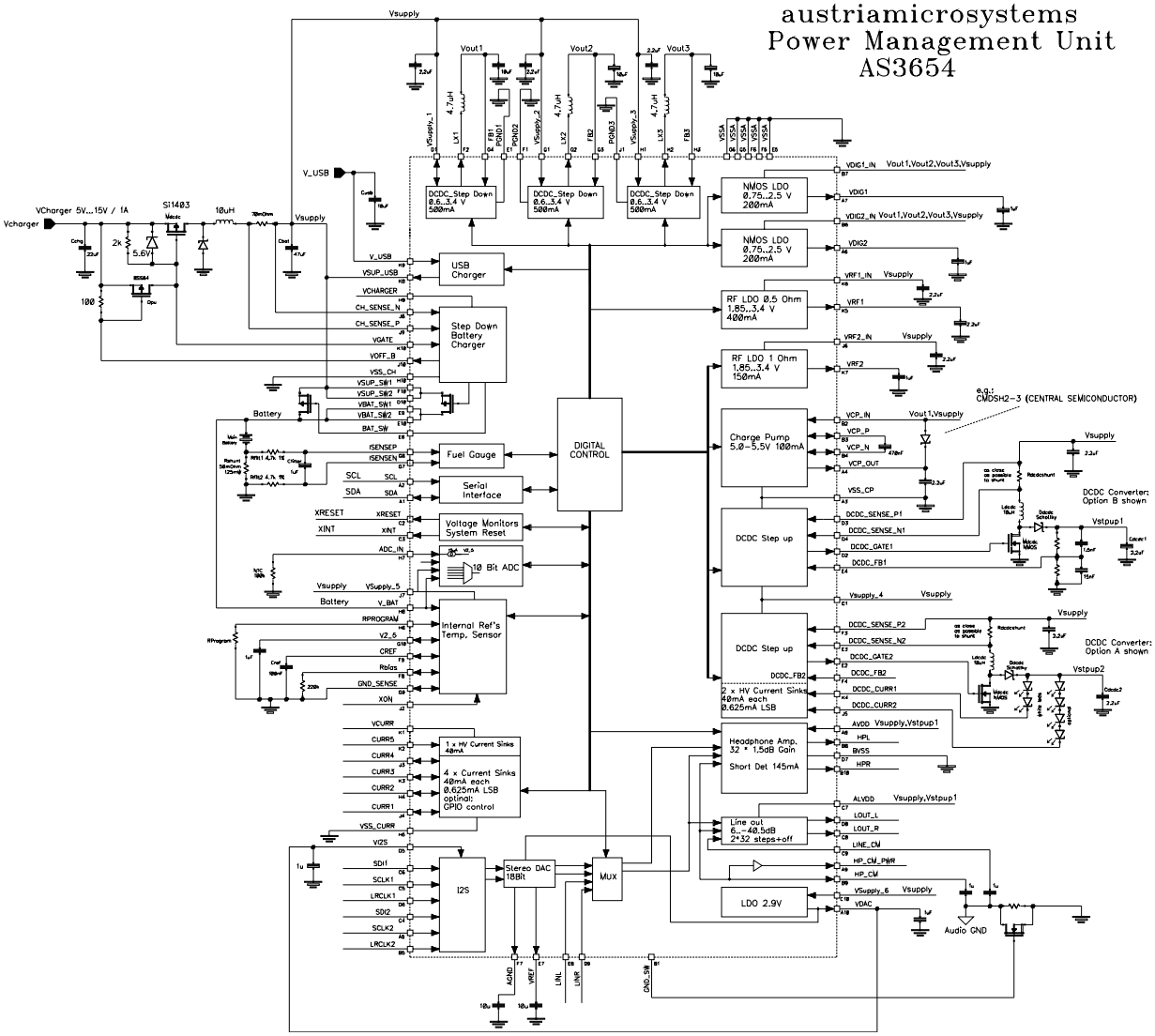
Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{HV}	High Voltage	0.0		15.0	V	VCHARGER, VGATE, DCDC_CURR1,DCDC_CURR2
V_{BAT}, V_{SUPPLY}	Battery, Supply Voltage	3.0	3.6	5.5	V	For pins V_BAT, VSUPPLY1-6 (always connect all VSUPPLY1-6 pins together), VSUP_SW1-2, VBAT_SW1-2, VRF1_IN, VRF2_IN, VCP_IN, AVDD, ALVDD, VCURR (1)
V2_5	Voltage on Pin V2_5	2.4	2.5	2.6	V	Internally generated
VCP_OUT	Output Voltage charge pump	4.9	5.2	5.6	V	Voltage generated by charge pump
T_{AMB}	Ambient Temperature	-30	25	85	deg.	
$I_{LOWPOWER}$	Low power mode current consumption		7 200		mA µA	Current consumption in low power mode with step down charger on(2) With step down charger off(3)
$I_{PowerOff}$	Power Off mode current consumption		16		µA	Current consumption in power off mode (4)

Notes

(1) During startup from the AC/DC adapter, the battery voltage can be below 3.0V
(2) with register bit **low_power_on** = 1, only Rf1=3.3V,Vout2=1.2V,Battery 3.6V,Vcharger=6.0V, no additional external loads
(3) with register bit **low_power_on** = 0, All regulators switched off, no additional external loads
(4) after setting register bit **xon_enable**=1 and **power_off**=1; only V2_5 is active in Power Off mode

6 General Description

Figure *2 – Blockdiagram AS3654*



7 Detailed Functional Descriptions

7.1 Step Up DC/DC Converter

Figure *3 – DC/DC step-up Converter 1*

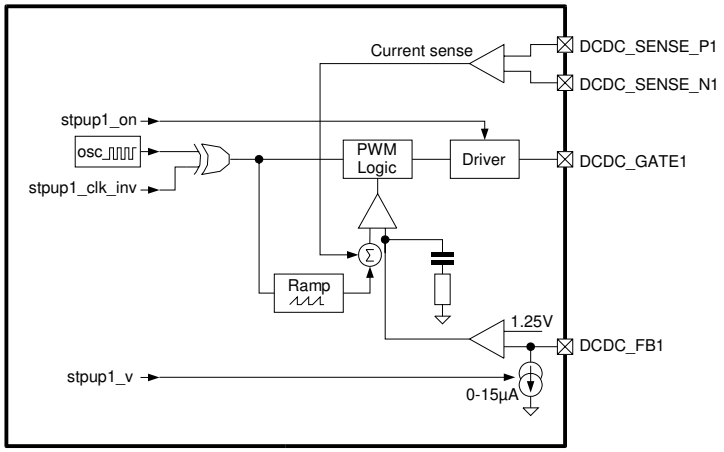


Figure *4 – DC/DC step-up Converter 2*

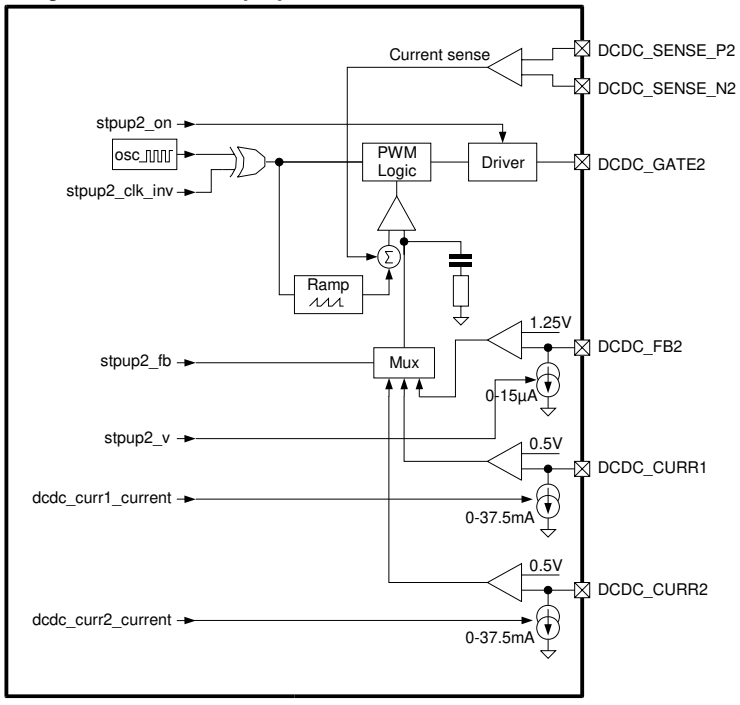


Table 3 – DC/DC Converter parameters

Symbol	Parameter	Min	TYP	Max	Unit	Note
I_{VDD}	Quiescent Current		140		µA	Pulse skipping mode
V_{FB1}	Feedback voltage for external resistor divider:	1.20	1.25	1.30	V	for constant voltage control
V_{FB2}	Feedback voltage for current sink regulation		0.5		V	DCDC_CURR1 or DCDC_CURR2
I_{DCDC_FB}	Additional tuning current at DCDC_FB	0		15	µA	adjustable by software in 1µA steps
	Accuracy of feedback current	-4		4	%	@ full scale
V_{rsense_max}	Current limit voltage at Rsense		100		mV	(e.g.: 0.65A for 0.15Ω sense resistor
R_{SW}	switch resistance			1	Ω	ON-resistance of external switching transistor
I_{load}	Load current	0		50	mA	at 15V output voltage
f_{IN}	Switching frequency		$f_{clk\_int}/2$		MHz	internal CLK frequency/2 Programmable: 0.8 to 1.15 MHz
C_{out}	Output capacitor		2.2		µF	ceramic, ±20%
L	Inductor		10		µH	Use inductors with small $C_{parasitic}$ (<100pF) to get high efficiency
t_{MIN_ON}	Minimum on time		130		ns	
MDC	Maximum duty cycle		91		%	

DC/DC Step Up converter is a high efficiency current mode PWM regulator, which provides an output voltage up to 20V and a load current up to 50mA . A constant switching frequency results in a low noise on supply and output voltage.

Feedback selection

For step up DCDC 1, the feedback is always DCDC_FB1.

For step up DCDC 2 following feedback selections are possible:
Stpup2_fb selects the type of feedback for the DCDC_step_up2 converter:
DCDC_CURR1, DCDC_CURR2 or DCDC_FB2 feedback (see Fig.3)

Setting stpup2_fb to 00b enables the feedback on DCDC_FB2, stpup2_fb to 01b enables feedback at pin DCDC_CURR1 , setting step_up_fb to 10b enables feedback at pin DCDC_CURR2. The Step-up converter is regulated such that the required current at the feedback path can be supported.
Always choose the path with the higher voltage drop as feedback to guarantee adequate supply for the other, unregulated path.
To protect the DCDC output voltage against overvoltage, if a LED string is broken, set stpup2_prot=1. In this mode the output voltage will be limited by limiting the DCDC_FB voltage to 1.25V (select the external resistor network to adjust this limitation voltage).

Figure *5 – DC/DC step up 2 converter with regulation of LED string on pin DCDC_CURR1 or DCDC_CURR2*

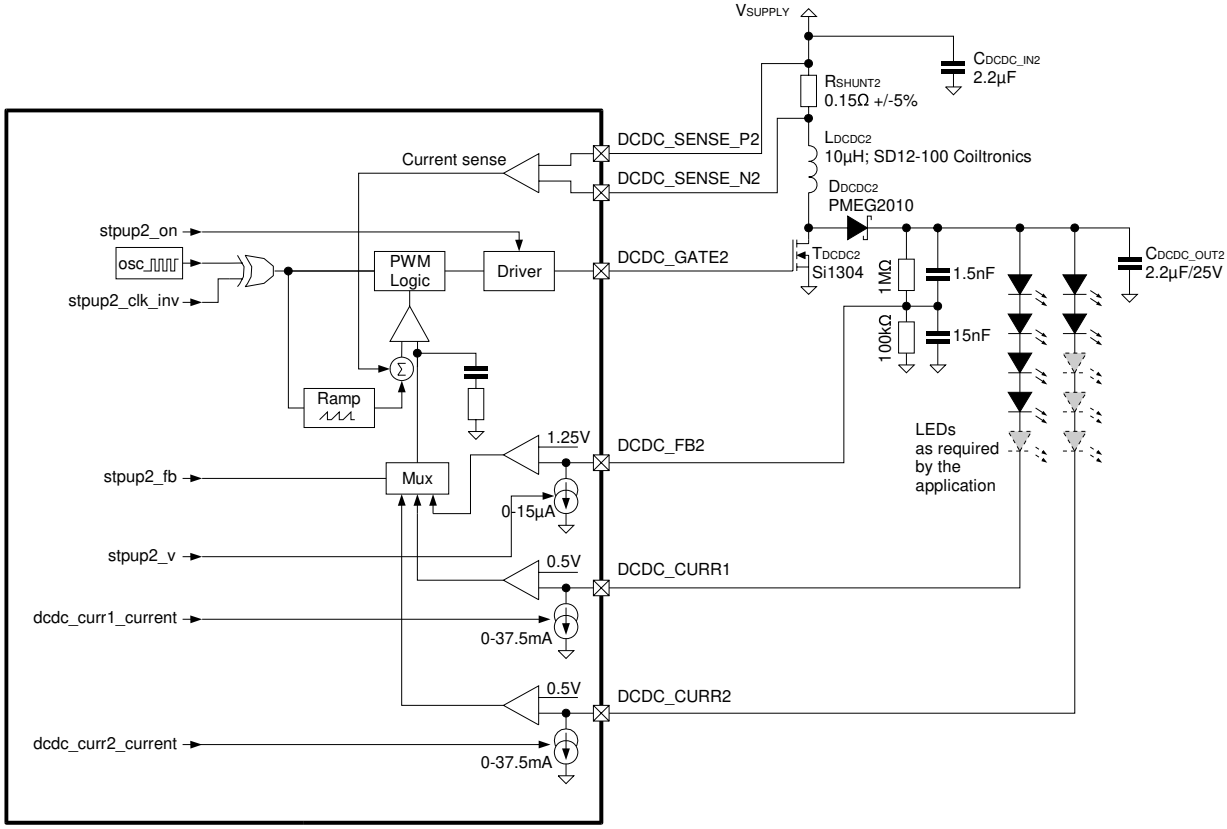
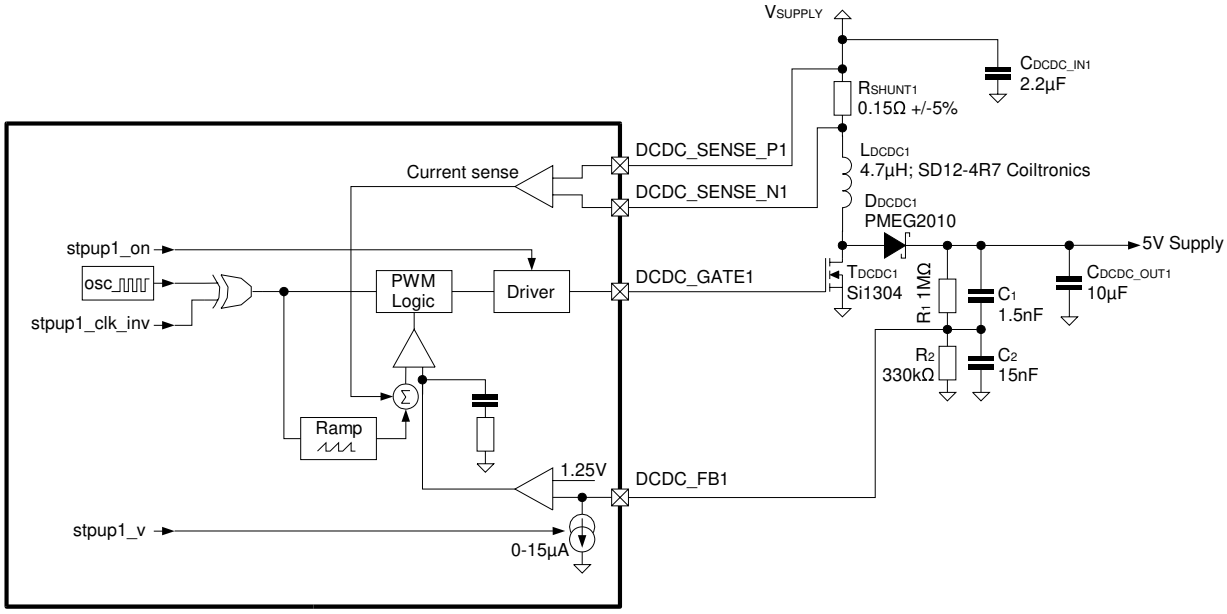


Figure *6 – DC/DC step up 1 converter with regulated output voltage of 5V. Feedback is at pin DCDC_FB1*



Voltage Feedback : (see Fig.5)

For Step UP DCDC 1 voltage feedback is always selected on pin DCDC_FB1. For Steup UP DCDC 2 set step2_fb to 00 to enable voltage feedbback at pin DCDC_FB2.
Bit stepX_res (X = 1 or 2) should be set to 1 in voltage feedback mode using two resistors.

The output voltage is regulated to a constant value, given by:

$$V_{stepup\_out} = \frac{R_1 + R_2}{R_2} 1.25 + I_{I_{DCDC\_FB}} \bullet R_1$$

If R2 is not used, the output voltage is:

$$V_{stepup\_out} = 1.25 + I_{I_{DCDC\_FB}} \bullet R_1$$

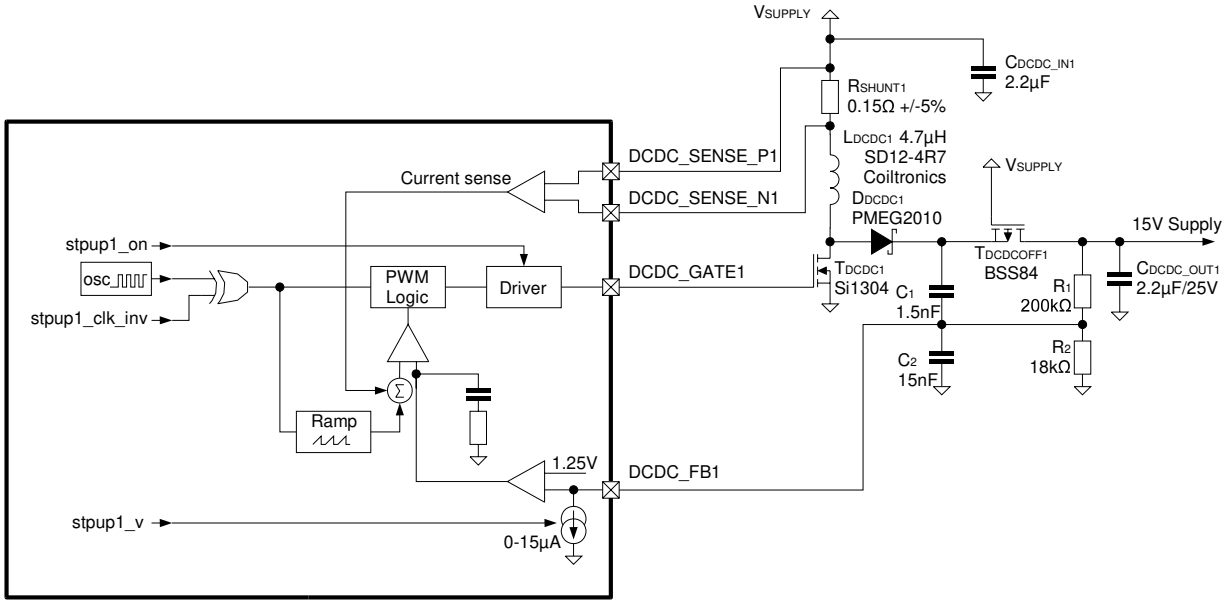
V_{stepup_out}	Step up regulator output voltage
R_1	Feedback resistor R1
R_2	Feedback resistor R2
$I_{Vtuning}$	Tuning current on DCDC_FB pin: stpupX_v (0µA to 15µA (1µA steps)) (X= 1 or 2)

Examples:

$I_{vtuning}$ µA	V_{stepup_out} R1=1MΩ,R2 not used	V_{stepup_out} R1=500kΩ,R2=64kΩ
0	-	11
1	-	11.5
2	-	12
3	-	12.5
4	-	13
5	6.25	13.5
6	7.25	14
7	8.25	14.5
8	9.25	15
9	10.25	15.5
10	11.25	16
11	12.25	16.5
12	13.25	17
13	14.25	17.5
14	15.25	18
15	16.25	18.5

Note: The voltage on pin DCDC_CURR1 and DCDC_CURR2 must never exceed 15V

Figure *7 – DC/DC step up converter 1 with regulated output voltage (15V), and switch off function of output voltage, to reduce shutdown current*



As the output voltage is always on, an additional output transistor can be added to reduce shutdown current through R1, R2 and the connected output circuit.
Note: A similar circuit can be used for step up converter 2.

Table 4 – Step Up DC/DC Bit definitions

Name	Default	Access	Description
stpupX_on	ROM	R/W	On/Off control of the step up dc/dc converter; (X=1 or 2)
stpupX_clkinv	ROM	R/W	Invert input clock of step up converter; (X=1 or 2) 0 Use positive edge of internal clk 1 Use negative edge of internal clk
stpup2_fb	ROM	R/W	Controls the feedback source 00 DCDC_FB enabled (external resistor divider) 01 DCDC_CURR1 feedback enabled (feedback through white LEDs) 10 DCDC_CURR2 feedback enabled (feedback through white LEDs) 11 reserved (don't use)
stpupX_freq	ROM	R/W	Defines the clock frequency of the step up dc/dc converter; (X=1 or 2) 0 $f_{clk\_int}/2$ (0.8 to 1.15 MHz) 1 $f_{clk\_int}/4$ (0.4 to 0.575 MHz)
stpupX_v	ROM	R/W	Defines the tuning current at DCDC_fb pin; (X=1 or 2) 0000 0 µA 0001 1 µA . 1111 15 µA
stpupX_res	ROM	R/W	Gain selection for DCDC step_up: (X=1 or 2) 0 Select 0 if DCDC is used with current feedback (DCDC_CURR1,DCDC_CURR2) or if DCDC_FB is used with current feedback only (Only R1,C1 connected; see Fig.6) 1 Select 1 if DCDC_FB1 or DCDC_FB2 is used with external resistor divider (2 resistors)
stpupX_fastskip	ROM	RW	DCDC converter output voltage at low loads, when pulse skipping is active: ; X=1 or 2 0: accurate output voltage, higher ripple (normal operation) 1: elevated output voltage, less ripple
stpup2_prot	ROM	RW	DCDC converter 2 overvoltage protection to prevent damage of external NFET, if DCDC_CURR1 or DCDC_CURR2 feedback selected, and no LED string connected: 0: Overvoltage protection disabled. 1: Switch off DCDC step up 2 if the voltage on DCDC_FB2 exceeds 1.25V
stpup1_shortprot	ROM	RW	Enables Protection and Detection circuit for DCDC step up1 – see next section 0: No protection and load detection 1: Short protection and load detection enabled
stpup1_oc_timeout	ROM	RW	Controls GPIOx switch off, after overcurrent timeout (5ms) for DCDC step up 1 0: disabled 1: enabled

Table 5 – Step Up Registermap

Register Definition	Addr.[1]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Step Up DC/DC Control	15	ROM (00h)	stpup2_res	stpup2_fastskip	stpup2_freq		stpup1_res	stpup1_fastskip	stpup1_freq	
Step Up1 DC/DC Control	16	ROM (00h)		stpup1_oc_timeout	stpup1_shortprot	stpup1_clkinv	stpup1_v			
Step Up2 DC/DC Control	17	ROM (00h)	stpup2_prot	stpup2_clkinv	stpup2_fb		stpup2_v			
Reg Power2 Ctrl	31	ROM					stpup2_on	stpup1_on	rf2_sw	rf1_sw

7.2 Stepup1 load detection and overcurrent protection circuit

This circuit protects the DCDC step up1 converter during short circuit and startup, by regulation of the output current.
An additional feature is the detection of a minimum output load of the StepUp converter. It is also possible to use this circuit without the DCDC step up converter, by using the sense resistor only:

- Detection circuit
  If the voltage on R_{sense} exceeds V_{DETECT} for more than 1msecond, or the DCDC Step up converter is not in Pulseskip for more than 1 msecond, the stepup1_det bit will be set.
- Overcurrent protection
  If the Overcurrent voltage $V_{OVCURRENT}$ has been exceeded by more than 5 msec the Bit stpup1_oc will be set and can only reset, by switching off and on the Protection circuit by writing Stpup1_shortprot 0 – 1.
  If stepup1_oc is set the load will be disconnected, if Stpup1_oc_timeout=1

Table 6 – StepUp1 protection/detection circuit parameters

Symbol	Parameter	Min	TYP	Max	Unit	Note
V_{DETECT}	Detection Threshold	2	12.5	20	mV	For Rsense=0.150Ohm => 83mA typ.
$V_{OVCURRENT}$	Overcurrent Threshold rising	150	180	215	mV	For Rsense=0.150Ohm => 1.2A typ.
$V_{OVhysteresis}$	Overcurrent Hysteresis		50		mV	
$t_{OV\_timeout}$	Overcurrent timeout		5		ms	Interrupt and/or external PMOS switching off after timeout f_{clk_int} = 2.2MHz
t_{detect}	Detection denounce time		1		ms	f_{clk_int} = 2.2MHz

[1] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence

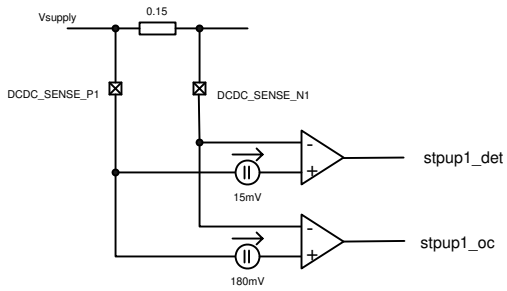


Table 7 – Low voltage status Bit definitions (stpup1_det and stpup1_oc)

Name	Default	Access	Description
stpup1_det	NA	R	Step up detection status register 0 V_{Rsense} < V_{DETECT} for more than 1msecond, and DCDC Step up converter is in Pulseskip for more than 1 msecond 1 V_{Rsense} > V_{DETECT} for more than 1msecond, or the DCDC Step up converter is not in Pulseskip for more than 1 msecond
stpup1_oc	NA	R	Step up overcurrent status bit 0 V_{Rsense} < $V_{OVCURRENT}$ 1 V_{Rsense} > $V_{OVCURRENT}$ for more than 5 msec (latched state)

Table 8 – Step Up protection Registermap

Register Definition	Addr.[2]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Low voltage Status	47	40h	stpup1_det	stpup1_oc	hpdet	dig2_lv	dig1_lv	sd3_lv	sd2_lv	sd1_lv

[2] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence

7.3 Current Sinks

These are general-purpose current sinks intended to control the backlight(s), buzzer and vibrator. The low voltage current sink has an integrated protection against over voltage and can therefore also drive inductive loads ($V_{PROTECT}$).

DCDC_CURR1 and DCDC_CURR2, CURR5 are high voltage (15V) current sinks, e.g. for series of white LEDs
CURR1,CURR2, CURR3, CURR4 are four 5V, 40mA current sinks, e.g. for buzzer, vibrator, LEDs

CURR1, CURR2, CURR3, CURR4 can be used as general propose Input/Output (GPIO) functions optional

7.3.1 High voltage Current Sinks 40mA (CURR5, DCDC_CURR1 and DCDC_CURR2):

Current sinks CURR5 DCDC_CURR1 and DCDC_CURR2 can be controlled individually. The step-up DCDC converter may supply them with voltages up to15V.

Table 9 – Current Sinks Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
$I_{DCDC\_Curr1,2,5}$	DCDC_CURR1,2 and CURR5 current, 00h-3Fh	0		40	mA	For V(CURRx) > 0.45V resolution = 0.625mA
$I_{DCDC\_protect}$	Current sink protection Current		2		µA	Protection Current if stpup2_on=1 and dcdc_currx_current=00h
Δ	absolute Accuracy	-20%		+20%		All Current sinks
V_{DCDC_Curr1}, V_{DCDC_Curr2}	Voltage compliance	0.45		15	V	during normal operation

Table *10 – Current Sink Bit definitions*

Name	Default	Access	Description
dcdc_currX_current, curr5_current	(00)h	R/W	Defines the current into DCDC_CURRX (X = 1…4) 00h power down (default state) 01h 0.625mA … 3Fh 39.375mA
dcdc_currX_low_bias, curr5_low_bias	0b	R/W	Reduces bias current by 2 0 Normal current (LSB=0.625mA, max current= 39.375mA) 1 Current reduction by 2 (LSB=0.3125mA, max current= 19.687mA)
dcdc_currX_ctrl, curr5_ctrl	00b	R/W	On/Off control of the pad DCDC_CURR1,2 and CURR5 00 Pad is turned off 01 Pad is active 1X don't use

7.3.2 Low voltage Current Sink 40mA (CURR1, CURR2, CURR3, CURR4):

Curr1, Curr2, Curr3, Curr4 can be controlled individually. Each one can sink up to 40mA.

Table *11 – Current Sinks Characteristics*

Symbol	Parameter	Min	Typ	Max	Unit	Note
$I_{CURR1,2,3,4}$	Curr1,2,3,4 current, 00h-1Fh	0		40	mA	For V(CURRx) > 0.2V resolution = 0.625mA, each current sink
Δ	absolute Accuracy	-20%		+20%		All Current sinks
$V_{Curr1,2,3,4}$	Voltage compliance	0.2		Vcurr.	V	during normal operation, New pin will be added

Table *12 – Current Sink Bit definitions*

Name	Default	Access	Description
currX_current	(00)h	R/W	Defines the current into CURRX (X = 1…4), if Register *GPIOXmode=011b or 100b* 00h power down (default state) 01h 0.625mA … 3Fh 39.375mA
currX_low_bias	0b	R/W	Reduces bias current by 2 for CURRX (X = 1…4) 0 Normal current (LSB=0.625mA, max current= 39.375mA) 1 Current reduction by 2 (LSB=0.3125mA, max current= 19.687mA)

Table 13 – Currentsink registermap

Register Definition	Addr.[3]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
DCDC_CURR1 value	35	00h		dcdc_curr1_low_bias	dcdc_curr1_current					
DCDC_CURR2 value	36	00h		dcdc_curr2_low_bias	dcdc_curr2_current					
CURR1 value	37	00h		curr1_low_bias	curr1_current					
CURR2 value	38	00h		curr2_low_bias	curr2_current					
CURR3 value	39	00h		curr3_low_bias	curr3_current					
CURR4 value	40	00h		curr4_low_bias	curr4_current					

[3] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30…Power1 Control states at startup sequence

Register Definition	Addr.[3]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
CURR5 value	41	00h		curr5_low_bias	curr5_current					
CURR control	51	00h			curr5_ctrl		dcdc_curr2_ctrl		dcdc_curr1_ctrl	

7.4 General Purpose Input / Output (GPIO) Pins

7.4.1 High Current GPIO Pins (Same pins as Current sinks CURR1…4)

The device contains 4 high current GPIO pins, which using the same pins CURR1...4, that are capable of sinking 100mA from any supply or VSUPPLY voltage. Each of the pins can be configured as open drain NMOS or push-pull output with VCURR high levels, as high impedance output or as digital input. When configured as output the output source can be a register bit, or the PWM generator, furthermore the output signal can be inverted. Integrated active clamp circuits can be enabled for the open drain NMOS output mode by setting *GPIOxPulls*=11b, thus allowing to use the high current GPIO pins for driving inductive loads. A pull-up resistor to VCURR can be enabled for the open drain NMOS output mode by setting *GPIOxPulls*=10b. When configured as digital input the logic level (*GPIOxInvert*='0') or the inverted logic level (*GPIOxInvert*='1') of the pin is reflected by bit *GPIOxBit* in the *GPIO Bit* register. Moreover, a special function can be selected for each digital input pin and a pull-up resistor to VCURR or a pull-down resistor can be enabled.

Table 14 – High Current GPIO Pin Characteristics (GPIO1…4)

$V_{VSUPPLY}$=3.0…5.5V; T_{amb}=–20…+70°C; unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{GPIOMAX}$	Maximum voltage on GPIO1…4 pins			$V_{Vcurr.}$+0.3	V	
V_{OLH}	Low level output voltage switch mode	–0.3		+0.35	V	I_{OL}=+100mA; digital output (GPIOxMode=100b and currentx=3Fh)
V_{OL}	Low level output voltage	–0.3		+0.4	V	I_{OL}=+1mA; digital output (GPIOxMode=000b ... 010b)
V_{OH}	High level output voltage	0.8·$V_{Vcurr.}$		$V_{Vcurr.}$	V	I_{OH}=–1mA; digital push-pull output
V_{IL}	Low level input voltage	–0.3		0.4	V	digital input
V_{IH}	High level input voltage	1.3		$V_{Vcurr.}$	V	digital input
$I_{LEAKAGE}$	Leakage current			10	µA	high impedance
$R_{pull-up}$	Pull-up resistance		78		kΩ	*GPIOxMode*=x0b; *GPIOxPulls*=10b; VCURR=3.6V
$R_{pull-down}$	Pull-down resistance		161		kΩ	digital input; *GPIOxPulls*=01b; VCURR=3.6V

Table 15 – GPIO 1…4 Register

R/W access;

Bit	Symbol	Default	Description
2…0	*GPIOxMode*	ROM	000b digital open drain NMOS output 001b digital push-pull output 010b digital input 011b digital open drain current sink operation Current defined by CURRx_current 100b digital open drain switch operation On resistance defined by CURRx_current101b to 111b .high impedance (

Bit	Symbol	Default	Description
4…3	*GPIOxIOSF*		00b input / output signal is written to or set by *GPIOxBit* in the *GPIO Bit* register 01b PWM (O) / WDOG (I) if used for PWM, pwm_h_time and pwm_l_time define the high and low time of this output 10b Protection of DCDC stepUp1 GPIO X (O) 11b NA
5	*GPIOxInvert*		0 normal polarity of input / output signal 1 inverted polarity of input / output signal
7…6	*GPIOxPulls*		00b no pull-up or pull-down resistor is enabled in all modes 01b pull-down resistor is enabled in digital input mode (clamp disabled) 10b pull-up resistor is enabled for *GPIOxMode*=000b,010b,011b,100b (clamp disabled) 11b enable active clamp circuit for *GPIOxMode*=000b,010b,011b,100b (pull-up/down disabled)

Table 17 – GPIO Bit Register

Address 58; R/W access; register is reset at power-on-reset only and at each reset cycle.

Bit	Symbol	Default	Description
0	*GPIO1*	0	This bit determines the output signal of the GPIO1 pin when selected as output source
1	*GPIO2*	0	This bit determines the output signal of the GPIO2 pin when selected as output source
2	*GPIO3*	0	This bit determines the output signal of the GPIO3 pin when selected as output source
3	*GPIO4*	0	This bit determines the output signal of the GPIO4 pin when selected as output source
4	*GPIO1_in*	NA	This bit reflects the logic level of the GPIO1 pin when configured as digital input pin
5	*GPIO2_in*	NA	This bit reflects the logic level of the GPIO2 pin when configured as digital input pin
6	*GPIO3_in*	NA	This bit reflects the logic level of the GPIO3 pin when configured as digital input pin
7	*GPIO4_in*	NA	This bit reflects the logic level of the GPIO4 pin when configured as digital input pin

Table 18 – PWM Frequency Control High Time Registers

Address 49; R/W access; register is reset at power-on-reset only and at each reset cycle.

Bit	Symbol	Default	Description
7-0	*pwm_h_time*	00h	This bit defines the high time of the pwm generator in $2/f_{clk\_int}$ units 0 = $2/ f_{clk\_int}$ 1 = $3/ f_{clk\_int}$ 2 = $4/ f_{clk\_int}$ … FFh = $257/ f_{clk\_int}$

Table 19 – PWM Frequency Control Low Time Registers

Address 49; R/W access; register is reset at power-on-reset only and at each reset cycle.

Bit	Symbol	Default	Description
7-0	*pwm_l_time*	00h	This bit defines the low time of the pwm generator in $2/f_{clk\_int}$ units 0 = $2/ f_{clk\_int}$ 1 = $3/ f_{clk\_int}$ 2 = $4/ f_{clk\_int}$ … FFh = $257/ f_{clk\_int}$

The following settings are not allowed: **pwm_h_time - pwm_l_time = 1** or **pwm_h_time - pwm_l_time = -1**

Table 20 – GPIOs Registermap

Register Definition	Addr.[4]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
GPIO 1	18	ROM (07h)	gpio1_pulls		gpio1_invert	gpio1_iosf		gpio1_mode		
GPIO 2	19	ROM (07h)	gpio2_pulls		gpio2_invert	gpio2_iosf		gpio2_mode		
GPIO 3	20	ROM (07h)	gpio3_pulls		gpio3_invert	gpio3_iosf		gpio3_mode		
GPIO 4	21	ROM (07h)	gpio4_pulls		gpio4_invert	gpio4_iosf		gpio4_mode		
GPIO Signal	48	NA	gpio4_in	gpio3_in	gpio2_in	gpio1_in	gpio4	gpio3	gpio2	gpio1
PWM Frequency Control High Time	49	00h	pwm_h_time							
PWM Frequency Control Low Time	50	00h	pwm_l_time							

7.5 ADC

Table *21 –ADC Characteristics*

Parameter	Symbol	Min	Typ	Max	Unit	Note
Resolution		10			Bit	
Input Voltage Range	Vin	0		1.8	V	
Differential Nonlinearity	DNL		± 0.25		LSB	1LSB ≈ 1.76mV
Integral Nonlinearity	INL		± 0.5		LSB	
Input Offset Voltage	Vos		2		LSB	
Input Impedance	Rin	100			Mohms	
Input Capacitance	Cin			9	pF	
Power Supply Current	Idd		500		µA	During conversion only
Power Down Current	Idd		100		NA	
Transient Parameters (25°C)						
Conversion Time	Tc		40		µs	
Clock Frequency	fc		$f_{clk\_int}/8$		kHz	internal CLK frequency/8 Programmable: 0.2 to 0.2875 MHz
Settling time of S&H	ts	1			µs	
ADC_IN pull up current		14.25	15	15.75	µA	Pull up current, if adc_idc=1111b

[4] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30…Power1 Control states at startup sequence

Table *22 - ADC Bit definitions*

Name	Default	Access	Description
start_conversion	0b	W	Writing a 1 into this bit starts one ADC conversion.
adc_on	0b	R/W	Writing a 1 into this bit activates the ADC and the input multiplexer. The ADC and the MUX are also activated for a conversion period when start_conversion is set to '1'
adc_select	000b	R/W	Selects an ADC channel 000 ADC_IN (LSB = 1.76mV) 001 not used 010 VBAT (Battery voltage divided by 3) (LSB=5.27mV) 011 Vcharger (Charger voltage divided by 10) (LSB=17. 6mV) clamping at 10V! 100 USB Voltage (USB voltage divided by 3) (LSB=5.27mV) 101 not used 110 vtemp (temperature sensor output voltage) (LSB=1.76mV) 111 ADC test channel
adc_idac	000b	R/W	Current source at ADC_IN input 0000 0µA 0001 1µA ... 1111 15 µA
adc_test	0b	R/W	always 0, don't change
adc_slow	0b	R/W	select ADC sampling frequency 0 275kHz (conversion time: 60us) 1 70kHz (conversion time: 240us)
result_not_ready	NA	R	Indicates end of conversion 0 result is ready 1 conversion is running
D0 - D9	NA	R	ADC result register

Figure *8 – ADC Timing-diagram*

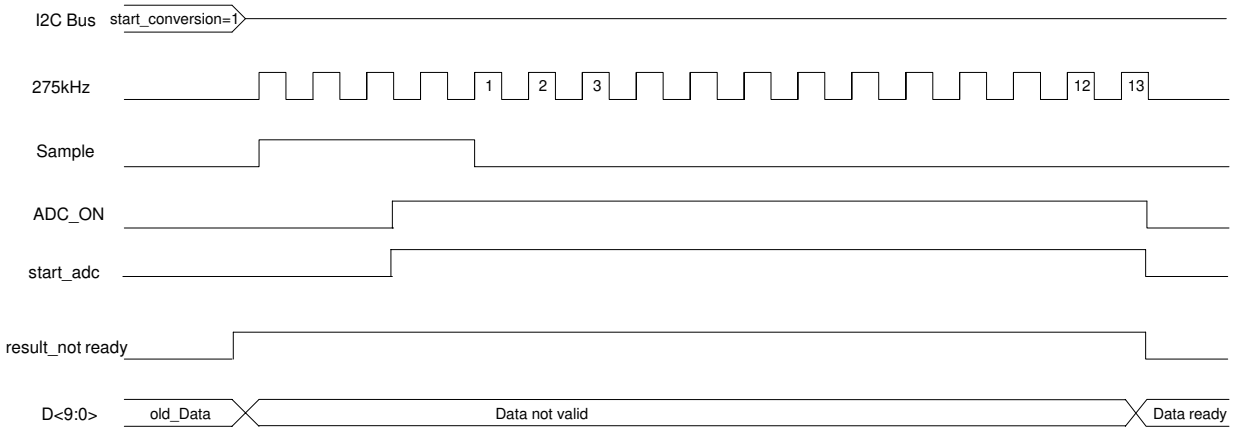


Table *23 – ADC register map*

Register Definition	Addr.[5]	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
ADC_control	63	00h	start_conversion	adc_on		adc_slow	adc_test	adc_select		
ADC_MSB result	64	NA	result_not_ready	D9	D8	D7	D6	D5	D4	D3
ADC_LSB result	65	NA						D2	D1	D0
ADC Idac	42	00h					adc_idac			

7.6 Internal Battery switch (Vsupply , Battery)

The internal Battery switch enables normal operation of the System during trickle charging of a deeply discharged battery.
The Switch provides the following functions:

- Trickle charging, if Vbattery is smaller than ResVolt. The current is defined in TrickleCurrent[1:0]
  PMOS is switched on if Vbattery is greater then ResVolt.
- Current limitation during tricklecharge, to avoid inrush current : $I_{trickle\_Ilimit}$
- Undervoltage protection of Vsupply during trickle charge. The trickle current is switched of , if Vsupply drops below $V_{trickleoff}$
- Ideal diode operation in Isolate Battery mode and disable charging mode, if charger is unplugged. This operation is for the internal battery switch only. External battery switch is open in that mode. Regulation will start, if the VSUPPLY voltage drops by more then V_{Diode} below the VBattery voltage

Table *24 – Battery switch parameters*

Symbol	Parameter	Min	TYP	Max	Unit	Note
V_{Supply}	Input voltage	3.0		5.5	V	PIN VSUP_SW1,VSUP_SW2
$I_{trickle\_limit}$	Trickle current limit		400		mA	
V_{Diode}	Ideal Diode start voltage		50		mV	
$V_{trickleoff}$	Vsupply threshold for trickle enable	-6%	3.9	3%	V	Trickle current will be switched of, if vsupply drops below this level
R_{SW}	P-Switch ON resistance		0.15		Ω	VSUP_SW=3.6V

Table *25 – Battery switch status Bit definitions*

Name	Default	Access	Description
batsw_mode		R	0 Trickle charging, if batsw_on=1. External PMOS switch disabled 1 Switch on Battery switch, if batsw_on=1. External PMOS switch enabled.
batsw_on		R	0 Battery switch off 1 Battery switch on (Mode defined by batsw_mode)

[5] Register address codes 00 – 31 are identical to Boot-ROM address codes
ROM-adr. 25-30...Power1 Control states at startup sequence