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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

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The technical content of this austriamicrosystems datasheet is still valid.

**Contact information:**

**Headquarters:**
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten, Austria
Tel: +43 (0) 3136 500 0
e-Mail: ams_sales@ams.com

Please visit our website at **www.ams.com**

# AS3658

**Data Sheet Confidential**

## Power and Audio Management Unit for Portable Devices

## 1 General Description

The AS3658 is highly integrated power and audio management unit. The AS3658 is designed to include sophisticated audio features like high performance audio DAC and ADC. It has several analog and digital audio interface which are explained in detail in the following sections. The AS3658 is an integrated solution for power supply generation and monitoring, battery management including charging.

## 2 Key Features

- System Control
  - Serial Control Interface
  - On/Off Control Module with Boot-ROM / GPIO
  - Reset Generation for system controller
  - Programmable Interrupt Controller and Watchdog
  - Low power off mode (9µA; 2.5V LDO on)
  - 88 bit unique ID or Boot fuse array
  - Reset with long ON-Keypress (SW-Interuptable)
  - Touchscreen Interface (10 bit, interrupt)
- Supply Voltage Generation
  - 2 RF Programmable Low Noise LDOs (250mA) (1 LDO can be a current controlled switch for hotplug (200mA ± 40%))
  - 1 RF Programmable Low Noise LDO (400mA)
  - 4 Programmable Dig. Low Power LDOs(200mA)
  - 2 General Purpose PWM DC/DC step up converter with three programmable current sinks (e.g. for-white led); for current mode feedback is automatically slected (DCDC_CURR1,2,3)
  - 3 General Purpose high efficiency DC/DC step down converter (DCDC 1 support DVM)
  - 1 Low noise charge pump with 5V output voltage
  - 1 Ultra Low Power 2.5V LDO (always on)
- Current sinks
  - 4 programmable(8-bit) from 0.15mA to 38.25mA (±5% ) optional useable as GPIOs
  - 3 programmable high voltage (15V) (8-bit) from 0.15mA to 38.25mA (±5% )
  - internal PWM generator (extended time range) (can control DCDC_CURR1,2,3)
- 10-bit 40µs Successive Approximation ADC
  - Two external Inputs (ADC_IN1, ADC_IN2)
- Battery Management
  - Full featured chemistry independent step down charger with Gas Gauge and Current limitation
  - High Current (1.0A) Linear Charger with external pass transistor (no step down charger)
  - 0.1 Ω Battery switch for start-up and trickle charge
  - Integrated USB charger up to 880mA (can be used as wall adapter charger); current accuracy 440-500mA for USB specification, in-circuit trimmable (±1.2% trimsteps)
  - Autonomous Battery Temperature Supervision (0ºC-45ºC or 0ºC- 50ºC) for 10k and 100k NTC
  - Charging Timeout (1h-8h in 30min steps)
  - Charging in Stanby mode
  - Completely Autonomous (no SW)
- Power Management Features
  - Wide Battery Supply Range 3.0…5.5V
  - On-Chip Bandgap Tuning for High Accuracy (±1%)
  - Thermal and Current Protection (int. sensor)
  - Standby Mode exit by interrupt e.g. Onkey/RTC
- Audio
  - 94dB Audio DAC, 16-48kHz sampling rate
  - Two Digital Audio Inputs (2 x I2S interface)
  - 2.9V low Noise LDO for Audio DAC
  - Two Headphone Amplifier Output with GND separation
  - Two I2S Inputs and one I2S Output
  - I2S master mode with programmable sample rate (controlled by internal PLL)
  - GND Buffer for Headphone Amplifier
  - Line/ Headphone outputs with GND separation
  - Audio ADC, 82dB SNR with 16ksps
  - Microphone Bias Supply and Amplifier (mono)
  - 5 Band Adjustable Audio Equalizer (± 12dB in 3dB gain steps)
  - SPDIF Output
  - Audio Mixer and Gain Stages
  - PCM Interface
- Real Time Clock (RTC)
  - Alarm and Time function
  - Repeated Wakeup (every second or minute)
  - 32kHz output
  - Backup Battery Charger and Switchover
- Programmable System clock
  - 1.6 MHz to 2.3 MHz with 100 kHz steps
- Package
  - BGA124 8x8mm, 0.5mm pitch (can be assembled without micro via boards)

# 3 Applications

The AS3658 is ideal for PDA, PMP, GPS-Navigation Systems and 1 Cell Li+ or 3 Cell NiMH powered devices.

*Figure 1. Blockdiagram* AS3658

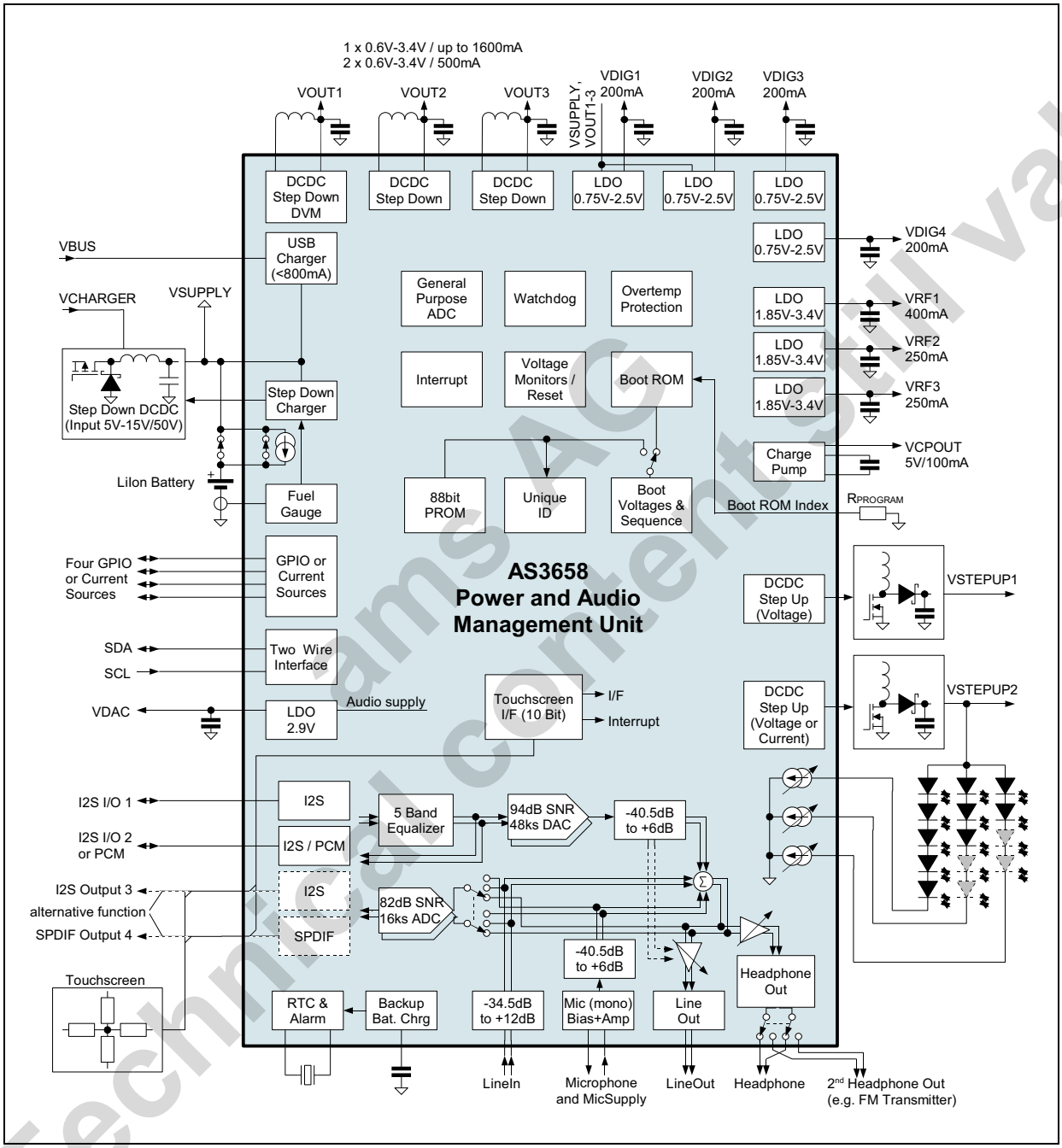
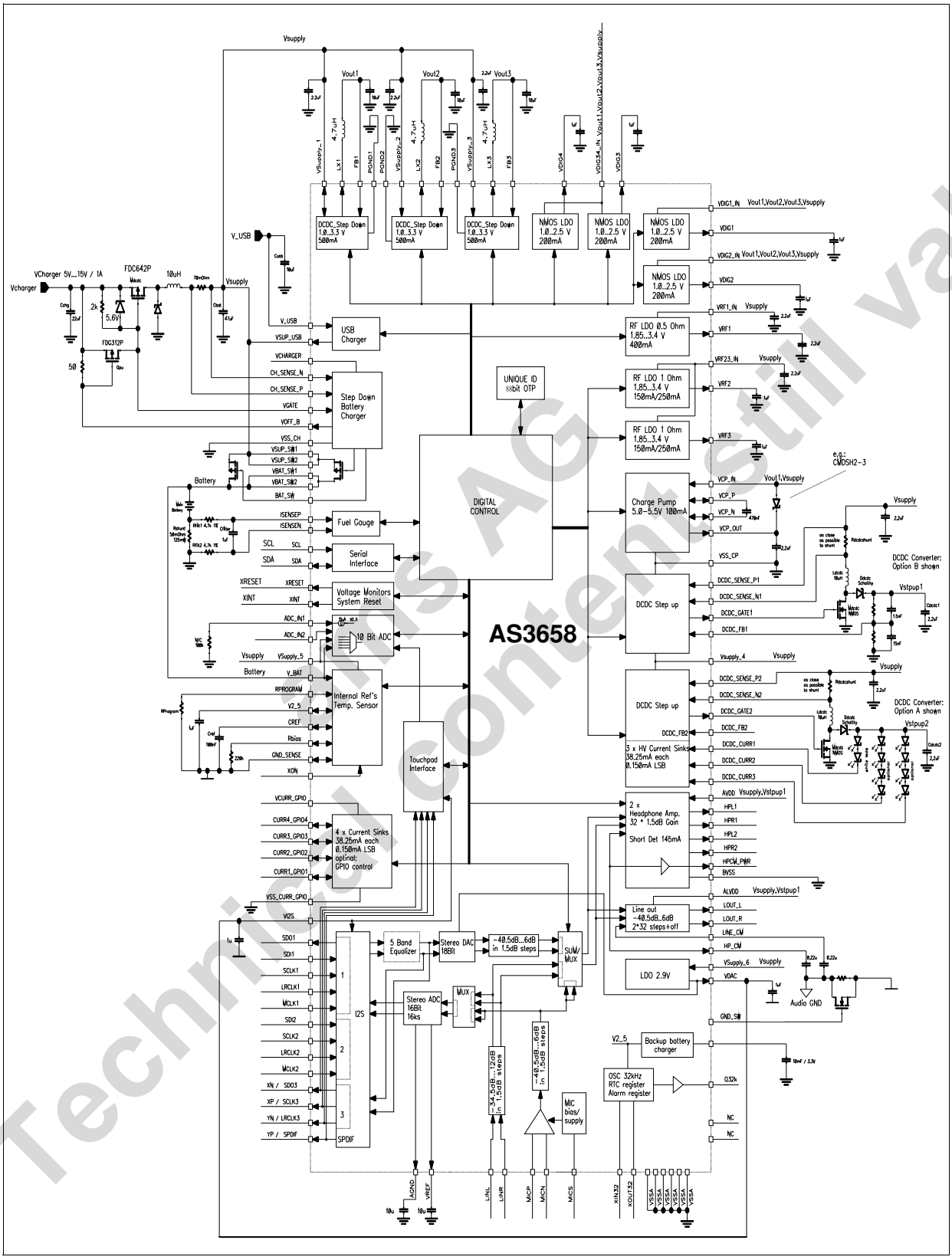


*Figure 2. Application Diagram*



## Table of Contents

## Document Revision History

*Table 1. Revision History*

| Chapter | Rev | Description of Changes | Date | Author |
|---|---|---|---|---|
| | 1v00 | - | 23.3.2009 | pkm |
| 9.1; 12 | 1v10 | - updated package drawings<br>- updated audio path drawings | 15.4.2009 | pkm |
| 12,13 | 1v11 | - updated packagemarkings and ordering information | 23.9.2009 | pkm |
| 12,13 | 1v12 | - updated packagemarkings and ordering information | 23.10.2009 | pkm |
| | 1v13 | - typo corrections | 23.9.2010 | pkm |

# 4 Pin Assignments

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC/ VSS _CP | LRC LK1 | SCL K3 | VI2S | SDO 1 | VCP _N | VCP _P | VCP _OU T | VDI G34 _IN | VDI G1_I N | LOU T_R | LINE _CM | HPL 1 | NC/ BV SS |
| B | SDI2 | | SCLK1 | SDI1 | SDA | VSS_C P | VCP_I N | VDIG_ 2 | VDIG2 _IN | VDIG_ 1 | LOUT_ L | HP_C M | | HPR 2 |
| C | Q32k | SCLK2 | | | | | | | | | | | HPR1 | HPL2 |
| D | DCDC _SENS E_P1 | MCLK 2 | | | SDO3 | SCL | VDIG_ 4 | VDIG_ 3 | MCLK 1 | LRCLK 2 | | | ALVD D | HP_ CM_ PWR |
| E | VSUP PLY_4 | DCDC _SENS E_N1 | | LRCLK 3 | | | | | | | BVSS | | AVDD | LINR |
| F | VSUP PLY_3 | DCDC _GATE 1 | | SPDIF | | | XRES ET | XINT | | | MICS | | VDAC | LINL |
| G | LX3 | DCDC _GATE 2 | | DCDC _SENS E_N2 | | DCDC _SENS E_P2 | | | VSSA | | MICN | | VSUP PLY_6 | VSU P_S W12 |
| H | PGND 3 | PGND 2 | | DCDC _FB1 | | FB3 | | | VSSA | | MICP | | VBAT_ SW12 | VSU P_S W12 |
| J | LX2 | VSS_C H | | DCDC _FB2 | | | FB2 | VSSA | | | VREF | | BAT_S W | VBAT _SW 12 |
| K | VSUP PLY_1 | VSUP PLY_2 | | FB1 | | | | | | | AGND | | ISENS N | ISEN SP |
| L | LX1 | VOFF_ B | | | CURR 4_GPI O4 | DCDC _CUR R1 | DCDC _CUR R3 | GND_ SW | RPRO GRAM | CREF | | | GND_ SENS E | RBIA S |
| M | PGND 1 | VGAT E | | | | | | | | | | | V_BAT | VBA CK |
| N | PGAT E1 | | VSUP PLY_5 | XON | CURR 1_GPI O1 | CURR 3_GPI O3 | DCDC _CUR R2 | ADC_I N1 | ADC_I N2 | VRF_2 | VCHA RGER | V2_5 | | XOU T32 |
| P | NC/ VSSA | CH_S ENSE_ P | CH_S ENSE_ N | VCUR R_GPI O | VSS_C URR | CURR 2_GPI O2 | VSUP_ USB | V_USB | VRF1_ IN | VRF_1 | VRF23 _IN | VRF_3 | XIN32 | NC/ VSS A |

## 4.1 Pin Description

*Table 2. Pin list CTBGA124, 8x8MM (*AS3658*)*

| Pin Name | Pin Number | Pin Type | Supply | Description |
|---|---|---|---|---|
| **Charger** | | | | |
| V_USB | P8 | P | | USB voltage supply input |
| VSUP_USB | P7 | P | | Supply output of USB charger (connect to Vsupply) |
| VCHARGER | N11 | P | | High voltage input coming from the charger; if the charger is used connect a ceramic capacitor of 1µF |
| VGATE | M2 | A | | Switch ON control pin for the external PMOS Fet transistor of the charger step down converter |
| VOFF_B | L2 | A | | Switch OFF control pin for the external PMOS Fet transistor of the charger step down Buck converter |
| VSS_CH | J2 | P | | Ground pad of Step down Charger |
| VBAT_SW12 | H13 | P | $V_{BAT}$ | Battery switch input1 (battery side) |
| VBAT_SW12 | J14 | P | $V_{BAT}$ | Battery switch input2 (battery side) |
| VSUP_SW12 | G14 | P | $V_{SUPPLY}$ | Battery switch input1 (supply side) |
| VSUP_SW12 | H14 | P | $V_{SUPPLY}$ | Battery switch input2 (supply side) |
| BAT_SW | J13 | A | | Battery switch output for external PMOS |
| CH_SENSE_N | P3 | A | $V_{SUPPLY}$ | Charger step down converter, external shunt resistor negative connection |
| CH_SENSE_P | P2 | A | $V_{SUPPLY}$ | Charger step down converter, external shunt resistor positive connection |
| ISENSP | K14 | A | V2_5 | Positive sensing input voltage for the external charging current shunt resistor |
| ISENSN | K13 | A | V2_5 | Negative sensing input voltage for the external charging current shunt resistor |
| **Serial Interface** | | | | |
| SCL | D6 | DI | $V_{SUPPLY}$ | SCL input in $I^2C$ mode |
| SDA | B5 | DIO | $V_{SUPPLY}$ | SDA input / output in $I^2C$ mode |
| **Control Interfaces** | | | | |
| XRESET | F7 | OD | $V_{SUPPLY}$ | Bidirectional Reset Pin – add an external pull-up resistor to the digital supply |
| XINT | F8 | OD | $V_{SUPPLY}$ | Interrupt Pin - add an external pull-up resistor to the digital supply |
| XON | N4 | IPU | V2_5 | Input pin to startup the system (power on), internal pull-up, apply zenerzap-programming voltage here |
| **RTC** | | | | |
| Q32K | C1 | OD | $V_{SUPPLY}$ | 32kHz oscillator digital output |
| XIN32 | P13 | A | V2_5 | 32kHz crystal oscillator input |
| XOUT32 | N14 | A | V2_5 | 32kHz crystal oscillator output |

*Table 2. Pin list CTBGA124, 8x8MM (*AS3658*)*

| Pin Name | Pin Number | Pin Type | Supply | Description |
|---|---|---|---|---|
| **Internal Refs** | | | | |
| VSUPPLY_5 | N3 | P | | Supply for voltage Measurement, **always** connect to VSUPPLY |
| V_BAT | M13 | P | $V_{BAT}$ | Battery supply for Reference blocks. |
| RPROGRAM | L9 | A | V2_5 | Select register setup at startup. |
| V2_5 | N12 | P | | Internal regulator analogue output |
| CREF | L10 | A | V2_5 | Reference voltage bypass capacitor connection |
| RBIAS | L14 | A | V2_5 | Internal Bias Reference Resistor (connect 220kΩ resistor) |
| GND_SENSE | L13 | P | VSSA | GND reference for analog blocks (connect to GND plane separate) |
| ADC_IN1 | N8 | A | V2_5 | Analog input1 for ADC10 |
| ADC_IN2 | N9 | A | V2_5 | Analog input2 for ADC10 |
| VBACK | M14 | A | | Backup battery connection |
| **Current Sinks** | | | | |
| CURR1_GPIO1 | N5 | A | $V_{CURR\_GPIO}$ | Current sink 1, or GPIO1 |
| CURR2_GPIO2 | P6 | A | $V_{CURR\_GPIO}$ | Current sink 2, or GPIO2 |
| CURR3_GPIO3 | N6 | A | $V_{CURR\_GPIO}$ | Current sink 3, or GPIO3 |
| CURR4_GPIO4 | L5 | A | $V_{CURR\_GPIO}$ | Current sink 4, or GPIO4 |
| DCDC_CURR1 | L6 | A | $V_{CURR\_GPIO}$ | Step up DC/DC converter2 current source 1 |
| DCDC_CURR2 | N7 | A | $V_{CURR\_GPIO}$ | Step up DC/DC converter2 current source 2 |
| DCDC_CURR3 | L7 | A | $V_{CURR\_GPIO}$ | Step up DC/DC converter2 current source 3 |
| VCURR_GPIO | P4 | A | | Supply voltage of GPIOs and current sinks |
| VSS_CURR_GPIO | P5 | A | $V_{CURR\_GPIO}$ | Ground pad of Current sink / GPIO pads |
| **General Purpose DC/DC Step up Converter 1 and 2** | | | | |
| VSUPPLY_4 | E1 | P | | Supply for DCDC step up and control interface, always connect to VSUPPLY |
| DCDC_FB1 | H4 | A | $V_{SUPPLY}$ | Step up DC/DC converter1 feedback input |
| DCDC_GATE1 | F2 | A | $V_{SUPPLY}$ | Step up DC/DC converter1 control for external mosfet |
| DCDC_SENSE_P1 | D1 | A | $V_{SUPPLY}$ | Step up DC/DC converter1 external shunt resistor positive connection |
| DCDC_SENSE_P2 | G6 | A | $V_{SUPPLY}$ | Step up DC/DC converter2 external shunt resistor positive connection |
| DCDC_SENSE_N1 | E2 | A | $V_{SUPPLY}$ | Step up DC/DC converter1 external shunt resistor negative connection |
| DCDC_SENSE_N2 | G4 | A | $V_{SUPPLY}$ | Step up DC/DC converter2 external shunt resistor negative connection |

*Table 2. Pin list CTBGA124, 8x8MM (*AS3658*)*

| Pin Name | Pin Number | Pin Type | Supply | Description |
|---|---|---|---|---|
| DCDC_GATE2 | G2 | A | $V_{SUPPLY}$ | Step up DC/DC converter2 control for external mosfet |
| DCDC_FB2 | J4 | A | $V_{SUPPLY}$ | Step up DC/DC converter2 feedback input |
| **Linear Regulators (LDOs)** | | | | |
| VRF1_IN | P9 | P | $V_{SUPPLY}$ | Supply Pad for RF1 LDO (VRF_1), always connect to Supply>3.0V |
| VRF_1 | P10 | A | $V_{RF1\_IN}$ | Output voltage of one of the RF LDO's; can be used as High-Side Switch, if used as LDO connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%) |
| VRF23_IN | P11 | P | $V_{SUPPLY}$ | Supply Pad for RF2 and RF3 LDO (VRF_2, VRF_3), always connect to Supply>3.0V |
| VRF_2 | N10 | A | $V_{RF23\_IN}$ | Output voltage of one of the RF LDO's; can be used as High-Side Switch, if used as LDO connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%) |
| VRF_3 | P12 | A | $V_{RF23\_IN}$ | Output voltage of one of the RF LDO's; can be used as High-Side Switch, if used as LDO connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%) |
| VDIG1_IN | A10 | P | $V_{SUPPLY}$ | Supply Pad for DIG1 LDO (VDIG_1) |
| VDIG_1 | B10 | A | $V_{DIG1\_IN}$ | Output voltage of one of the DIG LDO's. Connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%) |
| VDIG2_IN | B9 | P | $V_{SUPPLY}$ | Supply Pad for DIG2 LDO (VDIG_2) |
| VDIG_2 | B8 | A | $V_{DIG2\_IN}$ | Output voltage of one of the DIG LDO's. Connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%) |
| VDIG34_IN | A9 | P | $V_{SUPPLY}$ | Supply Pad for DIG3 and DIG4 LDO (VDIG_3, VDIG_4) |
| VDIG_3 | D8 | A | $V_{DIG3\_IN}$ | Output voltage of one of the DIG LDO's. Connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%) |
| VDIG_4 | D7 | A | $V_{DIG4\_IN}$ | Output voltage of one of the DIG LDO's. Connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%) |
| **Charge Pump** | | | | |
| VCP_IN | B7 | P | $V_{SUPPLY}$ | Supply Pad for Charge Pump, **always** connect to Supply>3.0V |
| VCP_N | A6 | A | $V_{SUPPLY}$ | HVS charge pump flying capacitor positive side |
| VCP_P | A7 | A | | HVS charge pump flying capacitor negative side |
| VCP_OUT | A8 | A | | Charge pump output, connect a ceramic capacitor of 2.2µF (+100%/-50%) |
| VSS_CP | B6 | A | $V_{SUPPLY}$ | Ground pad of charge pump |
| **DCDC Step Down Converters** | | | | |
| PGATE1 | N1 | A | $V_{SUPPLY}$ | Gate output for external PMOS.(DCDC step down controller 1) |
| VSUPPLY_1 | K1 | P | | Supply Pad for DCDC_Step down converter1, **always** connect to VSUPPLY |
| LX1 | L1 | A | $V_{SUPPLY}$ | DC/DC step down converter1 output |
| FB1 | K4 | A | $V_{SUPPLY}$ | DC/DC step down converter1 feedback |
| PGND1 | M1 | A | $V_{SUPPLY}$ | Power Ground of DCDC step down converter1 |

*Table 2. Pin list CTBGA124, 8x8MM (*AS3658*)*

| Pin Name | Pin Number | Pin Type | Supply | Description |
|---|---|---|---|---|
| VSUPPLY_2 | K2 | P | | Supply Pad for DCDC_Step down converter2, **always** connect to VSUPPLY |
| LX2 | J1 | A | $V_{SUPPLY}$ | DC/DC step down converter2 output |
| FB2 | J7 | A | $V_{SUPPLY}$ | DC/DC step down converter2 feedback |
| PGND2 | H2 | A | $V_{SUPPLY}$ | Power Ground of DCDC step down converter2 |
| VSUPPLY_3 | F1 | P | | Supply Pad for DCDC_Step down converter3, **always** connect to VSUPPLY |
| LX3 | G1 | A | $V_{SUPPLY}$ | DC/DC step down converter3 output |
| FB3 | H6 | A | $V_{SUPPLY}$ | DC/DC step down converter3 feedback |
| PGND3 | H1 | A | $V_{SUPPLY}$ | Power Ground of DCDC step down converter3 |
| **Audio** | | | | |
| VSUPPLY_6 | G13 | P | | Supply for VI2S Regulator |
| VI2S | A4 | P | | Supply Pad for I2S Interface, Connect to VDAC Supply |
| SDI1 | B4 | I | VI2S | I2S_1 Data input to DAC |
| SDO1 | A5 | O | VI2S | I2S_1 Data output from ADC |
| SCLK1 | B3 | I/O | VI2S | I2S_1 Shift clock input or output |
| LRCLK1 | A2 | I/O | VI2S | I2S_1 Left/Right clock input or output |
| MCLK1 | D9 | I/O | VI2S | Master clock input or output for I2S1: DAC (128*Fsdac or 256 *Fsdac) |
| SDI2 | B1 | I | VI2S | I2S_2 Data input to DAC |
| SCLK2 | C2 | I | VI2S | I2S_2 Shift clock |
| LRCLK2 | D10 | I | VI2S | I2S_2 Left/Right clock |
| MCLK2 | D2 | I | VI2S | Master clock input for I2S2: DAC (128*Fsdac or 256 *Fsdac) |
| SDO3(X-) | D5 | I/O | VI2S | I2S_3 Data output (if touchpen interface disabled)<br>Touchpen Interface X- Input/Output (if touchpen interface enabled) |
| SCLK3(X+) | A3 | I/O | VI2S | I2S_3 Shift clock output (if touchpen interface disabled)<br>Touchpen Interface X+ Input/Output (if touchpen interface enabled) |
| LRCLK3(Y-) | E4 | I/O | VI2S | I2S_3 Left/Right clock output (if touchpen interface disabled)<br>Touchpen Interface Y- Input/Output (if touchpen interface enabled) |
| SPDIF(Y+) | F4 | I/O | VI2S | SPDIF digital output (if touchpen interface disabled)<br>Touchpen Interface Y+ Input/Output (if touchpen interface enabled) |
| AGND | K11 | A | VDAC | CM voltage bypass capacitor connection (1.45V) |
| VREF | J11 | A | VDAC | VDAC voltage bypass capacitor connection (2.9V) |
| LINL | F14 | A | VDAC | Line input left channel. |
| LINR | E14 | A | VDAC | Line input right channel |
| GND_SW | L8 | O | $V_{SUPPLY}$ | Digital output for controlling the external NMOS |

*Table 2. Pin list CTBGA124, 8x8MM (*AS3658*)*

| Pin Name | Pin Number | Pin Type | Supply | Description |
|---|---|---|---|---|
| VDAC | F13 | A | VDAC | 2.9V Output voltage of one of DAC LDO; Connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%) |
| HP_CM | B12 | A | AVDD | Bypass capacitor connection of common mode voltage of Audio headphone amplifier (AVDD/2) |
| HP_CM_PWR | D14 | A | AVDD | Buffered voltage of HP_CM |
| LINE_CM | A12 | A | ALVDD | Bypass capacitor connection of common mode voltage of Audio line out amplifier (ALVDD/2) |
| LOUT_L | B11 | A | ALVDD | Line out output Left channel |
| LOUT_R | A11 | A | ALVDD | Line out output Right channel |
| ALVDD | D13 | P | | Supply pad of Line out amplifier |
| AVDD | E13 | P | | Supply pad of headphone amplifier |
| HPL1 | A13 | A | AVDD | Headphone output1 left channel |
| HPR1 | C13 | A | AVDD | Headphone output1 right channel |
| HPL2 | C14 | A | AVDD | Headphone output2 left channel |
| HPR2 | B14 | A | AVDD | Headphone output2 right channel |
| MICN | G11 | A | VDAC | Microphone Input N |
| MICP | H11 | A | VDAC | Microphone Input P |
| MICS | F11 | A | $V_{SUPPLY}$ | Microphone Supply (2.95V) / Remote Input |
| **VSS** | | | | |
| BVSS | E11 | P | AVDD | Power ground of headphone amplifier |
| VSSA | G9 | VSS | | Analog Ground Pad |
| VSSA | H9 | VSS | | Analog Ground Pad |
| VSSA | J8 | VSS | | Analog Ground Pad |
| NC/VSS_CP | A1 | VSS | | Analog Ground Pad |
| NC/VSSA | P1 | VSS | | Analog Ground Pad |
| NC/VSSA | P14 | VSS | | Analog Ground Pad |
| NC/BVSS | A14 | VSS | | Power ground of headphone amplifier |

**Note:** The following are the Pin Types

- **I**: Digital Input Pin
- **IPD**: Digital Input Pin with internal pull-down resistor
- **IPU**: Digital Input Pin with internal pull-up resistor
- **IODPU**: Digital Input / Open Drain Output Pin with internal pull-up resistor
- **O**: Digital Output Pin
- **OD**: Digital Open Drain Output Pin; requires external pull-up resistor
- **IO**: Digital Input / Output Pin
- **A**: Analog Pin
- **P**: Power Pin

# 5 Absolute Maximum ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 13 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Table 3. Absolute Maximum Ratings*

| Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|
| High voltage pins ($V_{IN\_HV}$) | -0.3 | 17.0 | V | Applicable for high voltage pins[1] |
| 5V pins ($V_{IN\_MV}$) | -0.3 | 7.0 | V | Applicable for pins 5V-pins[2] |
| 3.3V pins ($V_{IN\_LV}$) | -0.3 | 5.0 | V | Applicable for 3.3V-Pins[3] |
| Input pin current ($I_{IN}$) | -25 | +25 | mA | At 25 ºC, Norm: Jedec 78 |
| Storage Temperature Range ($T_{strg}$) | -55 | 125 | ºC | |
| Humidity | 5 | 85 | % | Noncondens |
| Electrostatic discharge 1kV ($V_{ESD}$) | -1000 | 1000 | V | Norm: MIL 883 E Method 3015; Setup[4] Applicable for pins: all |
| Total Power Dissipation | | 1 | W | $T_A$ = 70ºC |
| | | 0.72 | W | $T_A$ = 84ºC |
| Package Body Temperature | | 260 | °C | *IPC/JEDEC J-STD-020C, reflects moisture sensitivity level only* The lead finish for Pb-free leaded packages is matte tin (100% Sn). |
| Solder Profile[5] | 235 | 245 | °C | $T_{PEAK}$ |
| | 30 | 45 | s | $D_{Well}$, above 217 °C |
| Moisture Sensitive Level | 3 | | 1 | Represents a max. floor live time of 168h |

1. HV pins
   VCHARGER, VGATE, VOFF_B, DCDC_CURR1, DCDC_CURR2, DCDC_CURR3
2. 5V pins are
   V_USB, CH_SENSE_N, CH_SENSE_P, VSUP_SW1, VSUP_SW2, VBAT_SW1, VBAT_SW2, V_BAT, SCL, SDA, XRESET, XINT, VSUPPLY_3, CURR1_GPIO1…CURR4_GPIO4, DCDC_GATE1, DCDC_GATE2, DCDC_SENSE_P1, DCDCSENSE_P2, DCDC_SENSE_N1, DCDC_SENSE_N2, DCDC_FB1, DCDC_FB2, VCL, VCP_OUT, VCP_N, VCP_P, VCP_IN, VCP_IN, VRF1, VREF1_IN, VRF2, VRF23_IN, VRF3, VDIG1, VDIG1_IN, VDIG2, VDIG2_IN, VDIG34_IN, VDIG_3, VDIG_4, PGATE1 VSUPPLY_1, VSUPPLY_2, LX1, LX2, GND_SW, VSUPPLY_4, LINE_CM, HP_CM_PWR, HP_CM, HPLx, HPRx, ALVDD, AVDD, LSP_R, BVSS, LSP_L, AVDD, VSUPPLY_5, VSUPPLY_6
3. 3.3V pins are
   ISENSEP, ISENSEN, ADC_INx, RPROGRAM, V2_5, CREF, ON, VI2S, SDIx, SCLKx, MCLKx, LRCLKx, SDOx, SPDIF, AGND, VREF, LINL,LINR, VDAC, Q32K, XIN32, XOUT32, VBACK, MICS, MICN, MICP
4. The following pins are connected to ESD setup:

   VSUPPLY_1...VSUPPLY_6, VCP_IN, VRF1_IN, VRF2_IN, VCURR connected together
   VDIG1_IN, VDIG2_IN, VDIG34_IN connected together
   AVDD, ALVDD connected together
   VBAT_SW1 and VBAT_SW2 connected together
   VSUP_SW1 and VSUP_SW2 connected together
   All VSS connected together

5. austriamicrosystems strongly recommends to use underfill.

# 6 Electrical Characteristics

*Table 4. Electrical Characteristics*

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Operating Conditions** | | | | | | |
| VHV | High Voltage | VCHARGER, VGATE, DCDC_CURR1,DCDC_CURR2, DCDC_CURR3 | 0.0 | | 15.0 | V |
| VBAT, VSUPPLY, VCURR_GPIO | Battery, Supply Voltage | For pins V_BAT, VSUPPLY1-6 (always connect all VSUPPLY1-6 pins together), VSUP_SW1-2, VBAT_SW1-2, VRF1_IN, VRF2_IN, VCP_IN, AVDD, ALVDD | 3.0 | 3.6 | 5.5 | V |
| V2_5 | Voltage on Pin V2_5 | Internally generated | 2.4 | 2.5 | 2.6 | V |
| VCP_OUT | Output Voltage charge pump | Voltage generated by charge pump | 4.9 | 5.2 | 5.6 | V |
| TAMB | Ambient Temperature | | -40 | 25 | 85 | ºC |
| ILOWPOWER | Low power mode current consumption | Current consumption in low power mode with step down charger on[1] | | 7 | | mA |
| | | With step down charger off[2] | | 280 | | µA |
| IPOWEROFF | Power Off mode current consumption | Current consumption in power off mode[3] | | 10 | | µA |

1. With register bit low_power_on = 1, only Rf1=3.3V,Vout2=1.2V, Battery 3.6V,Vcharger=6.0V, no additional external loads
2. With register bit low_power_on = 0, All regulators switched off, no additional external loads
3. After setting register bit xon_enable=1 and power_off=1; only V2_5 is active in Power Off mode
4. During startup from the AC/DC adapter, the battery voltage can be below 3.0V

# 7 Typical Operating Characteristics

see individual block description

# 8 Detailed Description-Power Management Functions

The power management function consist of the DCDC Step up converters, Current Sink, GPIOs, general purpose 10 bit ADC, backup battery charger, main battery charger and power path management (consisting of the battery switch, external step down/linear charger, USB charger and battery charge controller), step down dc/dc converters, low dropout regulators (LDOs) and 5V charge pump.

## 8.1 Step Up DC/DC Converters

*Figure 3. DC/DC step-up Converter 1*

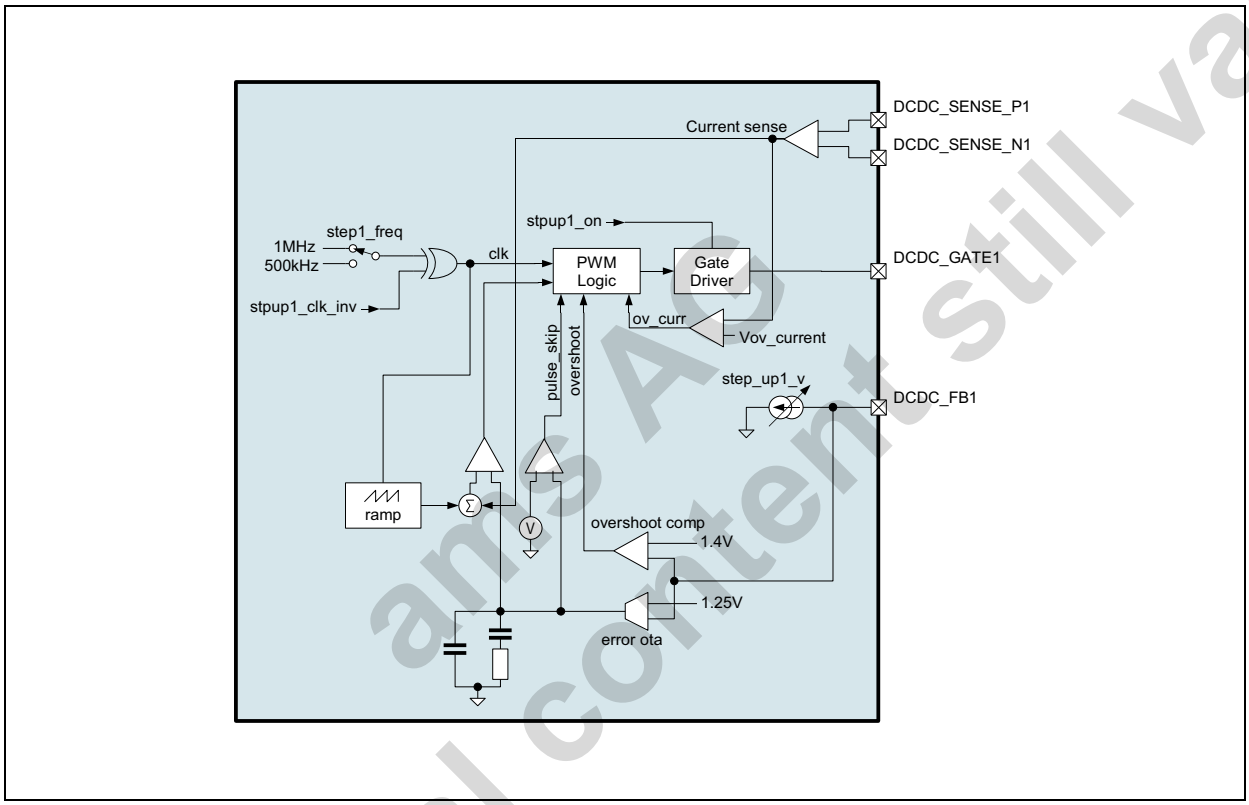


*Figure 4. DC/DC step-up Converter 2*

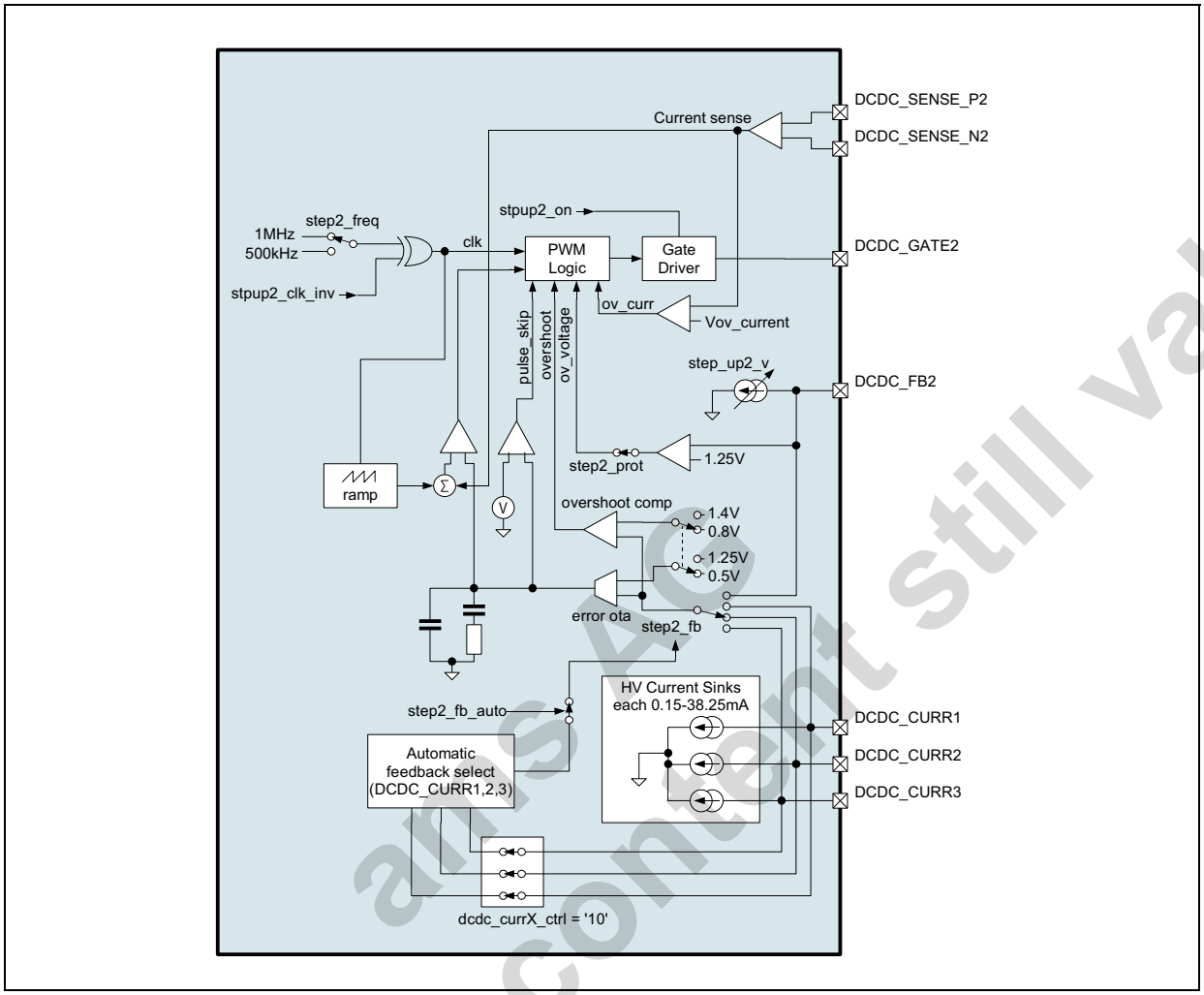



*Table 5. DC/DC Converter parameters*

| Symbol | Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| $I_{VDD}$ | Quiescent Current | | 140 | | µA | Pulse skipping mode |
| $V_{FB1}$ | Feedback voltage for external resistor divider: | 1.20 | 1.25 | 1.30 | V | for constant voltage control |
| $V_{FB2}$ | Feedback voltage for current sink regulation | | 0.5 | | V | DCDC_CURR1, DCDC_CURR2 or DCDC_CURR3 |
| $I_{DCDC\_FB}$ | Additional tuning current at DCDC_FB | 0 | | 31 | µA | adjustable by software in 1µA steps |
| | Accuracy of feedback current | -5 | | 5 | % | @ full scale |
| $V_{rsense\_max}$ | Current limit voltage at Rsense | | 100 | | mV | E.g.: 0.65A for 0.15Ω sense resistor |
| $R_{SW}$ | switch resistance | | | 1 | Ω | ON-resistance of external switching transistor |
| $I_{load}$ | Load current | 0 | | 50 | mA | at 15V output voltage |
| $f_{IN}$ | Switching frequency | | $f_{clk\_int}/2$ | | MHz | internal CLK frequency/2 Programmable: 0.8 to 1.15 MHz |

*Table 5. DC/DC Converter parameters*

| Symbol | Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| $C_{out}$ | Output capacitor | | 2.2 | | µF | ceramic, ±20% |
| L | Inductor | | 10 | | µH | Use inductors with small $C_{parasitic}$ (<100pF) to get high efficiency |
| $t_{MIN\_ON}$ | Minimum on time | | 130 | | ns | |
| MDC | Maximum duty cycle | | 91 | | % | |

The DC/DC Step Up converter is a high efficiency current mode PWM regulator, which provides an output voltage dependent on the maximum VDS voltage of the external transistor, and maximum load current selectable by the external shunt resistor.
For Example:

5V,500mA @ 1.1Mhz

25V,50mA @ 1.1MHz

40V,20mA @ 550kHz

A constant switching frequency results in a low noise on supply and output voltage.

### 8.1.1 Feedback selection

For step up DCDC 1, the feedback is always DCDC_FB1.

For step up DCDC 2 following feedback selections are possible:

Stpup2_fb selects the type of feedback for the DCDC_step_up2 converter:

DCDC_CURR1, DCDC_CURR2, DCDC_CURR3 or DCDC_FB2 feedback (see Figure 5)

Setting stpup2_fb to 00b enables the feedback on DCDC_FB2, stpup2_fb to 01b enables feedback at pin DCDC_CURR1, setting step_up_fb to 10b enables feedback at pin DCDC_CURR2 and setting step_up_fb to 11b enables feedback at pin DCDC_CURR3. The Step-up converter is regulated such that the required current at the feedback path can be supported.

Always choose the path with the higher voltage drop as feedback to guarantee adequate supply for the other, unregulated path.

To protect the DCDC output voltage against overvoltage, if a LED string is broken, set stpup2_prot=1. In this mode the output voltage will be limited by limiting the DCDC_FB voltage to 1.25V (select the external resistor network to adjust this limitation voltage).

*Figure 5. DC/DC step up 2 converter with regulation of LED string on pin DCDC_CURR1,2 or 3*

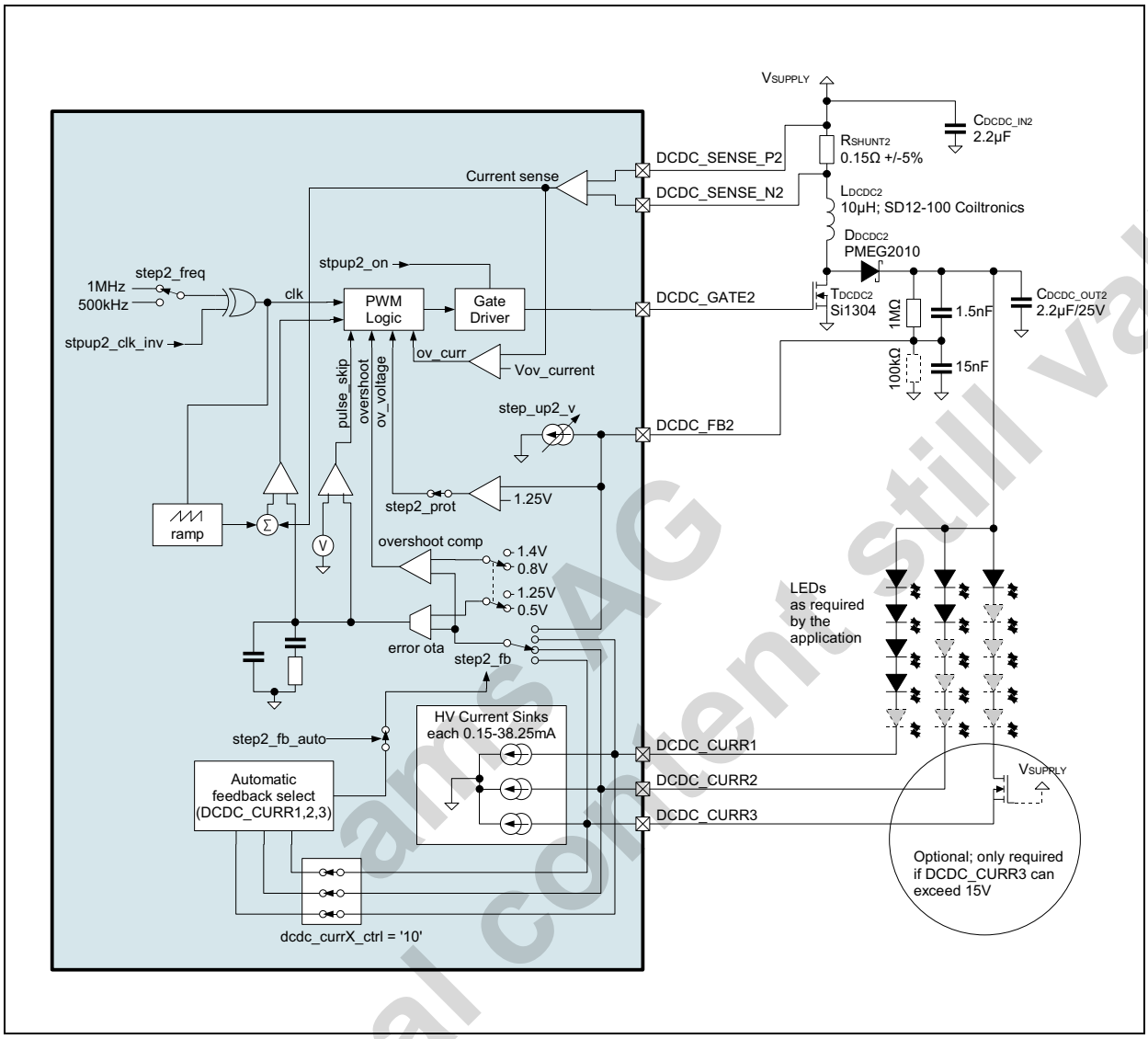
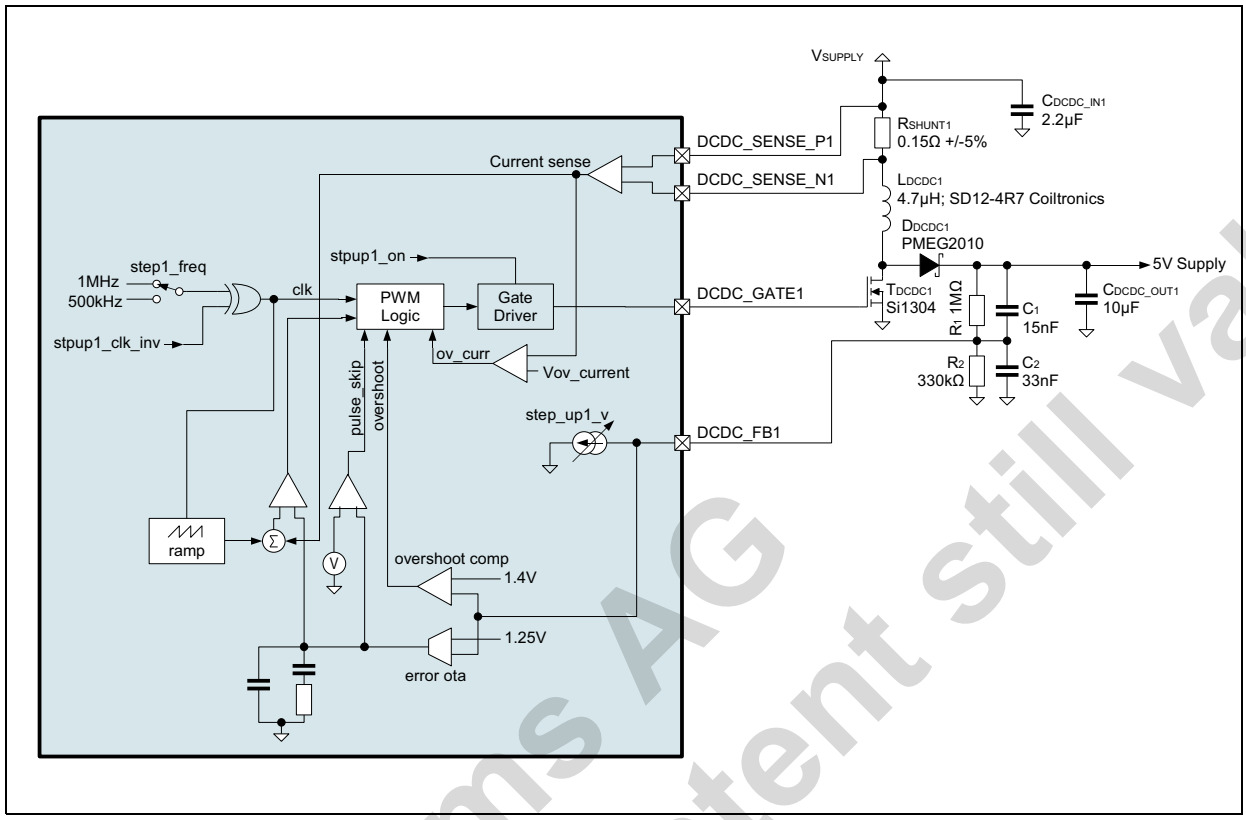


*Figure 6. DC/DC step up 1 converter with regulated output voltage of 5V. Feedback is at pin DCDC_FB1*




Voltage Feedback: (see Figure 6)

For Step UP DCDC 1 voltage feedback is always selected on pin DCDC_FB1. For Step-up UP DCDC 2 set step2_fb to 00 to enable voltage feedback at pin DCDC_FB2.

Bit stepX_res (X = 1 or 2) should be set to 1 in voltage feedback mode using two resistors.

The output voltage is regulated to a constant value, given by:

$$V_{stepup\_out} = \frac{R_1 + R_2}{R_2} 1.25 + I_{I_{DCDC\_FB}} \bullet R_1$$

If R2 is not used, the output voltage is:

$$V_{stepup\_out} = 1.25 + I_{I_{DCDC\_FB}} \bullet R_1$$

$V_{stepup\_out}$: Step up regulator output voltage

$R_1$ Feedback resistor R1

$R_2$ Feedback resistor R2

$I_{Vturning}$: Tuning current on DCDC_FB pin: stpupX_v (0µA to 15µA (1µA steps)) (X= 1 or 2)

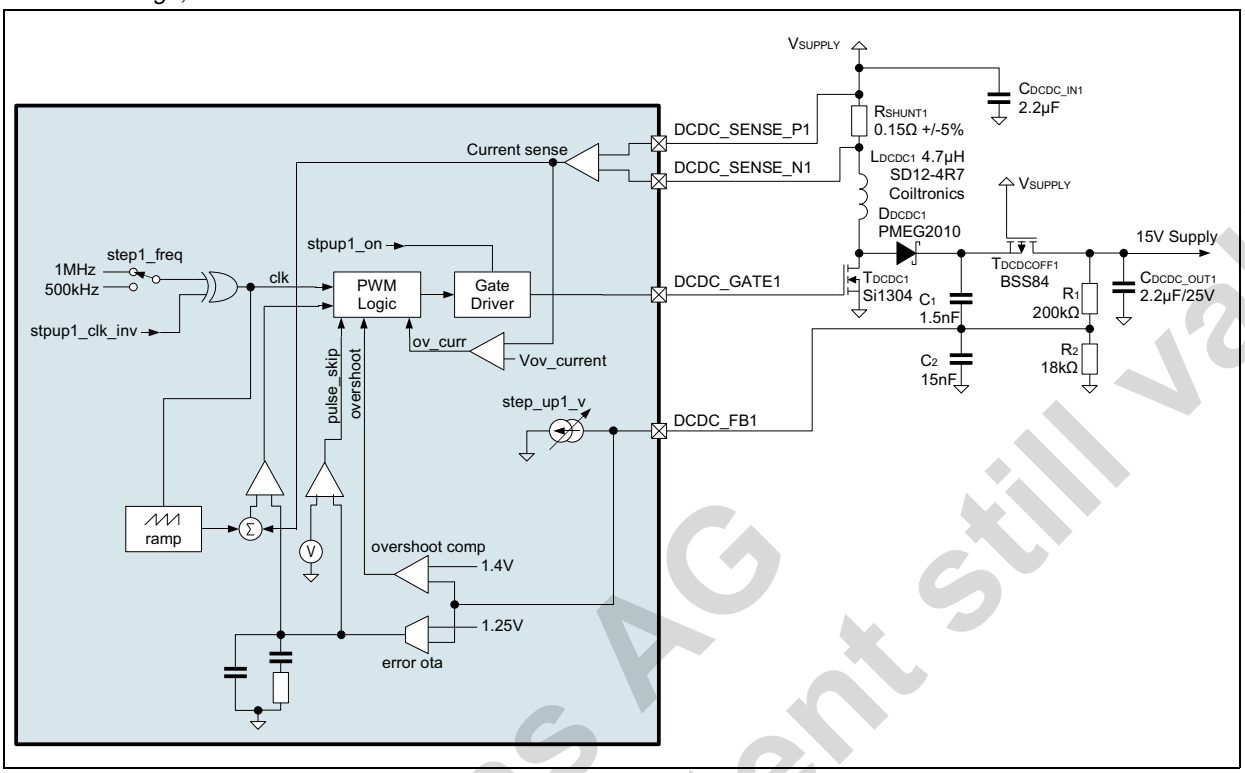
Example:

*Table 6. Step Up Output Voltage (Voltage mode or protection voltage)*

| $I_{vtuning}$ | $V_{stepup\_out}$ | $V_{stepup\_out}$ |
|---|---|---|
| **µA** | **R1=1M Ω,R2 not used** | **R1=500k Ω,R2=64k Ω** |
| 0 | - | 11 |
| 1 | - | 11.5 |
| 2 | - | 12 |
| 3 | - | 12.5 |
| 4 | - | 13 |
| 5 | 6.25 | 13.5 |
| 6 | 7.25 | 14 |
| 7 | 8.25 | 14.5 |
| 8 | 9.25 | 15 |
| 9 | 10.25 | 15.5 |
| 10 | 11.25 | 16 |
| 11 | 12.25 | 16.5 |
| 12 | 13.25 | 17 |
| 13 | 14.25 | 17.5 |
| 14 | 15.25 | 18 |
| 15 | 16.25 | 18.5 |

**Note:** The voltage on pin DCDC_CURR1, DCDC_CURR2 and DCDC_CURR3 must never exceed 15V

*Figure 7. DC/DC step up converter 1 with regulated output voltage (15V), and switch off function of output voltage, to reduce shutdown current*




As the output voltage is always on, an additional output transistor can be added to reduce shutdown current through R1, R2 and the connected output circuit.

**Note:** A similar circuit can be used for step up converter 2.

### 8.1.2 StepUp1 Load Detection and Overcurrent Protection Circuit

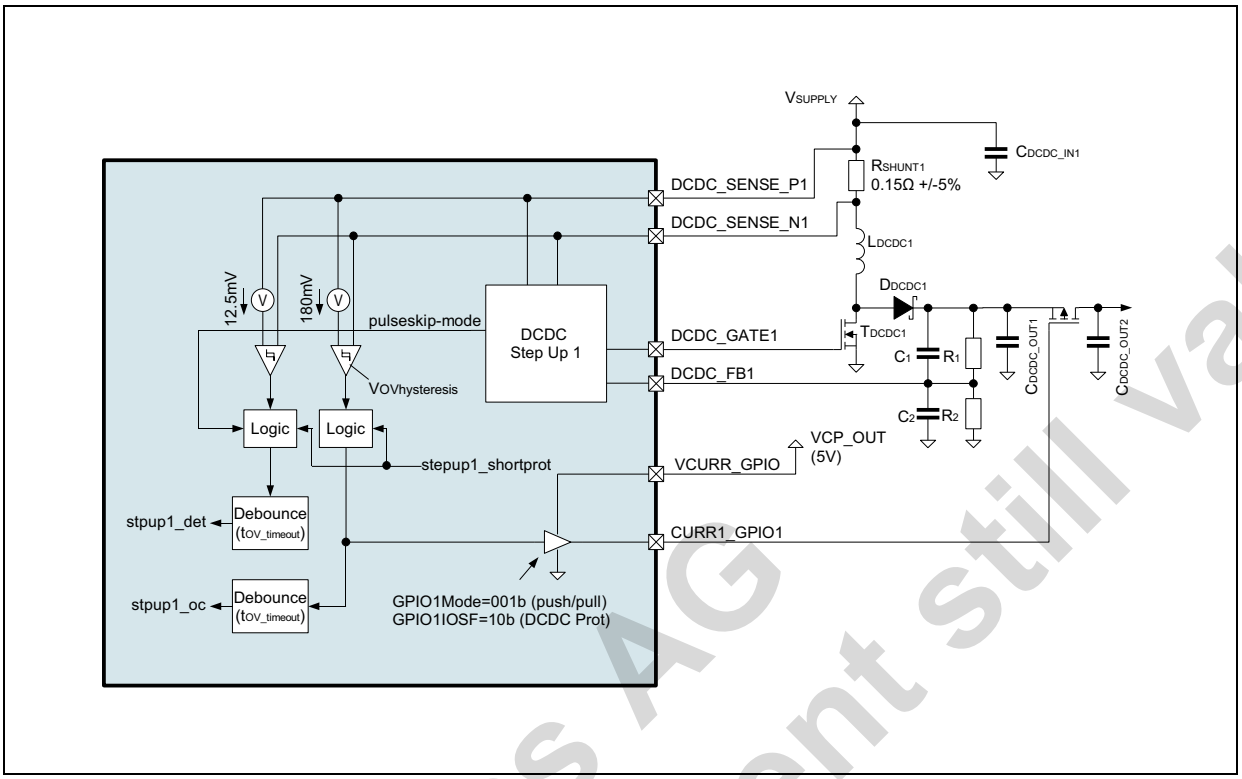
This circuit protects the DCDC step up1 converter during short circuit and startup, by regulation of the output current. An additional feature is the detection of a minimum output load of the Step-up converter. It is also possible to use this circuit without the DCDC step up converter, by using the sense resistor only:

- Detection circuit: If the voltage on $R_{sense}$ exceeds $V_{DETECT}$ for more than 1msecond, or the DCDC Step up converter is not in Pulseskip for more than 1 millisecond, the stepup1_det bit will be set.
- Overcurrent protection: If the Overcurrent voltage $V_{OVCURRENT}$ has been exceeded by more than 5 msec the Bit stpup1_oc will be set and can only reset, by switching off and on the Protection circuit by writing Stpup1_shortprot 0 – 1. If stepup1_oc is set the load will be disconnected, if Stpup1_oc_timeout=1

*Table 7. StepUp1 protection/detection circuit parameters*

| Symbol | Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| VDETECT | Detection Threshold | 2 | 12.5 | 25 | mV | For Rsense=0.150Ω => 83mA typ. |
| VOVCURRENT | Overcurrent Threshold rising | 150 | 180 | 215 | mV | For Rsense=0.150Ω => 1.2A typ. |
| VOVhysteresis | Overcurrent Hysteresis | | 50 | | mV | |
| tOV_timeout | Overcurrent timeout | | 5 | | ms | Interrupt and/or external PMOS switching off after timeout $f_{clk\_int}$ = 2.2MHz |
| tdetect | Detection denounce time | | 1 | | ms | $f_{clk\_int}$ = 2.2MHz |

*Figure 8. StepUp 1 Load Detection and Overcurrent Protection Application Circuit*



### 8.1.3 Step Up DCDC Converter Registers

*Table 8. Step Up DC/DC Bit definitions*

| Addr: 30 | | Step Up DC/DC control | | |
|---|---|---|---|---|
| | | This register controls the different modes of the step up DCDC converter | | |
| **Bit** | **Bit Name** | **Default** | **Access** | **Description** |
| 5 | stpup1_on | ROM | R/W | On/Off control of the step up dc/dc converter1 |
| 6 | stpup2_on | ROM | R/W | On/Off control of the step up dc/dc converter2 |

*Table 9. Step Up DC/DC Bit definitions*

| Addr: 32 | | Step Up DC/DC control | | | |
|---|---|---|---|---|---|
| | | This register controls the different modes of the step up DCDC converter | | | |
| **Bit** | **Bit Name** | **Default** | **Access** | **Description** | |
| 0 | stpup2_clkinv | 00h | R/W | Invert input clock of step up2 converter | |
| | | | | 0 | Use positive edge of internal clk |
| | | | | 1 | Use negative edge of internal clk |
| 1 | stpup1_freq | 00h | R/W | Defines the clock frequency of the step up1 dc/dc converter;<br>0$f_{clk_int}$/2 (0.8 to 1.15 MHz)<br>1$f_{clk_int}$/4 (0.4 to 0.575 MHz) | |
| 2 | - | 00h | n/a | Always set to 0 | |
| 3 | stpup1_res | 00h | R/W | Gain selection for DCDC step_up1: | |
| | | | | 0 | Select 0 if DCDC is used with current feedback (DCDC_CURR1,DCDC_CURR2,DCDC_CURR3) or if DCDC_FB is used with current feedback only (Only R1,C1 connected; (see Figure 6)) |
| | | | | 1 | Select 1 if DCDC_FB1 or DCDC_FB2 is used with external resistor divider (2 resistors) |
| 4 | stpup2_fb_auto | 00h | RW | 0 | step_up_fb select the feedback of the DCDC converter |
| | | | | 1 | The feedback is automatically chosen within the current sinks DCDC_CURR1,DCDC_ CURR2 and DCDC_CURR3 (never DCDC_FB). Only those are used for this selection, which are enabled and connected to the step up converter (currX_ctrl must be 10) |
| 5 | stpup2_freq | 00h | R/W | Defines the clock frequency of the step up2 dc/dc converter | |
| | | | | 0 | $f_{clk\_int}$/2 (0.8 to 1.15 MHz) |
| | | | | 1 | $f_{clk\_int}$/4 (0.4 to 0.575 MHz) |
| 6 | - | 00h | n/a | | Always set to 0 |
| 7 | stpup2_res | 00h | R/W | Gain selection for DCDC step_up2: | |
| | | | | 0 | Select 0 if DCDC is used with current feedback (DCDC_CURR1,DCDC_CURR2,DCDC_CURR3) or if DCDC_FB is used with current feedback only (Only R1,C1 connected; (see Figure 6)) |
| | | | | 1 | Select 1 if DCDC_FB1 or DCDC_FB2 is used with external resistor divider (2 resistors) |

*Table 10. Step Up DC/DC Bit definitions*

| Addr: 33 | | Step Up1 DC/DC control<br>This register controls the different modes of the step up1 DCDC converter | | | |
|---|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Description** | |
| 4:0 | stpup1_v | 00h | R/W | Defines the tuning current at DCDC_fb1 pin; | |
| | | | | 00000 | 0 µA |
| | | | | 00001 | 1 µA |
| | | | | ..... | |
| | | | | 11111 | 31 µA |
| 5 | stpup1_clkinv | 00h | R/W | Invert input clock of step up1 converter; | |
| | | | | 0 | Use positive edge of internal clk |
| | | | | 1 | Use negative edge of internal clk |
| 6 | stpup1_shortprot | 00h | RW | Enables Protection and Detection circuit for DCDC step up1 | |
| | | | | 0 | No protection and load detection |
| | | | | 1 | Short protection and load detection enabled |
| 7 | stpup1_oc_timeout | 00h | RW | Controls GPIO1 switch off, after overcurrent timeout (5ms) for DCDC step up1 | |
| | | | | 0 | disabled |
| | | | | 1 | enabled |

*Table 11. Step Up DC/DC Bit definitions*

| Addr: 34 | | Step Up2 DC/DC control<br>This register controls the different modes of the step up2 DCDC converter | | | |
|---|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Description** | |
| 4:0 | stpup2_v | 00h | R/W | Defines the tuning current at DCDC_fb2 pin; | |
| | | | | 00000 | 0 µA |
| | | | | 00001 | 1 µA |
| | | | | ..... | |
| | | | | 11111 | 31 µA |
| 6:5 | stpup2_fb | 00h | R/W | Controls the feedback source | |
| | | | | 00 | DCDC_FB enabled (external resistor divider) |
| | | | | 01 | DCDC_CURR1 feedback enabled (feedback through white LEDs) |
| | | | | 10 | DCDC_CURR2 feedback enabled (feedback through white LEDs) |
| | | | | 11 | DCDC_CURR3 feedback enabled (feedback through white LEDs) |