Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AS3661

Programmable 9-channel LED Driver

1 General Description

The AS3661 is a 9-channel LED driver designed to produce lighting effects for mobile devices. A high-efficiency charge pump enables LED driving over full Li-Ion battery voltage range. The device is equipped with an internal program memory, which allows operation without processor control. The AS3661 maintains excellent efficiency over a wide operating range by autonomously selecting the best charge pump gain based on LED forward voltage requirements. AS3661 is able to automatically enter power-save mode when LED outputs are not active, thus lowering idle current consumption down to 10 µA (typ).

The AS3661 has an I2C-compatible control interface with four pin selectable addresses. Also, the device has a flexible General Purpose Output (GPO), which can be used as a digital control pin for other devices. INT pin can be used to notify processor when a lighting sequence has ended (interrupt - function). Also, the device has a trigger input interface, which allows synchronization between multiple devices.The device requires only four small and low-cost ceramic capacitors.

The AS3661 is available in a tiny WL-CSP-25 (2.285x2.285mm) 0.4mm pitch package.

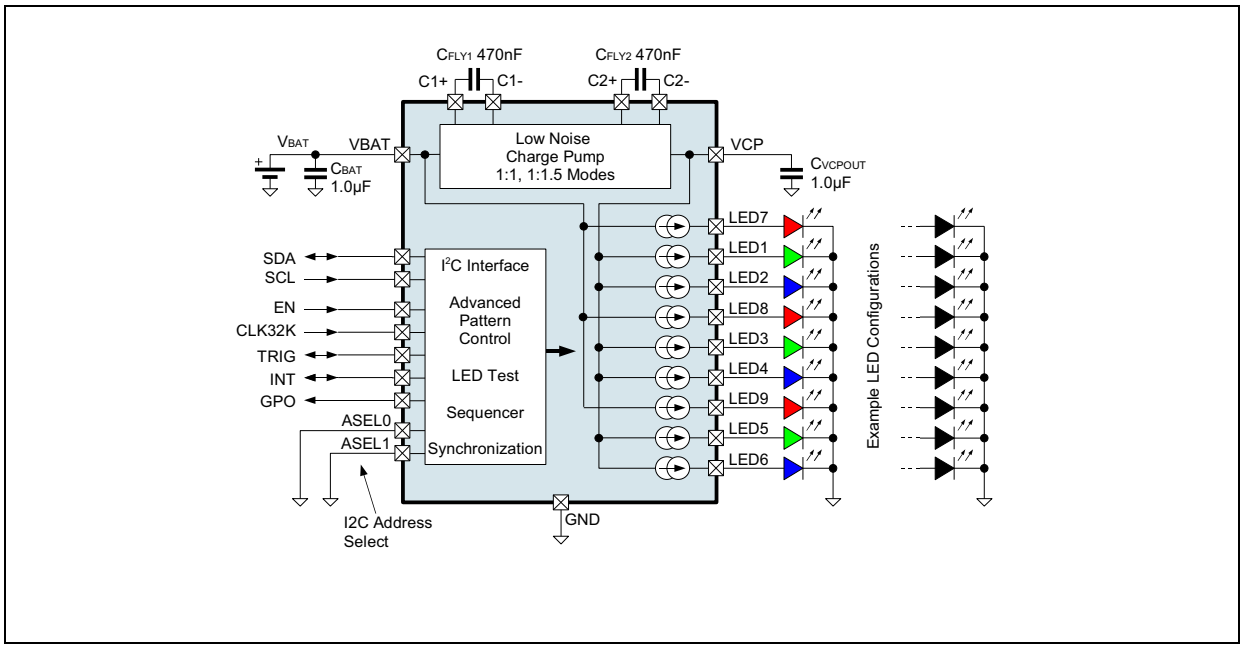
2 Key Features

- Three independent program execution engines; 9 programmable outputs with 25.5 mA full-scale current, 8- bit current setting resolution and 12-bit PWM control resolution
- Adaptive charge pump with 1x and 1.5x gain provides up to 95% LED drive efficiency
- Charge pump with soft start and overcurrent/short circuit protection
- Built-in LED test
- Automatic power save mode; IVDD = 10 µA (typ.)
- Two wire, I2C-compatible, control interface
- Flexible instruction set
- Large SRAM program memory
- Small application circuit
- Source (high side) drivers
- Minimum number of external components
- Architecture supports color control

3 Applications

The product is ideal for fun and indicator lights, LED backlighting, and programmable current source.

Figure 1. AS3661 LED Driver Block Diagram

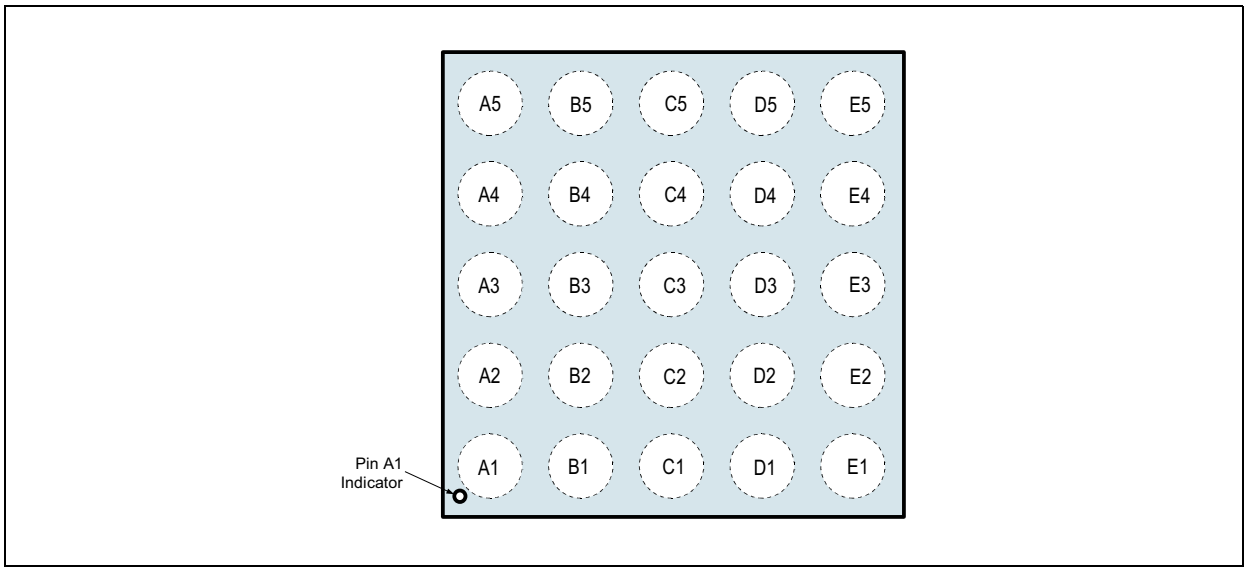


Contents

4 Pinout

4.1 Pin Assignment

Figure 2. Pin Assignments (Top View)



4.2 Pin Description

Table 1. Pin Description for AS3661

Pin Number	Pin Name	Description
A1	LED1	**LED1 Output**. Current source from VCP.
A2	LED2	**LED2 Output**. Current source from VCP.
A3	VCP	**Charge Pump output.** make a short connection to capacitor CVCPOUT.
A4	C2-	**Charge Pump flying capacitor 2.** make a short connection to capacitor CFLY2.
A5	C2+	**Charge Pump flying capacitor 2.** make a short connection to capacitor CFLY2.
B1	LED3	**LED3 Output**. Current source from VCP.
B2	LED4	**LED4 Output**. Current source from VCP.
B3	ASEL1	**Digital input - I²C address select**
B4	C1-	**Charge Pump flying capacitor 1.** make a short connection to capacitor CFLY1.
B5	C1+	**Charge Pump flying capacitor 1.** make a short connection to capacitor CFLY1.
C1	LED5	**LED5 Output**. Current source from VCP.
C2	LED6	**LED6 Output**. Current source from VCP.
C3	ASEL0	**Digital input - I²C address select**
C4	EN	**Enable.** Active high digital input.
C5	VBAT	**Positive Power Supply Input**
D1	LED7	**LED7 Output**. Current source from VBAT.
D2	LED8	**LED8 Output**. Current source from VBAT.
D3	INT	**Interrupt Output.** Open drain digital output for microcontroller unit, leave unconnected if not used.
D4	CLK32K	**Digital Clock Input.** Connect a 32kHz signal; if this signal is not available, connect this pin to GND.

Table 1. Pin Description for AS3661

Pin Number	Pin Name	Description
D5	GND	**Ground**
E1	LED9	**LED9 Output**. Current source from VBAT.
E2	GPO	**General Purpose Output.** Leave unconnected if not used.
E3	TRIG	**Trigger Input.** Open drain, connect to ground if not used.
E4	SDA	**Serial-Data I/O**. Open drain digital I/O I²C data pin.
E5	SCL	**Serial-Clock Input**

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3. Electrical Characteristics on page 8 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VBAT, VCP, C1+, C1-, C2+, C2- to GND	-0.3	+7.0	V	
VCP to VBAT	-0.3		V	Diode between VCP and VBAT
LED1, LED2....LED9 to GND	-0.3	+7.0	V	
SDA, SCL, EN, CLK32K, TRIG, INT, GPO, ASEL0, ASEL1 to GND	-0.3	+7.0	V	
Electrostatic Discharge				
ESD HBM (LED1 to LED2)	8		kV	JEDEC JESD22-A114
ESD HBM (all other pins)	2.5		kV	
ESD MM	250		V	JEDEC JESD22-A115
ESD CDM	1		kV	JEDEC JESD22-C101
Temperature Ranges and Storage Conditions				
Continous Power Dissipation				Internally limited (overtemperature protection)[1]
Junction Temperature (T_{JMAX})		+125	ºC	
Storage Temperature Range	-55	+125	ºC	
Body Temperature during Soldering		+260	ºC	IPC/JEDEC J-STD-020
Junction to Ambient Thermal Resistance (θ_{JA})[2]		87	ºC/W	
Moisture Sensitive Level	1			Represents a max. floor life time of *unlimited*
Recommended Operating Conditions				
Recommended charge pump load current	0	100	mA	

1. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150ºC (typ.) and disengages at T_J = 130ºC (typ.).
2. Junction to ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

6 Electrical Characteristics

V_{BAT} = 3.6V, V_{EN} = 1.65V, C_{BAT} = C_{VCPOUT} = 1.0µF, C_{FLY1-2} = 0.47µF, T_{AMB} = -30ºC to +85ºC, typical values @ T_{AMB} = +25ºC (unless otherwise specified)[1].

Table 3. Electrical Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
General Operating Conditions							
V_{BAT}	Supply Voltage			2.7		5.5	V
I_{VBAT}	Standby supply current	EN = 0V or CHIP_EN=0 (bit), external 32 kHz clock running or not running			1.4	4	µA
	Normal Mode supply current	External 32 kHz clock running, charge pump and current source outputs disabled			0.16	0.22	mA
		Charge pump in 1x mode, no load, current source outputs disabled			0.16	0.22	mA
		Charge pump in 1.5x mode, no load, current source outputs disabled			1.4		mA
	Power Save Mode supply current	External 32 kHz clock running			3.1	5	µA
		Internal oscillator running			0.16	0.23	mA
f_{OSC}	Internal Oscillator Frequency Accuracy	T_{AMB} = +25ºC		-4		+4	%
				-7		+7	
T_{AMB}	Operating Temperature[1]			-30	25	85	℃
Charge Pump							
R_{OUT}	Charge Pump Output Resistance	Gain = 1.5 and V_{BAT} = 2.9V			6		Ω
		Gain = 1 and V_{BAT} = 2.9V			1		
		Gain = 1.5 and V_{BAT} = 3.6V			1.4		
		Gain = 1 and V_{BAT} = 3.6V			1		
f_{SW}	Switching Frequency			1.2	1.25	1.3	MHz
I_{GND}	Ground current	Gain = 1.5			1.2		mA
		Gain = 1			1		µA
t_{ON}	V_{CP} Turn-On Time[2]	V_{BAT} = 3.6V, I_{OUT} = 60 mA			100		µs
I_{LOAD}	Charge Pump load current	Recommended charge pump load current		0		100	mA
LED Driver							
I_{LEAK}	Leakage Current (LED1 to LED9)	PWM = 0%			0.1	1	µA
I_{MAX}	Maximum Source Current	Outputs LED1 to LED9			25.5		mA
I_{OUT}	Output Current[3] Accuracy	Output Current set to 17.5 mA	T_{AMB} = +25ºC	-2.5%		+2.5%	%
				-5		+5	
I_{MATCH}	Matching	Output Current set to 17.5 mA			1	2.5	%
f_{LED}	LED Switching Frequency				312		Hz
V_{SAT}	Saturation Voltage[4]	Output Current set to 17.5 mA			45	100	mV
LED Test							

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
LSB	Least Significant Bit			30		mV
EABS	Total Unadjusted Error[5]	VIN_TEST = 0V to VBAT		<±3	±4	LSB
tCONV	Conversion Time			2.7		ms
VIN_TEST	DC Voltage Range		0		5	V
Logic Interface						
Logic Input EN						
VIL	Input Low Level				0.5	V
VIH	Input High Level		1.2			V
IIN	Input Current		-1.0		1.0	µA
tDELAY	Input Delay[6]			2		µs
Logic Input SCL, SDA, TRIG, CLK32K, ASEL0, ASEL1						
VIL	Input Low Level				0.2x VEN	V
VIH	Input High Level		0.8x VEN			V
IIN	Input Current		-1.0		1.0	µA
Logic Output SDA, TRIG, INT						
VOL	Output Low Level	IOUT = 3 mA (pull-up current)		0.3	0.5	V
IL	Output Leakage Current	VCP = 2.8V			1.0	µA
Logic Output GPO						
VOL	Output Low Level	IOUT = 3 mA		0.3	0.5	V
VOH	Output High Level	IOUT = -2 mA	VBAT - 0.5	VBAT - 0.3		V
IL	Output Leakage Current	VCP = 2.8V			1.0	µA
Logic Input CLK32K						
fCLK	Clock Frequency			32.7		kHz
fCLKH	High Time		6			µs
fCLKL	Low Time		6			µs
tR	Clock Rise Time	10 to 90%			2	µs
tF	Clock Fall Time	90 to 10%			2	µs

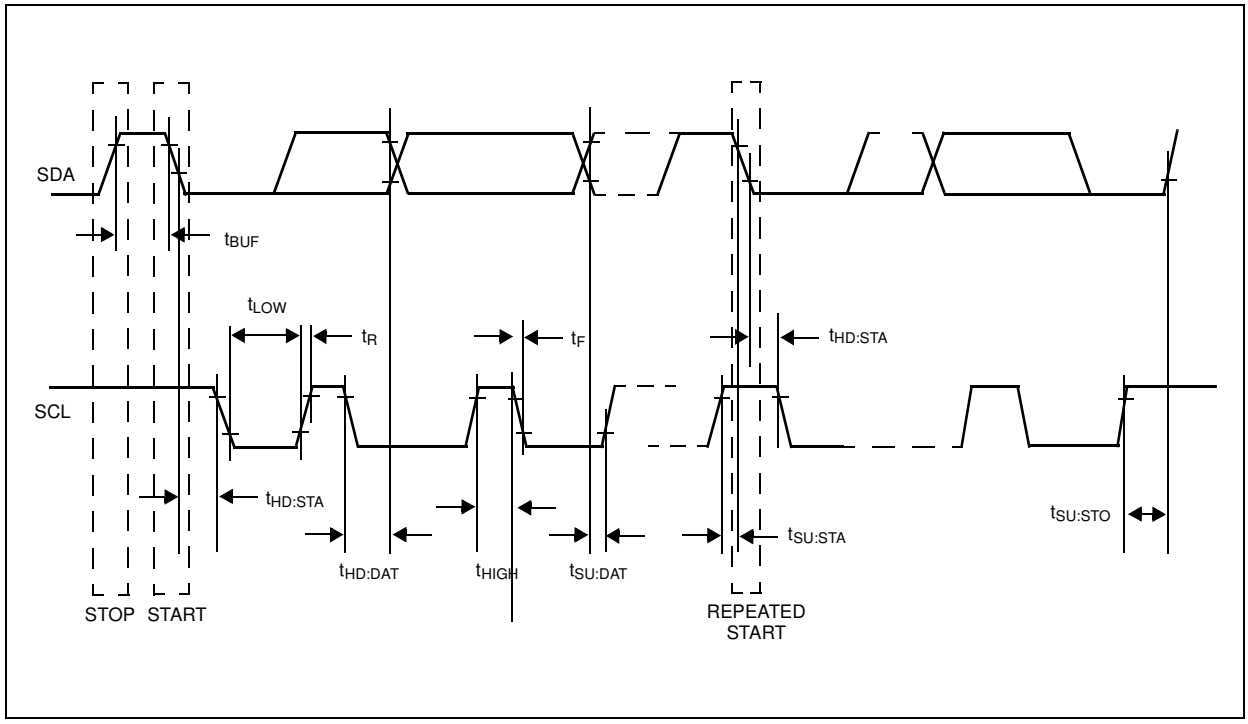
1. In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{Amb-MAX}$) is dependent on the maximum operating junction temperature (T_{J-MAX} =125°C), the maximum power dissipation of the devi ce in the application (P_{D-MAX}) and the junction to ambient thermal resistance of the part/package in the application (θ_{JA}) as given by the following equation: $T_{Amb-MAX} = T_{J-MAX} - (\theta_{JA} * P_{D-MAX})$.
2. Turn-on time is measured from the moment the charge pump is activated until the V_{CP} crosses 90% of its target value

1. Low-ESR Surface-Mount Ceramic Capacitors 8MLCCs) used in setting electrical characteristics.

3. Output current accuracy is the difference between actual value of the output current and programmed value of this current. IMATCH is determined as follows:

   For the constant current D1 to D9, the following are determined: The maximum current (max) and the minimum current (min), then the IMATCH is calculated with: IMATCH = 100*(((max-min)/2)+((max+min)/2))/((max+min)/2)-100
4. Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at V_{CP} - 1V.
5. Total unadjusted error includes offset, full-scale and linearity errors.
6. The I2C host should allow at least 500µs before sending data the AS3661after the rising edge of the enable line.

Figure 3. I^2C mode Timing Diagram



.

Table 4. Electrical Characteristics I^2C[1]

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I^2C mode timings - see Figure 3 on page 10						
f_{SCLK}	SCL Clock Frequency		0		400	kHz
t_{BUF}	Bus Free Time Between a STOP and START Condition		1.3			µs
$t_{HD:STA}$	Hold Time (Repeated) START Condition[2]		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs

Table 4. Electrical Characteristics (Continued)I²C[1]

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{SU:STA}$	Setup Time for a Repeated START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time[3]		50			ns
$t_{SU:DAT}$	Data Setup Time[4]		100			ns
t_R	Rise Time of Both SDA and SCL Signals		20 + 0.1C_B		300	ns
t_F	Fall Time of Both SDA and SCL Signals		15+ 0.1C_B		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	Load of one Picofarad corresponds to one nanosecond.	10		200	ns
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

1. Specification is guaranteed by design and is not tested in production. V_{EN} = 1.65V to V_{BAT}.
2. After this period the first clock pulse is generated.
3. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
4. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ = to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max + $t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

7 Typical Operating Characteristics

V_{BAT} = 3.6V, V_{EN} = 1.65V, C_{BAT} = C_{VCPOUT} = 1.0µF, C_{FLY1-2} = 0.47µF, T_{AMB} = +25ºC, unless otherwise specified

Figure 4. Charge Pump 1.5 x Efficiency vs. Load

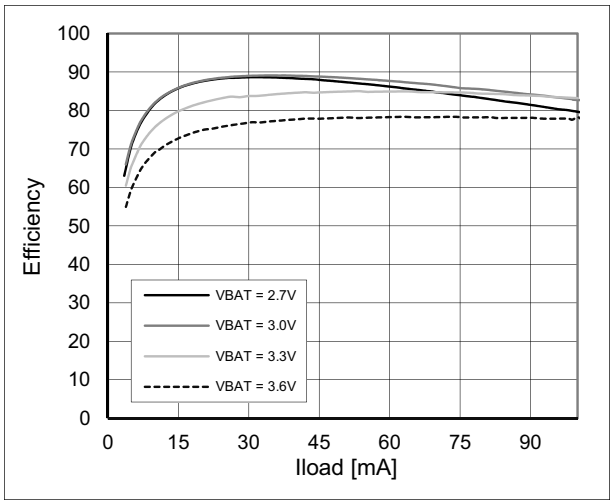


Figure 5. Output Voltage vs. Load Current (1.5 x CP)

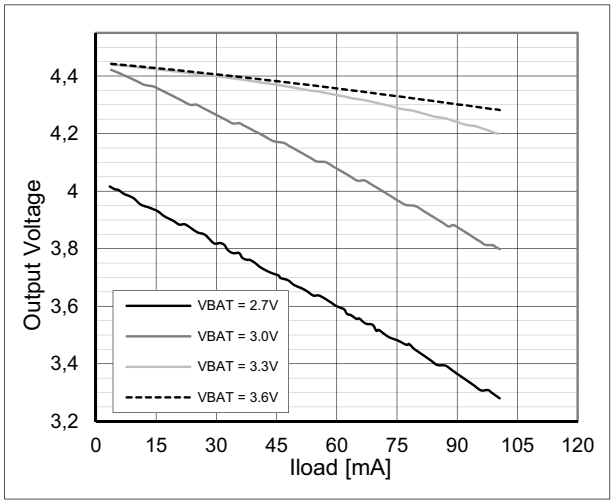


Figure 6. Gain Change Hysteresis Loop (6x1mA load)

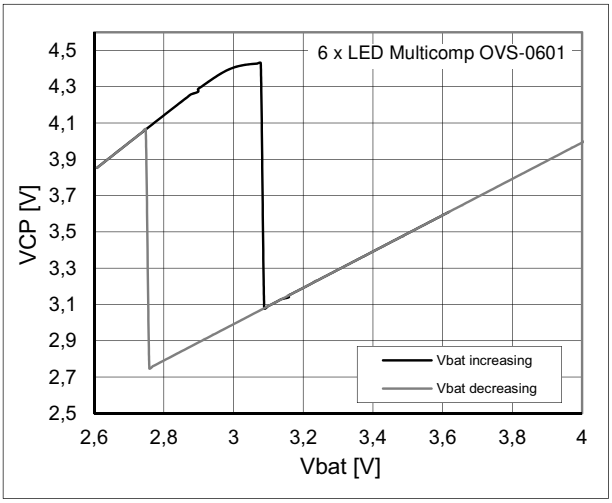


Figure 7. Effect of adap. hyst. on width of hyst. loop

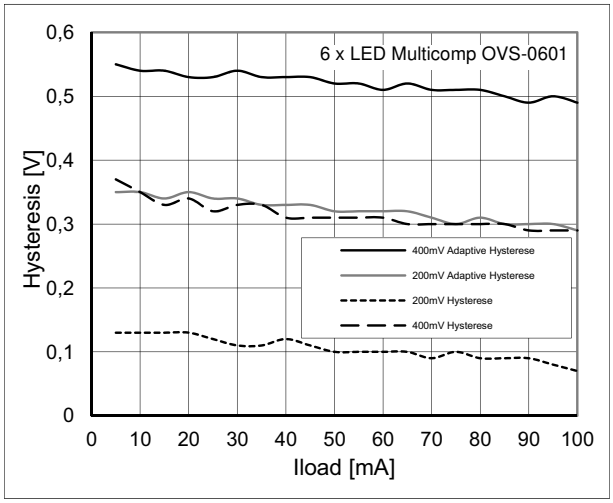


Figure 8. LED Current matching distribution @17.5mA

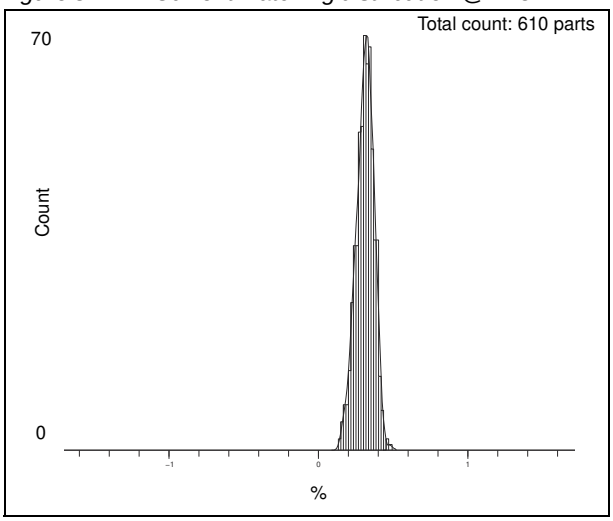


Figure 9. LED current Accuracy distribution @17.5mA

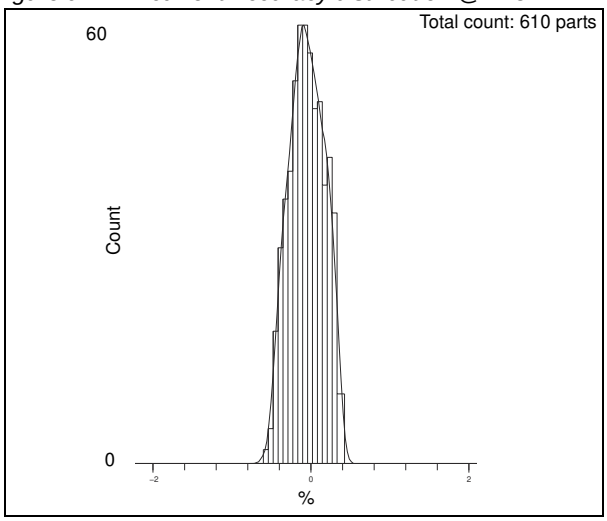


Figure 10. Power Save Mode Supply Current vs. VBAT, Charge Pump in 1x mode

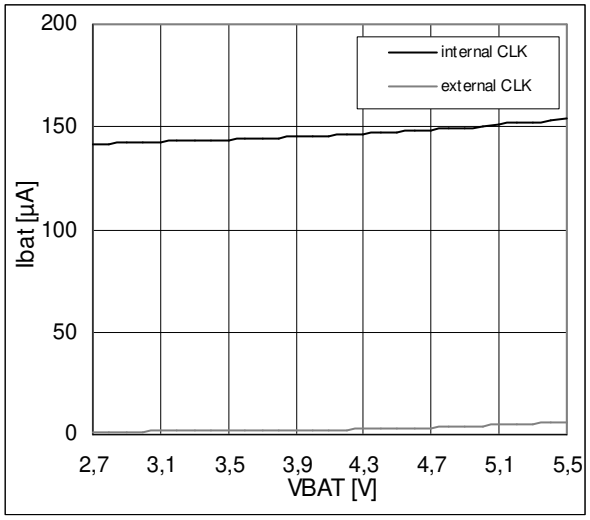


Figure 11. Serial Bus Write and Charge Pump Start-up, I_{LOAD} = 60mA

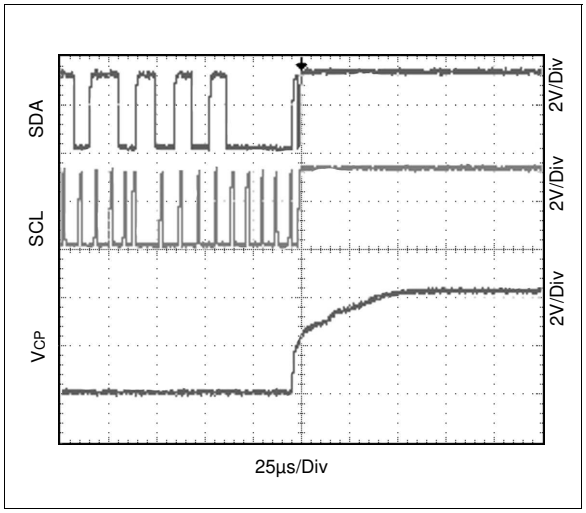


Figure 12. Line Trans. and Charge Pump autom. Gain Change 1.5 to 1, 6LEDs@1mA 100% PWM

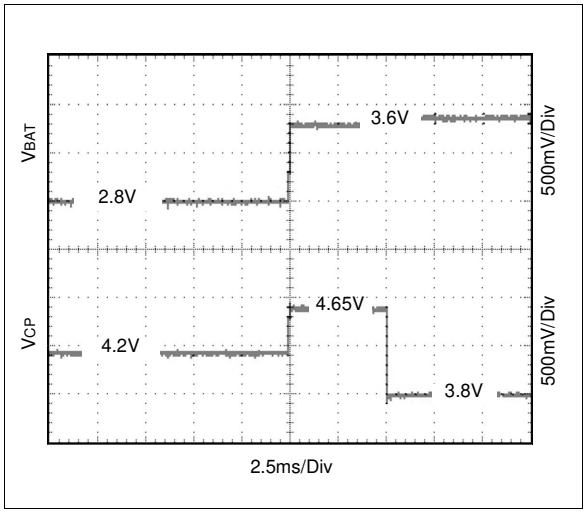


Figure 13. Line Trans. and Charge Pump autom. Gain Change 1 to 1.5, 6LEDs@1mA 100% PWM

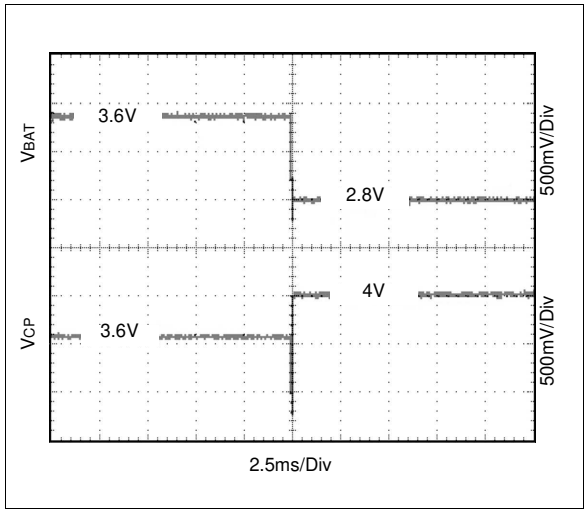


Figure 14. 100% PWM RGB LED Efficiency vs. VBAT

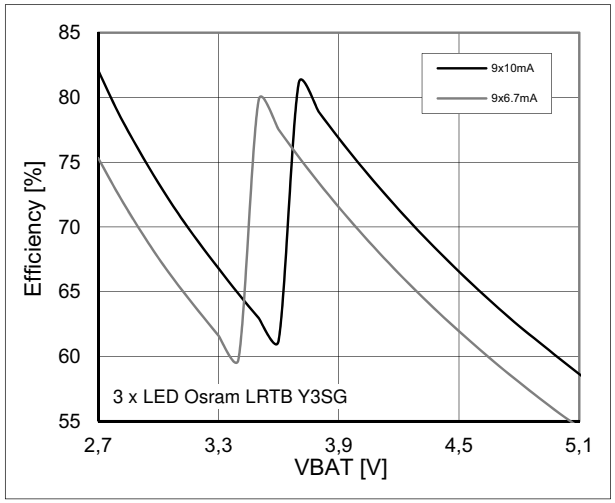
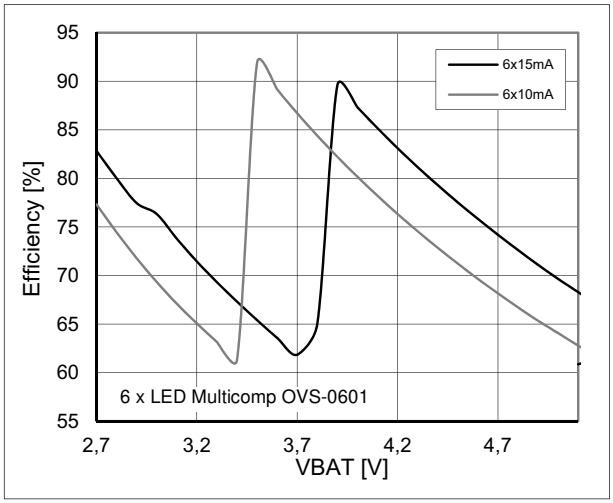


Figure 15. 100% PWM WLED Efficiency vs. VBAT



8 Detailed Description

The AS3661 is a fully integrated lighting management unit for producing lighting effects for mobile devices. The AS3661 includes all necessary power management, high-side current sources, temperature compensation, two wire control interface and programmable pattern generators. The overall maximum current for each driver is set by an 8-bit register. The AS3661 controls LED luminance with a pulse width modulation (PWM) scheme with a resolution of 12 bits. The temperature compensation is also done by a PWM.

8.1 Programming

The AS3661 provides flexibility and programmability for dimming and sequencing control. Each LED can be controlled directly and independently through the serial bus or LED drivers can be grouped together for pre-programmed flashing patterns. The AS3661 has three independent program execution engines, so it is possible to form three independently programmable LED banks. LED drivers can be grouped based on their function so that, for example, the first bank of drivers can be assigned to the keypad illumination, the second bank to the “funlights” and the third group to the indicator LED(s). Each bank can contain 1 to 9 LED driver outputs. Instructions for program execution engines are stored in the program memory. The total amount of the program memory is 96 instructions and the user can allocate the memory as required by the engines.

8.2 LED Error Detection

AS3661 has a built-in LED error detection. Error detection does not only detect open and short circuit, but provides an opportunity to measure the V_F’s of the LEDs. The test event is activated by a serial interface write and the result can be read through the serial interface during the next cycle. This feature can also be addressed to measure the voltage on VBAT, VCP and INT pins. Typical example usage includes monitoring battery voltage or using INT pin as a light sensor interface.

8.3 Energy Efficiency

When charge pump automatic mode selection is enabled, the AS3661 monitors the voltage over the drivers of LED1 to LED6 so that the device can select the best charge pump gain and maintain good efficiency over the whole operating voltage range. The red LED element of an RGB LED typically has a forward voltage of about 2V. For that reason, the outputs LED7, LED8 and LED9 are internally powered by VBAT, since battery voltage is high enough to drive red LEDs over the whole operating voltage range. This allows to drive three RGB LEDs with good efficiency because the red LEDs doesn't load the charge pump. AS3661 is able to automatically enter power-save mode, when LED outputs are not active and thus lowering idle current consumption down to 10 µA (typ.). During the “downtime” of the PWM cycle (constant current output status is low) additional power savings can be achieved when the PWM power save feature is enabled.

8.4 Temperature Compensation

The luminance of an LED is typically a function of its temperature even though the current flowing through the LED remains constant. Since luminance is temperature dependent, many LED applications require some form of temperature compensation to decrease luminance and color purity variations due to temperature changes. The AS3661 has a build in temperature sensing element and PWM duty cycle of the LED drivers changes linearly in relationship to changes in temperature. User can select the slope of the graph (31 slopes) based on the LED characteristics. This compensation can be done either constantly, or only right after when the device wakes up from power save mode, to avoid error due to self-heating of the device. Linear compensation is considered to be practical and accurate enough for most LED applications. Compensation is effective over the temperature range from -40°C to +90°C.

Figure 16. Temperature Compensation Principle

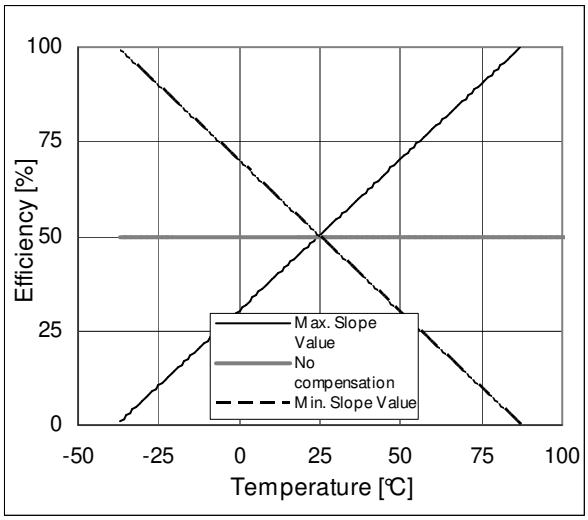
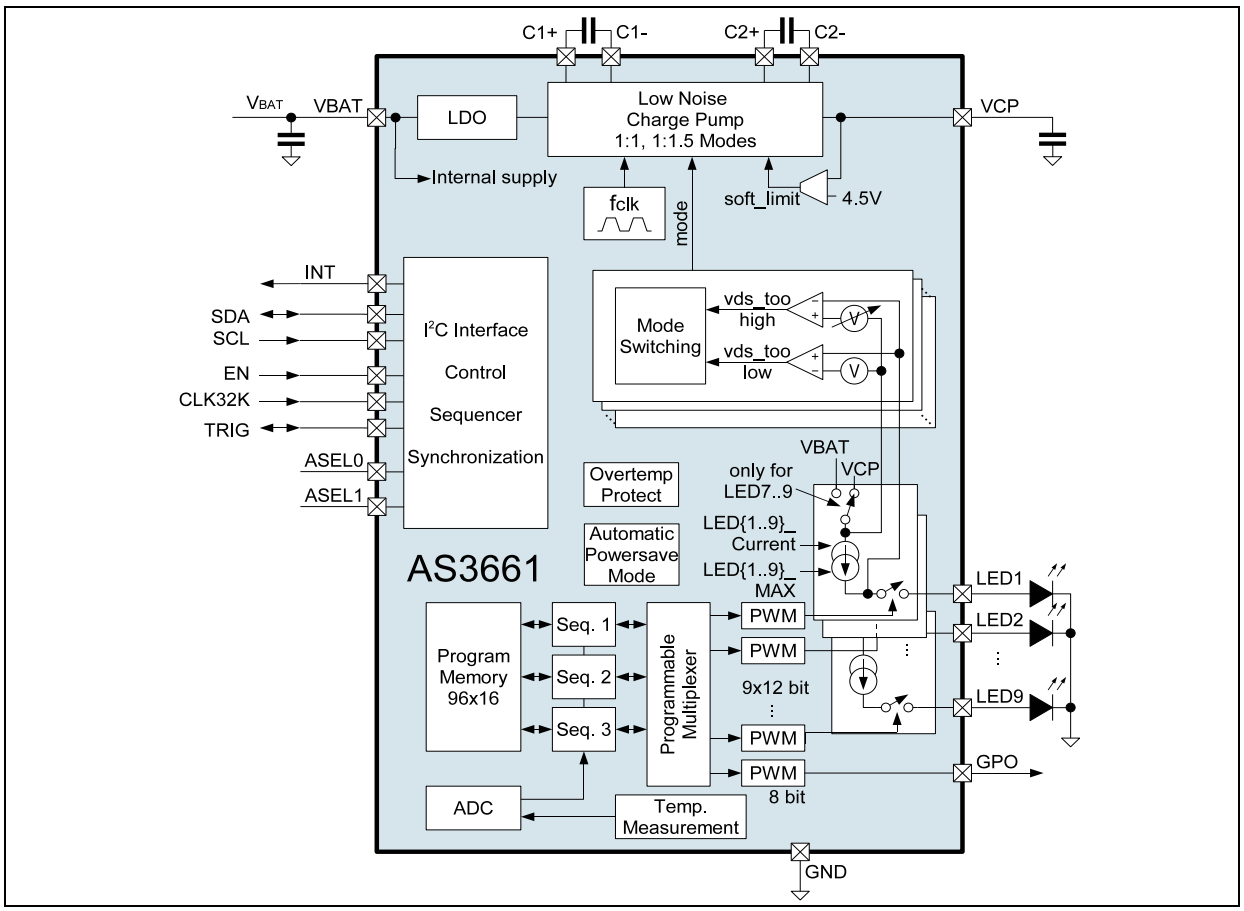


Figure 17. AS3661 - Block Diagram



8.5 Modes of Operation

The following are the different modes of operation of AS3661

8.5.1 RESET

In the RESET mode all the internal registers are reset to the default values. Reset is entered always if Reset Register (3DH) is written FFH or internal Power On Reset is active. Power On Reset (POR) will activate during the chip startup or when the supply voltage VBAT fall below 1.5V (typ.). Once VBAT rises above 1.5V (typ.) POR will be inactivate and the chip will continue to the STANDBY mode. CHIP_EN control bit is low after POR by default.

8.5.2 STANDBY

The STANDBY mode is entered if the register bit CHIP_EN or EN pin is logic low and Reset is not active. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode if EN pin is logic high so that the control bits will be effective right after the start up.

8.5.3 STARTUP

When CHIP_EN bit is written high and the EN pin is high, the INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks (VREF, Bias, Oscillator etc.). Startup delay is 500 µs. If the chip temperature rises too high, the Thermal Shutdown (TSD) disables the chip operation and chip waits in STARTUP mode until no thermal shutdown event is present.

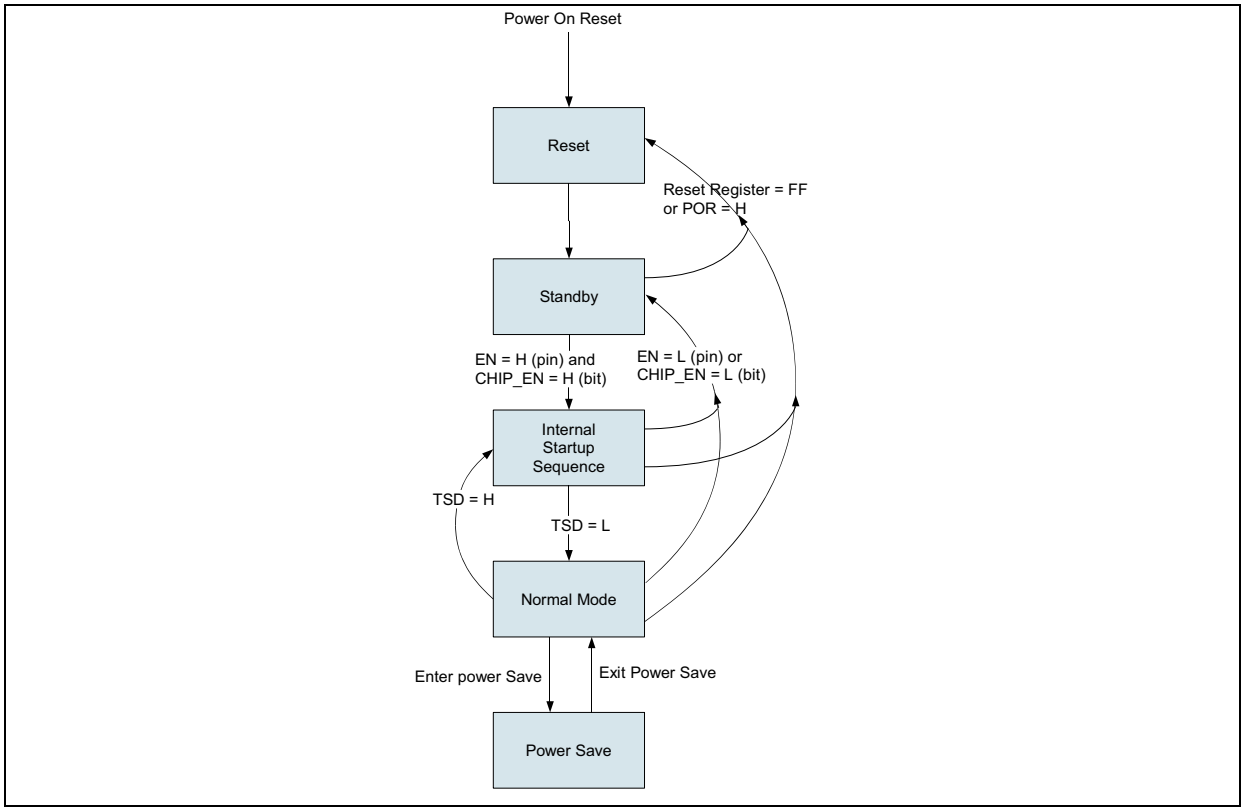
8.5.4 NORMAL

During NORMAL mode the user controls the chip using the Control Registers.

8.5.5 POWER SAVE

In POWER SAVE mode analog blocks are disabled to minimize power consumption. (see Automatic Power Save Mode on page 19)

Figure 18. Mode Select

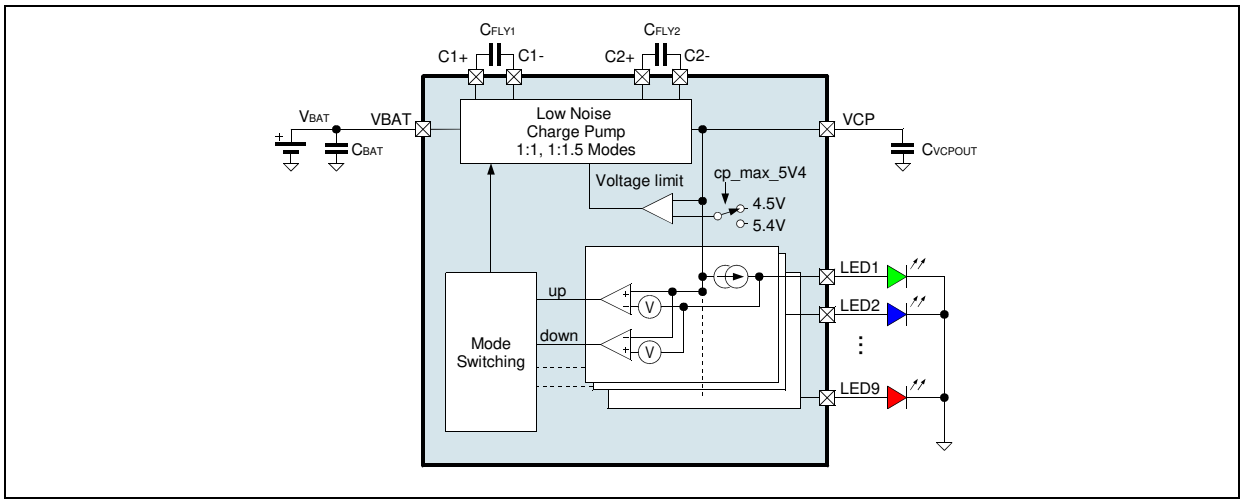


8.6 Charge Pump Operational Description

8.6.1 Overview

The AS3661 includes a pre-regulated switched-capacitor charge pump with a programmable voltage multiplication of 1 and 1.5x. In 1.5x mode by combining the principles of a switched-capacitor charge pump and a linear regulator, it generates a regulated 4.5V output from Li-Ion input voltage range. A two-phase non-overlapping clock generated internally controls the operation of the charge pump. During the charge phase, both flying capacitors (C_{FLY1} and C_{FLY2}) are charged from input voltage. In the pump phase that follows, the flying capacitors are discharged to output. A traditional switched capacitor charge pump operating in this manner will use switches with very low on-resistance, ideally 0Ω, to generate an output voltage that is 1.5x the input voltage. The AS3661 regulates the output voltage by controlling the resistance of the input-connected pass-transistor switches in the charge pump.

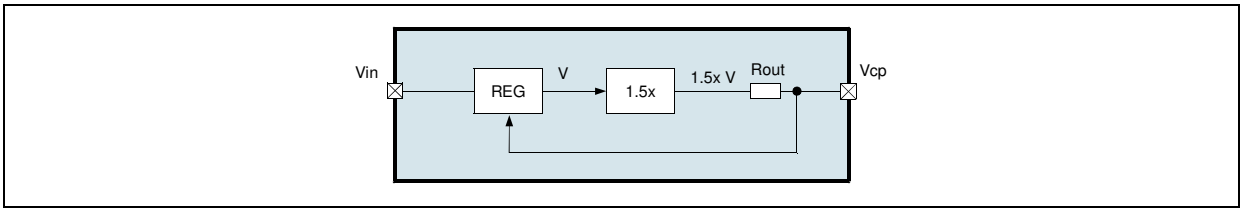
Figure 19. Charge Pump



8.6.2 Output Resistance

At lower input voltages, the charge pump output voltage may degrade due to effective output resistance (R_{OUT}) of the charge pump. The expected voltage drop can be calculated by using a simple model for the charge pump illustrated in Figure 20 below.

Figure 20. Charge Pump Output Resistance



The model shows a linear pre-regulation block (REG), a voltage multiplier (1.5x), and an output resistance (R_{OUT}). The output resistance models the output voltage drop that is inherent to switched capacitor converters. The output resistance is 3.5Ω (typ.), and it is a function of switching frequency, input voltage, flying capacitors' capacitance value, internal resistances of the switches and ESR of the flying capacitors. When the output voltage is in regulation, the regulator in the model controls the voltage V to keep the output voltage equal to 4.5V (typ.). With increased output current, the voltage drop across R_{OUT} increases. To prevent drop in output voltage, the voltage drop across the regulator is reduced, V increases, and V_{CP} remains at 4.5V. When the output current increases to the point that there is zero voltage drop across the regulator, V equals the input voltage, and the output voltage is "on the edge" of regulation. Additional output current causes the output voltage to fall out of regulation, so that the operation is similar to a basic open-loop 1.5x charge pump. In this mode, output current results in output voltage drop proportional to the output resistance of the charge pump. The out-of-regulation output voltage can be approximated by:

$V_{CP} = 1.5 \times V_{IN} - I_{OUT} \times R_{OUT}$.

8.6.3 Controlling the Charge Pump

The charge pump is controlled with two CP_MODE bits in MISC register (address 36H). When both of the bits are low, the charge pump is disabled and the output voltage is pulled down with an internal 300 kΩ (typ.) resistor. The charge pump can be forced to bypass mode, so that the battery voltage is connected directly to the current sources. In 1.5x mode the output voltage is boosted to 4.5V. In automatic mode the charge pump operation mode is determined by saturation of constant current drivers, like described in chapter LED Forward Voltage Monitoring.

8.6.4 LED Forward Voltage Monitoring

When the charge pump automatic mode selection is enabled, the voltages over the LED drivers LED1 to LED6 are monitored.

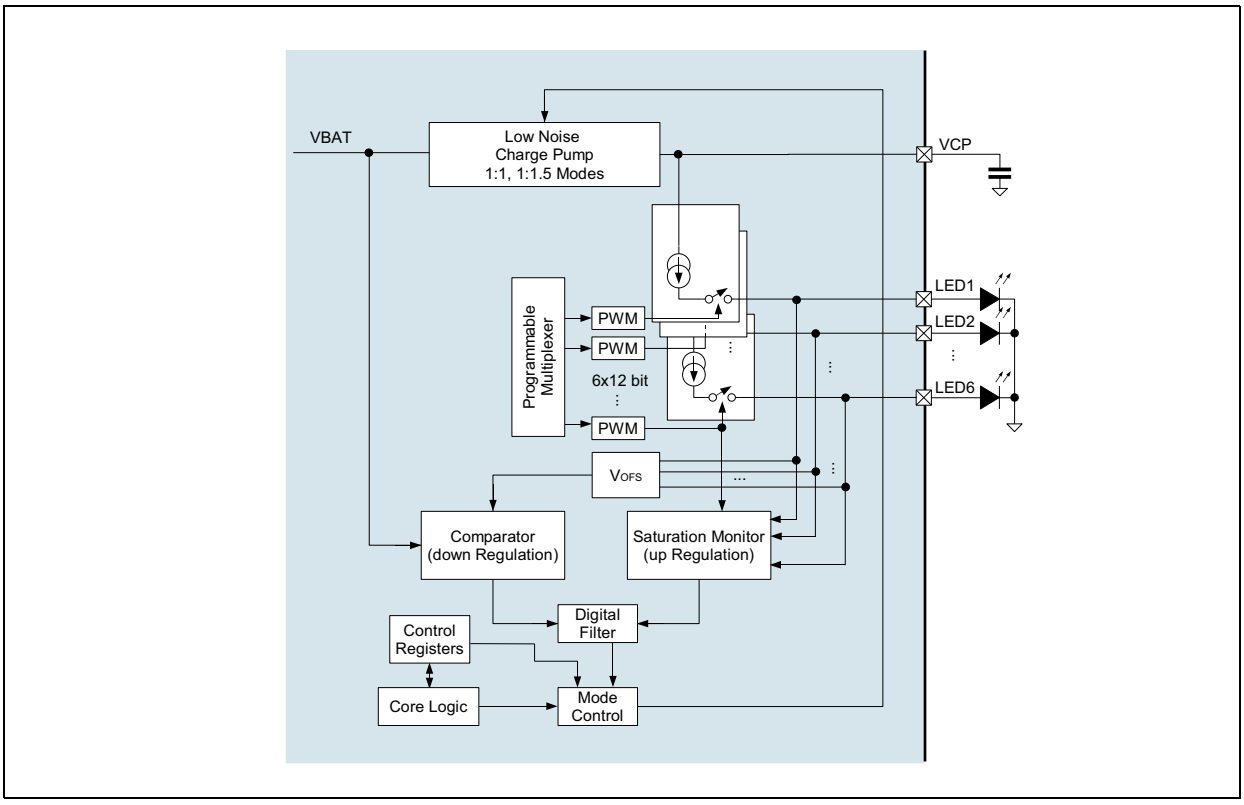
Note: Power input for current source outputs LED7, LED8 and LED9 are internally connected to the VBAT pin.

If the LED1 to LED6 drivers do not have enough headroom, the charge pump gain is set to 1.5x. Driver saturation monitor does not have a fixed voltage limit, since saturation voltage is a function of temperature and current. The charge pump gain is set to 1x, when the battery voltage is high enough to supply all LEDs. In automatic gain change mode, the charge pump is switched to bypass mode (1x), when LEDs are inactive for over 50 ms.

8.6.5 Gain Change Hysteresis

The charge pump gain control utilizes digital filtering to prevent supply voltage disturbances (for example, the transient voltage on the power supply during the GSM burst) from triggering unnecessary gain changes. Hysteresis is provided to prevent periodic gain changes, which would occur due to LED driver and charge pump voltage drop in 1x mode. The hysteresis of the gain change is user configurable, default setting is factory programmable. Flexible configuration ensures, that the hysteresis can be minimized or set to desired level in each application. LED forward voltage monitoring and gain control block diagram is shown in Figure 21.

Figure 21. Forward Voltage Monitoring and Gain Control Block



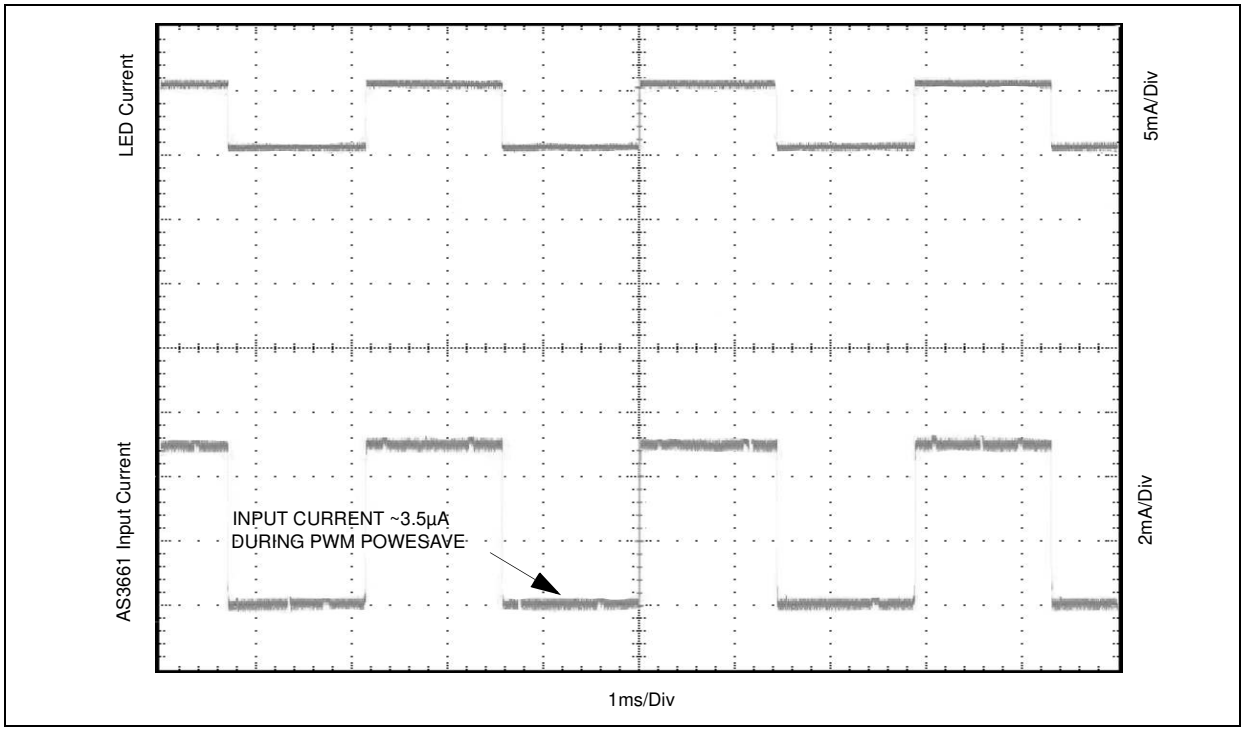
8.6.6 Automatic Power Save Mode

Automatic power save mode is enabled when POWERSAVE_EN bit in register address 36H is ‘1’. Almost all analog blocks are powered down in power save, if an external clock signal is used. Only the charge pump protection circuits remain active. However, if the internal clock has been selected, only charge pump and LED drivers are disabled during the power save; the digital part of the LED controller needs stay active. In both cases the charge pump enters to the weak 1x mode. In this mode the charge pump utilizes a passive current limited keep-alive switch, which keeps the output voltage at the battery level. During the program execution AS3661 can enter power save if there is no PWM activity in any of the LED driver outputs. To prevent short power save sequences during program execution, AS3661 has an instruction look-ahead filter. During program execution engine 1, engine 2 and engine 3 instructions are constantly analyzed, and if there is time intervals of more than 50ms in length with no PWM activity on LED driver outputs, the device will enter power save. In power save mode program execution continues uninterruptedly. When an instruction that requires PWM activity is executed, a fast internal startup sequence will be started automatically.

8.6.7 PWM Power Save Mode

PWM cycle power save mode is enabled when register 36 bit [2] PWM_PS_EN is set to '1'. In PWM power save mode analog blocks are powered down during the "down time" of the PWM cycle. Blocks that are powered down depends whether external or internal clock is used. While the Automatic Power Save Mode (see above) saves energy when there is no PWM activity at all, the PWM Power Save mode saves energy during PWM cycles. Like the Automatic Power Save Mode, PWM Power Save Mode works also during program execution.

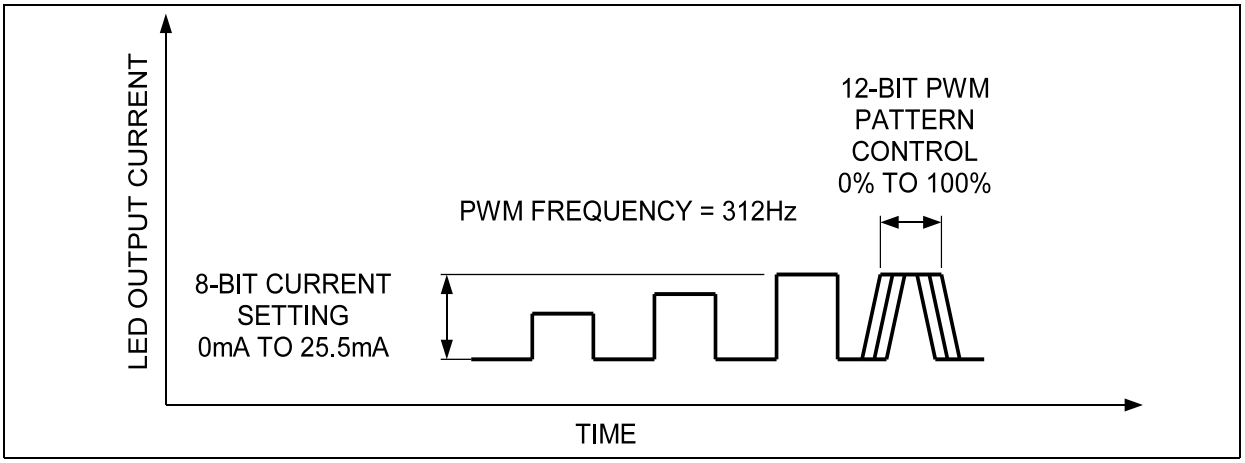
Figure 22. PWM Powersave Principle with external clock (VDD =3.6V, 50% PWM, I_{LED9}=5mA)



8.7 LED Driver Operational Description

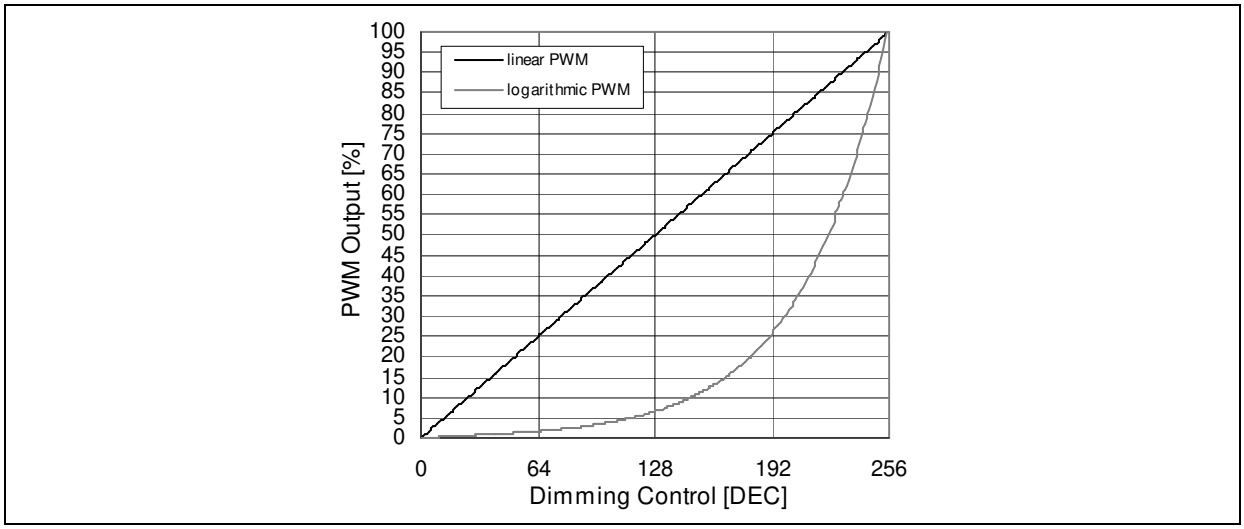
AS3661 LED drivers are constant current sources. The output current can be programmed by control registers up to 25.5 mA. The overall maximum current is set by 8-bit output current control registers with 100 µA step size. Each of the 9 LED drivers has a separate output current control register. The LED luminance pattern (dimming) is controlled with PWM (pulse width modulation) technique, which has internal resolution of 12 bits (8-bit control can be seen by user). PWM frequency is 312 Hz (see Figure 23 on page 20).

Figure 23. LED Pattern and Current Control Principle



LED dimming is controlled according to a logarithmic or linear scale(see Figure 24). Logarithmic or linear scheme can be set for both the program execution engine control and direct PWM control.

Figure 24. Logarithmic vs. Linear Dimming



Note: If the temperature compensation is active, the maximum PWM duty cycle is limited to 50% at +25°C. This is required to allow enough headroom for temperature compensation over the whole temperature range -40 °C to 90°C.

8.7.1 Powering LEDs

Although the AS3661 is very suitable for white LED and general purpose applications, it is particularly well suited to use with RGB LEDs. The AS3661 architecture is optimized for use with three RGB LEDs. Typically, the red LEDs have forward voltages below 2V and thus red LEDs can be powered directly from V_{BAT}. In AS3661 the LED7, LED8 and LED9 drivers are directly powered from the battery voltage (V_{BAT}), not from the charge pump output. The LED1 to LED6 drivers are internally connected to the charge pump output and these outputs can be used for driving green and blue (V_F = 2.7V to 3.7V) or white LEDs. Of course, LED7, LED8 and LED9 outputs can be used for green, blue or white LEDs if the VBAT voltage is high enough. An RGB LED configuration example is given in the Typical Applications section.

8.7.2 Controlling the High-side LED Drivers

- Direct PWM Control

  All AS3661 LED drivers, LED1 to LED9, can be controlled independently through the two-wire serial I²C compatible interface. For each high-side driver there is a PWM control register. Direct PWM control is active by default.

- Controlling by Program Execution Engines

  Engine control is used when the user wants to create programmed sequences. The program execution engine has higher priority than direct control registers. Therefore if the user has set to PWM register a certain value it will be automatically overridden when the program execution engine controls the driver. LED control and program execution engine operation is described in the chapter Control Register Details.

- Master Fader Control

  In addition to LED-by-LED PWM register control, the AS3661 is equipped with so called master fader control, which allows the user to fade in or fade out multiple LEDs by writing to only one register. This is an useful function to minimize serial bus traffic between the MCU and the AS3661. The AS3661 has three master fader registers, so it is possible to form three master fader groups. Master fader control can be used with the engines as well.

8.8 I2C Compatible Control Interface

The AS3661 supports the I^{2}C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The AS3661 operates as a slave on the I^{2}C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The AS3661 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCLTable 5

8.8.1 I^{2}C Address selection

The slave address can be selected depending on the connection of the two address selection pins ASEL0 and ASEL1. The selected address for reading and writing depending on the state of ASEL0 and ASEL1 can be found inTable 5 below.

Table 5. Chip Address Configuration

ASEL1	ASEL0	Address (Hex)	8 bit Hex Address R/W
GND	GND	32	64/65
GND	VEN	33	66/67
VEN	GND	34	68/69
VEN	VEN	35	6A/6B

The following bus protocol has been defined (Figure 25):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

8.8.2 Bus Not Busy

Both data and clock lines remain HIGH.

8.8.3 Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

8.8.4 Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

8.8.5 Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

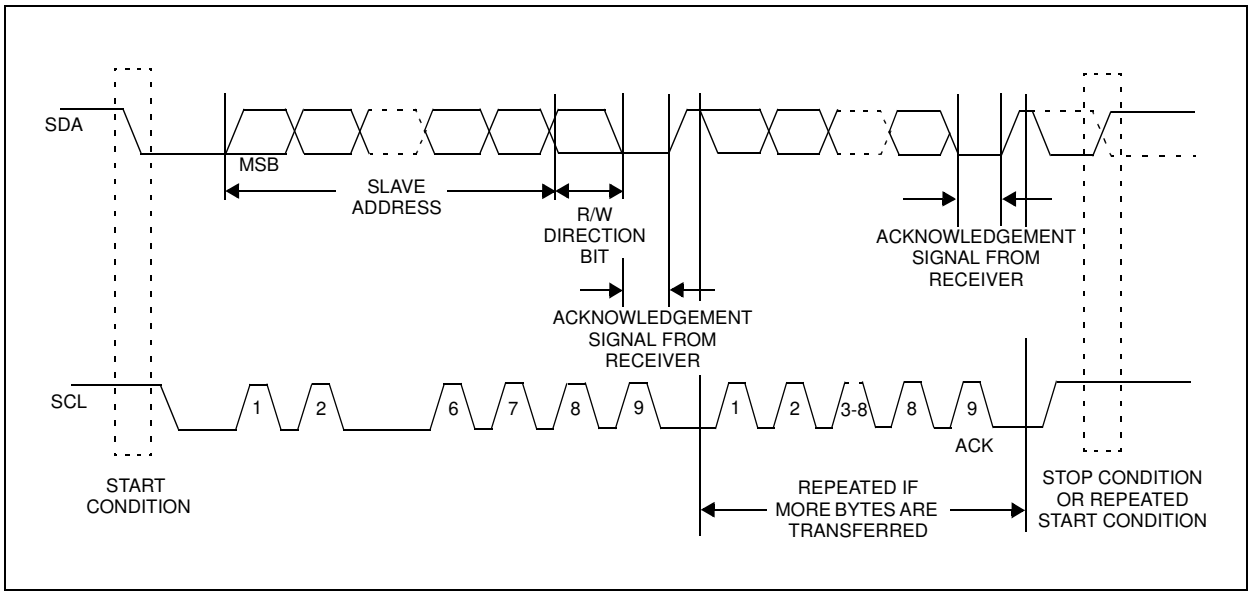
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

8.8.6 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 25. Data Transfer on I²C Serial Bus



Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.
2. **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The AS3661 can operate in the following two modes:

1. **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 26). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit AS3661 address, which is 0110010^{2}, followed by the direction bit (R/W), which, for a write, is 0.[3] After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the AS3661 acknowledges the slave address + write bit, the master transmits a register address to the AS3661. This sets the register pointer on the AS3661. The master may then transmit zero or more bytes of data (if more than one data byte is written see also Blockwrite/read boundaries on page 24), with the AS3661 acknowledging each byte received. The

2. ’XXX’ depends on the external connection of ASEL0 and ASEL1; see Chip Address Configuration on page 22
3. The address for writing to the AS3661 is 8Xh = 01100100b - see Table 5

address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2. **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the AS3661 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 26 and Figure 27). The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit AS3661 address, which is 0110010, followed by the direction bit (R/W), which, for a read, is 1.[4] After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The AS3661 then begins to transmit data starting with the register address pointed to by the register pointer (if more than one data byte is read see also Blockwrite/read boundaries on page 24). If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The AS3661 must receive a “not acknowledge” to end a read.

Figure 26. Data Write - Slave Receiver Mode

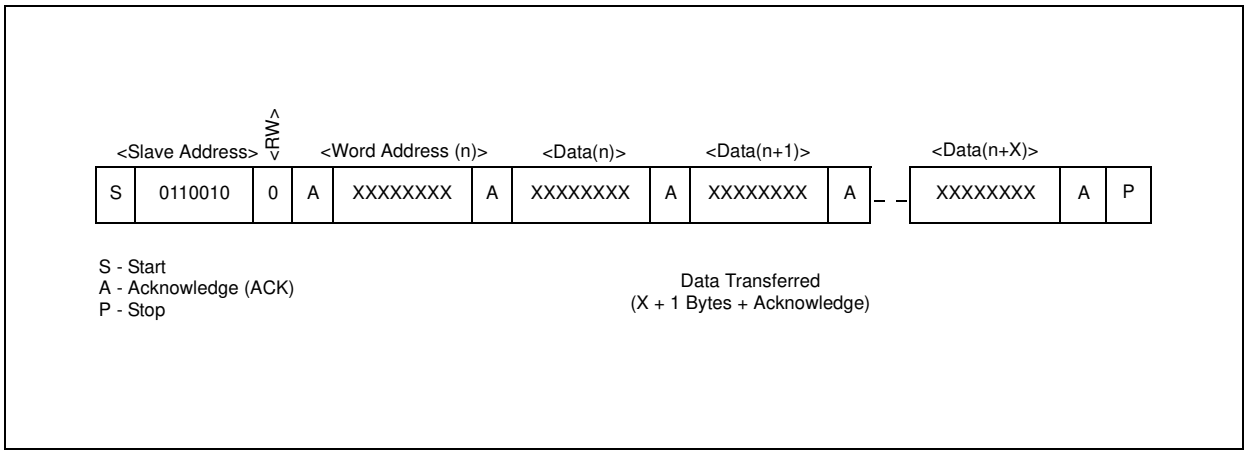
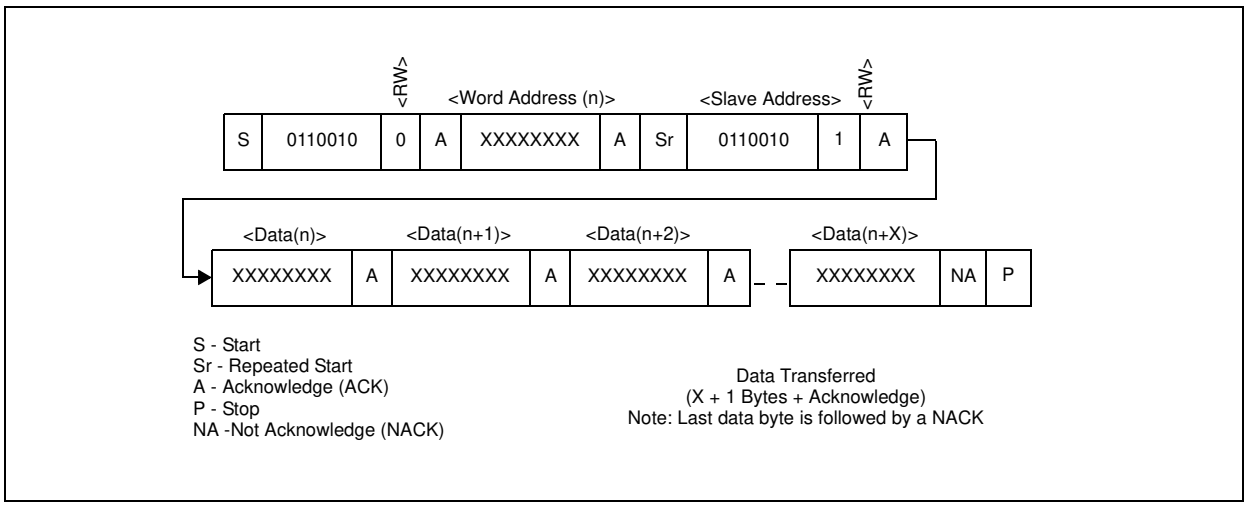


Figure 27. Data Read (Write Pointer, Then Read) - Slave Receive and Transmit



4. The address for read mode from the AS3661 is 8Xh+1 = 01100101b - see Table 5

8.8.7 Program Downloading

First the register page_select is set to the program page, which should be accessed. Then the program page (part of or full page) can be downloaded to the registers Cmd_0_MSB, Cmd_0_LSB, Cmd_1_MSB, Cmd_1_LSB...Cmd_F_MSB, Cmd_F_LSB (I^2C registers area 50h to 6Fh).

Table 6. Page_Select Register

Addr: 4Fh		Page_Select Register			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2:0	page_select	000b	R/W	Selects program page for download	
				000	page 0 - Addr 00h-0Fh
				001	page 1 - Addr 10h-1Fh
				010	page 2 - Addr 20h-2Fh
				011	page 3 - Addr 30h-3Fh
				100	page 4 - Addr 40h-4Fh
				101	page 5 - Addr 50h-5Fh
				110	don't use
				111	don't use

8.9 Register Set

The AS3661 is controlled by a set of registers through the two wire serial interface port. Some register bits are reserved for future use. Table below lists device registers, their addresses and their abbreviations. A more detailed description is given in chapter Control Register Details.

Table 7. Description of Registers

Hex Address	Register Name	Bit(s)	Type	Default Value After Reset	Description	
00	ENABLE / ENGINE CNTRL1	[6]	R/W	x0xxxxxx	CHIP_EN	
					0	AS3661 not enabled
					1	AS3661 enabled
		[5:4]		xx00xxxx	ENGINE1_EXEC Engine 1 program execution control	
		[3:2]		xxxx00xx	ENGINE2_EXEC Engine 2 program execution control	
		[1:0]		xxxxxx00	ENGINE3_EXEC Engine 3 program execution control	
01	ENGINE CNTRL2	[5:4]	R/W	xx00xxxx	ENGINE1_MODE ENGINE 1 mode control	
		[3:2]		xxxx00xx	ENGINE2_MODE ENGINE 2 mode control	
		[1:0]		xxxxxx00	ENGINE3_MODE ENGINE 3 mode control	
02	OUTPUT DIRECT/ RATIOMETRIC MSB	[0]	R/W	xxxxxxx0	LED9_RATIO_EN Enables ratiometric dimming for LED9 output	