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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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AS3668

4 Channel Breathlight Controller

1 General Description

The AS3668 is a 4-channel LED driver designed to produce lighting effects for portable devices. A highly efficient charge pump enables LED driving over full Li-Ion battery voltage range. The device is equipped with an internal program memory, which allows control of LED patterns even without processor control. This helps the whole system to save power and extend for example battery life time in every mobile application. The AS3668 maintains excellent efficiency over a wide operating range by automatically selecting the best charge pump gain based on the LED forward voltage requirements and the device input voltage.

Furthermore the chip supports an automatic power-save mode which gets active when LED outputs are not active. The special power-save mode has a extremely low current consumption below 10µA (typ.).the AS3668 has an I2C-compatible control interface which supports two slave address without having a dedicated address selection pin. For fancy lighting effects synchronized with an audio signal the device supports special digital filter modes in order to make music literally visible on the 4 independent configurable current sources.

The AS3668 is available in a very tiny 12-pin WL-CSP (1.255x1.680mm) 0.4mm pitch package.

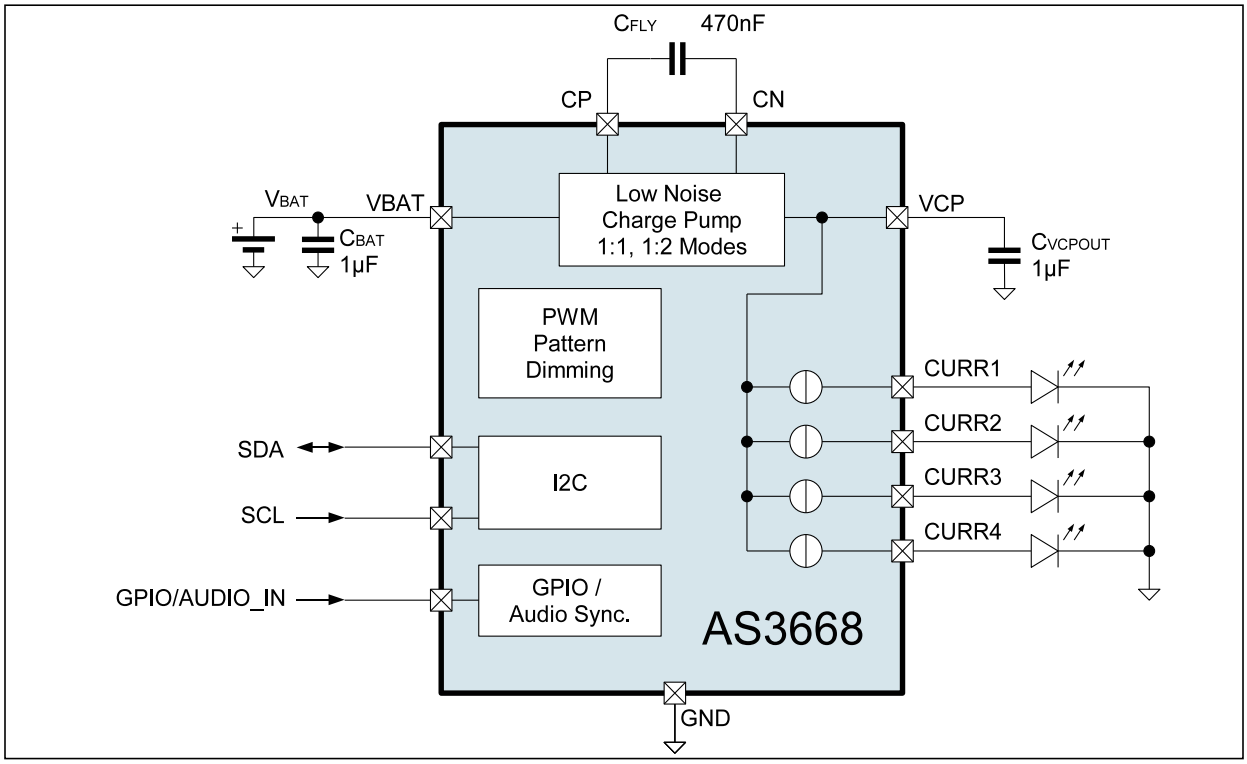
2 Key Features

- High efficiency capacitive 60mA charge pump with 1:1 and 1:2 mode
- Automatic mode switching for charge pump
- Automatic Pattern Mode without digital control
- Highly accurate 4 Channel High Side 25.5mA current sources
- Audio Controlled Lighting with internal digital filters
- Charge Pump with soft start and overcurrent/short circuit protection
- Integrated “easy to use” pattern generator for breathlight LED function with logarithmic 12bit dimming
- Small application circuit
- Minimum number of external components
- Available in 12-pin WL-CSP (1.255x1.680mm) with 0.4mm pitch

3 Applications

The product is perfect for Mobilephones, MP3 Player, Portable Navigation Devices, Digital Cameras, USB Dongles/Modems, Game Controllers and can be used for fun and indicator lights, backlighting and as programmable current sources.

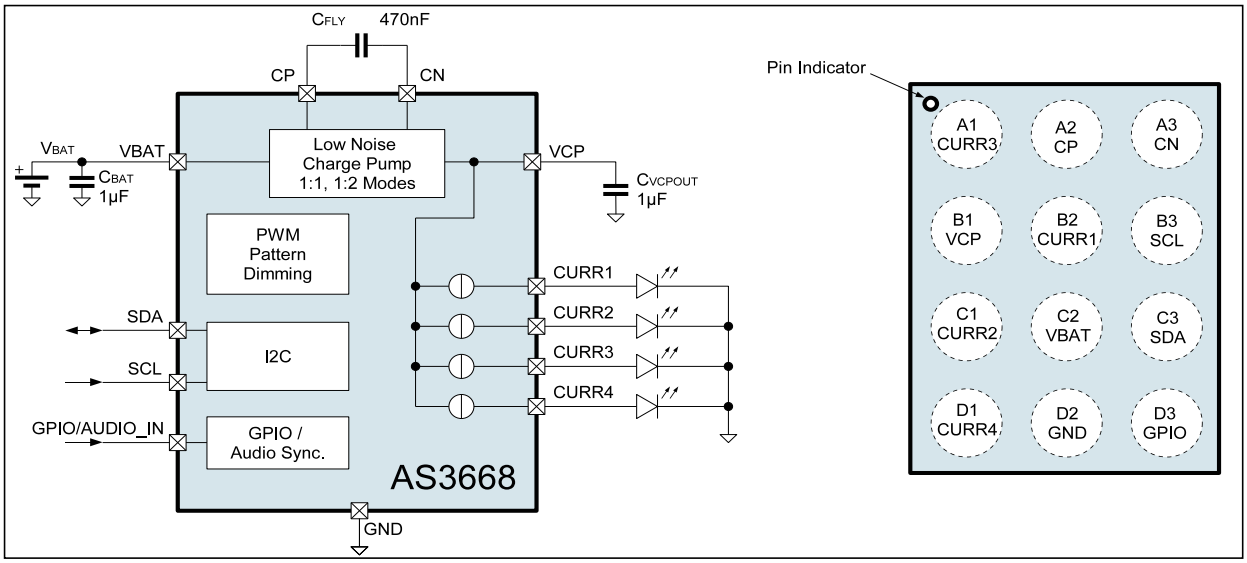
Figure 1. AS3668 Block Diagram



Contents

4 Pin Assignments

Figure 2. Pin Assignments 12-pin WL-CSP (1.255x1.680mm)(Top View)



4.1 Pin Description

Table 1. Pin Descriptions

Pin Name	Pin Number	Description
V_{BAT}	C2	Positive Power Supply Input for AS3668.
GND	D2	Signal and Power Ground. Provide a short, direct PCB path between this pin and the negative side of the output capacitor of the charge pump capacitor C_{VCPOUT}.
SCL	B3	Serial Clock Input for the two wire I2C interface.
SDA	C3	Serial-Data I/O for I2C interface. This pin is a open drain digital I/O which requires a pull up resistor for data transfer.
GPIO/AUDIO_IN	D3	General Purpose Input/Output or Audio Input. Depending on AS3668 configuration this pin provided three different features. It can either be configured as general purpose input/output[1] or as analogue audio input for music playback synchronization of AS3668 with an audio source. Furthermore it is possible to use it as power up pin starting up with a default PWM pattern sequence for LED1. If the pin is not used it is mandatory to connect it to ground.
CURR1	B2	CURR1 Output. This pin is a current source output which can be used to operate a LED. The current source is internally connected to V_{CP}. If the AS3668 is powered up with GPIO/AUDIO_IN pin this current source is active with a default PWM pattern.
CURR2	C1	CURR2 Output. This pin is a current source output which can be used to operate a LED. The current source is internally connected to V_{CP}.
CURR3	A1	CURR3 Output. This pin is a current source output which can be used to operate a LED. The current source is internally connected to V_{CP}.
CURR4	D1	CURR4 Output. This pin is a current source output which can be used to operate a LED. The current source is internally connected to V_{CP}.
V_{CP}	B1	Charge Pump Output. This pin requires an external blocking capacitor. The capacitor must be placed as close as possible to V_{CP} terminal.
CP	A2	Charge Pump Flying Capacitor. This is the positive terminal for the charge pump flying capacitor. The capacitor should be placed as close as possible to AS3668. In addition it is mandatory to keep the signal trace between the capacitor and CP terminal as short as possible.
CN	A3	Charge Pump Flying Capacitor. This is the negative terminal for the charge pump flying capacitor. The capacitor should be placed as close as possible to AS3668. In addition it is mandatory to keep the signal trace between the capacitor and CN terminal as short as possible.

1. The output is an open-drain output only. Therefore an external Pull-Up resistors is required for output operation.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
V_{BAT}, V_{CP}, CN, CP to GND	-0.3	7	V	
V_{CP} to GND	-0.3	7	V	Protection diode between V_{CP} and GND
LED1, LED2, CURR3, CURR4 to GND	-0.3	7	V	
SCL, SDA, GPIO/AUDIO_IN to GND	-0.3	7	V	
Input Pin Current without causing latch up	-100	+100	mA	At 25ºC, Norm: EIA/JESD78
Electrostatic Discharge				
ESD HBM (CURR1 to CURR4)	2		kV	JEDEC JESD22-A114
ESD HBM (all other pins)	2		kV	
ESD MM	100		V	JEDEC JESD22-A115
ESD CDM	500		V	JEDEC JESD22-C101
Storage Temperature Range	-55	+125	ºC	
Temperature Ranges and Storage Conditions				
Continuous Power Dissipation		0.83	W	Internally limited (over temperature protection)[1]
Storage Temperature Range	-55	+125	ºC	
Junction to Ambient Thermal Resistance (θ_{JA})[2]		60	°C/W	
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	1			Represents a max. floor life time of unlimited.
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/ JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices”.

1. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 140°C (typ.) and disengages at T_J = 135°C (typ.).
2. Junction to ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

6 Electrical Characteristics

V_{BAT} = 3.6V, C_{BAT} = C_{VCPOUT} = 1µF, C_{FLY} = 470nF, T_{AMB} = -30ºC to +85ºC, typical values @ T_{AMB} = +25ºC (unless otherwise specified) .

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
General Operating Conditions						
V_{BAT}	Supply Voltage		2.7		5.5	V
I_{VBAT}	Standby supply current	SCL = 0V and GPIO = 0V		0.2	3	µA
	Normal Mode supply current	SCL = V_{BAT} and SDA = V_{BAT}, no I2C communication and no internal block enabled		10		µA
		Charge pump in 1x mode, no load, current source outputs disabled		70		µA
		Charge pump in 2x mode, no load, current source outputs disabled		2.5		mA
f_{OSC}	Internal Oscillator Frequency Accuracy		-10		+10	%
T_{AMB}	Operating Temperature[1]		-30	25	85	°C
Charge Pump						
R_{OUT}	Charge Pump Output Resistance	Operating Mode 1:1		2		Ω
		Operating Mode 1:2; V_{BAT} = 3.0V		20		
f_{SW}	Switching Frequency			1		MHz
t_{ON}	V_{CP} Turn-On Time[2]	no load, current sources CURR1 - CURR4 deactivated		30		µs
		I_{OUT} = 50mA, current sources CURR1 - CURR4 deactivated		40		µs
Current Sources						
I_{LEAK}	Leakage Current (LED1 to CURR4)	PWM = 0%		0.1	1	µA
I_{MAX}	Maximum Source Current	Outputs CURR1 to CURR4		25.5		mA
I_{OUT}	Output Current Accuracy	Output Current set to 25.5 mA	-15		+15	%
I_{MATCH}	Matching Accuracy	Output Current set to 25.5 mA	-10		+10	%
f_{LED}	Switching Frequency	PWM mode with internal oscillator		122		Hz
Logic Interface						
Logic Input SCL, SDA and GPIO/AUDIO_IN						
V_{IL}	Input Low Level				0.52	V
V_{IH}	Input High Level		1.38		V_{BAT}	V
I_{IN}	Input Current		-1.0		1.0	µA
V_{OLGPIO}	Low Level Output voltage	Pin GPIO/AUDIO_IN at 4mA		0.2		V
V_{HYS}	Hysteresis			0.1		V
f_{EXT}	External PWM input	Only possible with GPIO/AUDIO_IN			1	MHz
Analogue Input						
Analogue Audio Input GPI/AUDIO_IN						
V_{AUDIO}	Input Signal Level				2.5	V_{PEAK}
R_{AUDIO_IN}	Audio Input Resistance	Audio Preamplifier Gain = -6dB		400		kΩ
		Audio Preamplifier Gain = +20dB		60		kΩ

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{AUDIO_IN}	Input Capacitance			10		pF
A_{Audio}	Programmable Amplifier Gain		-6		25	dB

1. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 140°C (typ.) and disengages at T_J = 135°C (typ.).
2. Turn-on time is measured from the moment the charge pump is activated until the V_{CP} crosses 90% of its target value

6.1 Timing Characteristics

VBAT = 3.6V, CBAT = CVCPOUT = 1µF, CFLY = 470nF, TAMB = -30ºC to +85ºC, typical values @ TAMB = +25ºC (unless otherwise specified) .

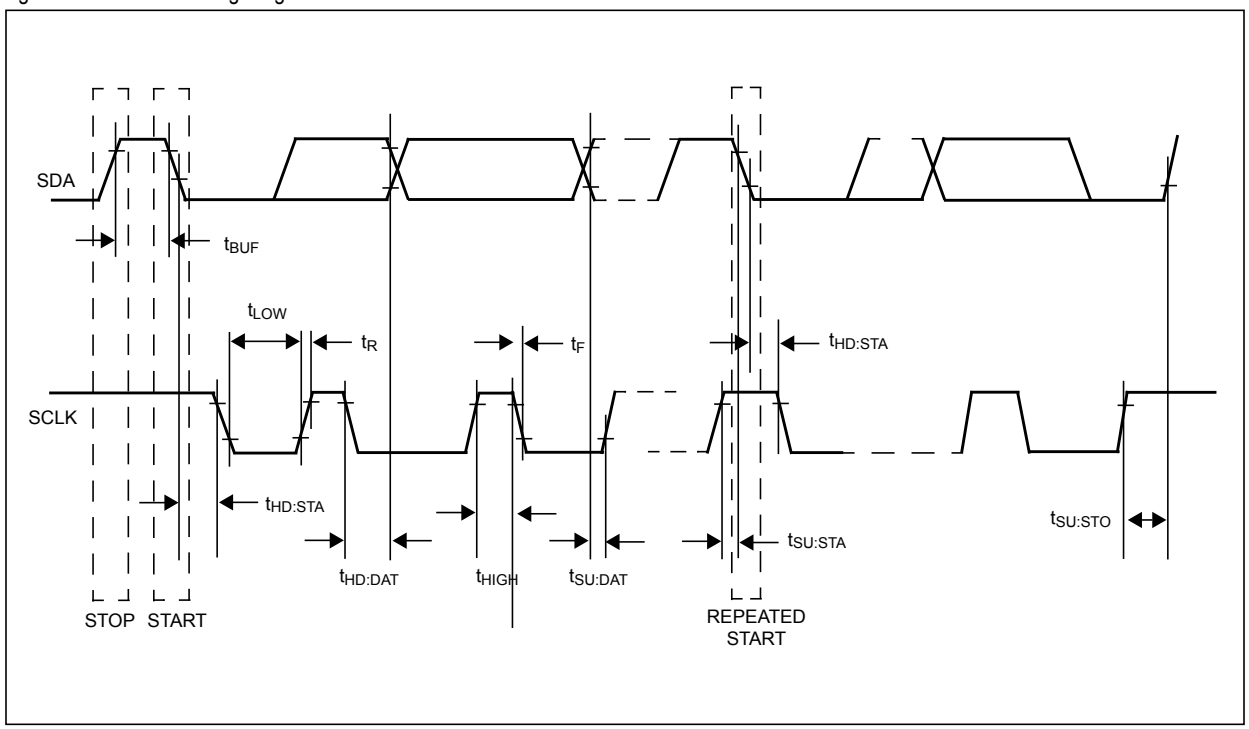
Table 4. Electrical Characteristics I^2C[1]

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I2C mode timings - see						
fSCLK	SCL Clock Frequency		1/35ms		400	kHz
t_{BUF}	Bus Free Time Between a STOP and START Condition		1.3			µs
$t_{HD:STA}$	Hold Time (Repeated) START Condition[2]		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for a Repeated START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time[3]		0		0.9	µs
$t_{SU:DAT}$	Data Setup Time[4]		100			ns
t_R	Rise Time of Both SDA and SCL Signals		20 + $0.1C_B$		300	ns
t_F	Fall Time of Both SDA and SCL Signals		20 + $0.1C_B$		300	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			µs
C_B	Capacitive Load for Each Bus Line	C_B — total capacitance of one bus line in pF			400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL)				10	pF

1. Specification is guaranteed by design and is not tested in production. V_{EN} = 1.65V to VBAT.
2. After this period the first clock pulse is generated.
3. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.
4. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ = to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDA line t_R max + $t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCLK line is released.

6.2 Timing Diagrams

Figure 3. I2C Mode Timing Diagram



7 Typical Operating Characteristics

V_{BAT} = 3.6V, C_{BAT} = C_{VCPOUT} = 1µF, C_{FLY} = 470nF, T_{AMB} = -30ºC to +85ºC, typical values @ T_{AMB} = +25ºC (unless otherwise specified).

Figure 4. Off Mode Current vs. VBAT

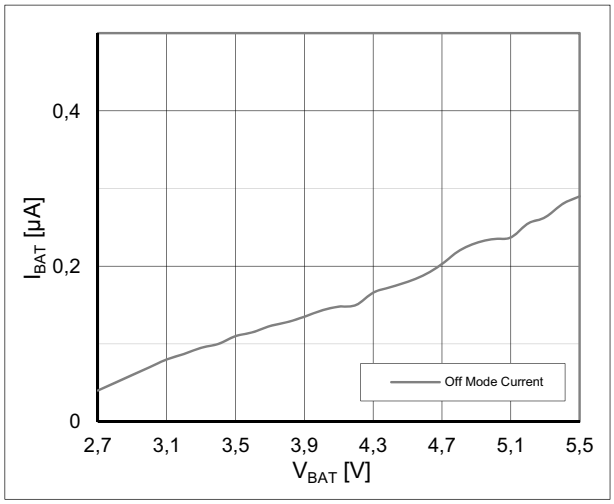


Figure 5. CURRx linearity (0mA - 25.5mA) vs. Code

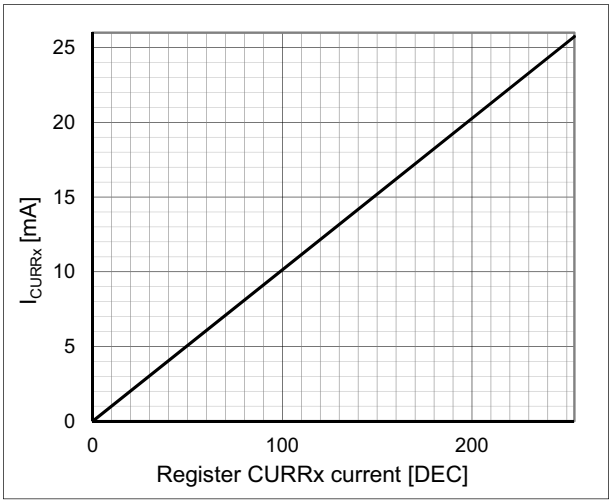


Figure 6. Output Voltage vs. load current (1:1, 4.2V,3,6V, 3,3V) L

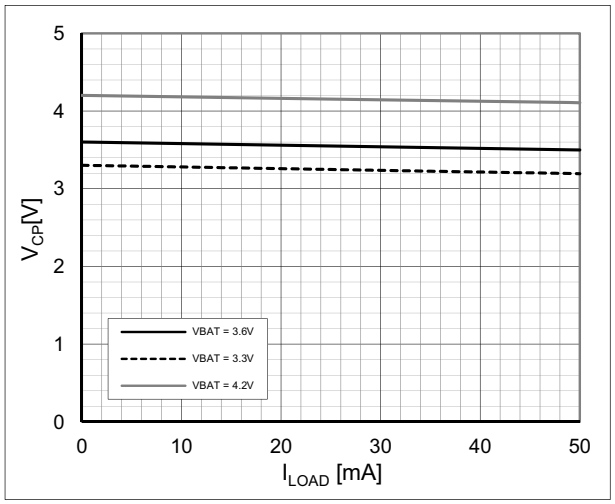


Figure 7. Output voltage. vs. load current (1:2, 4.2V,3,6V, 3,3V)

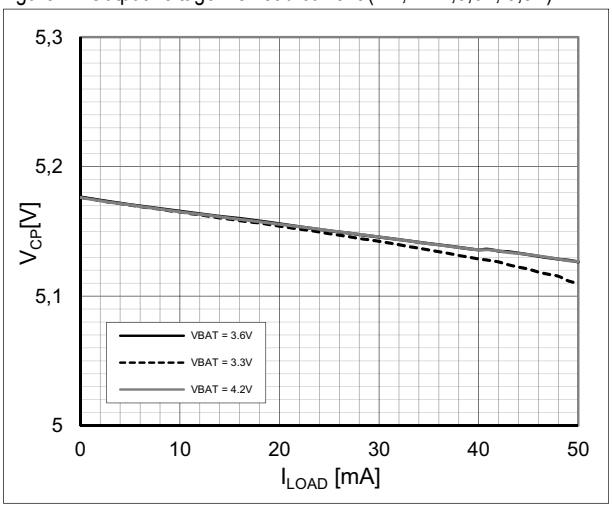


Figure 8. CP Efficiency vs.V*BAT* in 1:2 MODE(10mA,30mA,60mA)

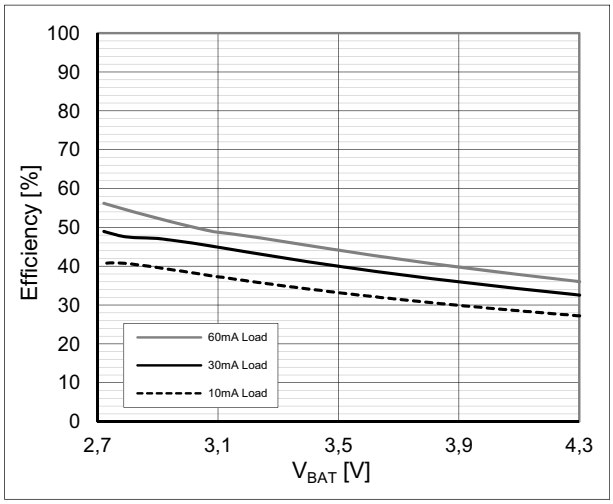


Figure 9. CP Efficiency vs. V*BAT* in 1:1 Mode(10mA,30mA,60mA)

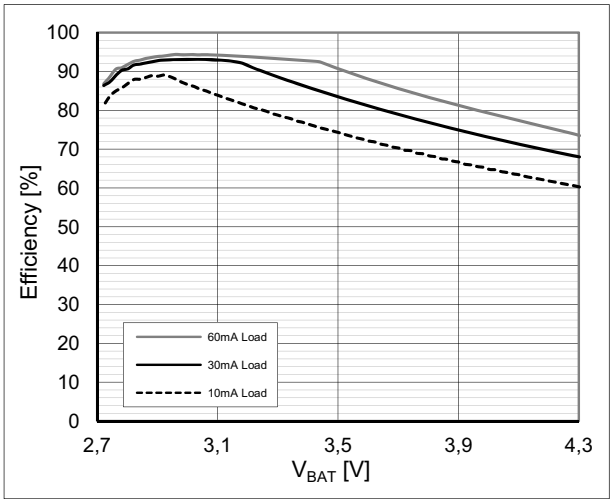


Figure 10. CURRx logarithmic PWM Ramp

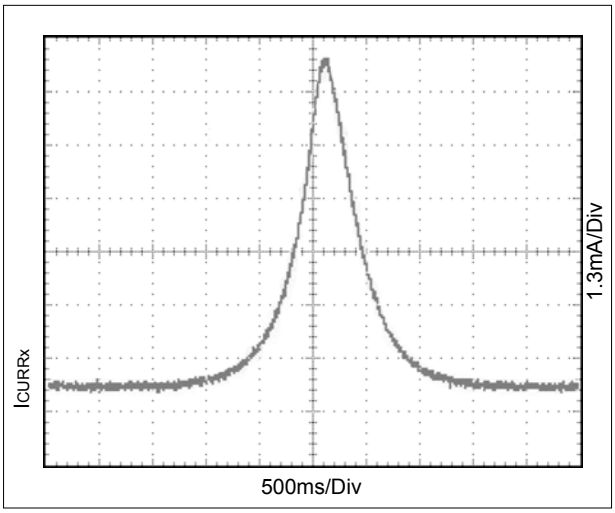


Figure 11. V*CP* and VBAT in 1:2 Mode and 50mA load current

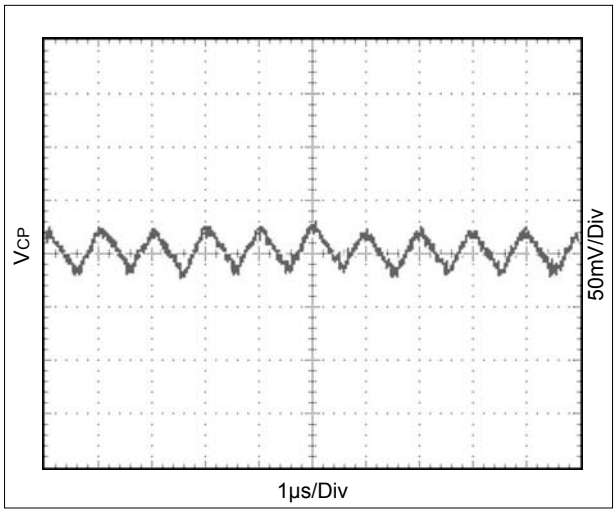


Figure 12. V*CP* with charge pump in 1:2 mode and 10mA load current

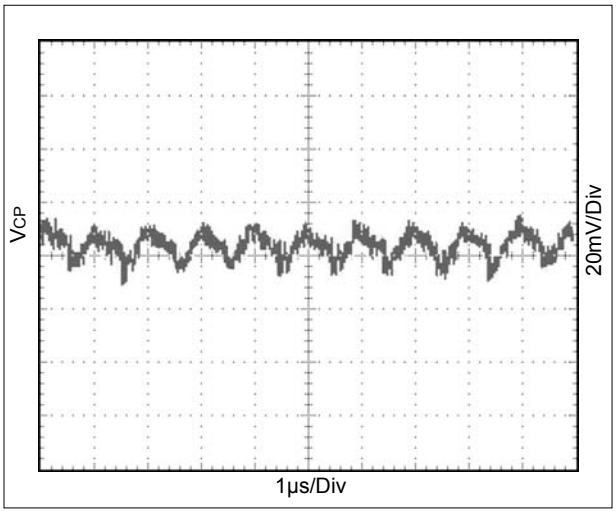


Figure 13. Line Regulation autom. gain change to 1:2 mode with 1mA load current

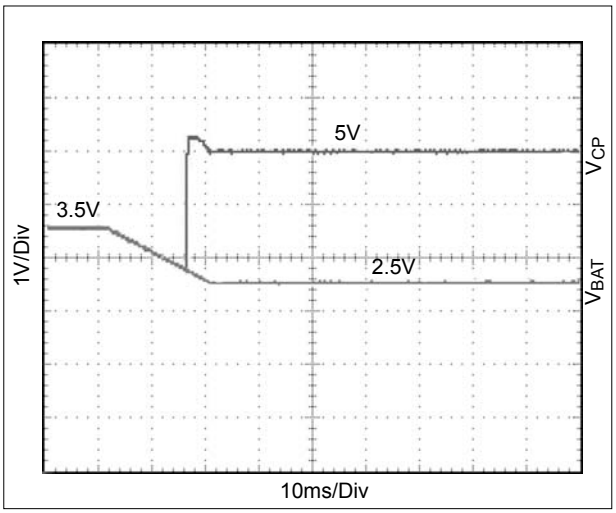


Figure 14. Line Regulation autom. gain change to 1:2 mode with 10mA load current

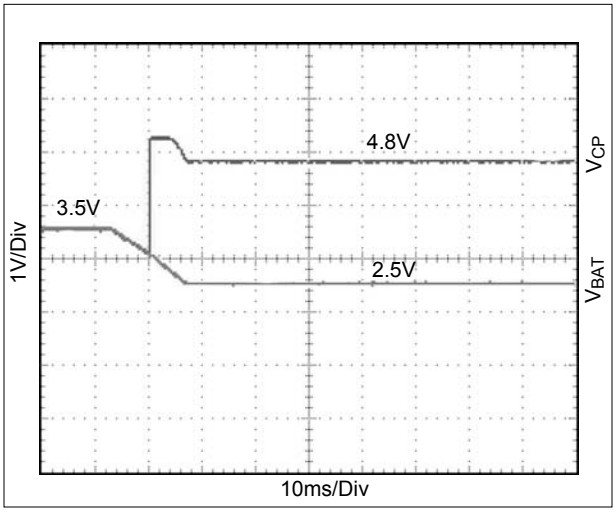


Figure 15. Line Regulation autom. gain change to 1:2 mode with 25.5mA load current

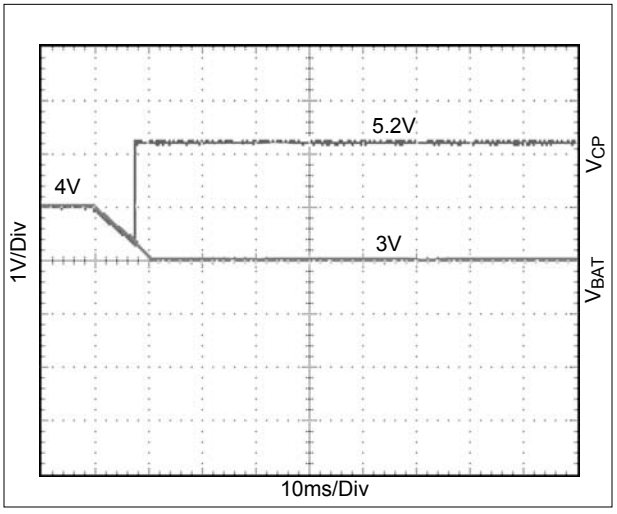


Figure 16. Output current of CURRx vs. U(CURRx) with 25,5mA CURRx output current

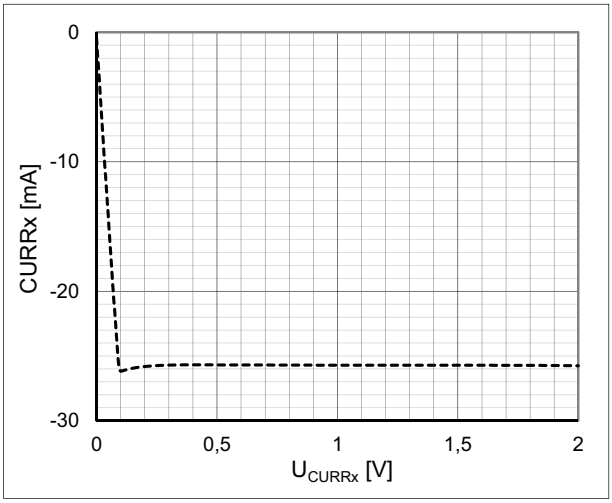


Figure 17. Output current of CURRx vs. U(CURRx) with 10mA CURRx output current

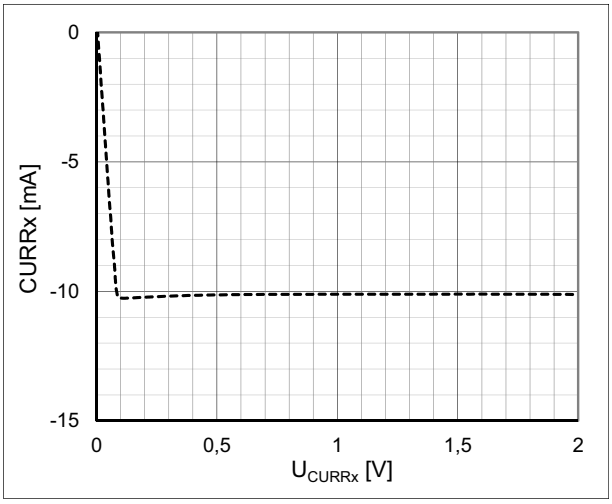


Figure 18. Output current of CURRx vs. U(CURRx) with 1mA CURRx output current)

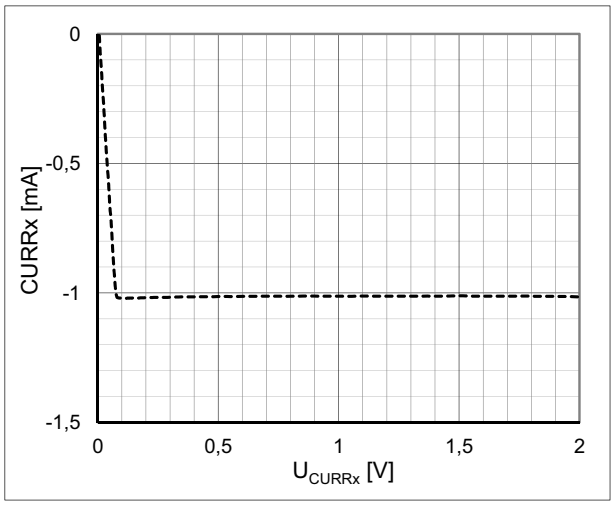


Figure 19. Battery Current vs. VBAT with CP in 1:2 Mode (10mA, 30mA, 60mA

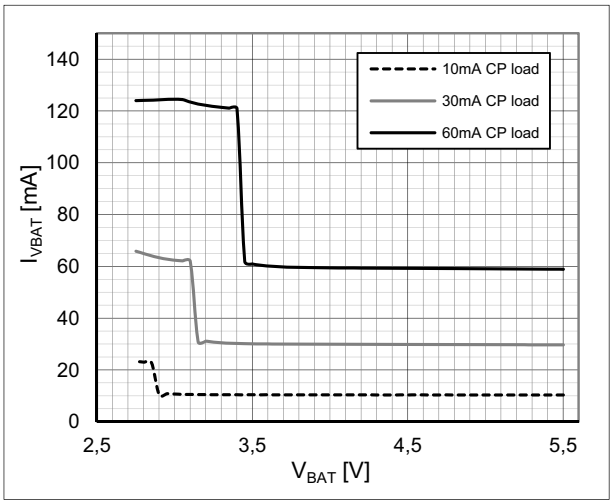


Figure 20. CP efficiency vs. V*BAT* with automatic CP mode switching

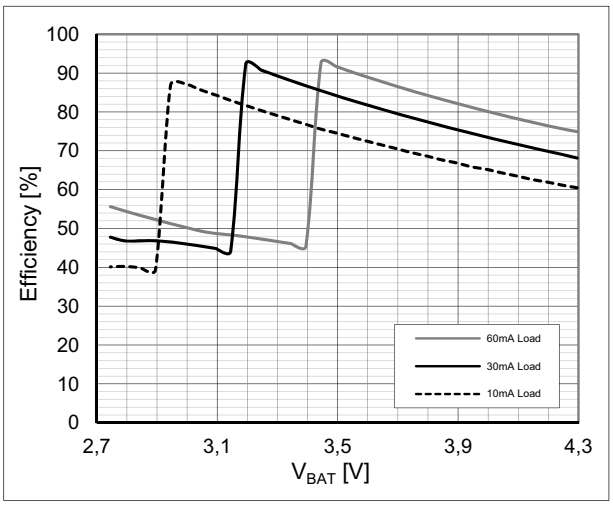
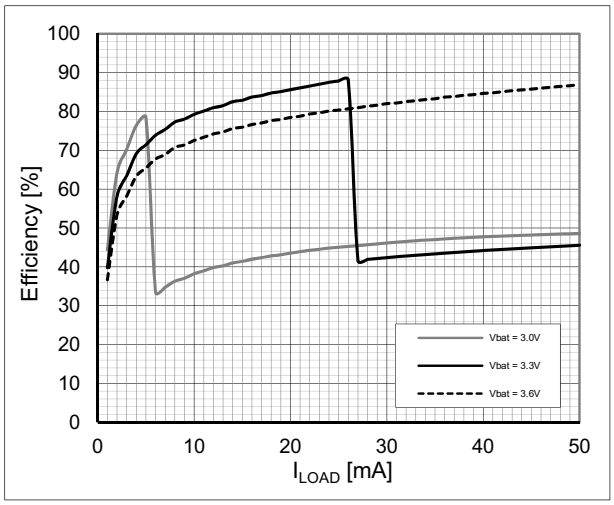


Figure 21. CP efficiency vs. I*LOAD* with automatic CP mode switching



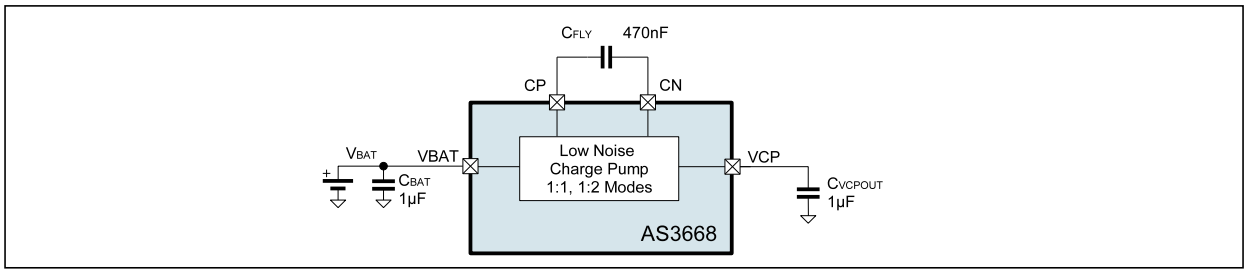
8 Detailed Description

8.1 Charge Pump

The Charge Pump uses the external flying capacitor CFLY to generate output voltages higher than the battery voltage. There are two different operating modes of the charge pump itself:

- 1:1 Bypass Mode
  - Battery input and output are connected by a low-impedance switch
  - battery current = output current.
- 1:2 Mode
  - The output voltage is up to 2 times the battery voltage (without load), but is limited to VCPOUTmax all the time
  - battery current = 2 times output current

Figure 22. Charge Pump Block Diagram .



As the battery voltage decreases, the Charge Pump must be switched from 1:1 mode to 1:2 mode in order to provide enough supply for the current sinks. Depending on the actual current the mode with best overall efficiency can be automatically or manually selected:

The charge pump mode switching can be done manually or automatically with the following possible software settings:

- Automatic
  - Start with 1:1 mode
  - Switch up automatically to 1:2 mode
- Manual
  - Set modes 1:1 and 1:2 by software

The Charge Pump requires the external components listed in the following table:

Table 5. Charge Pump External Components

Symbol	Parameter	Condition	Min	Typ	Max	Unit
CFLY	External Flying Capacitor	Ceramic low-ESR capacitor between pins CP and CN		470		nF
CVCPOUT	External Storage Capacitor	Ceramic low-ESR capacitor between pins VCP and VSS		1.0		µF

Note: The connections of the external capacitors CVCPOUT and CFLY should be kept as short as possible.

.

Table 6. Charge Pump Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICPOUT	Output Current Continuous	Depending on PCB layout	0.0		60	mA
VCPOUTmax	Output Voltage	Internally limited, Including output ripple			5.6	V
η	Efficiency	Including current sink loss; ICPOUT = 60mA.		88		%
ICP1_2	Power Consumption without Load, fclk = 1 MHz	1:2 Mode		2.5		mA

Table 6. Charge Pump Characteristics

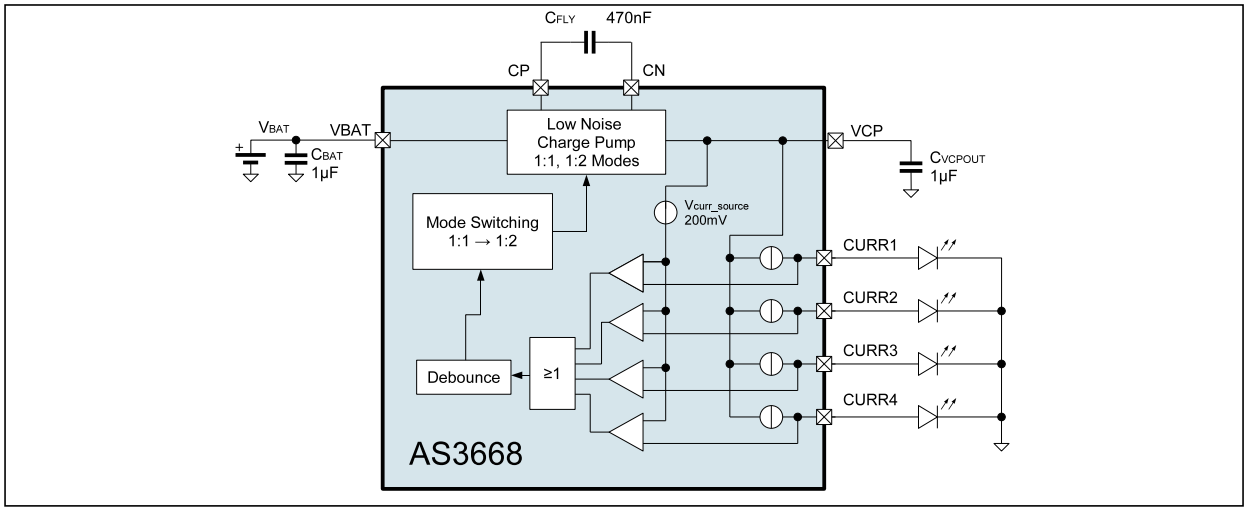
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Rcp1_1	Effective Charge Pump Output Resistance (Open Loop, fclk = 1MHz)	1:1 Mode; V_{BAT} = 3.6V		2.5		Ω
Rcp1_2		1:2 Mode; V_{BAT} = 3V		20		
fclk Accuracy	Accuracy of Clock Frequency		-10		10	%
V_{curr_source}	LED1 - CURR4 current source dropout voltage	If the voltage drops below this threshold, the charge pump will use the next available mode (1:1 -> 1:2)			0.2	V
I_{soft_start}	Current limit for soft start feature			400		mA
t_{deb}	CP automatic up-switching debounce time	cp_start_debounce=0		32		ms
		cp_start_debounce=1		200		µs

8.1.1 Charge Pump Mode Switching

If automatic mode switching is enabled the charge pump monitors the current sources, which are directly connected to the output of the charge pump V_{CP}. In order to identify the enabled current sources, the related registers should be setup before starting the charge pump. If any of the voltage on these current sources drops below the threshold (V_{curr_source}), the higher mode is selected after the debounce time (t_{deb}).

The charge pump mode switching supports only a mode change to a higher charge pump mode (e.g.: mode 1:1 to mode 1:2). In case V_{BAT} increases again during operation the automatic mode switching will not change the operation mode from 1:2 down to 1:1. In order to change the mode all current sources must be switched off to reset the charge pump mode switching mechanism. After enabling the current sources again the mode switching mechanism chooses the appropriate mode for the optimized operation of the charge pump either in 1:1 mode or 1:2 mode. In case an automatic pattern is used the current sources get a reset after each pattern cycle because the current sources are automatically switched off when executing a pattern after each cycle.

Figure 23. Charge Pump Mode Switching .



8.1.2 Soft Start

An implemented soft start mechanism reduces the inrush current. Battery current is smoothed when switching the charge pump on and also at each switching condition. This precaution reduces electromagnetic radiation significantly.

8.1.3 Unused Charge Pump

If the charge pump is not used, capacitors C_{FLY} and C_{VCPOUT} can be removed. The pins CP, CN and V_{CP} should be left open and keep register cp_on and cp_auto_on at 0 (default value).

8.1.4 Charge Pump Control Register .

Table 7. Reg Control Register

0x00 Reg Control register				
Bit	Bit Name	Default	Access	Bit Description
2	cp_on	0	R/W	This bit enables the charge pump for operation if at lease one current source is enabled and the current source has a low voltage condition. Once the charge pump is running it will be keep on even if all current sources are switched off. 0: Chargepump off 1: Charge Pump on

Table 8. CP Control Register

0x23 Current Control Register				
Bit	Bit Name	Default	Access	Bit Description
6	cp_auto_on	1	R/W	This bit enables the charge pump for operation. Once at last one current source is enabled and minimum one current source has a low voltage condition the charge pump is switched on. If all current sources are switched off again the charge will also switch of automatically. 0: Chargepump off 1: Chargepump on in automatic mode
5	cp_start_debounce	0	R/W	Selects the startup debounce time of the charge pump 0: 32ms debounce time. 1: 240µs debounce time
4	cp_mode_switching	0	R/W	Allows the user to select between automatic mode switching or manual mode switching of the charge pump. If the bit is set, the user can change register cp_mode in order to select 1:1 mode or 1:2 mode of the charge pump. 0: Automatic CP Mode Switching 1: Manual CP Mode Switching using register cp_mode
2	cp_mode	0	R/W	Selects the charge pump operating mode if register cp_mode_switching is set to 1. Reading the register return the mode in which the charge pump is operating, either 1:1 or 1:2 mode. 0: 1:1 mode 1: 1:2 mode
0	cp_clk	0	R/W	Selects the charge pump clock frequency. 0: 1Mhz 1: 500kHz

8.2 Current Sources

The AS3668 features four general purpose current sources. All current sources and be controlled independently from each other and share internally the same power supply V_{CP}.

Table 9. Current Sink Function Overview

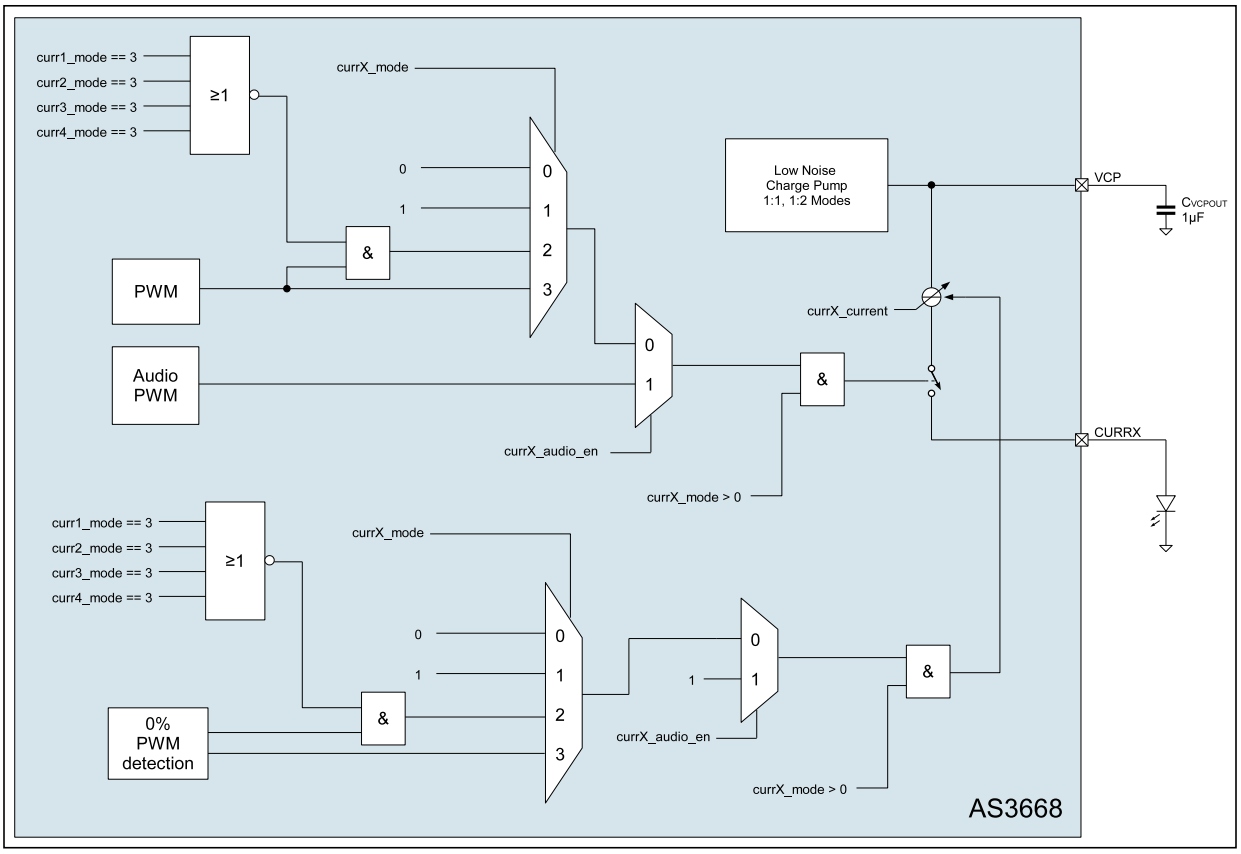
Current Sink	Max. Voltage (V)	Max. Current (mA)	Resolution		Software Current Control	Hardware On/Off Control
			(Bits)	(mA)		
CURR1	5.5	25.5	8	0.1	Separate for each current source	Internal PWM; external PWM at GPIO/AUDIO_IN, Pattern generator
CURR2						
CURR3						
CURR4						

.

Table 10. Current Sources Characteristiks

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{BIT7}	Current sink if Bit7 = 1	CURR1, CURR2, CURR3, CURR4 > 0.2V		12.8		mA
I_{BIT6}	Current sink if Bit6 = 1			6.4		
I_{BIT5}	Current sink if Bit5 = 1			3.2		
I_{BIT4}	Current sink if Bit4 = 1			1.6		
I_{BIT3}	Current sink if Bit3 = 1			0.8		
I_{BIT2}	Current sink if Bit2 = 1			0.4		
I_{BIT1}	Current sink if Bit1 = 1			0.2		
I_{BIT0}	Current sink if Bit0 = 1			0.1		
I_{MATCH}	Matching Accuracy	CURR1, CURR2, CURR3 and CURR4	-10		+10	%
I_{OUT}	Absolute Accuracy		-15		+15	%
V_{CUR1-4}	Voltage Compliance		0		V_{CP}-0.2	V

Figure 24. Internal processing of current sources



8.2.1 Unused Current Sources

Unused current sources can be left open. There are no external connections or components necessary if they are not used.

8.2.2 Current Source Registers .

Table 11. Current Control Register

0x01 Current Control Register				
Bit	Bit Name	Default	Access	Bit Description
7:6	curr4_mode	0	R/W	00: Current Source CURR4 is in off mode 01: Current Source CURR4 is in on mode 10: Current source CURR4 is in PWM control mode 11: Current source CURR4 is in LED pattern generation mode
5:4	curr3_mode	0	R/W	00: Current Source CURR3 is in off mode 01: Current Source CURR3 is in on mode 10: Current source CURR3 is in PWM control mode 11: Current source CURR3 is in LED pattern generation mode
3:2	curr2_mode	0	R/W	00: Current Source CURR2 is in off mode 01: Current Source CURR2 is in on mode 10: Current source CURR2 is in PWM control mode 11: Current source CURR2 is in LED pattern generation mode
1:0	curr1_mode	3	R/W	00: Current Source CURR1 is in off mode 01: Current Source CURR1 is in on mode 10: Current source CURR1 is in PWM control mode 11: Current source CURR1 is in LED pattern generation mode

Table 12. Current Source Register LED1

0x02 Current Control Register				
Bit	Bit Name	Default	Access	Bit Description
7:0	curr1_current	0x40	R/W	0000 0000: 0mA current output from source CURR1 0000 0001: 0.1mA current output from source CURR1 0000 0010: 0.2mA current output from source CURR1 0000 0011: 0.3mA current output from source CURR1 ... 1111 1111: 25.5mA current output from source CURR1

Table 13. Current Control Register LED2

0x03 Current Control Register				
Bit	Bit Name	Default	Access	Bit Description
7:0	curr2_current	0	R/W	0000 0000: 0mA current output from source CURR2 0000 0001: 0.1mA current output from source CURR2 0000 0010: 0.2mA current output from source CURR2 0000 0011: 0.3mA current output from source CURR2 ... 1111 1111: 25.5mA current output from source CURR2

Table 14. Current Control Register CURR3

0x04 Current Control Register				
Bit	Bit Name	Default	Access	Bit Description
7:0	curr3_current	0	R/W	0000 0000: 0mA current output from source CURR3 0000 0001: 0.1mA current output from source CURR3 0000 0010: 0.2mA current output from source CURR3 0000 0011: 0.3mA current output from source CURR3 ... 1111 1111: 25.5mA current output from source CURR3

Table 15. Current Control Register CURR4

0x05 Current Control Register				
Bit	Bit Name	Default	Access	Bit Description
7:0	curr4_current	0	R/W	0000 0000: 0mA current output from source CURR4 0000 0001: 0.1mA current output from source CURR4 0000 0010: 0.2mA current output from source CURR4 0000 0011: 0.3mA current output from source CURR4 ... 1111 1111: 25.5mA current output from source CURR4

Table 16. CURRx Low Voltage Status Register

0x2b Current Source Low Voltage Status Register				
Bit	Bit Name	Default	Access	Bit Description
3	curr4_low_v	0	R	This is a read only register and returns 0 if the voltage on current source CURR4 is ok. If the voltage drops below 200mV across the current source the bit is set to 1. 0: CURR4 voltage is OK 1: CURR4 voltage is too low
2	curr3_low_v	0	R	This is a read only register and returns 0 if the voltage on current source CURR3 is ok. If the voltage drops below 200mV across the current source the bit is set to 1. 0: CURR3 voltage is OK 1: CURR3 voltage is too low
1	curr2_low_v	0	R	This is a read only register and returns 0 if the voltage on current source CURR2 is ok. If the voltage drops below 200mV across the current source the bit is set to 1. 0: CURR2 voltage is OK 1: CURR2 voltage is too low
0	curr1_low_v	0	R	This is a read only register and returns 0 if the voltage on current source CURR1 is ok. If the voltage drops below 200mV across the current source the bit is set to 1. 0: CURR1 voltage is OK 1: CURR1 voltage is too low

8.3 Power - On Reset

The AS3668 provides an power - on reset feature that is controlled by two different sources:

- V_{BAT} supply voltage
- Serial interface state (SCL only)

If the internal V_{BAT} supply voltage reset is forced, when the supply voltage V_{BAT} of AS3668 drops below a predefined voltage, the device enters shutdown mode. This predefined voltage is 2V (typ.) and is defined as V_{POR_VBAT}. Besides this hard wired voltage level where an internal reset is forced to shut down the device, AS3668 supports an additional V_{BAT} monitoring feature. This means that the designer can select according to its application requirements a reset level which is appropriate for mobile Li-Ion battery powered applications. The use case for this second V_{BAT} monitoring is to make sure that if a mobile device switches off suddenly, at a dedicated voltage, to make sure that also AS3668 enters power down mode. Otherwise unwanted LED effects could occur even if the digital system is not running any more. AS3668 allows the designer now to set the V_{BAT} monitoring level to the same voltage level the whole system is powering down. There's no need any more for the CPU to reset or power down AS3668 in a low battery case any more. The device can handle this use case automatically.

In addition to the V_{BAT} voltage monitoring the device supports also a shut down function forced by the serial interface. If the voltage on the serial interface pin SCL is below 1V (typ.) and GPIO/AUDIO_IN pin is low, the device forces a reset. To prevent the system against wrong resets caused by electromagnetically influences there is also a debounce timer integrated with a typical debounce time of 100ms. This debounce time is used for V_{BAT} monitoring as well. If the serial interface monitoring is not supposed to be used in an application it is also possible to disable the feature using the corresponding register bit.

Figure 25. Reset Circuit Block Diagram

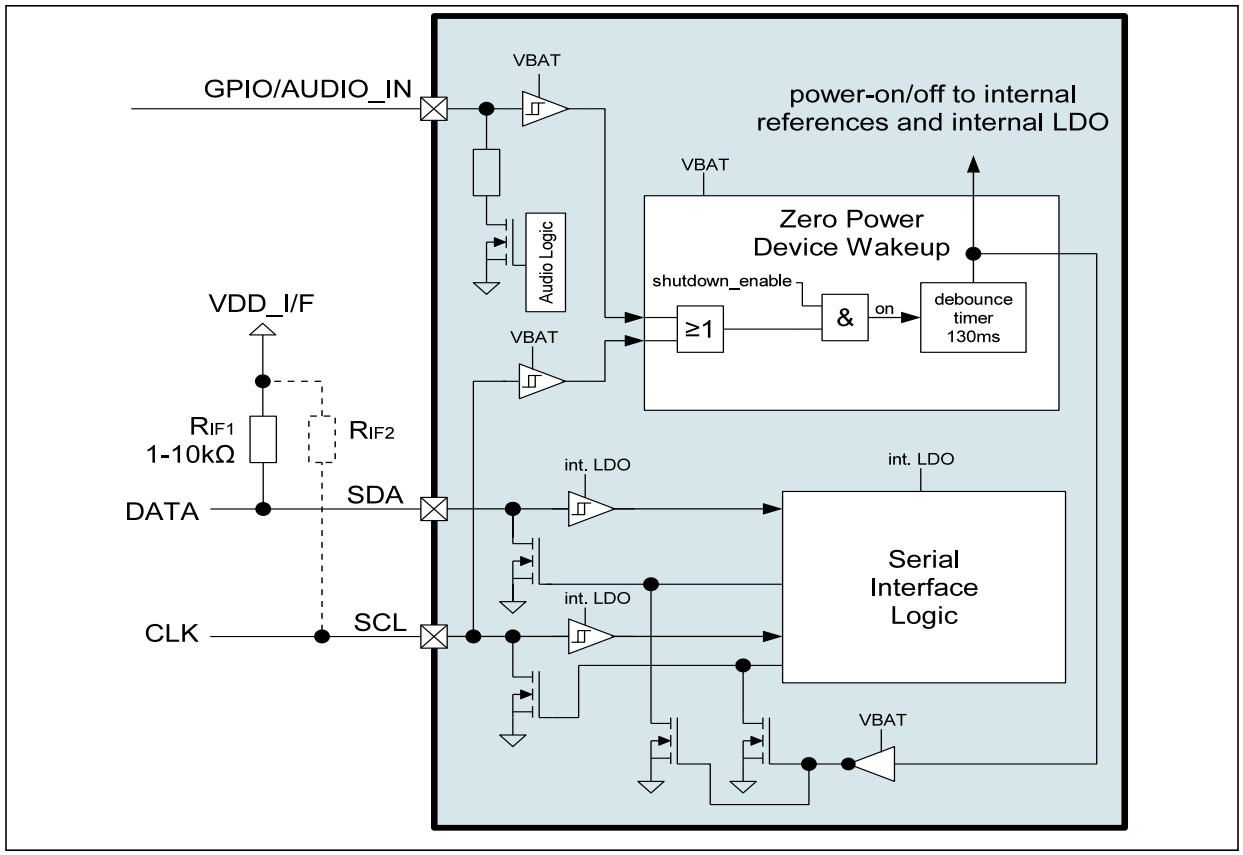


Table 17. Power On Reset Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VPOR_VBAT	Overall Power-On Reset	Monitor voltage on VBAT; power-on reset for all internal functions.		2.0		V
VMON_VBAT	Register defined stand by mode voltage	depending on register setting the voltage can be configured	3.0V		3.3V	
VPOR_PERI	Reset Level for pins SCL	Monitor voltage on pin SCL		1.0		V
tPOR_DEB	Reset debounce time for pins SCL		110	130	150	ms
tstart	Interface Startup Time			3		ms

8.4 VBAT Monitor

The V*BAT* monitor is a supervisory circuit. The monitor is per default disabled when the AS3668 is powered up. The function can be used in order to send the device automatically into standby mode if the supply voltage of AS3668 drops below the defined values in register vmon_vbat. All together the user can select between three different voltage thresholds for this function with 3.375V, 3.3V and 3.0V. If the function is disabled the device switches of if the battery voltage drops below 2.0V. The monitor function has also a debouncer with 100ms implemented in order to filter the 217Hz GSM noise pulses from the battery supply voltage. Without the debouncer the chip would be susceptible to this noise and maybe enter into standby mode due to a misinterpretation of the supply voltage.

Figure 26. V*BAT* Monitor Block Diagram

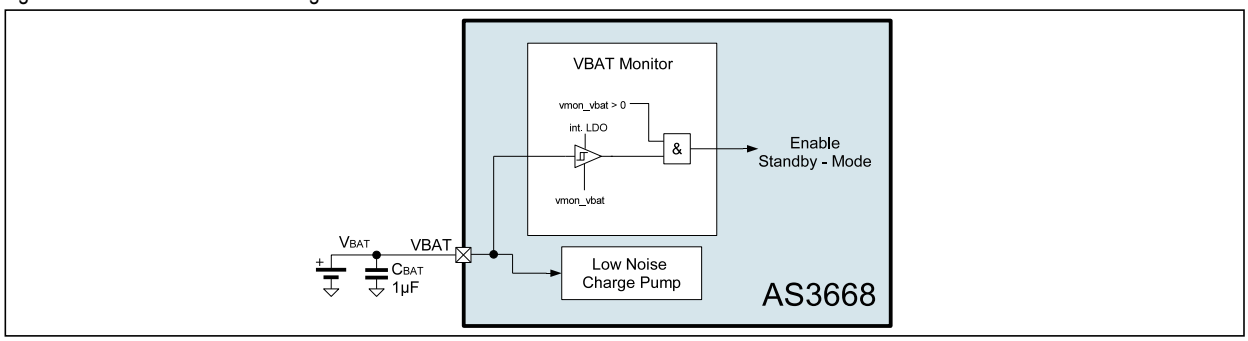


Table 18. V*BAT* Monitor Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VMON_VBAT	Register defined stand by mode voltage	depending on register setting the voltage can be configured	3.0V		3.3V	

8.4.1 VBAT Monitor Registers .

Table 19. Overtemperature Control / VBAT Monitor Register

0x29 Overtemperature Control / V**BAT** Monitor Register				
Bit	Bit Name	Default	Access	Bit Description
6:5	vmon_vbat	0	R/W	0: Device enters shutdown mode if V**BAT** voltage drops below ~2.0V 1: Device enters standby mode if VBAT voltage drops below 3.0V 2: Device enters standby mode if VBAT voltage drops below 3.15V 3:Device enters standby mode if VBAT voltage drops below 3.3V
4	shutdown_enable	1	R/W	This bit allows the user to disable the I2C shutdown feature. If the bit is set to '0' both I2C signal lines can be low without shutting down AS3668. 0: disables the automatic shutdown of AS3668 1: enables the automatic shutdown of AS3668
2	rst_ov_temp	0	W	This register is a self clearing register. Write a '1' to this register to clear ov_temp.
1	ov_temp	0	R	This is a read only register and provides feedback about the junction temperature of the chip. The bit is usually set if the junction temperature reaches about 140°C. 0: Junction temperature OK 1: Junction Overtemperature
0	ov_temp_on	1	R/W	This bit allows the user the enable/disable the junction temperature monitoring for AS3668. 0: Temperature supervision OFF 1: Temperature supervision ON

8.5 Temperature Supervision

An integrated temperature sensor provides over-temperature protection for the AS3668. This sensor generates a flag if the device temperature reaches the over temperature threshold of 140º. The threshold has a hysteresis to prevent oscillation effects.

If the device temperature exceeds the T140 threshold all current sources and the charge pump get disabled and the ov_temp flag is set. After decreasing the temperature by THYST operation is resumed. Although the device resumes ordinary operation after a overtemperature event, the register ov_temp keeps set to 1. Even a read operation from the register doesn't reset the register. Therefore it's necessary to use the register rst_ov_temp to reset the overtemperature register ov_temp.

The ov_temp flag can only be reset by first writing a 1 to the register bit rst_ov_temp. If bit ov_temp_on = 1 activates temperature supervision Table 20. It is recommend to leave this bit set (default state).

Table 20. Overtemperature Detection

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{140}	ov_temp Rising Threshold			140		°C
T_{HYST}	ov_temp Hysteresis			5		°C

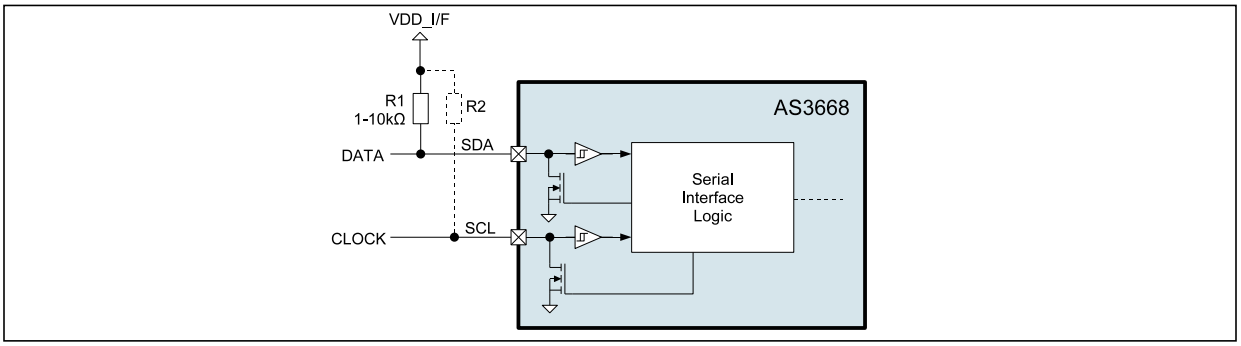
Table 21. Overtemperature Control / V_{BAT} Monitor Register

0x29 Overtemerature Control / V_{BAT} Monitor Register				
Bit	Bit Name	Default	Access	Bit Description
2	rst_ov_temp	0	W	Write a 1 to this register to reset ov_temp
1	ov_temp	0	R	0: Junction temperature is ok and below T_{140} 1: Junction temperature is too high and above T_{140}
0	ov_temp_on	1	R/W	0: Disables the overtemperature supervision (not recommended) 1: Enabled the overtemperature supervision

8.6 I²C Serial Interface Bus

The AS3668 supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. The AS3668 operates as a slave on the I²C bus. Due to the reason that the device is also power up/down with the I²C interface there is a debouncer (130ms) on the signal lines integrated to avoid a system shut down while having I²C traffic on the bus.

Figure 27. Serial Interface Block Diagram



The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The clock line SCL is never held low by AS3668 because clock stretching of the bus is not supported.

Figure 28. AS3668 Interface Initialization

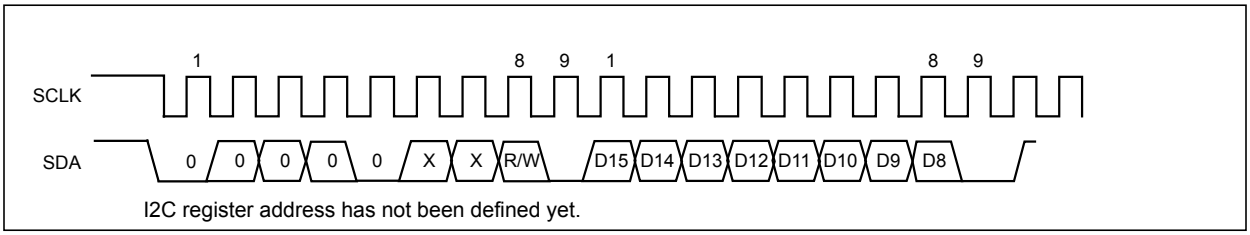
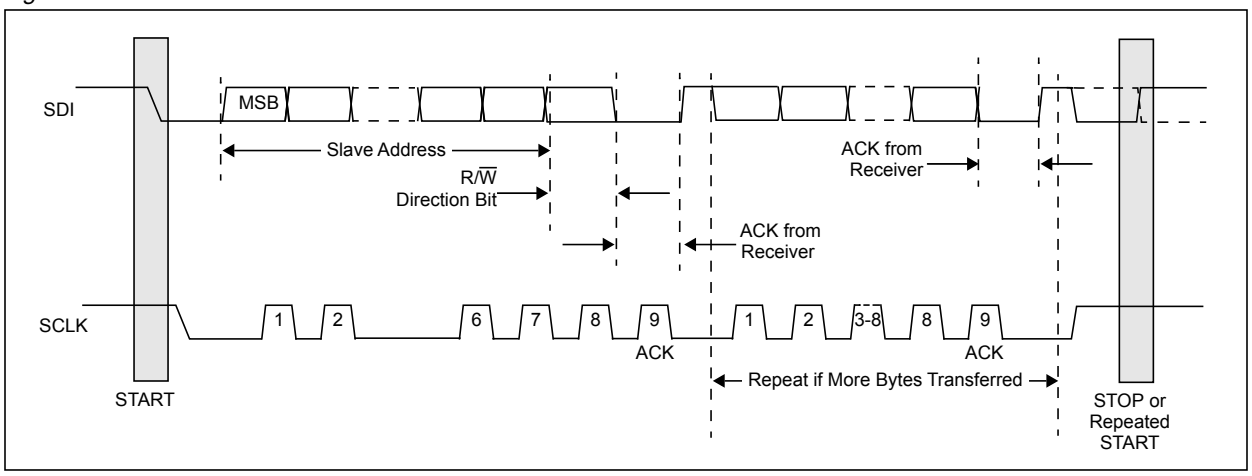


Figure 29. Bus Protocol



The bus protocol (as shown in Figure 29) is defined as:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The bus conditions are defined as:

- Bus Not Busy. Data and clock lines remain HIGH.
- Start Data Transfer. A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.
- Stop Data Transfer. A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.
- Data Valid. The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.
  Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit.
  Within the I²C bus specifications a high-speed mode (3.4MHz clock rate) is defined.
- Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.
- Figure 29 on page 23 details how data transfer is accomplished on the I²C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:
- Master Transmitter to Slave Receiver. The first byte transmitted by the master is the slave address, followed by a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
- Slave Transmitter to Master Receiver. The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

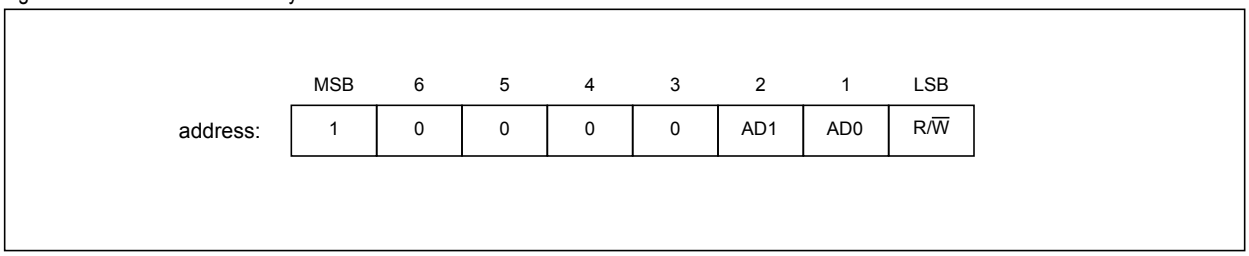
The AS3668 can operate in the following slave modes:

- Slave Receiver Mode. Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- Slave Transmitter Mode. The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the AS3668 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

8.6.1 I²C Device Address Byte

The address byte (see Figure 30) is the first byte received following the START condition from the master device. The 7 bit device address is 0x42.

Figure 30. I²C Device Address Byte



- Bit 1 and bit 2 of the address byte are defined by the external bus connection of the slave to the master shown in chapter 8.6.3. A maximum of two devices can be connected in parallel on the same bus at one time.
- The last bit of the address byte (R/$\overline{W}$) define the operation to be performed. When set to a 1 a read operation is selected; when set to a 0 a write operation is selected.

Following the START condition, the AS3668 monitors the I²C bus, checking the device type identifier being transmitted. Upon receiving the address code, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

8.6.2 Command Byte

The AS3668 operation, (see Table 29 on page 23) is determined by a command byte (see Table 31).

Figure 31. Command Byte

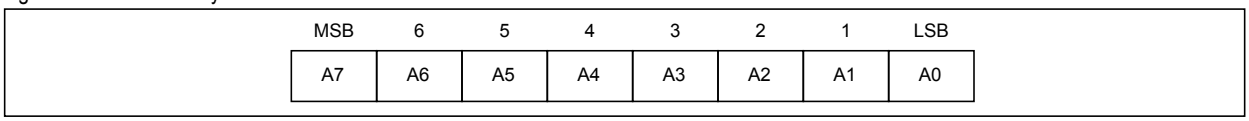


Figure 32. Command and Single Data Byte received by AS3668

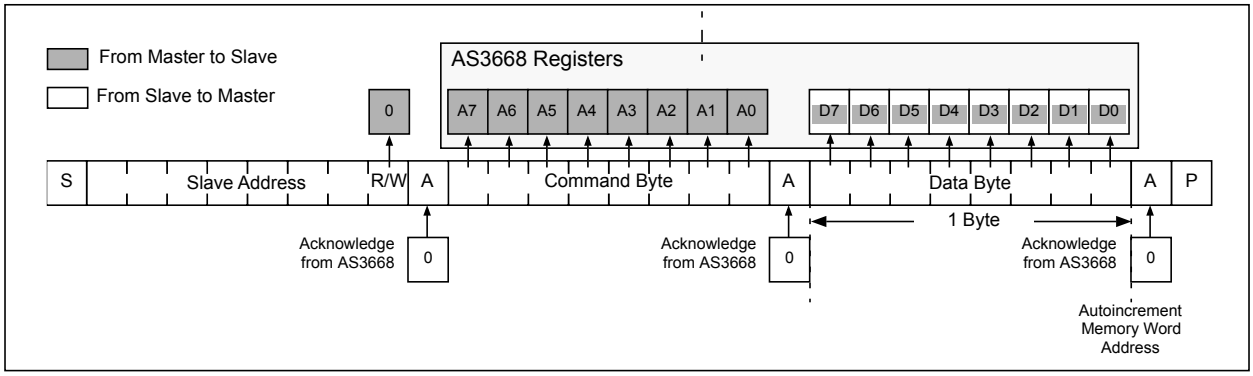


Figure 33. Setting the Pointer to a Address Register to select a Data Register for a Read Operation

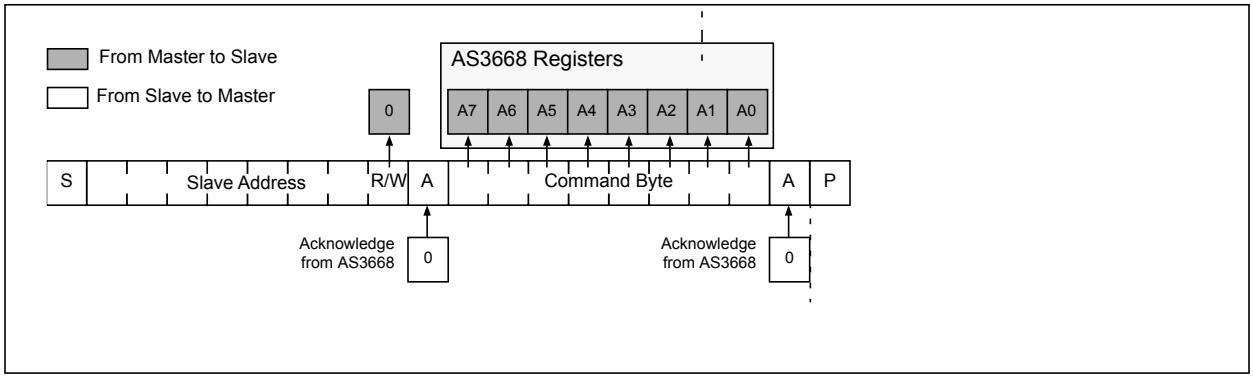
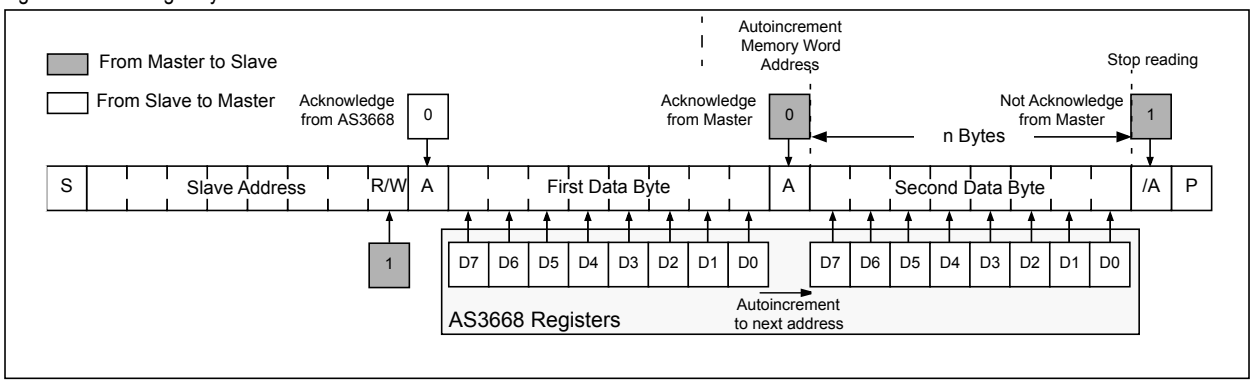


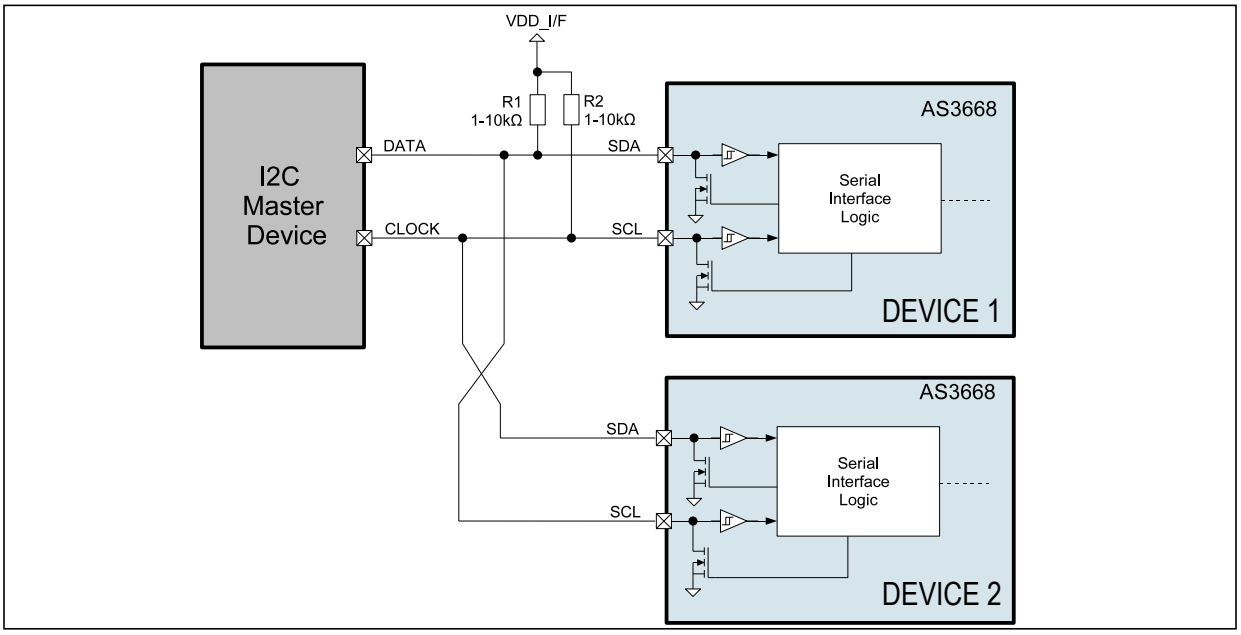
Figure 34. Reading n Bytes from AS3668



8.6.3 I²C Device Address Selection

The AS3668 features two I²C slave addresses without having a dedicated address selection pin. The selection of the I²C address is done with the interconnection of AS3668 to the bus lines shown in Figure 35 below. The serial interface logic inside AS3668 is able to distinguish between a direct I2C connection to the master or a second option where data and clock line are crossed. Therefore it is only possible to address a maximum of two AS3668 slaves on one I²C bus.

Figure 35. I²C Address Selection Application Diagram



The I²C addresses for the devices in the different connection modes can be found in Table 22.

Table 22. I²C Addresses for AS3668

DEVICE Number	7 bit I²C address	8 Bit read address	8 Bit write address
1(default)	0x42	0x85	0x84
2	0x43	0x87	0x86

8.7 Operating Modes

Due to the reason that AS3668 has no dedicated enable or power - on pin the device is basically controlled with the I²C signal lines SDA and SCL. If the voltages on these pins are less than V_{POR_PERI} for > t_{POR_DEB} and GPIO/AUDIO_IN input is low, the AS3668 is in shut down mode with a minimized current consumption of I_{VBAT} = 1µA (typ.). All blocks inside AS3668 are basically switched off except the power up reset circuit is always active.