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AS3676

Flexible Lighting Management (CP, DCDC, 13 Current Sinks, ADC, LED Test, LDO, DLS and Ambient Light sensing)

1 General Description

The AS3676 is a highly-integrated CMOS Power and Lighting Management Unit for mobile telephones, and other 1-cell Li+ or 3-cell NiMH powered devices.

The AS3676 incorporates one Step Up DC/DC Converter for white backlight LEDs, one high-power Charge Pump, one Analog-to-Digital Converter, 13 current sinks, LED in-circuit function test, a two wire serial interface, and control logic all onto a single device. It supports **ambient light sensor** processing and a Dynamic Luminance Scaling (**DLS**) input. Output voltages and output currents are fully programmable.

The AS3676 is part of the austriamicrosystems AS3675, AS3687/87XM and AS3689 lighting management unit family. It is software compatible to AS3687/87XM and AS3689 and pin and software compatible to AS3675.

2 Key Features

- High-Efficiency Step Up DC/DC Converter
 - Up to 26V/50mA for White LEDs
 - Programmable Output Voltage with External Resistors and Serial Interface
 - Over voltage Protection
- High-Efficiency High-Power Charge Pump
 - 1:1, 1:1.5, and 1:2 Mode
 - Automatic Up Switching (can be disabled and 1:2 mode can be blocked)
 - Output Current up to 400mA/500mA pulsed
 - Efficiency up to 95%
 - Very Low effective Resistance (2.5 Ω typ. in 1:1.5)
 - Only 4 External Capacitors Required:
 2 x 1µF Flying Capacitors, 2 x 2.2µF Input/Output Capacitors
 - Supports LCD White Backlight LEDs, or RGB LEDs
- 13 Current Sinks
 - All 13 current sinks fully Programmable (8-bit) from: 0.15mA to 38.5mA (up to 75.6mA for CURR30...CURR33)
 - Three current sinks are High Voltage capable (CURR1, CURR2, CURR6)
 - Programmable Hardware Control (Strobe, and Preview or PWM)
 - Selectively Enable/Disable Current Sinks
 - Dynamic Luminance Scaling (DLS) support to improve backlight operating time (can adjust any current source)

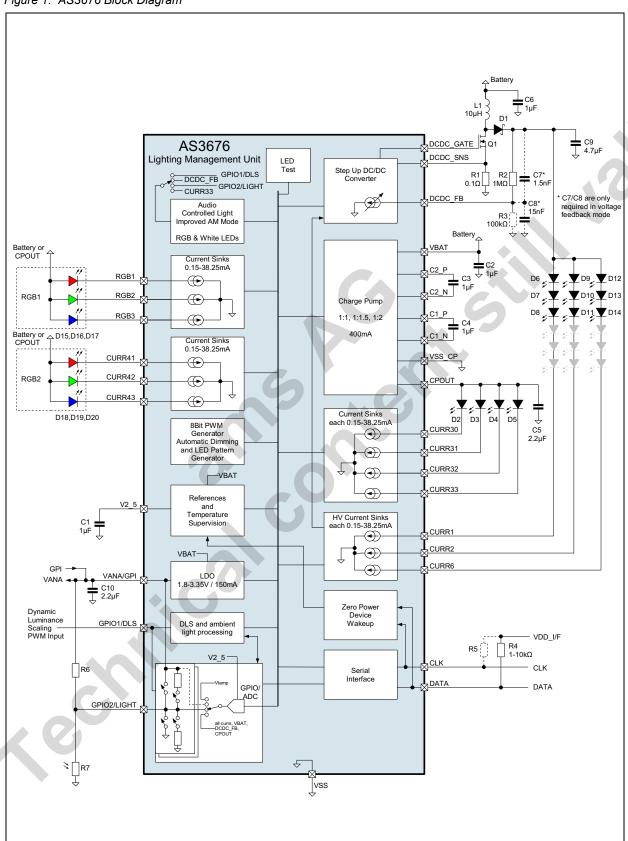
- Light Sensor input with internal hardware processing to control backlight according to ambient light using 3 groups any current source can select one of the groups or no light sensor control
- Internal PWM Generation
 - 8 Bit resolution
 - Autonomous Logarithmic up/down dimming
- Led Pattern Generator
 - Autonomous driving for Fun RGB LEDs
 - Support indicator LEDs
- 10-bit Successive Approximation ADC
 - 27µs Conversion Time
 - Selectable Inputs: VANA/GPI, GPIO1/DLS, GPIO2/LIGHT, all current sources, VBAT, CPOUT, DCDC_FB
 - Internal Temp. Measurement
 - Light Sensor input with Java support (JSR-256): read ADC processed value
- Support for automatic LED testing (open and shorted LEDs can be identified)
- Strobe Timeout protection
 - Up to 1600ms
 - Three different timing modes
- Two General Purpose Inputs/Output
 - GPIO1/DLS, GPIO2/LIGHT
 - Digital Input, Digital Output using VANA/GPI supply and Tristate
 - GPIOs Programmable Pull-Up/Down
- Programmable LDO
 - 1.8 to 3.35V, 150mA
 - Programmable via Serial Interface
- Standby LDO always on
 - Regulated 2.5V max. output 10mA
 - 3µA Quiescent Current
- Audio can be used to drive RGB LED(s)
 - Color and Brightness depends on audio amplitude
- Wide Battery Supply Range: 3.0 to 5.5V
- Two Wire Serial Interface Control
- Over current and Thermal Protection
- WL-CSP30 3x2.5mm, 0.5mm pitch Package

3 Applications

Power- and lighting-management for mobile telephones and other 1-cell Li+ or 3-cell NiMH powered devices.



Figure 1. AS3676 Block Diagram





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4 Pinout

Table 1. Pin Description for AS3676

Pin Number	Pin Name	Туре	Description
A1	GPIO1/DLS	AIO	Digital Luminance Scaling PWM input and General Purpose Input Output 1
A2	VANA/GPI	AIO	LDO Output/General Purpose Input
А3	C2_N	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 500nF to this pin.
A4	C1_P	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 500nF to this pin.
A5	CPOUT	АО	Output voltage of the Charge Pump; connect a ceramic capacitor of 1µF (±20%).
A6	DATA	DIO	Serial interface data input/output.
B1	GPIO2/LIGHT	AIO	Ambient Light Sensor input and General Purpose Input Output 2
B2	VSS_CP	GND	Ground Pad for Charge Pump
В3	C1_N	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 500nF to this pin.
B4	C2_P	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 500nF to this pin.
B5	DCDC_GATE	AO	DCDC gate driver.
В6	CLK	DI	Clock input for serial interface.
C1	CURR41	Al	Analog current sink input
C2	RGB3	Al	Analog current sink input
СЗ	VSS	GND	Ground pad
C4	VBAT	S	Supply pad. Connect to battery.
C5	CURR30	Al	Analog current sink input, intended for activity icon LED
C6	DCDC_SNS	Al	Sense input of shunt resistor for Step Up DC/DC Converter.
D1	CURR43	Al	Analog current sink input
D2	RGB1	Al	Analog current sink input
D3	CURR33	Al	Analog current sink input, intended for activity icon LED
D4	CURR31	Al	Analog current sink input, intended for activity icon LED
D5	CURR2	AI_HV	Analog current sink input (intended for Keyboard backlight)
D6	DCDC_FB	Al	DCDC feedback. Connect to resistor string.
E1	CURR42	Al	Analog current sink input
E2	RGB2	Al	Analog current sink input
E3	CURR32	Al	Analog current sink input, intended for activity icon LED
E4	CURR6	AI_HV	Analog current sink input (intended for Keyboard backlight)
E5	CURR1	AI_HV	Analog current sink input (intended for Keyboard backlight)
E6	V2_5	AO3	Output voltage of the Low-Power LDO; always connect a ceramic capacitor of $1\mu F$ ($\pm 20\%$) or $2.2\mu F$ ($\pm 100\%$ /- 50%).



4.1 Pin Definitions

Table 2. Pin Type Definitions

Туре	Description
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
AIO	Analog Pad
Al	Analog Input
AI_HV	High-Voltage (26V) Pin
AO3	Analog Output (3.3V)
S	Supply Pad
GND	Ground Pad



5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 4, "Operating Conditions," on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
VIN_HV	26V Pins	-0.3	26	٧	Applicable for high-voltage current sink pins CURR1, CURR2, CURR6
VIN_MV	5V Pins	-0.3	7.0	V	Applicable for 5V pins VBAT, CURR30-33, CURR41-43, RGB1-3, C1_N, C2_N, C1_P, C2_P, CPOUT, DCDC_FB, DCDC_GATE, CLK, DATA;
VIN_LV	VIN_LV 3.3V Pins		5.0	V	Applicable for 3.3V pins V2_5; DCDC_SNS, GPIO1/ DLS, GPIO2/LIGHT, VANA/ GPI
	Input Pin Current	-25	+25	mA	At 25°C, Norm: JEDEC 17
Tstrg	Storage Temperature Range	-55	125	°C	
lin	Humidity	5	85	%	Non-condensing
VESD	Electrostatic Discharge	-2000	2000	V	Norm: MIL 883 E Method 3015
Pt	Total Power Dissipation		0.75	W	TA = 70 °C, Tjunc_max = 125°C
TBODY	Peak Body Temperature		260	°C	T = 20 to 40s, in accordance with IPC/JEDEC J-STD 020.
MSL	MSL Moisture Sensitivity Level		SL 1		Represents a max. floor life time of unlimited

6 Electrical Characteristics

Table 4. Operating Conditions

Symbol	Parameter	Condition	Min	Тур	Max	Unit			
General Operating Conditions									
VHV	High Voltage	Applicable for high-voltage current sink pins CURR1, CURR2 and CURR6.	0.0		26.0	V			
VBAT	Battery Voltage	Pin VBAT	3.0	3.6	5.5	V			
VPERI	Periphery Supply Voltage	For serial interface pins.	1.5		5.5	V			
V2_5	Voltage on Pin V2_5	Internally generated	2.4	2.5	2.6	V			
Тамв	Operating Temperature Range		-30	25	85	°C			
IACTIVE	Battery current	Normal Operating current (see Operating Modes on page 80)		110		μΑ			
ISTANDBY	Standby Mode Current	Current consumption in standby mode. Only 2.5V regulator on, interface active		8	13	μΑ			
Ishutdown	Shutdown Mode Current	interface inactive (CLKand DATA set to 0V)		0.1	3	μΑ			



7 Typical Operating Characteristics

Figure 2. DCDC Step Up Converter: Efficiency of +15V, Step Up to 15V vs. Load Current at VBAT=3.8V Figure 3. Charge Pump: Efficiency vs. VBAT

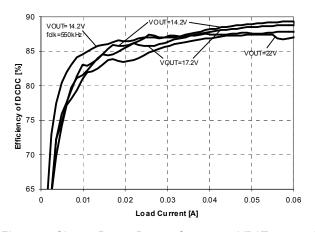
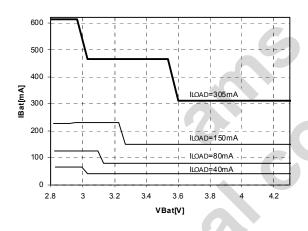


Figure 4. Charge Pump: Battery Current vs. VBAT





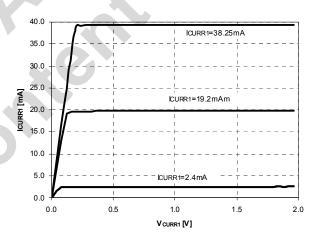


Figure 6.

Figure 7. Current Sink CURR3x vs. VBAT

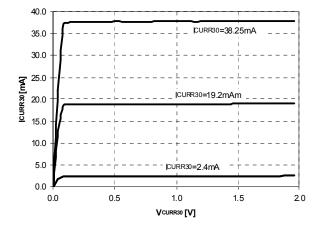
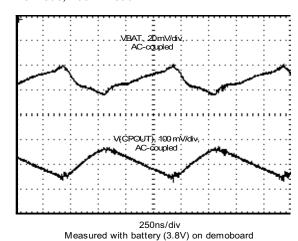


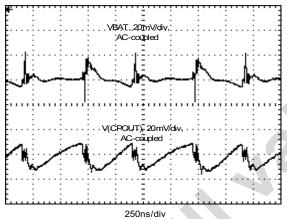


Figure 8. Charge Pump Input and Output Ripple 1:1.5 Mode, 100mA load



VBAT = 3.6V, $T_A = +25$ °C (unless otherwise specified).

Figure 9. Charge Pump Input and Output Ripple 1:2 Mode, 100mA load



Measured with battery (3.0V) on demoboard



8 Detailed Description

8.1 Analog LDO

The LDO is a general purpose LDO and the output pin connected to VANA/GPI. The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of $1\mu\text{F}$ ±20% (X5R) or $2.2\mu\text{F}$ +100/-50%(Z5U). The low ESR of these capacitors ensures low output impedance at high frequencies. The low impedance of the power transistor enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease in performance.

The LDO is off by default after start-up.

Figure 10. Analog LDO Block Diagram

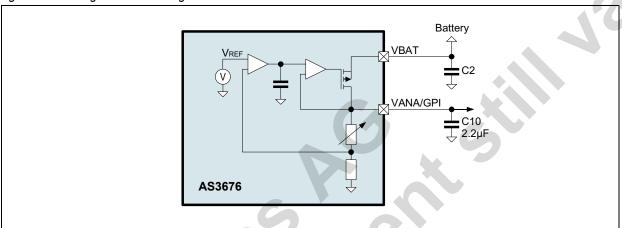


Table 5. Electrical Characteristics

Symbol	Parameter	Condition	Min	Тур	Max	Unit
VBAT	Supply Voltage Range		3.0		5.5	٧
Ron	On Resistance	@150mA, full operating temperature range			1.0	Ω
VDROPOUT	Dropout Voltago	@150mA			150	mV
VDROPOUT	Dropout Voltage	@50mA			50	mV
Ion	Supply Current Without load			50		
ION	Supply Current	With 150mA load		150		μΑ
loff	Shutdown Current	Without load			100	nA
tstart	Start-up Time				200	μs
Vout_tol	Output Voltage Tolerance		-3		+3	%
		VBAT = 3.0V and IOUT=150mA	1.8		2.85	٧
Vouт	Output Voltage	Full Programmable Range; VBAT > VOUT+ 150mV and IOUT<=150mA	1.8		3.35	V
ILIMIT ¹	LDO Current Limit	Pin VANA/GPI. LDO acts as current source if the output current exceeds ILIMIT.	300	450 ²		mA

- 1. Not production tested guaranteed by design and laboratory verification
- 2. During startup of the LDO the current limit is half the value of I_{LIMIT}



8.1.1 LDO Registers

Table 6. Reg. control Register

Addr: 00		Reg. control				
		This register enables/disables the LDOs, Charge Pumps, Charge Pump LEDs current sinks, the Step Up DC/DC Converter, and low-power mode.				
Bit	Bit Name	Default	Access	Description		
0	ldo on	0	R/W	0	Analog LDO is switched off	
U	100_011	U	FC/VV	1	Analog LDO is switched on	

Table 7. LDO Voltage Register

	Addr: 07h		LDO Voltage				
Addr: 0711		This register sets the output voltage (VANA/GPI) for the LDO.					
Bit	Bit Name	Default	Access	Description			
				Controls LDO voltage selection.			
4:0	ldo voltago	00000b R/W 00000b 1.8V LSB=50mV 11111b 3.35V	00000b 1.8V				
4.0	ldo_voltage (R/VV	LSB=50mV			
				11111b 3.35V			



8.2 Step Up DC/DC Converter

The Step Up DC/DC Converter is a high-efficiency current mode PWM regulator, providing output voltage up to e.g. 25V/50mA¹. A constant switching-frequency results in a low noise on the supply and output voltages.

Figure 11. Step Up DCDC Converter Block Diagram Option: Current Feedback with Over voltage protection

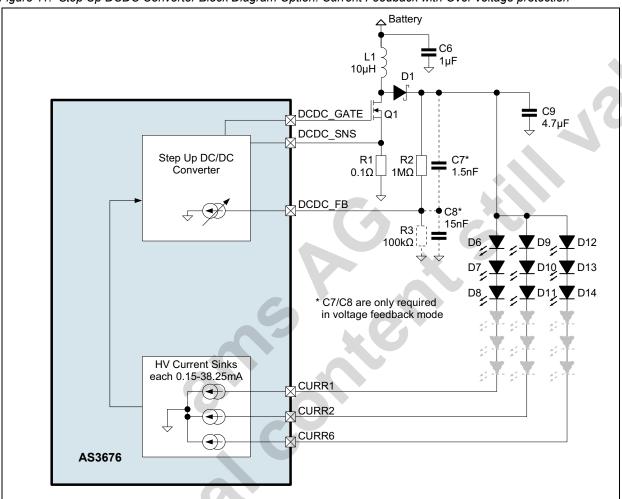


Table 8. Step Up DC/DC Converter Parameters

Symbol	Parameter	Condition	Min	Тур	Max	Unit
IVDD	Quiescent Current	Pulse skipping mode.		140		μΑ
VFB1	Feedback Voltage for External Resistor Divider	For constant voltage control. step_up_res = 1	1.20	1.25	1.30	>
VFB2	Feedback Voltage for Current Sink Regulation	on CURR1, CURR2 or CURR6 in regulation. step_up_res = 0	0.4	0.5	0.6	V

The AS3676 internal driver structure allows output voltage higher than 25V. The Over voltage Protection in Current Feedback Mode (see page 13) or Voltage Feedback (see page 14) should be set to fit to the external components used (maximum voltage rating of Q1, C9 and D1).



Table 8. Step Up DC/DC Converter Parameters

Symbol	Parameter	Condition	Min	Тур	Max	Unit
IDCDC_FB	Additional Tuning Current at Pin DCDC_FB and over voltage protection	Adjustable by software using Register DCDC control1 1µA step size (0-31µA) V _{PROTECT} = 1.25V +	0		31	μΑ
	Accuracy of Feedback Current at full scale	I _{DCDC_FB} * R ₂	-6		6	%
		e.g., 1.32A for 0.1Ω sense resistor R ₁ .	92	132	170	
Vrsense_max	Current Limit Voltage at R1	For fixed startup time of 500us	50	66	86	mV
		60	86	114		
Rsw	Switch Resistance	ON-resistance of external switching transistor.			1	Ω
ILOAD	Load Current	At 26V output voltage	0		50	mA
fin	Switching Frequency	Internally trimmed	0.9	1	1.1	MHz
Соит	Output Capacitor	Ceramic, ±20%. Use nominal 4.7µF capacitors to obtain at least 0.7µF under all conditions (voltage dependence of capacitors)	0.7	4.7		μF
L	Inductor	Use inductors with small C _{parasitic} (<100pF) to get high efficiency.	7	10	13	μH
tmin_on	Minimum on Time		90	140	190	ns
MDC	Maximum Duty Cycle		90			%
Vripple	Voltage ripple >20kHz	Cout-4.7uE lout-0.45mA \/PAT-2.0.4.2\/			160	mV
Vripple	Voltage ripple <20kHz	Cout=4.7µF,lout=045mA, VBAT=3.04.2V			40	mV
Efficiency	Efficiency	lout=20mA,Vout=17V,VBAT=3.8V		85		%

To ensure soft startup of the dcdc converter, the over current limits are reduced for a fixed time after enabling the dcdc converter. The total startup time for an output voltage of e.g. 26V is less than 2ms. If C7 and C8 are mounted and the bit step_up_prot is set, the total startup time can exceed 2ms.

Note: If the DCDC converter is only used in current feedback mode (CURR1, CURR2 or CURR6 - and not used for a constant voltage source), the capacitors C7 and C8 can be removed.

8.2.1 Feedback Selection

Register DCDC control1 and DCDC control2 selects the type of feedback for the Step Up DC/DC Converter.

The feedback for the DC/DC converter can be selected either by current sinks (CURR1, CURR2, CURR6) or by a voltage feedback at pin DCDC_FB. If the register bit step_up_fb_auto is set, the feedback path is automatically selected between CURR1, CURR2 and CURR6 (the lowest voltage of these current sinks is used).

Setting step_up_fb enables feedback on the pins CURR1, CURR2 or CURR6. The Step Up DC/DC Converter is regulated such that the required current at the feedback path can be supported. (Bit step_up_res should be set to 0 in this configuration)

Note: Always choose the path with the highest voltage drop as feedback to guarantee adequate supply for the other (unregulated) paths or enable the register bit step up fb auto.



8.2.2 Over voltage Protection in Current Feedback Mode

The over voltage protection in current feedback mode (step_up_fb = 01, 10 or 11 or step_up_fb_auto = 1) works as follows: Only resistor R2 and C7/C8² is soldered and R3 is omitted. An internal current source (sink) is used to generate a voltage drop across the resistor R2. If then the voltage on DCDC_FB is above 1.25V and step_up_prot=1, the DCDC is momentarily disabled to avoid too high voltages on the output of the DCDC converter. When the voltage on DCDC_FB drops below 1.25V, the DCDC automatically resumes operation.

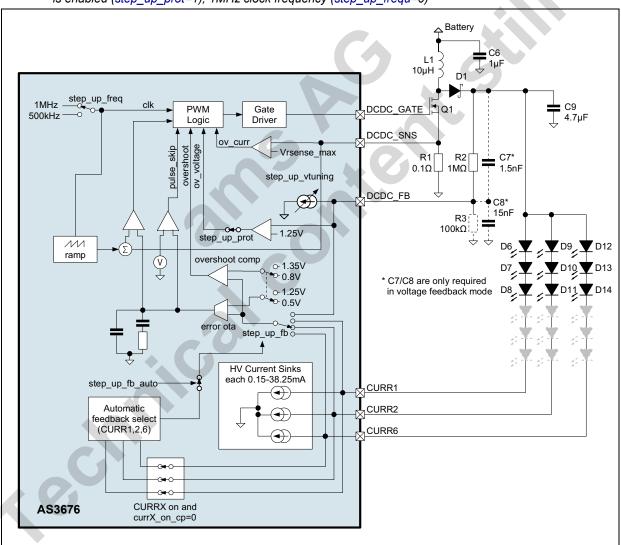
The protection voltage can be calculated according to the following formula:

$$VPROTECT = 1.25V + IDCDC_FB * R2$$
 (EQ 1)

Note: The voltage on the pin DCDC_FB is limited by an internal protection diode to VBAT + one diode forward voltage (typ. 0.6V).

If the over voltage protection is not used in current feedback mode, connect DCDC_FB to ground.

Figure 12. Step Up DC/DC Converter Detail Diagram; Option: Regulated Output Current, Feedback is automatically selected between CURR1, CURR2, CURR6 (step_up_fb_auto=1); over voltage protection is enabled (step_up_prot=1); 1MHz clock frequency (step_up_frequ=0)



^{2.} If the DCDC converter is only used in current feedback mode (CURR1, CURR2 or CURR6 - and not used for a constant voltage source), the capacitors C7 and C8 can be removed.



8.2.3 Voltage Feedback

Setting bit step_up_fb (see page 15) = 00 enables voltage feedback at pin DCDC_FB. Capacitors C7 and C8 have to be soldered in this operating mode.

The output voltage is regulated to a constant value, given by (Bit step up res should be set to 1 in this configuration)

$$U_{Step\ up\ out} = (R_2 + R_3)/R_3 *1.25 + I_{DCDC_FB} * R_2$$
 (EQ 2)

If R3 is not used, the output voltage is by (Bit step_up_res should be set to 0 in this configuration)

$$U_{Step\ up_out} = 1.25 + I_{DCDC_FB} * R_2$$
 (EQ 3)

Where:

U_{Step up out} = Step Up DC/DC Converter output voltage

R₂ = Feedback resistor R₂

R₃ = Feedback resistor R₃

IDCDC_FB = Tuning current at ball DCDC_FB; 0 to 31µA

Table 9. Voltage Feedback Example Values

IDCDC_FB	U _{Step up_out}	U _{Step up_out}
μΑ	R2 = 1M Ω , R3 not used	R2 = 500kΩ, R3 = 50kΩ
0	- (13.75
1	-	14.25
2	-	14.75
3	-	15.25
4	69 -	15.75
5	6.25	16.25
6	7.25	16.75
7	8.25	17.25
8	9.25	17.75
9	10.25	18.25
10	11.25	18.75
11	12.25	19.25
12	13.25	19.75
13	14.25	20.25
14	15.25	20.75
15	16.25	21.25
30	31.25	28.75
31	32.25	29.25

Note: The voltage on CURR1, CURR2 and CURR6 must not exceed 26V (see page 25)

8.2.4 PCB Layout Hints

To ensure good EMC performance of the DCDC converter, keep its external power components C6, R1, L1, Q1, D1 and C9 close together. Connect the ground of C6, R1 and C9 locally together and connect this with a short path to AS3676 VSS. This ensures that local high-frequency currents will not flow to the battery.

8.2.5 Unused DCDC converter

If the DCDC converter is not used, connect DCDC SNS to GND. DCDC FB³ and DCDC GATE can be left open.



8.2.6 Step up Registers

Table 10. Reg. control Register

Addr: 00		Reg. control					
		This register enables/disables the Charge Pump and the Step Up DC/DC Converter.					
Bit	Bit Name	Default	Access	Description			
		step_up_on 0 R/W			Enable the step up converter		
3	3 step_up_on 0 R/V		0b	Disable the Step Up DC/DC Converter			
				1b	Enable the Step Up DC/DC Converter		

Table 11. DCDC control1 Register

	Addr: 21h		DCDC control1					
	Addi. 2111	This register controls the Step Up DC/DC Converter.						
Bit	Bit Name	Default	Access		Description			
				Define	es the clock frequency of the Step Up DC/DC Converter.			
0	step_up_frequ	0	R/W	0	1MHz			
				1	500kHz			
				Control	s the feedback source if step_up_fb_auto = 0			
			5	00	DCDC_FB enabled (external resistor divider). Set step_up_fb=00 (DCDC_FB)			
2:1	2:1 step_up_fb	00	R/W	01	CURR1 feedback enabled (feedback via LEDs)			
				10	CURR2 feedback enabled (feedback via LEDs)			
				11	CURR6 feedback enabled (feedback via LEDs)			
				De	fines the tuning current at pin DCDC_FB.			
				00000	0 μΑ			
				00001	1 μΑ			
7.0	step_up_vtuning	00000	DAM	00010	2 μΑ			
7:3	step_up_vturiing	00000	R/W					
	• 0			10000	15 μΑ			
				11111	31 μΑ			

^{3.} DCDC_FB can be used as a general purpose ADC input (see Analog-to-Digital Converter on page 65)



Table 12. DCDC control2 Register

			DCDC control2					
	Addr: 22h	This register controls the Step Up DC/DC Converter and low-voltage current sinks CURR3x.						
Bit	Bit Name	Default	Access		Description			
				Gai	in selection for Step Up DC/DC Converter			
0	step_up_res	0	R/W	0	Select 0 if Step Up DC/DC Converter is used with current feedback (CURR1, CURR2, CURR6) or if DCDC_FB is used with current feedback only – R2, C7, C8 connected, R3 not used			
				1	Select 1 if DCDC_FB is used with external resistor divider using 2 resistors: R2 and R3			
				Step Up	DC/DC Converter output voltage at low loads, when pulse skipping is active			
1	skip_fast	0	R/W	0	Accurate output voltage, more ripple			
				1	Elevated output voltage, less ripple			
					Step Up DC/DC Converter protection			
2	step_up_prot	1	R/W	0	No over voltage protection			
				1	Over voltage protection on pin DCDC_FB enabled voltage limitation =1.25V on DCDC_FB			
				St	ep Up DC/DC Converter coil current limit			
3	step_up_lowcur	0	R/W	0	Normal current limit			
				1	Current limit reduced by approx. 33%			
				0	step_up_fb selects the feedback of the DCDC converter			
7	step_up_fb_auto	0	R/W	1	If step_up_fb is not DCDC_FB (00), then feedback is automatically chosen within the current sinks CURR1, CURR2 and CURR6. Only those are used for this selection, which are enabled (currX_mode must not be 00) and not connected to the charge pump (currX_on_cp must be 0).			

8.3 Charge Pump

The Charge Pump uses two external flying capacitors C3, C4 to generate output voltages higher than the battery voltage. There are three different operating modes of the charge pump itself:

- 1:1 Bypass Mode
 - Battery input and output are connected by a low-impedance switch
 - battery current = output current.
- 1:1.5 Mode
 - The output voltage is up to 1.5 times the battery voltage (without load), but is limited to VCPOUTmax all the time
 - battery current = 1.5 times output current.
- 1:2 Mode
 - The output voltage is up to 2 times the battery voltage (without load), but is limited to VCPOUTmax all the time
 - battery current = 2 times output current

As the battery voltage decreases, the Charge Pump must be switched from 1:1 mode to 1:1.5 mode and eventually in 1:2 mode in order to provide enough supply for the current sinks. Depending on the actual current the mode with best overall efficiency can be automatically or manually selected:

Examples:



(EQ 4)

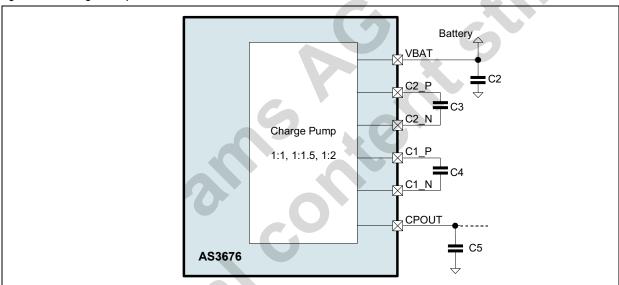
- Battery voltage = 3.7V, LED dropout voltage = 3.5V. The 1:1 mode will be selected and there is 200mV drop on the current sink and on the Charge Pump switch. Efficiency 95%.
- Battery voltage = 3.5V, LED dropout voltage = 3.5V. The 1:1.5 mode will be selected and there is 1.5V drop on the current sink and 250mV on the Charge Pump. Efficiency 66%.

The efficiency is dependent on the LED forward voltage given by:

The charge pump mode switching can be done manually or automatically with the following possible software settings:

- Automatic up all modes allowed (1:1, 1:1.5, 1:2)
 - Start with 1:1 mode
 - Switch up automatically 1:1 to 1:1.5 to 1:2
- Automatic up, but only 1:1 and 1:1.5 allowed
 - Start with 1:1 mode
 - Switch up automatically only from 1:1 to 1:1.5 mode; 1:2 mode is not used
- Manual
 - Set modes 1:1, 1:1.5, 1:2 by software

Figure 13. Charge Pump Pin Connections



The Charge Pump requires the external components listed in the following table:

Table 13. Charge Pump External Components

Symbol	Parameter	Condition	Min	Тур	Max	Unit
C2	External Decoupling Capacitor	Ceramic low-ESR capacitor between pins VBAT and VSS.		1.0		μF
C3, C4	External Flying Capacitor (2x)	Ceramic low-ESR capacitor between pins C1_P and C1_N, between pins C2_P and C2_N and between VBAT and VSS		1.0		μF
C5	External Storage Capacitor	Ceramic low-ESR capacitor between pins CPOUT and VSS, pins CPOUT and VSS. Use nominal 2.2µF capacitors (size 0603)		2.2		μF

Note: The connections of the external capacitors C2, C3, C4 and C5 should be kept as short as possible.



The maximum voltage on the flying capacitors C3 and C4 is VBAT.

Table 14. Charge Pump Characteristics

Symbol	Parameter	Condition	Min	Тур	Max	Unit
	Output Current Continuous	Depending on PCB layout	0.0		400	mA
ICPOUT	Output Current Pulsed	max. 200ms VCPOUT= VBAT * CPMODE – ILOAD * RCP	0.0		500	mA
VCPOUTmax	Output Voltage	Internally limited, Including output ripple			5.6	V
η	Efficiency	Including current sink loss; ICPOUT < 100mA.	60		90	%
ICP1_1.5	Power Consumption without Load	1:1.5 Mode		3.4		
ICP1_2	fclk = 1 MHz	1:2 Mode		3.8		mA
Rcp1_1	Effective Charge	1:1 Mode; VBAT ≥ 3.5V		0.57		
Rcp1_1.5	Pump Output Resistance (Open		2.65		Ω	
Rcp1_2	Loop, fclk = 1MHz)	1:1.2 Mode; VBAT ≥ 3.1V		3.25		
fclk Accuracy	Accuracy of Clock Frequency		-10		10	%
currhv_switch	CURR1, 2, 6 minimum voltage		,		0.45	٧
	CURR30-33, RGB1- 3, CURR41-3, minimum voltage	If the voltage drops below this threshold, the charge pump will use the next available mode			0.2	V
currlv_switch	CURR30-33 0-75.6mA range for strobe if curr3x_strobe_high=	(1:1 -> 1:1.5 or 1:1.5 -> 1:2)			0.4	>
	CP automatic up-	cp_start_debounce=0		240		μsec
tdeb	switching debounce time	After switching on CP (cp_on set to 1), if cp_start_debounce=1		2000		µsec

8.3.1 Charge Pump Mode Switching

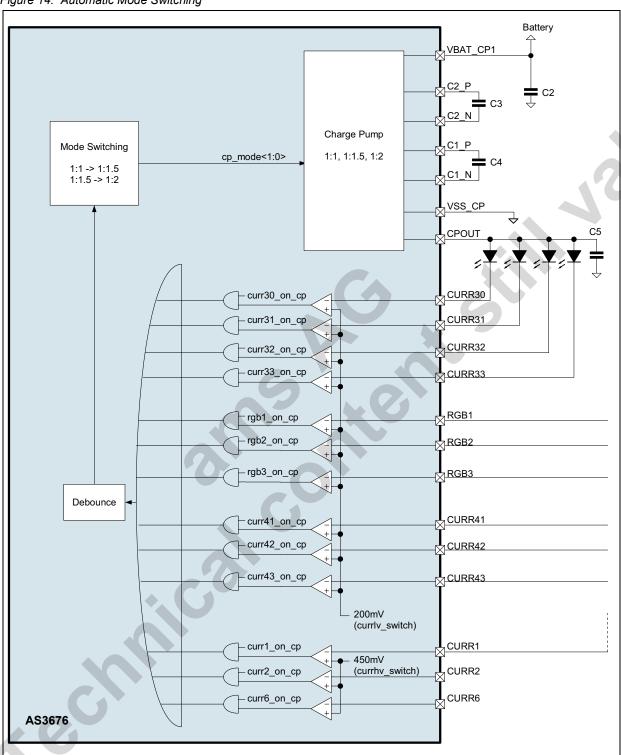
If automatic mode switching is enabled (cp_mode_switching (see page 20) = 00 or cp_mode_switching = 01) the charge pump monitors the current sinks, which are connected via a led to the output CPOUT. To identify these current sources (sinks), the registers CP mode Switch1 and CP mode Switch2 (register bits curr30_on_cp (see page 21) ... curr33_on_cp, rgb1_on_cp ... rgb3_on_cp, curr1_on_cp, curr2_on_cp, curr41_on_cp ... curr43_on_cp and curr6_on_cp) should be setup before starting the charge pump (cp_on (see page 20) = 1). If any of the voltage on these current sources drops below the threshold (currlv_switch, currhv_switch), the next higher mode is selected after the debounce time.

To avoid switching into 1:2 mode (battery current = 2 times output current), set cp_mode_switching = 01.

If the currX_on_cp=0 and the according current sink is connected to the charge pump, the current sink will be functional, but there is no up switching of the charge pump, if the voltage compliance is too low for the current sink to supply the specified current.



Figure 14. Automatic Mode Switching



8.3.2 Soft Start

An implemented soft start mechanism reduces the inrush current. Battery current is smoothed when switching the charge pump on and also at each switching condition. This precaution reduces electromagnetic radiation significantly.



8.3.3 Unused Charge Pump

If the charge pump is not used, capacitors C3, C4 and C5 can be removed. The pins C1_P, C1_N, C2_P, C2_N and CPOUT should be left open and keep register cp_on and cp_auto_on at 0 (default value).

8.3.4 Charge Pump Registers

Table 15. Reg. control Register

	Addr: 00h		Reg. control						
Addr: 00fi			This register controls the Charge Pump.						
Bit	Bit Name	Default	Access	Access Description					
2	cp_on	0 R/V	R/W	0	Set Charge Pump into 1:1 mode (off state) unless cp_auto_on is set				
	. –		1	Enable manual or automatic mode switching					

Table 16. CP control Register

		CP control						
	Addr: 23h	This re	This register enables/disables the Charge Pump and the Step Up DC/DC Converter.					
Bit	Bit Name	Default	Access		Description			
				Clock frequency selection.				
0	cp_clk	0	R/W	0	1 MHz			
				1	500 kHz			
				,	e Pump mode (in manual mode sets this mode, in utomatic mode reports the actual mode used) ¹			
0.4	an made	001	DAM	00	1:1 mode			
2:1	cp_mode	00b	R/W	01	1:1.5 mode			
				10	1:2 mode			
				11	NA			
					Set the mode switching algorithm			
				00	Automatic Mode switching; 1:1, 1:1.5 and 1:2 allowed			
4:3	cp_mode_switching	00b	R/W	01	Automatic Mode switching; only 1:1 and 1:1.5 allowed			
				10	Manual Mode switching; register cp_mode defines the actual charge pump mode used			
				11	Reserved			
				0	Mode switching debounce timer is always 240µs			
5	cp_start_debounce	0	R/W	1	Upon startup (cp_on set to 1) the mode switching debounce time is first started with 2ms then reduced to 240µs			
	5)			0	Charge Pump is switched on/off with cp_on			
6	cp_auto_on	0	R/W	1	Charge Pump is automatically switched on if a current sink, which is connected to the charge pump (defined by registers CP Mode Switch 1 & 2) is switched on			

^{1.} Direct switching from 1:1.5 mode into 1:2 in manual mode and vice versa is not allowed. Always switch over 1:1 mode.



Table 17. CP mode Switch1 Register

			CP mode Switch1						
Addr: 24h		Setup which current sinks are connected (via leds) to the charge pump; if set '1' the correspond current source (sink) is used for automatic mode selection the charge pump							
Bit	Bit Name	Default	Access		Description				
0	curr30_on_cp	0	R/W	0	current Sink CURR30 is not connected to charge pump				
				1	current sink CURR30 is connected to charge pump				
1	curr31_on_cp	0	R/W	0	current Sink CURR31 is not connected to charge pump				
				1	current sink CURR31 is connected to charge pump				
2	curr32_on_cp	0	R/W	0	current Sink CURR32 is not connected to charge pump				
				1	current sink CURR32 is connected to charge pump				
3	curr33_on_cp	0	R/W	0	current Sink CURR33 is not connected to charge pump				
				1	current sink CURR33 is connected to charge pump				
4	rgb1_on_cp	0	R/W	0	current Sink RGB1 is not connected to charge pump				
				1	current sink RGB1 is connected to charge pump				
5	rgb2_on_cp	0	R/W	0	current Sink RGB2 is not connected to charge pump				
	· · · · · · · · · · · · · · · · · · ·			1	current sink RGB2 is connected to charge pump				
6	rgb3_on_cp	0	R/W	0	current Sink RGB3 is not connected to charge pump				
	1950_011_0p			1	current sink RGB3 is connected to charge pump				

Table 18. CP mode Switch2 Register

Addr: 25h		CP mode Switch2					
		Setup which current sinks are connected (via LEDs) to the charge pump; if to '1' the correspond current source (sink) is used for automatic mode select of the charge pump					
Bit	Bit Name	Default	Access		Description		
0	curr1_on_cp	0	0 R/W	0	current Sink CURR1is not connected to charge pump		
				1	current sink CURR1 is connected to charge pump		
1	curr2_on_cp	0	R/W	0	current Sink CURR2 is not connected to charge pump		
				1	current sink CURR2 is connected to charge pump		
2	curr41_on_cp	0	R/W	0	current Sink CURR41 is not connected to charge pump		
				1	current sink CURR41 is connected to charge pump		
3	curr42 on cp 0	0	R/W	0	current Sink CURR42 is not connected to charge pump		
				1	current sink CURR42 is connected to charge pump		



Table 18. CP mode Switch2 Register (Continued)

		CP mode Switch2					
Addr: 25h		Setup which current sinks are connected (via LEDs) to the charge pum to '1' the correspond current source (sink) is used for automatic mode so of the charge pump					
Bit	Bit Name	Default	Access	Description			
4	curr43_on_cp	0	0 R/W		current Sink CURR43 is not connected to charge pump		
				1	current sink CURR43 is connected to charge pump		
7	curr6_on_cp	0	R/W	0	current Sink CURR6 is not connected to charge pump		
			1	current sink CURR6 is connected to charge pump			

Table 19. Curr low voltage status1 Register

			Curr low voltage status1						
Addr: 2Ah		Indicates the low voltage status of the current sinks. If the currX_low_v bit is set, the voltage on the current sink is too low, to drive the selected output current							
Bit	Bit Name	Default	Access		Description				
0	curr30 low v	NA	R	0	voltage of current Sink CURR30 >currlv_switch				
0	curso_low_v	INA	K	1	voltage of current Sink CURR30 <currlv_switch< td=""></currlv_switch<>				
1	curr21 low v	NA	R	0	voltage of current Sink CURR31 >currlv_switch				
'	curr31_low_v	INA	K	1	voltage of current Sink CURR31 <currlv_switch< td=""></currlv_switch<>				
2	ourr22 low v	NA	R	0	voltage of current Sink CURR32 >currlv_switch				
2	2 curr32_low_v			1	voltage of current Sink CURR32 <currlv_switch< td=""></currlv_switch<>				
2	ourr22 low v	NA		0	voltage of current Sink CURR33 >currlv_switch				
3	curr33_low_v	NA	R	1	voltage of current Sink CURR33 <currlv_switch< td=""></currlv_switch<>				
4	rah1 low v	NA	R	0	voltage of current Sink RGB1 >currlv_switch				
4	rgb1_low_v	NA	R	1	voltage of current Sink RGB1 <currlv_switch< td=""></currlv_switch<>				
_	rah? low v	NIA	_	0	voltage of current Sink RGB2 >currlv_switch				
5	rgb2_low_v	NA	R	1	voltage of current Sink RGB2 <currlv_switch< td=""></currlv_switch<>				
) NIA	D	0	voltage of current Sink RGB3 >currlv_switch				
6	rgb3_low_v	NA	R	1	voltage of current Sink RGB31 <currlv_switch< td=""></currlv_switch<>				
7	ourre low v	NA	R	0	voltage of current Sink CURR6 >currlv_switch				
/	7 curr6_low_v			1	voltage of current Sink CURR6 <currlv_switch< td=""></currlv_switch<>				

Table 20. Curr low voltage status2 Register

		Curr low voltage status2					
Addr: 2Bh		Indicate set, th	Indicates the low voltage status of the current sinks. If the currX_low_v bit is set, the voltage on the current sink is too low, to drive the selected output current				
Bit	Bit Name	Default	Access		Description		
0	0 curr1_low_v NA	NIA	ר	0	voltage of current Sink CURR1 >currhv_switch		
0		NA R	1	voltage of current Sink CURR1 <currhv_switch< td=""></currhv_switch<>			



Table 20. Curr low voltage status2 Register (Continued)

Addr: 2Bh		Curr low voltage status2					
			Indicates the low voltage status of the current sinks. If the currX_low_v bi set, the voltage on the current sink is too low, to drive the selected outpour current				
Bit	Bit Name	Default	Access		Description		
1	curr2 low v	NA	R	0	voltage of current Sink CURR2 >currhv_switch		
'	CuitZ_iow_v	INA	IX.	1	voltage of current Sink CURR2 <currhv_switch< td=""></currhv_switch<>		
2	curr41 low v	NA	R	0	voltage of current Sink CURR41 >currlv_switch		
2	Cu1141_low_v	INA	A K	1	voltage of current Sink CURR41 <currlv_switch< td=""></currlv_switch<>		
3	curr42 low v	NA	R	0	voltage of current Sink CURR42 >currlv_switch		
3	Cu1142_10W_V	INA	K	1	voltage of current Sink CURR42 <currlv_switch< td=""></currlv_switch<>		
4	4 curr43_low_v NA	NIA	R	0	voltage of current Sink CURR43 >currlv_switch		
4		ĸ	1	voltage of current Sink CURR43 <currlv_switch< td=""></currlv_switch<>			



8.4 Current Sinks

The AS3676 contains general purpose current sinks intended to control RGB LEDs, white LEDs (e.g. backlights) and can also be used for buzzers or vibrators. All current sinks have an integrated over voltage protection.

CURR1, CURR2 and CURR6 are also used as feedback for the Step Up DC/DC Converter (regulated to 0.5V in this configuration) see Feedback Selection on page 12.

- Current sinks CURR1, CURR2 and CURR6 are high-voltage compliant (26V) current sinks, used e.g., for series of white LEDs
- Current sinks CURR3x (CURR30, CURR31, CURR32 and CURR33) are parallel 5V current sinks, used for backlighting, indicator LEDs or RGB LEDs.
- Current sinks RGB1, RGB2, and RGB3 are general purpose current sinks e.g. for a fun LED.
- Current sinks CURR4x (CURR41, CURR42, and CURR43) are general purpose current sinks.

Table 21. Current Sink Function Overview

Current Sink	Max. Voltage (V)	Max. Current (mA)	Resolution		Software Current	Hardware On/Off	Can be assigned to Audio Controlled
			(Bits)	(mA)	Control	Control	LED Channel
CURR1	26.0	38.25	8	0.15	Separate	LED Pattern; Internal PWM; external PWM at GPIO1/DLS	ch1
CURR2							ch2
CURR6							ch3
CURR30	VBAT (5.5V)	38.25		0.15	Combined in Strobe/ Preview or Separated	Flash LED Strobe (CURR1 or CURR30) & Preview (CURR2); Internal PWM; LED Pattern; external PWM at GPIO1/DLS	Completely individual assignment of the audio channels ch1,ch2 and ch3 to the outputs
CURR31		(75.6mA for strobe					
CURR32		curr3x_str obe_high= 1)					
CURR33							
RGB1		38.25	8	0.15	Separate	LED Pattern; Internal PWM; external PWM at GPIO1/DLS	ch1
RGB2							ch2
RGB3							ch3
CURR41		38.25	8	0.15	Separate	LED Pattern; Internal PWM; external PWM at GPIO1/DLS	ch1
CURR42							ch2
CURR43							ch3

8.4.1 Unused Current Sinks

Unused current sinks can be left open or used as a ADC input (see Analog-to-Digital Converter on page 65).