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AS3701

Micro-PMIC

General Description

The AS3701 is a small compact PMU for small size and low power applications.

AS3701 features one 500mA DCDC buck converter operating from 1MHz up to 4MHz, two 200mA LDOs, two 40mA current sinks and offers additional GPIO functions. Further, the device contains an integrated linear battery charger with constant current and constant voltage operation. The wide charging current range going from 11mA up to 500mA and the integrated battery temperature monitoring with selectable NTC beta values make this device suitable for a great variety of applications.

The single supply voltage may vary from 2.7V to 5.5V and all functionalities of AS3701 can be controlled via the I^2C interface.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3701, Micro-PMIC are listed below:

Figure 1:
Added Value of Using AS3701

Benefits	Features
• Multiple rails in a compact design for low power applications	• 2 x 200mA universal LDO (1.2V to 3.3V) • 500mA Step-down DCDC (0.6125V to 3.35V) • 2 programmable current sources up to 40mA • Possible external PWM dimming input
• Self-contained Li-Ion battery charger with power path	• Linear charger with internal transistor • 500mA max charging current • Trickle-, Constant Current and Constant Voltage operation (3.82V to 4.44V) • Charger timeout and temperature supervision • NTC beta selection
• Flexible multi-purpose IOs for general control tasks and for standalone operation without I^2C interface	• Wake-up / Stand-by / Power-down input • PWM input/output • Interrupt input/output • Low battery and Power Good output • Charging and USB current setting input • Charger control input/output

Benefits	Features
• Flexible and fast adaption to different processors/applications	• OTP programmable Boot sequence
• Power saving control according to the processor´s needs	• Stand-by function with programmable voltages
• Self-contained start-up and safety shutdown feature	• I^2C control interface • ON-key with 4/8s emergency power-down • POR with Reset I/O
• Cost effective, small package optimized for PCB cost or size	• 17-balls WL-CSP with 0.4mm pitch • 20-balls WL-CSP with 0.4mm pitch

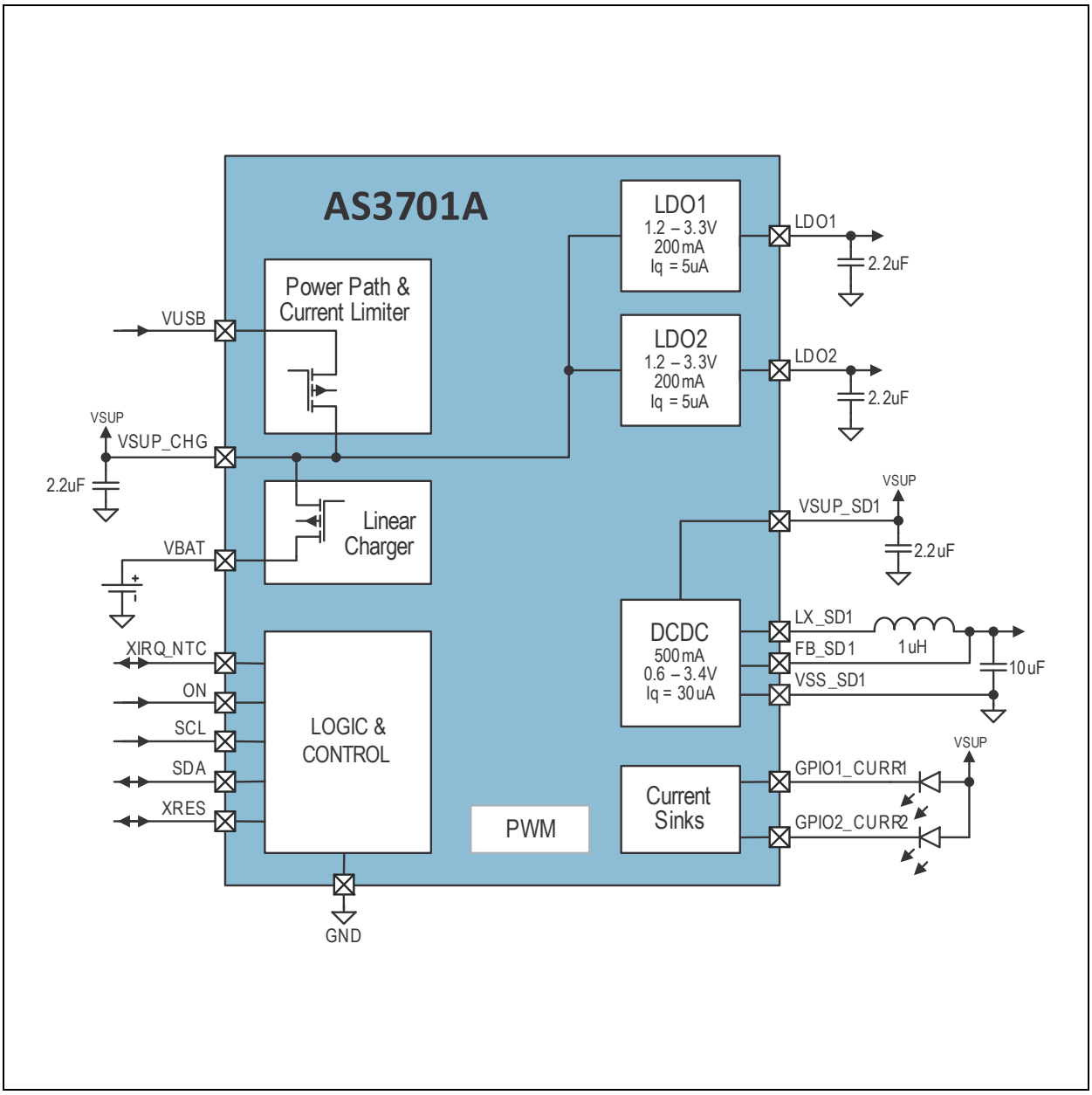
Applications

The device is a PMU for low power applications like sport watches, smart watches, handheld GPS devices, mobile phones and any other 1-cell Li+ powered devices.

Block Diagram

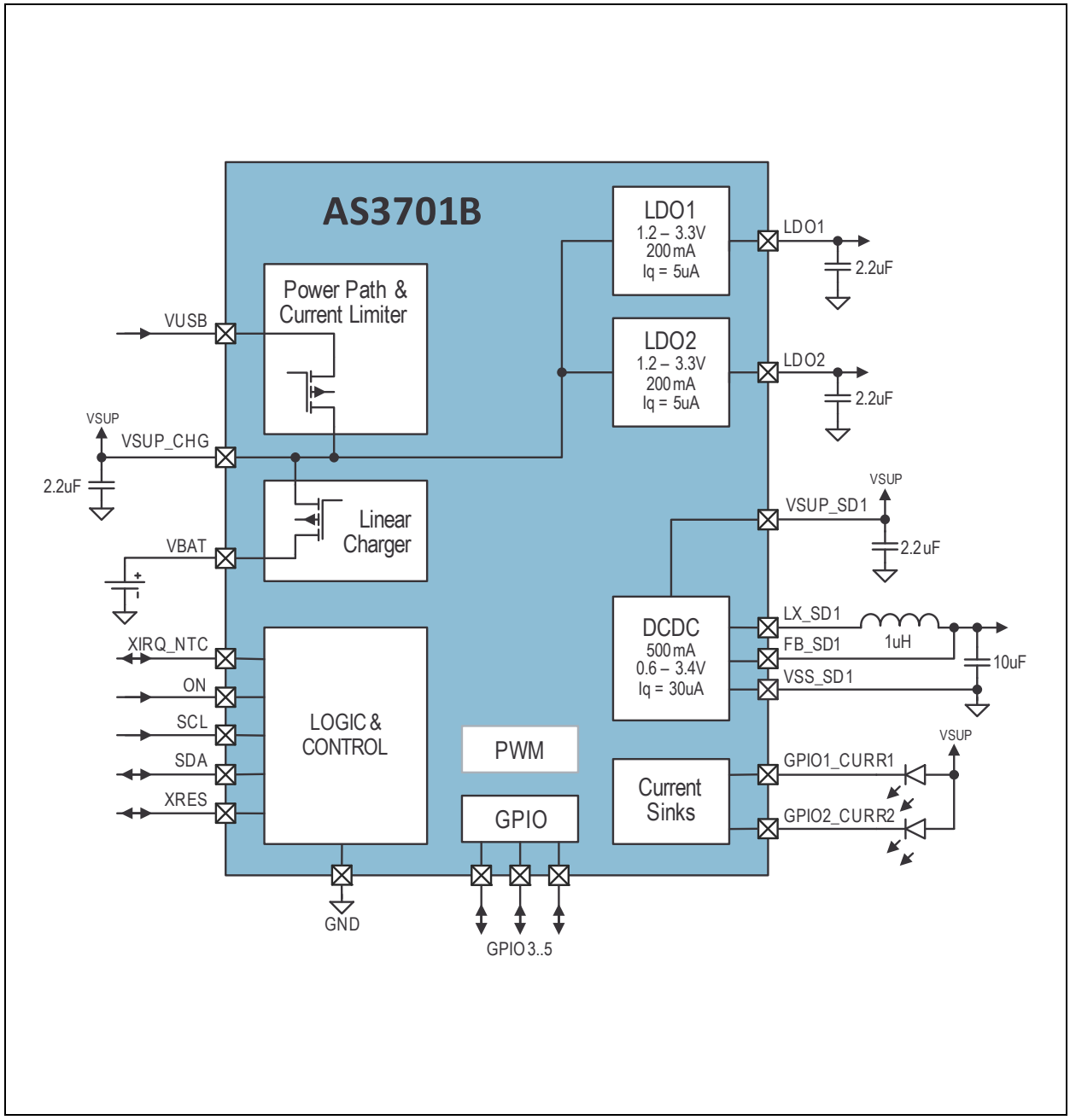
The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of AS3701A



Block Diagram: This figure shows the block diagram of the AS3701A

Figure 3:
Functional Blocks of AS3701B



Block Diagram: This figure shows the block diagram of the AS3701B

Pin Assignments

Figure 4:
17-balls WL-CSP Pin Assignment for AS3701A

Pin Assignments: Shows the top view pin assignment of the AS3701A

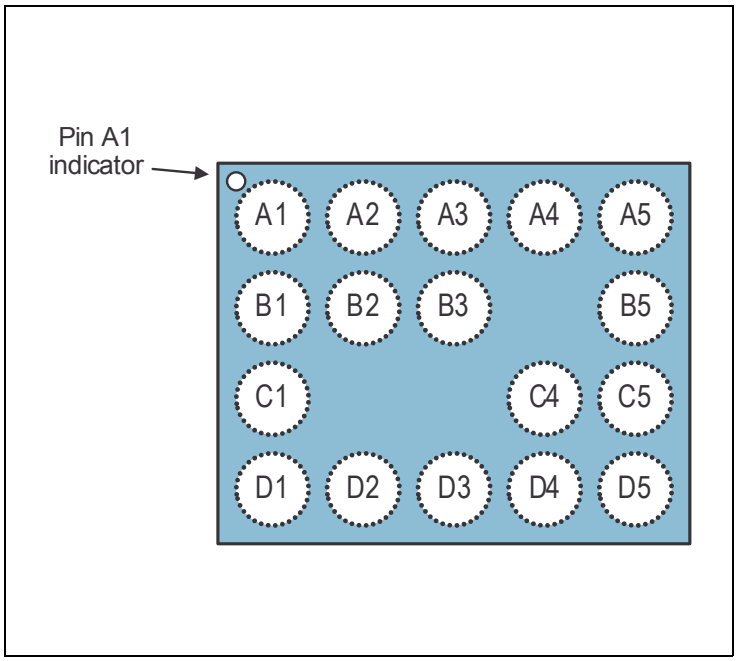


Figure 5:
20-balls WL-CSP Pin Assignment for AS3701B

Pin Assignments: Shows the top view pin assignment of the AS3701B

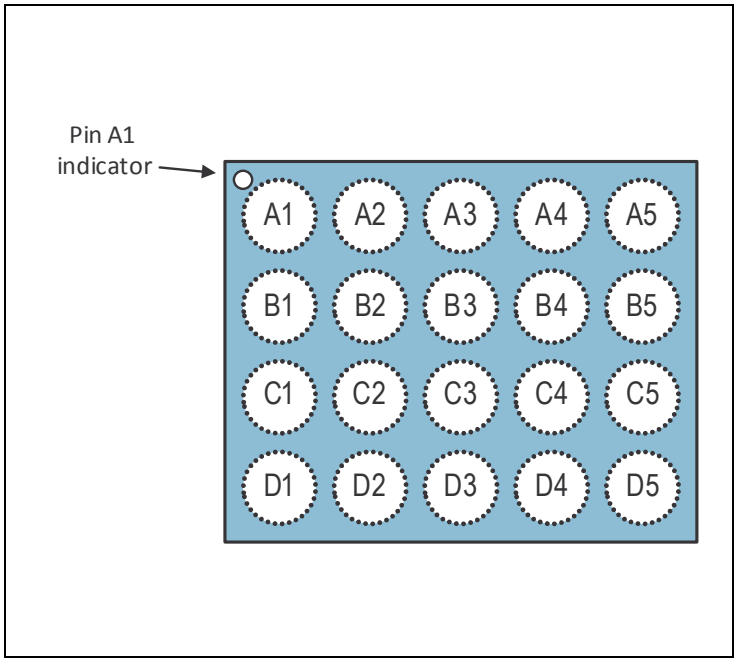


Figure 6:
Pin Description

Pin Number		Pin Name	I/O	Description	Max. Voltage	If Not Used
17 Balls	20 Balls					
A2	A2	VUSB	S	Wall adapter or USB Bus Power input (before protection)	5.5V	pull-down to GND
A1	A1	VSUP_CHG	SIO	Current limiter output, LDO1 & LDO2 pos. supply terminal	VSUP	Mandatory
D2	D2	VSUP_SD1	S	DCDC pos. supply terminal	VSUP	Mandatory
B1	B1	VBAT	S	Li-Ion Battery Terminal	5.5V	Open
A5	A5	GND	AIO	Reference GND	-	Mandatory
A4	A4	LDO1	AO	LDO1 Output	3.3V	Open
A3	A3	LDO2	AO	LDO2 Output	3.3V	Open
D1	D1	LX_SD1	AIO	DCDC Step Down Switch Output to Coil	5.5V	Open
B2	B2	FB_SD1	AI	DCDC Step Down Feedback Pin	3.6V	Open
D4	D4	XRES	DIO	Reset IO	VSUP	Open
D3	D3	ON	DI	Power Up Input	5.5V	Open
B3	B3	XIRQ_NTC	AIO	Interrupt Output or NTC Input	VSUP	Open
D5	D5	SCL	DI	2-wire Serial IF Clock Input	VSUP	pull-up to VSUP
C4	C4	SDA	DIO	2-wire Serial IF Data I/O	VSUP	pull-up to VSUP
C5	C5	GPIO1_ CURR1	DIO	General Purpose IO1 or LED Channel 1	VSUP	Open
B5	B5	GPIO2_ CURR2	DIO	General Purpose IO2 or LED Channel 2	VSUP	Open
-	B4	GPIO3	DIO	General Purpose IO3	VSUP	Open
-	C2	GPIO4	DIO	General Purpose IO4	VSUP	Open
-	C3	GPIO5	DIO	General Purpose IO5	VSUP	Open
C1	C1	VSS_SD1	AIO	GND connector of DCDC	-	Mandatory

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 7:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{GND}	Supply voltage to ground 5V pins	-0.5	7.0	V	Applicable for pins VSUP_CHG, VSUP_SD1, VBAT, VUSB, LX_SD1, SCL, SDA, ON, XRES, XIRQ_NTC, GPIO3, GPIO4, GPIO5, GPIO1_CURR1, GPIO2_ CURR2
V_{GND}	Supply voltage to ground 3V pins	-0.5	5.0	V	Applicable for pins LDO1, LDO2, FB_SD1
	Voltage difference between ground terminals	-0.5	0.5	V	Applicable for pins GND, VSS_SD1
I_{SCR}	Input current (latch-up immunity)	-100	100	mA	JEDEC JESD78
Continuous Power Dissipation (T_A = 70°C)					
P_T	Continuous power dissipation		0.96	W	P_T (1) for WL-CSP20 (R_{THJA} ~ *57K/W*)
Electrostatic Discharge					
ESD_{HBM}	Electrostatic discharge (human body model)	±2		kV	JEDEC JESD22-A114F

Symbol	Parameter	Min	Max	Units	Comments
Temperature Ranges and Storage Conditions					
T_A	Operating temperature	-40	85	°C	
R_{THJA}	Junction to ambient thermal resistance			°C/W	R_{THJA} typ. 57K/W
T_J	Junction temperature		125	°C	
T_{STRG}	Storage temperature range	-55	125	°C	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020 (2)
RH_{NC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level	1			Represents an unlimited floor life time

Note(s):

1. Depending on actual PCB layout and PCB used
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non hermetic Solid State Surface Mount Devices"

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 8:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range	Pin VSUP	2.7		5.5	V
I_{Q_ACTIVE}	Active mode quiescent current	Normal operating current		26		uA
$I_{Q\_STAND-BY}$	Stand-by quiescent current	Normal operating current (Oscillator ON)		26		
		Normal operating current (Oscillator OFF)		11.5		
$I_{POWEROFF}$	Shutdown current	*power_off* = 1		1.2		

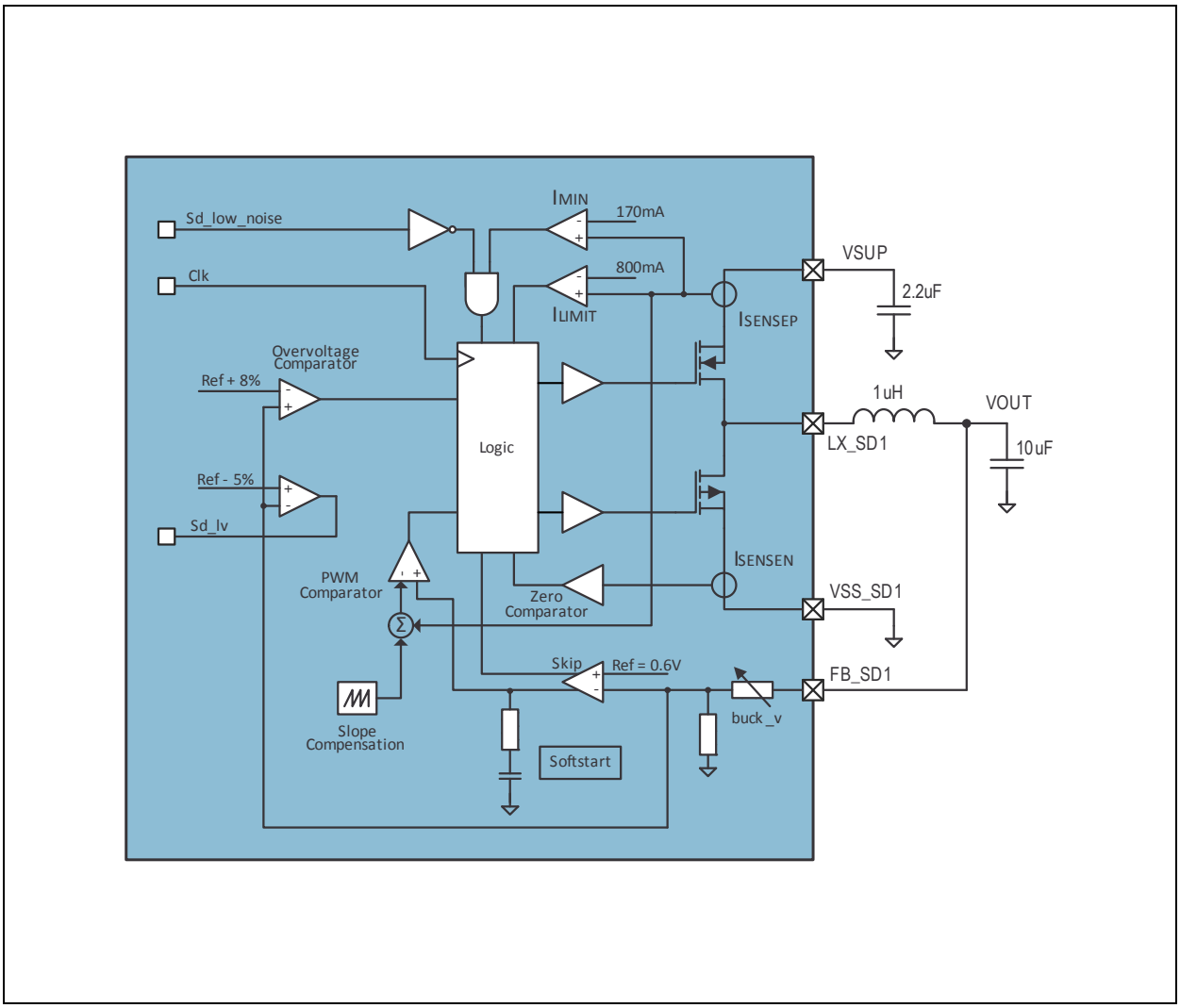
Electrical Characteristics: V_{SUP} = 3.7V, $V_{OUT} < V_{IN} - 0.5V$, T_{AMB} = -40°C to 85°C, typ. values @ T_{AMB} = 25°C (unless otherwise specified)

Detailed Description – Power Management Functions

Step Down Converter

The step-down converter is a high-efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches, efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to the maximum output current, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC Converter and the coil during overload condition.

Figure 9:
DCDC Step-Down Converter Block Diagram

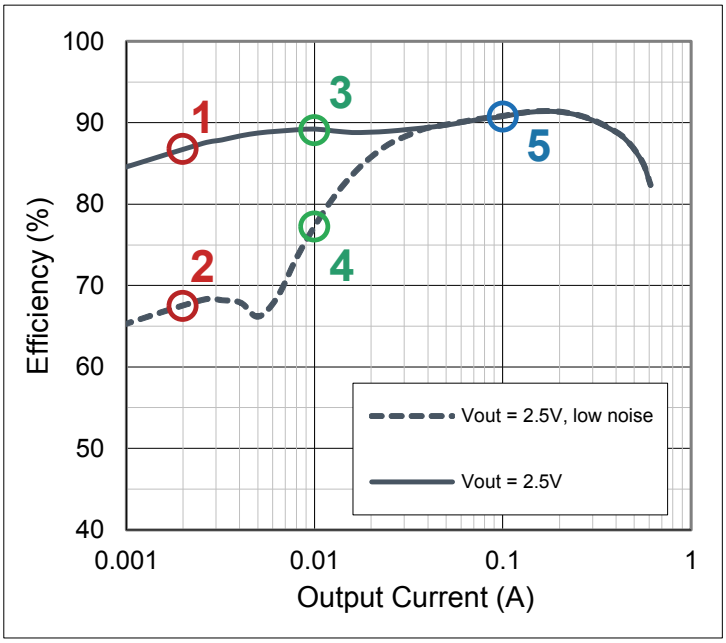


Mode Settings

To allow optimized performance in different applications, there are bit settings possible, to get the best compromise between high efficiency and low input/output ripple.

Figure 10:
DCDC Step-Down Converter Mode Settings

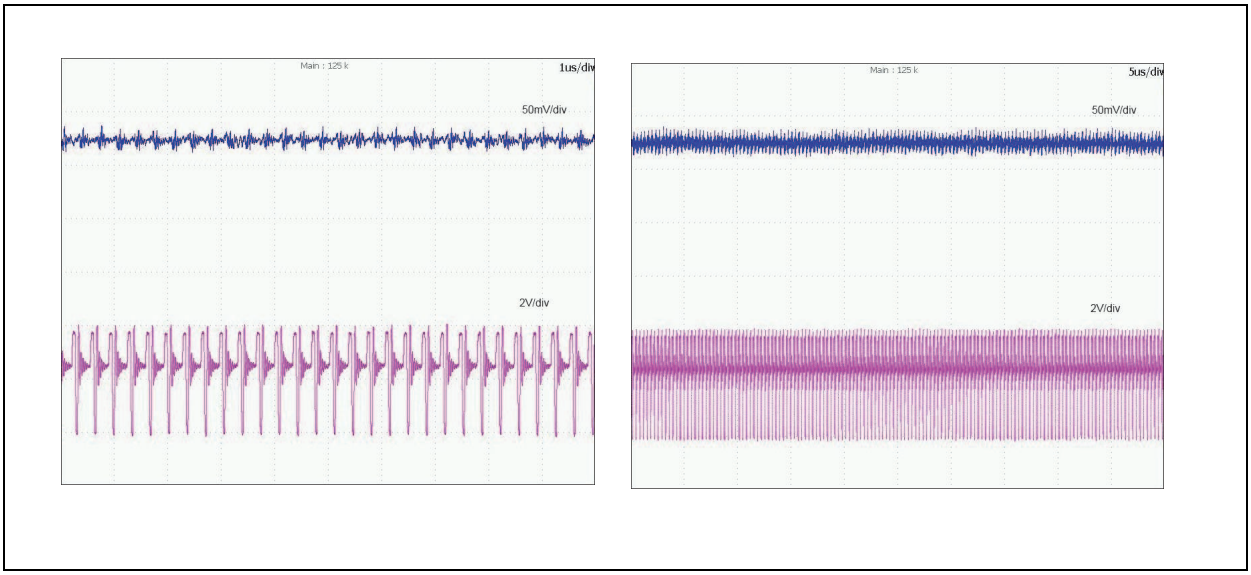
Mode Setting: This graph shows the difference of the efficiency curves for high efficiency and low noise mode setting. V_{SUP} = 3.7V, V_{OUT} = 2.5V, f_{SW} = 3MHz, T_{AMB} = 25°C.



Low-Ripple, Low-Noise Operation

Low-ripple, low-noise operation can be enabled by setting the bit *sd_low_noise [SD_control1]* to 1.
In this mode there is no minimum coil current necessary before switching OFF the PMOS. As long as the load current is superior to the ripple current, the device operates in continuous mode. When the load current gets lower, the discontinuous mode is triggered. Resultant the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to t_{MIN_ON} to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency at light loads, especially at low input to output voltage differences.

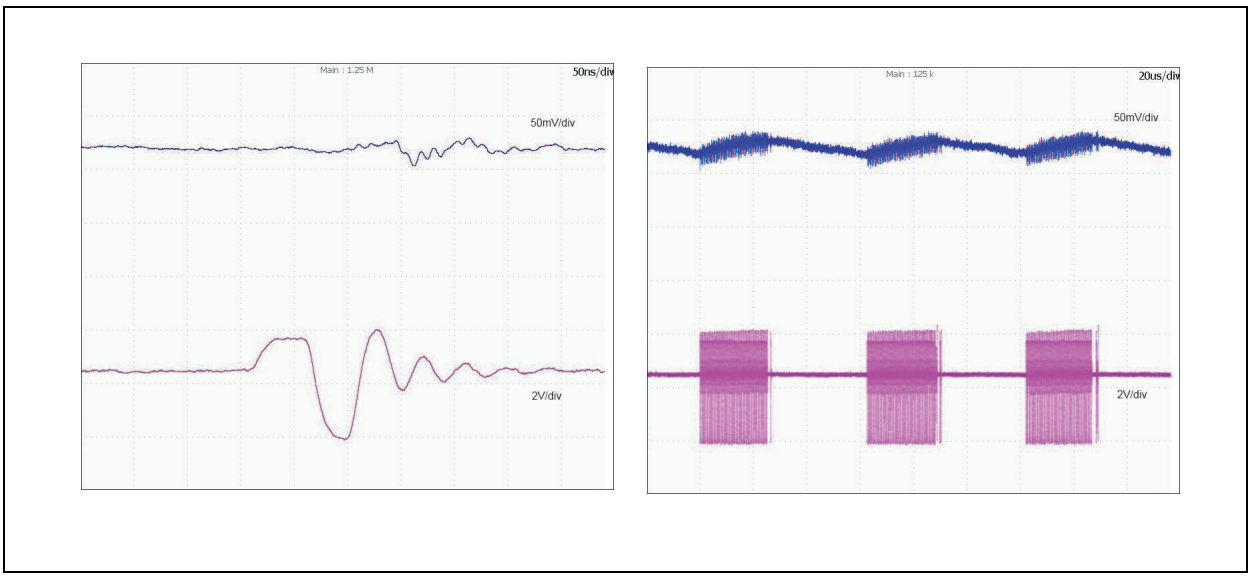
Figure 11:
Switching Behavior at Operating Point 4



Operating Point 4: These graphs show the switching behavior referring to the operating point 4 from figure10. Here the mode is set to low noise/low ripple operation and the DCDC is continuously switching at 10mA load current.

Only in the case the load current gets so small, that less than the minimum on time of the PMOS would be needed to keep the loop in regulation, the regulator will enter low power mode operation.

Figure 12:
Switching Behavior at Operating Point 2



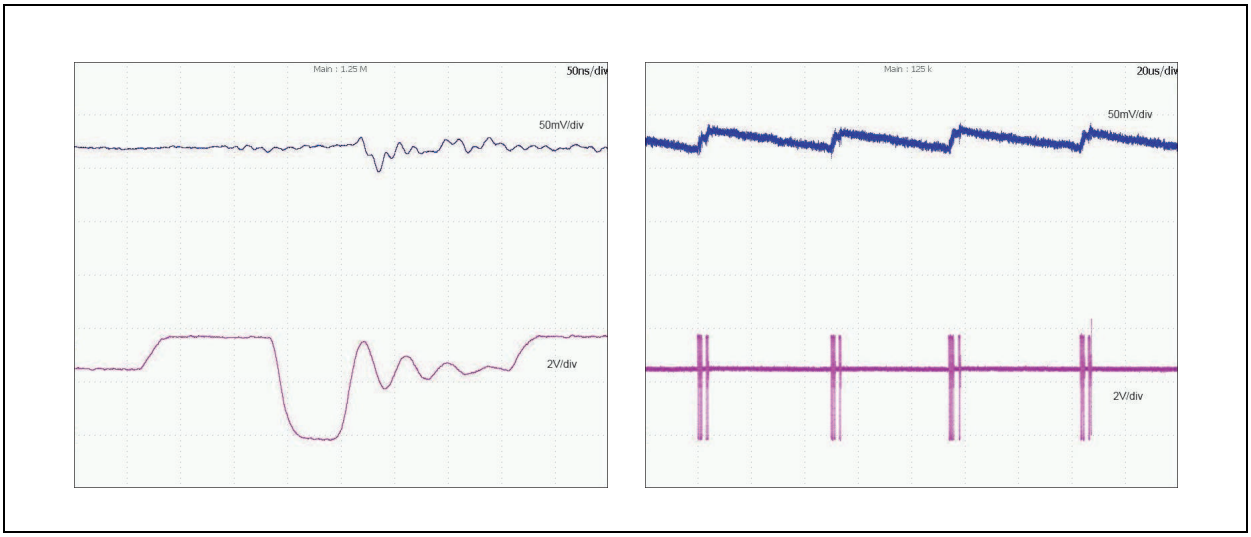
Operating Point 2: These graphs show the switching behavior referring to the operating point 2 from figure10. Here the mode is set to low noise/low ripple operation and the DCDC has already started to skip pulses, as the minimum PMOS ON time of 40ns has been reached and the load current is further decreasing down to 2mA.

High-Efficiency Operation (Default Setting)

High-efficiency operation is enabled by setting the bit sd_low_noise [SD_control1] to 0.

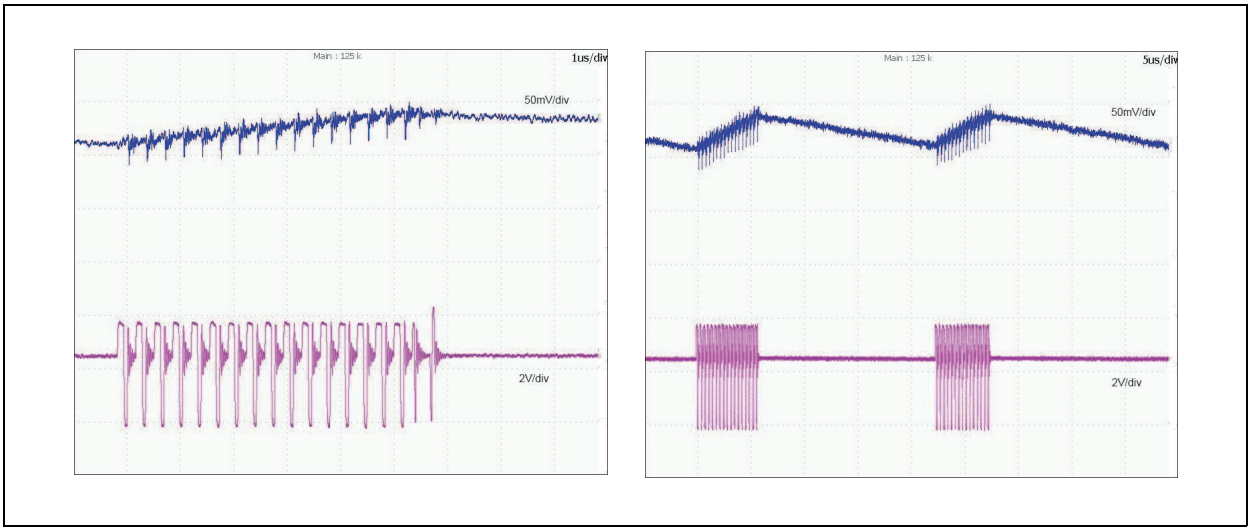
In this mode there is a minimum coil current necessary before switching OFF the PMOS. Resultant there are less pulses necessary at low output loads, and therefore the efficiency increases. As drawback, this mode increases the ripple up to a higher output current.

Figure 13:
Switching Behavior at Operating Point 1



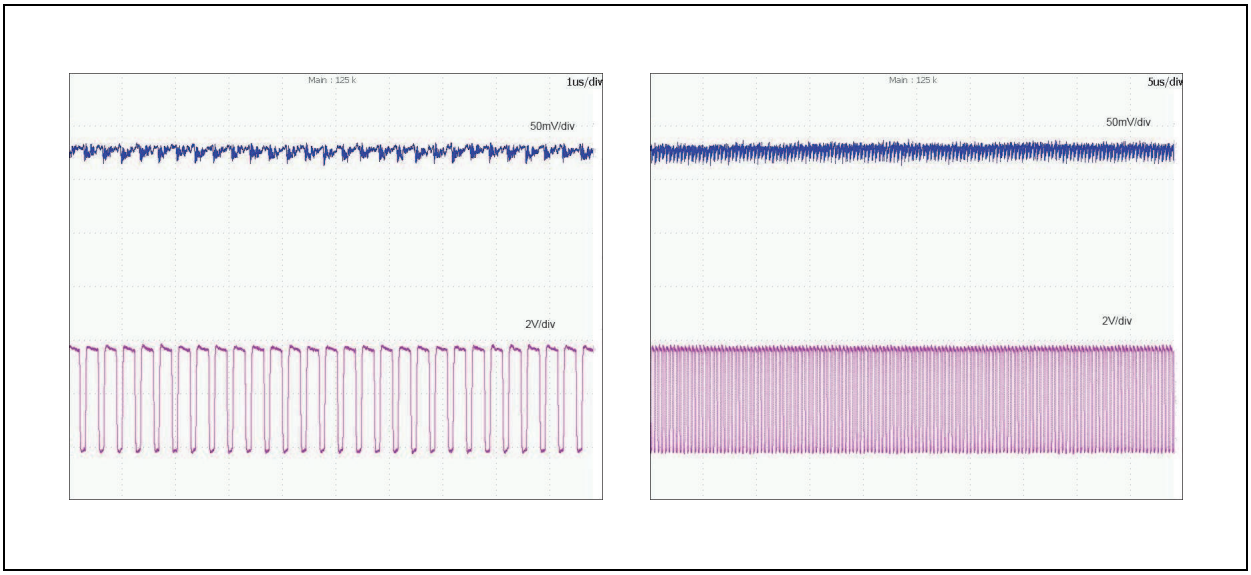
Operating Point 1: These graphs show the switching behavior referring to the operating point 1 from figure10. Here the mode is set to high efficiency operation and the DCDC is in skipping mode at 2mA load current. Here a minimum coil current during the PMOS ON time is needed, hence more energy can be stored, the duration between the bursts is longer and the efficiency increases.

Figure 14:
Output Voltage Ripple Measurement at Operating Point 3



Operating Point 3: These graphs show the switching behavior referring to the operating point 3 from figure10. Here the mode is set to high efficiency operation and comparing to operating point 4 the DCDC is still in skipping mode at 10mA load current and keeps the efficiency higher.

Figure 15:
Output Voltage Ripple Measurement at Operating Point 5



Operating Point 5: These graphs show the switching behavior referring to the operating point 5 from figure10. Here the load current is 100mA and high enough to keep the DCDC always in a continuous switching operation regardless of the mode setting.

Low Power Mode Operation (Automatically Controlled)

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at ±5% of the target value to react quickly on large over/undershoots by immediately turning ON the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

Dynamic Voltage Management

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled with *dvm_enable [SD_control2]*. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. The DVM time can be chosen between 8us and 16us by setting the bit *dvm_time [SD_control2]*. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs a 22uF output capacitor instead the 10uF one to guarantee the stability of the regulator.

The mode is enabled by setting the bit *sd_fast [SD_control1]* to 1.

Selectable Frequency Operation

Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency. The frequency can be set to 1, 2, 3 or 4MHz and this mode is selected by setting *sd1_freq [SD1Voltage]* and *sd1_fsel [SD_control1]* to the appropriate values.

Parameters

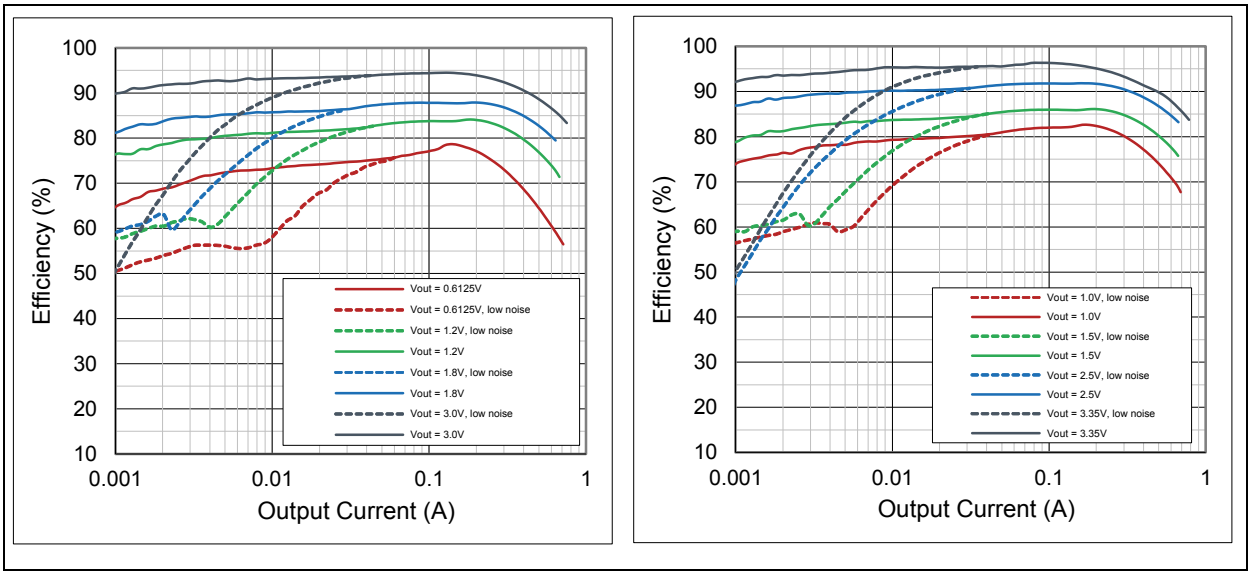
Figure 16:
DCDC Step-Down Converter Electrical Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IN}	Input Voltage	Pin VSUP	2.7		5.5	V
V_{OUT}	Regulated Output Voltage		0.6125		3.35	V
V_{OUT_TOL}	Output Voltage Tolerance	min. 40mV	-3		+3	%
I_{LIMIT}	Current Limit			800		mA
R_{PMOS}	P-switch ON resistance			0.36	1	Ω
R_{NMOS}	N-switch ON resistance			0.33	1	Ω
f_{SW}	Switching Frequency		1	3	4	MHz
I_{LOAD}	Load Current			500		mA
I_{SUP_DCDC}	Current Consumption	Operating Current without Load		27		uA
		Shutdown Current		0.1		
t_{MIN_ON}	Minimum ON Time			40		ns

Figure 17:
DCDC Step-Down Converter External Components

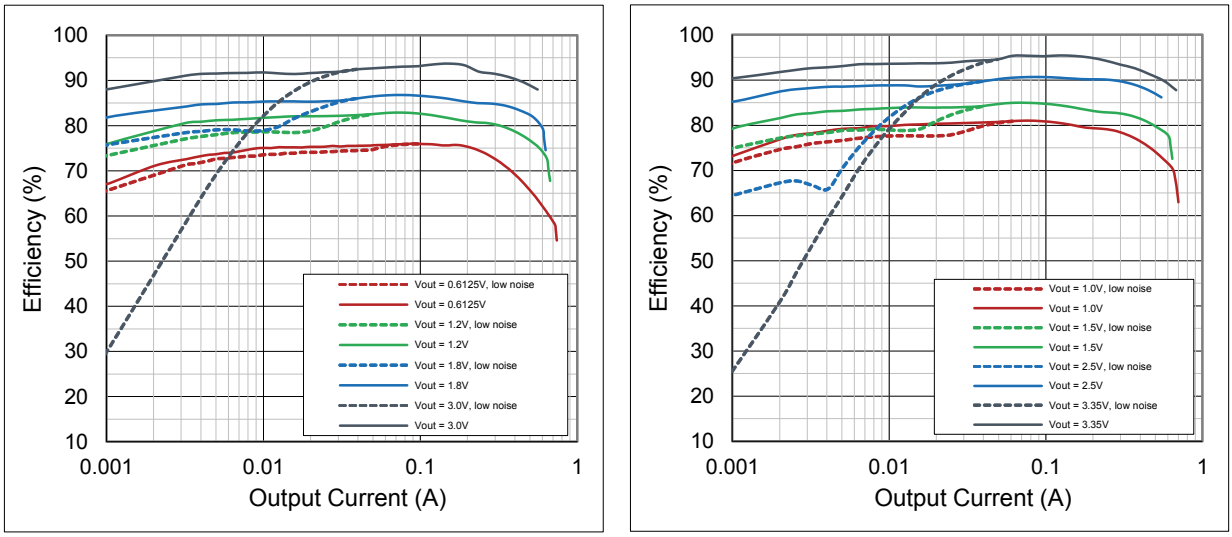
Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{FB_SD1}	Output Capacitor	Ceramic X5R or X7R	8	10		µF
C_{VSUP_SD1}	Input Capacitor	Ceramic X5R or X7R		2.2		µF
L_{SD1}	Inductor	4MHz operation		1		µH
		3MHz operation		1		
		2MHz operation		1		
		1MHz operation		2.2		

Figure 18:
DCDC Step Down Converter Efficiency vs. Load Current at 1MHz



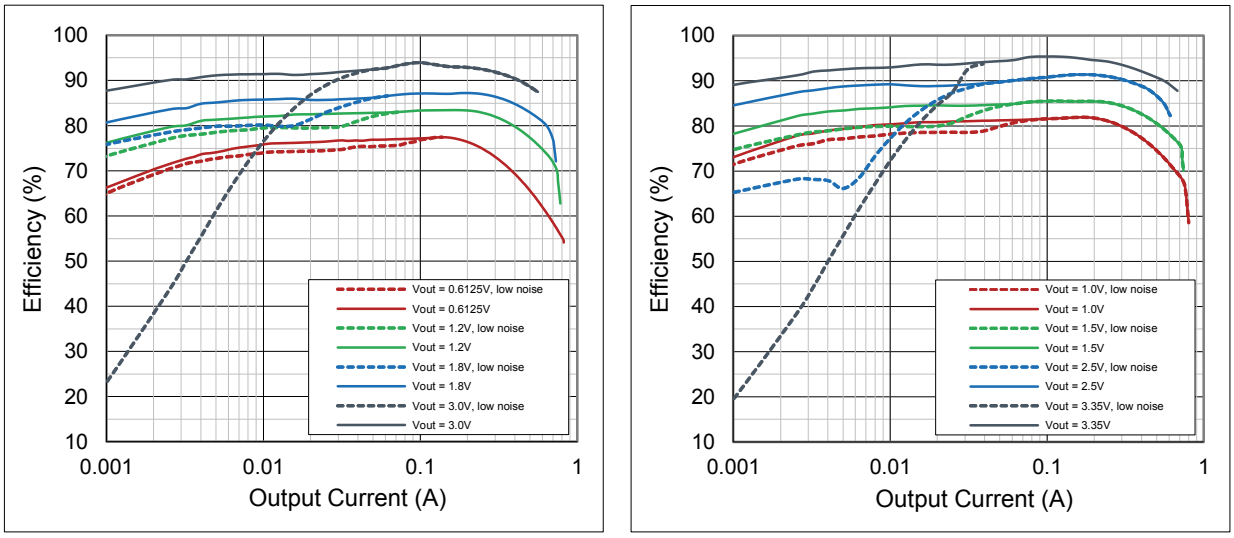
DCDC Efficiency vs. Output Current: V_{SUP} = 3.7V, f_{SW} = 1MHz, Murata LQM2HPN2R2MG0L 2.2µH coil, T_{AMB} = 25°C.

Figure 19:
DCDC Step Down Converter Efficiency vs. Load Current at 2MHz



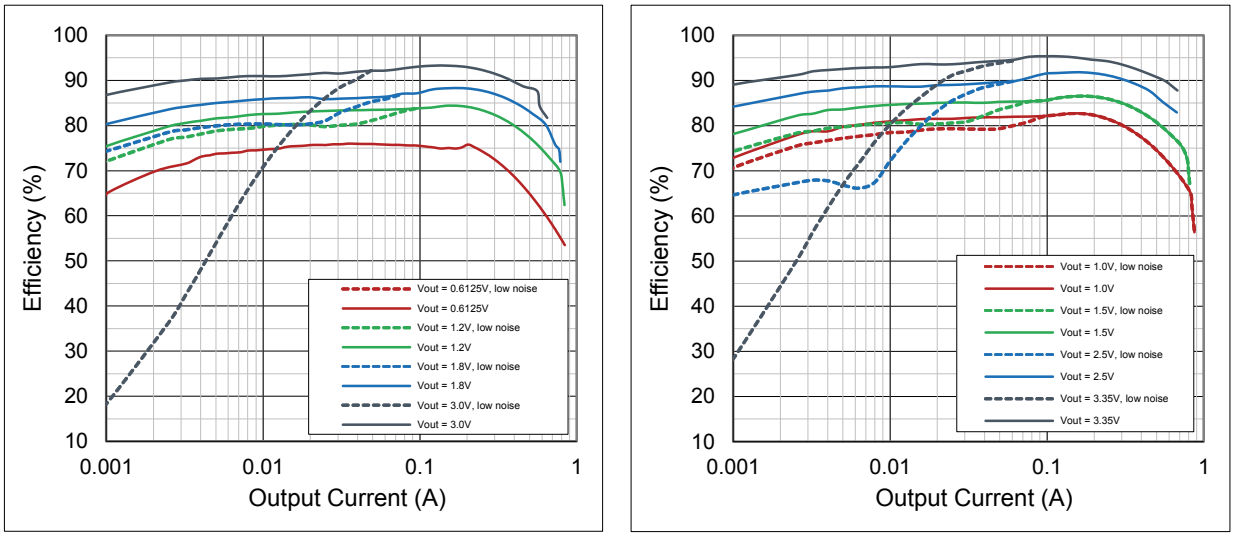
DCDC Efficiency vs. Output Current: V_{SUP} = 3.7V, f_{SW} = 2MHz, Murata LQM2HPN1R0MG0L 1uH coil, T_{AMB} = 25°C.

Figure 20:
DCDC Step Down Converter Efficiency vs. Load Current at 3MHz



DCDC Efficiency vs. Output Current: V_{SUP} = 3.7V, f_{SW} = 3MHz, Murata LQM2HPN1R0MG0L 1uH coil, T_{AMB} = 25°C.

Figure 21:
DCDC Step Down Converter Efficiency vs. Load Current at 4MHz

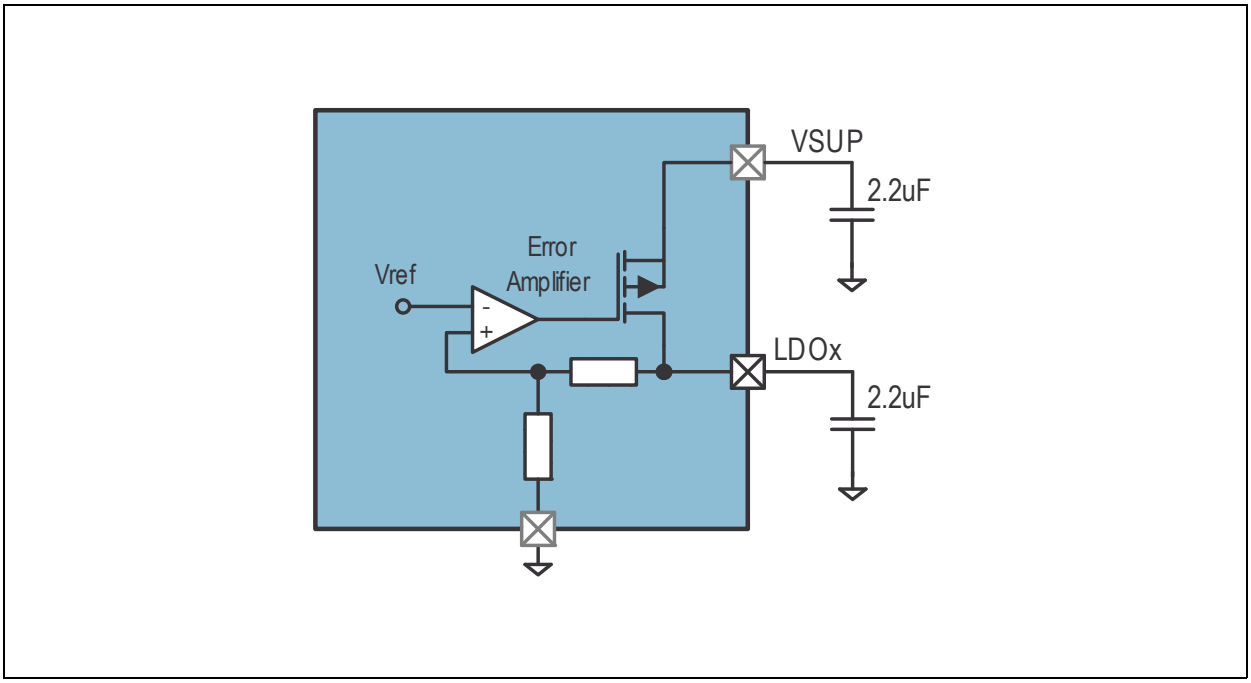


DCDC Efficiency vs. Output Current: V_{SUP} = 3.7V, f_{SW} = 4MHz, Murata LQM2HPN1R0MG0L 1uH coil, T_{AMB} = 25°C.

Universal IO LDO Regulator

This LDO is a low-power and low-quiescent current linear-regulator specifically designed for space-limited applications. This device can supply loads up to 200mA and consist of an error amplifier, and a P-channel MOSFET pass transistor.

Figure 22:
Universal IO LDO Regulator Block Diagram



Parameters

Figure 23:
Universal IO LDO Regulator Electrical Characteristics

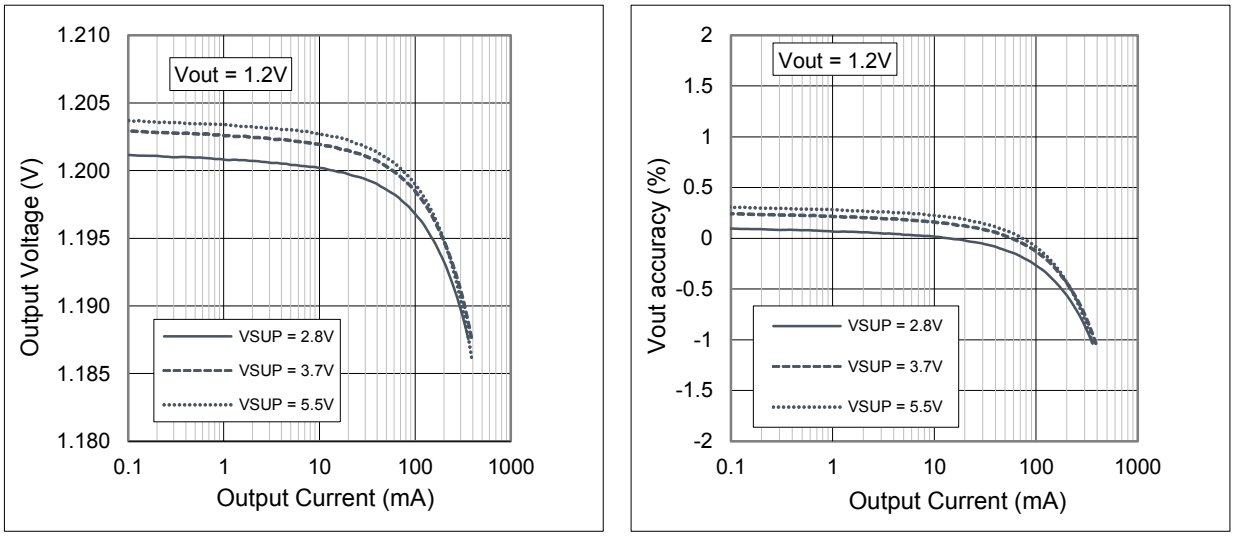
Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IN}	Input voltage	Pin VSUP	2.7		5.5	V
ΔV_{OUT}	Output voltage accuracy	I_{OUT} = 1mA, V_{OUT} > 2V T_{AMB} = 25°C	-2		+2	%
		I_{OUT} = 100uA to 200mA V_{OUT} > 2V	-3		+3	
		I_{OUT} = 1mA, V_{OUT} ≤ 2V T_{AMB} = 25°C	-20		+20	mV
		I_{OUT} = 100uA to 200mA V_{OUT} ≤ 2V	-50		+50	
V_{OUT}	Output voltage range		1.2		3.3	V

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{LNR}	Line regulation static	V_{IN} = 2.7V to 5.5V I_{OUT} = 1mA		0.07		%/V
	Line regulation dynamic	V_{IN} = 2.7V to 5.5V within 15us I_{OUT} = 1mA		20		mV
V_{LDR}	Load regulation static	I_{OUT} = 100uA to 200mA		0.014		%/mA
	Load regulation dynamic	I_{OUT} = 100uA to 200mA within 15us		30		mV
R_{ON}	ON resistance			0.5	1	Ω
I_{OUT}	Guaranteed load current	RMS	200			mA
I_{LIMIT}	Short-circuit	V_{OUT} = 0V		230		mA
I_Q	Quiescent current	no Load		5		uA
		I_{OUT} = 100µA		5		
		I_{OUT} = 200mA		15		
I_{OFF}	Shutdown supply current	LDO disabled		0.1	1	uA
t_{START}	Startup time			750		us
$t_{SHUTDOWN}$	Shutdown time			500		us

Figure 24:
Universal IO LDO Regulator External Components

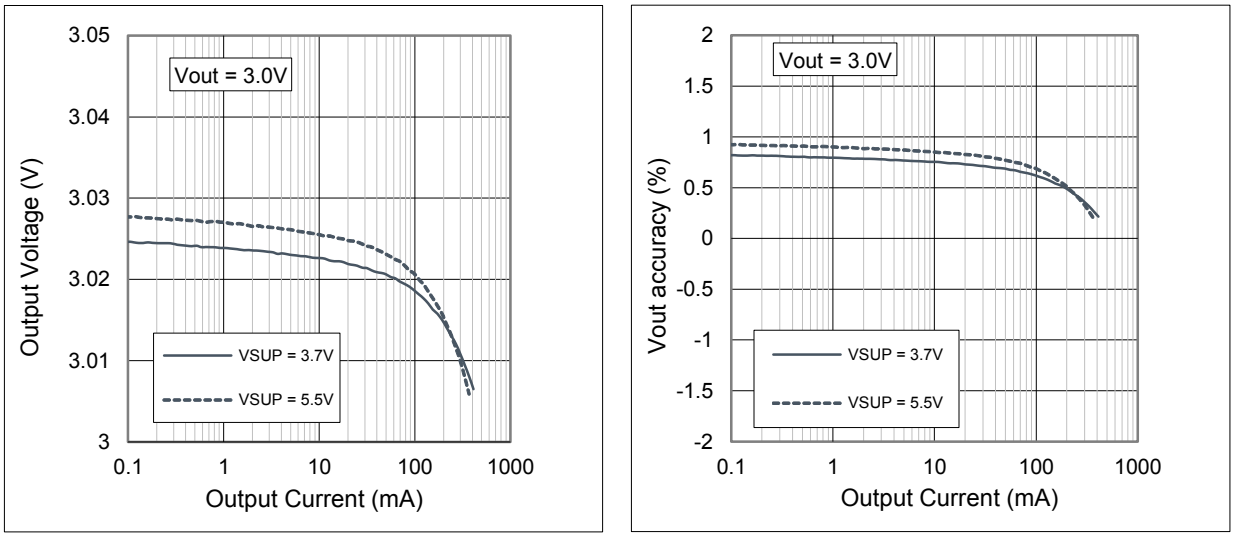
Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{LDOx}	Output capacitor	Ceramic X5R or X7R	2.2	10		µF

Figure 25:
LDO Output Voltage vs. Output Current 1/2



LDO Output Voltage vs. Output Current: V_{OUT} = 1.2V, T_{AMB} = 25°C.

Figure 26:
LDO Output Voltage vs. Output Current 2/2



LDO Output Voltage vs. Output Current: V_{OUT} = 3.0V, T_{AMB} = 25°C.

Figure 27:
LDO Load Transient Response 1/2

LDO Load Transient Response:
V_{SUP} = 3.7V, V_{OUT} = 1.2V, t_{RISE} = 15us,
I_{OUT} = 100uA to 200mA, T_{AMB} = 25°C.
(Blue channel: V_{OUT}; Red channel: I_{OUT})

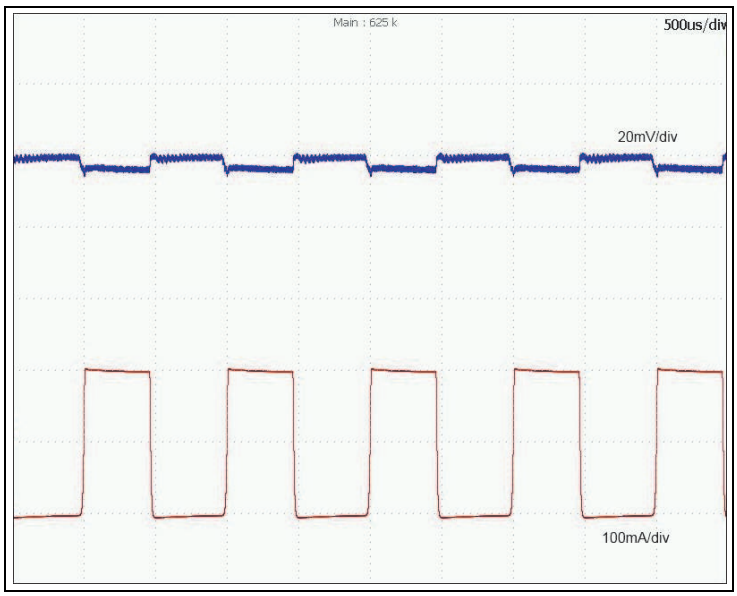
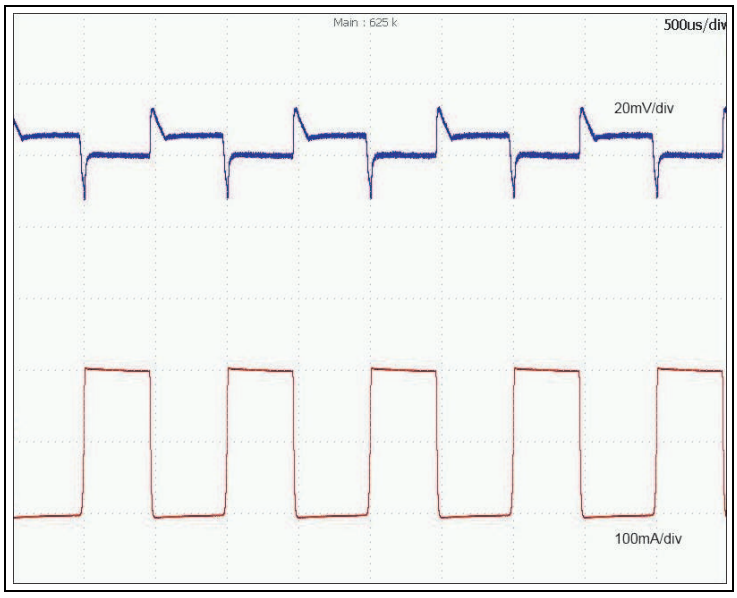


Figure 28:
LDO Load Transient Response 2/2

LDO Load Transient Response:
V_{SUP} = 3.7V, V_{OUT} = 3.0V, t_{RISE} = 15us,
I_{OUT} = 100uA to 200mA, T_{AMB} = 25°C.
(Blue channel: V_{OUT}; Red channel: I_{OUT})



Linear Charger

This block can be used to charge Li-Ion batteries. Requiring less external components, a full-featured battery charger with a high degree of flexibility can easily be realized. The main features of the controller are:

- Charge adapter detection
- Power Path management for dead battery startup
- Low current Trickle charging
- Constant current charging
- Constant voltage charging
- Operation without battery
- Battery presence indication
- NTC temperature supervision
- Input current limitation

Figure 29:
Linear Charger Block Diagram

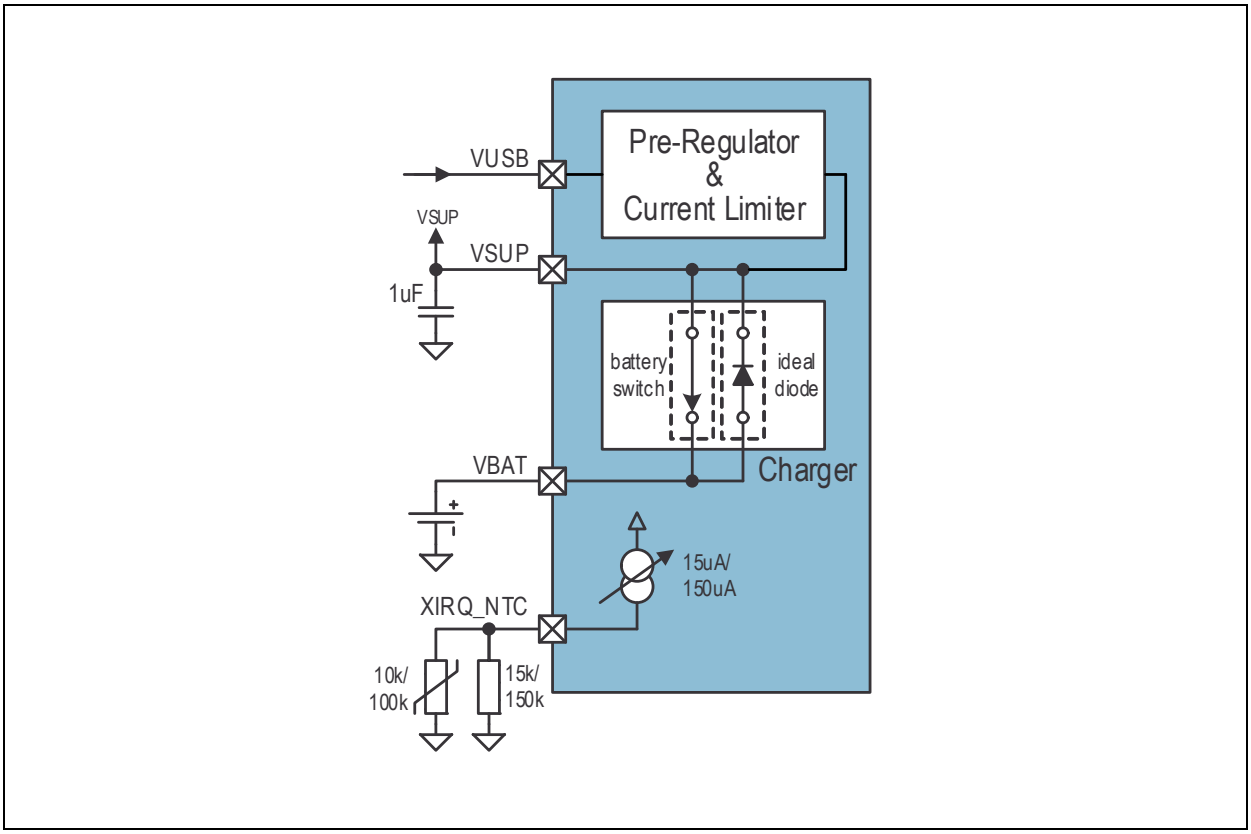
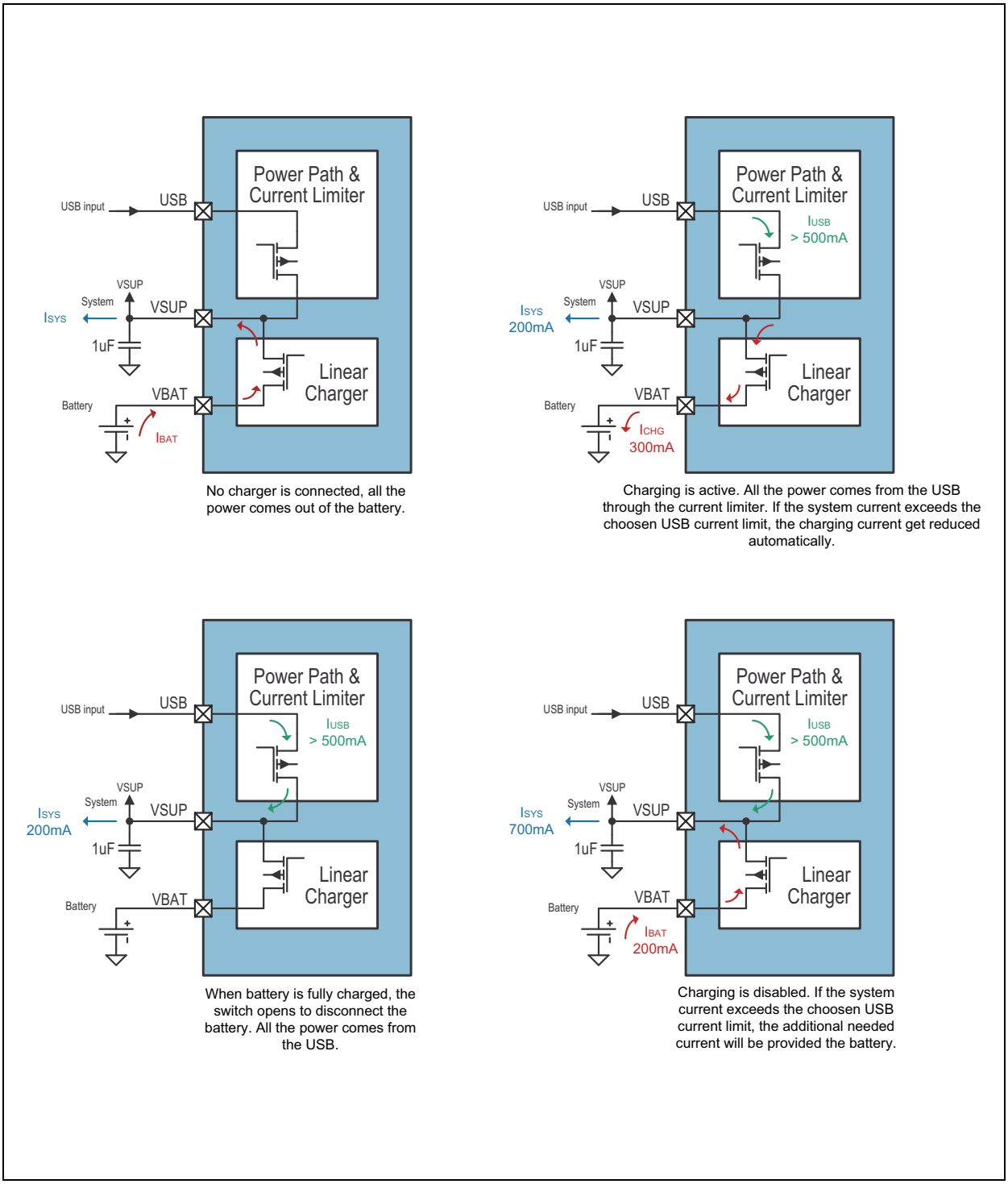


Figure 30:
Linear Charger Modes



Charging Modes: This figure describes the 4 different charger modes.

Charging Cycle Description

Charge Adapter Detection

The charge controller uses an integrated detection circuit to determine if an external charge adapter has been applied to the VUSB pin. If the adapter voltage exceeds the battery voltage at pin VBAT by V_{CHDET} the *ChDet [ChargerStatus2]* will be set. The detection circuit will reset the charge controller (bit *ChDet* is cleared) as soon as the voltage at the VUSB pin drops to only V_{CHMIN} above the battery voltage. In case the AS3701 device is reset the charge controller will also be reset, even if a charge adapter is applied to the VUSB pin. The Charger detection can be disabled by setting the bit *chdet_off [ChargerStatus2]* to "1", which results in a further decrease of internal power consumption.

Low Current (Trickle) Charging

Trickle charge mode is started when an external charge adapter has been detected, the bit *bat_charging_enable [ChargerControl]* is set and the battery voltage at pin VBAT is below the $V_{TRICKLE}$ threshold; bits *ChDet* and *Trickle [ChargerStatus1]* will be set. In this mode the charge current will be limited to TrickleCurrent *[ChargerCurrentControl]* to prevent undue stress in case of deeply discharged batteries. Once $V_{TRICKLE}$ has been exceeded, the charger will change over to constant current charging (Trickle is cleared).

Constant Current Charging

Constant current charging is initiated when *bat_charging_enable [ChargerControl]* and the battery voltage at pin VBAT is above the $V_{TRICKLE}$ and below V_{CHOFF}. The bit *CCM [ChargerStatus1]* is set when the charger has started, and the charge current will be limited by the battery charge controller. The current for the Constant Current Charging can be selected out of the range defined in *ConstantCurrent [ChargerCurrentControl]* if the bit *cc_range_select [ChargerControl]* is set to "0" or out of the range defined in *TrickleCurrent [ChargerCurrentControl]* if the bit *cc_range_select [ChargerControl]* is set to "1". When the battery approaches full charge, its voltage will reach the charge termination threshold V_{CHOFF}. V_{CHOFF} depends on the *ChVoltEOC [ChargerVoltageControl]* bits settings. Top-OFF charge will be started and the bit *CVM [ChargerStatus1]* will be set.

Constant Voltage Charging

Constant voltage charge mode is initiated and the bit *CVM [ChargerStatus1]* will be set when the V_{CHOFF} threshold has been reached. The charge current is monitored during constant voltage charging. It will be decreasing from its initial value during constant current charging and eventually drops below 5% or 50% of the Constant Current value (depends on the