Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AS3709

Micro-PMIC with 5 DC/DCs and 2 LDOs

General Description

The AS3709 is an ultra compact Micro-PMIC containing 5 high-efficiency, constant-frequency synchronous buck converters in addition with two universal IO LDOs are available for lower current power rails. The wide input voltage range (2.7V to 5.5V), automatic power-save mode and minimal external component requirements make the AS3709 perfect for any single Li-Ion battery-powered or fixed 3.3V/5V supply application. Typical supply current with no load is 110µA and decreases to ≤ 7µA in shutdown mode. An internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. The internally fixed switching frequency (2MHz, 3MHz or 4MHz) allows the use of small surface mount external components. Very low output voltages can be delivered with the internal 0.6V feedback reference voltage. The AS3709 is available in a 32-pin QFN 4x4mm package and in a very compact WL-CSP36 with 0.4mm pitch.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3709, Micro-PMIC with 5 DC/DCs and 2 LDOs are listed below:

Figure 1:
Added Value of Using AS3709

Benefits	Features
• Compact design due to small coils for IO and memory voltage generation	• 5 DC/DC step down regulators (2-4MHz)
• Independent voltage rails for general purpose IO supplies	• 2 universal IO LDOs
• Flexible and fast adaptation to different processors/applications	• OTP programmable boot sequence
• Power saving control according to the processor's needs.	• Stand-by function with selectable rails and programmable voltages
• Self-contained start-up and control for single-cell battery applications. Safety shutdown feature.	• Control Interface • I^2C control lines • ON key with 4s/8s emergency shut-down • POR with RESET I/O
• Dedicated packages for specific applications. Optimization for PCB cost or size.	• 32-pin QFN (4mmx4mm), 0.4mm pitch • 36-ball WL-CSP 0.4mm pitch

Applications

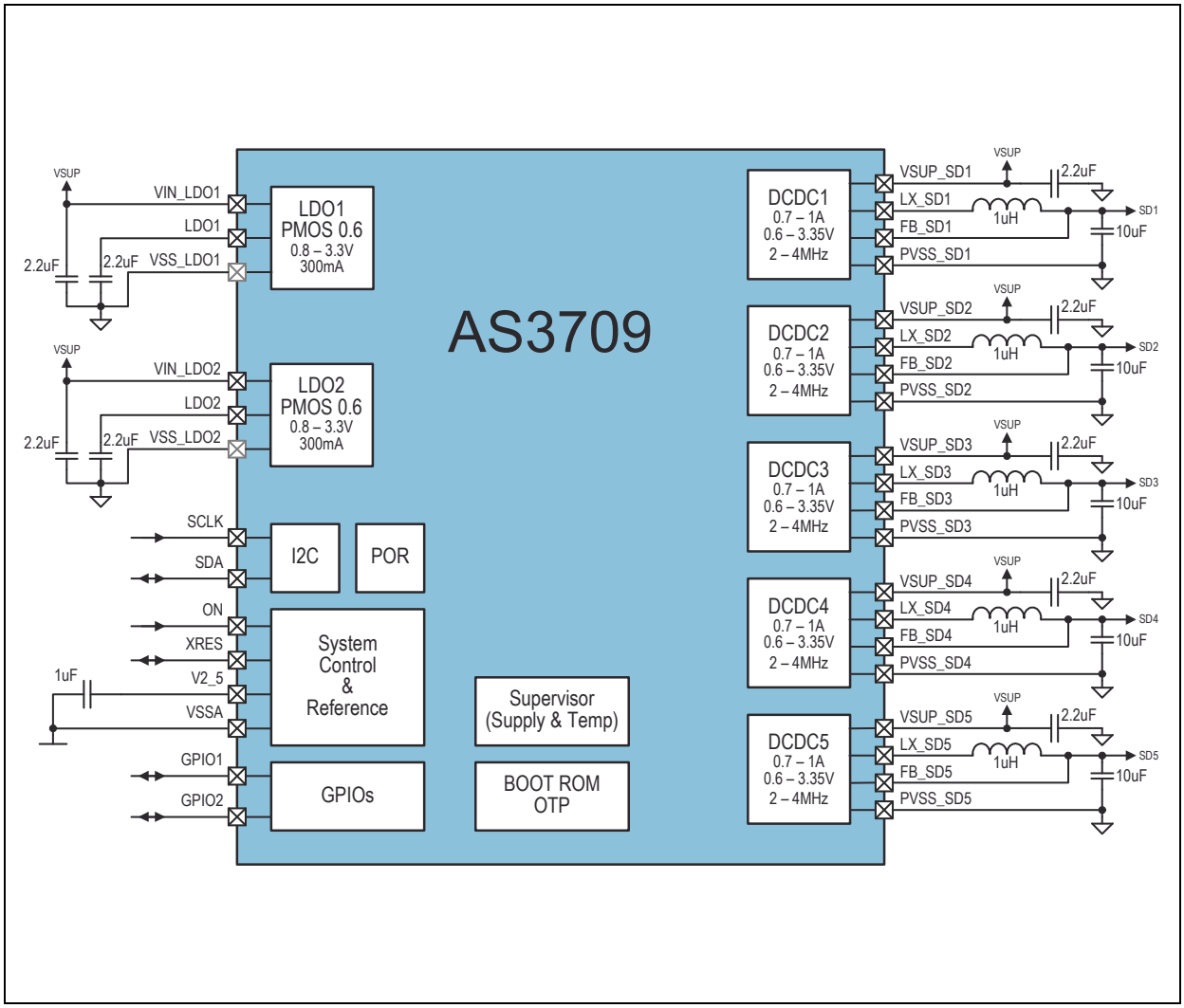
The device is ideal for:

- SSDs, mobile communication devices
- Laptops and PDAs
- Ultra-low-power systems
- Medical instruments or any other space-limited application with low power-consumption requirements.

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS3709 Block Diagram



Pin Assignments

The AS3709 pin assignments are described below.

Figure 3:
36 Balls WL-CSP with 0.4mm Pitch

Ball Assignments: Shows the top view ball assignment of the AS3709 WL-CSP.

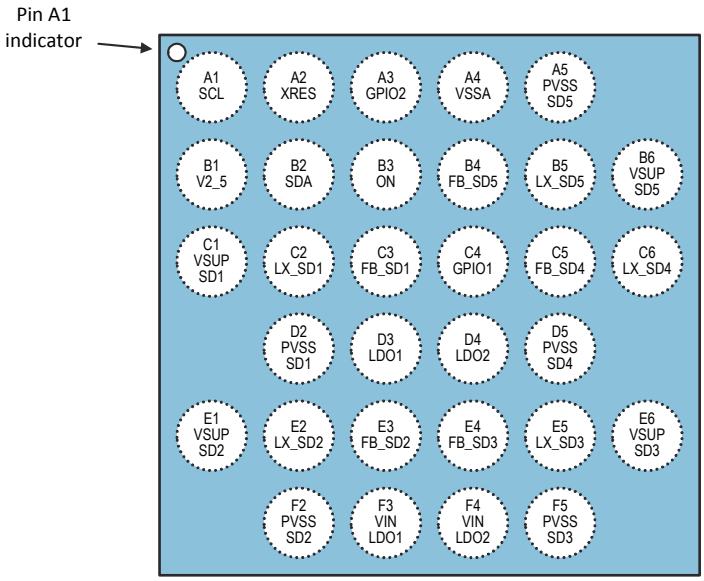


Figure 4:
32 Pins QFN 4x4 with 0.4mm Pitch

Pin Assignment: Shows the top view pin assignment of the AS3709 QFN package.

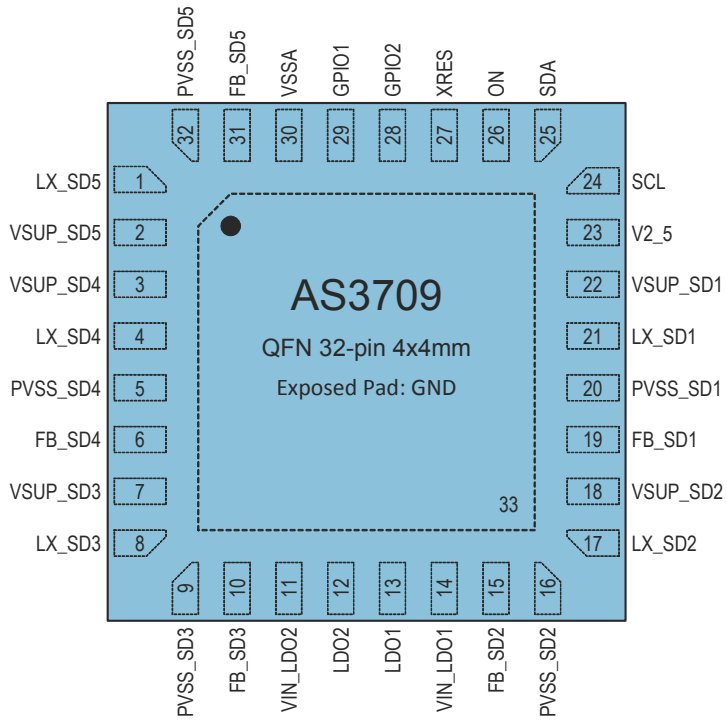


Figure 5:
Pin Description

Pin Number		Pin Name	Pin Type	Description	If Not Used
QFN	WL-CSP				
1	B5	LX_SD5	DIG OUT	DC/DC SD5 switch output to coil	Open
2	B6	VSUP_SD5	SUP IN	DC/DC SD5 pos supply terminal	Always needed
3	B6	VSUP_SD4	SUP IN	DC/DC SD4 pos supply terminal	Always needed
4	C6	LX_SD4	DIG OUT	DC/DC SD4 switch output to coil	Open
5	D5	PVSS_SD4	GND	DC/DC SD4 neg supply terminal	Always needed
6	C5	FB_SD4	ANA IN	DC/DC SD4 Feedback pin	Open
7	E6	VSUP_SD3	SUP IN	DC/DC SD3 pos supply terminal	Always needed
8	E5	LX_SD3	DIG OUT	DC/DC SD3 switch output to coil	Open
9	F5	PVSS_SD3	GND	DC/DC SD3 neg supply terminal	Always needed
10	E4	FB_SD3	ANA IN	DC/DC SD3 Feedback pin	Open
11	F4	VIN_LDO2	SUP IN	Supply pin for LDO2	Always needed
12	D4	LDO2	ANA OUT	Output Voltage of LDO2	Open
13	D3	LDO1	ANA OUT	Output Voltage of LDO1	Open
14	F3	VIN_LDO1	SUP IN	Supply pin for LDO1	Always needed
15	E3	FB_SD2	ANA IN	DC/DC SD2 Feedback pin	Open
16	F2	PVSS_SD2	GND	DC/DC SD2 neg supply terminal	Always needed
17	E2	LX_SD2	DIG OUT	DC/DC SD2 switch output to coil	Open
18	E1	VSUP_SD2	SUP IN	DC/DC SD2 pos supply terminal	Always needed
19	C3	FB_SD1	ANA IN	DC/DC SD1 Feedback pin	Open
20	D2	PVSS_SD1	GND	DC/DC SD1 neg supply terminal	Always needed
21	C2	LX_SD1	DIG OUT	DC/DC SD1 switch output to coil	Open
22	C1	VSUP_SD1	SUP IN	DC/DC SD1 pos supply terminal	Always needed
23	B1	V2_5	ANA OUT	Internal 2.5V regulator output	Always needed
24	A1	SCL	DIG IN	2-wire Serial IF Clock Input	Pull-up to V2_5
25	B2	SDA	DIG IO	2-wire Serial IF Data IO	Pull-up to V2_5
26	B3	ON	DIG IN	Power Up Input	Open
27	A2	XRES	DIG IO	Reset IO, external pull-up resistor needed	Always needed

Pin Number		Pin Name	Pin Type	Description	If Not Used
QFN	WL-CSP				
28	A3	GPIO2	ANA IO	General Purpose IO 2	Open
29	C4	GPIO1	ANA IO	General Purpose IO 1	Open
30	A4	VSSA	GND	GND Reference for analog blocks	Always needed
31	B4	FB_SD5	ANA IN	DC/DC SD5 Feedback pin	Open
32	A5	PVSS_SD5	GND	DC/DC SD5 neg supply terminal	Always needed
33		VSS	GND	Exposed Pad	Always needed

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
	Supply Voltage to Ground 5V Pins	-0.5	7.0	V	Applicable for pins: VSUP_SDx, VIN_LDOx, SCLK, SDA, ON, XRES, GPIOx, LX_SDx
	Supply Voltage to Ground 3V Pins	-0.5	5.0	V	Applicable for pins: V2_5, LDOx, FB_SDx
	Voltage Difference between Ground Terminals	-0.3	0.3	V	Applicable for pins: VSSA, PVSS_SDx, Exposed Pad
	Input Current (latch-up immunity)	-100	100	mA	JEDEC JESD78
Continuous Power Dissipation (T_A = 70°C)					
P_T	Continuous Power Dissipation		1.2	W	P_T (1) for QFN32 package (R_{THJA} ~ 45K/W)
			1.1	W	P_T (1) for WL-CSP36 package (RTHJA ~ 50K/W)
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±2		kV	JEDEC JESD22-A114F
Temperature Ranges and Storage Conditions					
T_A	Operating Temperature	-40	85	°C	
T_J	Junction Temperature		125	°C	
T_{STRG}	Storage Temperature Range	-55	150	°C	QFN
		-55	125	°C	WL-CSP
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	

Symbol	Parameter	Min	Max	Units	Comments
Temperature (Soldering)					
T_{BODY}	Package Body Temperature		260	°C	32-pin QFN: Norm IPC/JEDEC J-STD-020 (2) The lead finish for Pb-free leaded packages is matte tin (100% Sn)
			260	°C	36-ball WL-CSP: Norm IPC/JEDEC J-STD-020 (2)
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h (QFN)
		1			Represents an unlimited floor life time (WL-CSP)

Note(s):

1. Depending on actual PCB layout and PCB used.
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non hermetic Solid State Surface Mount Devices

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 7:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	Pin V_{SUP}	2.7		5.5	V
I_Q	Quiescent Current	Normal operating current. With bit Low_power_on = 0; only V2_5 active		155	200	µA
$I_{LOWPOWER}$	Low-Power Quiescent Current	Normal operating current. With bit Low_power_on = 1; only V2_5 active		110		
$I_{POWEROFF}$	Shutdown Current	With bit power_off = 1; only V2_5 is active in power OFF mode. Not tested, guaranteed by design		7	20	

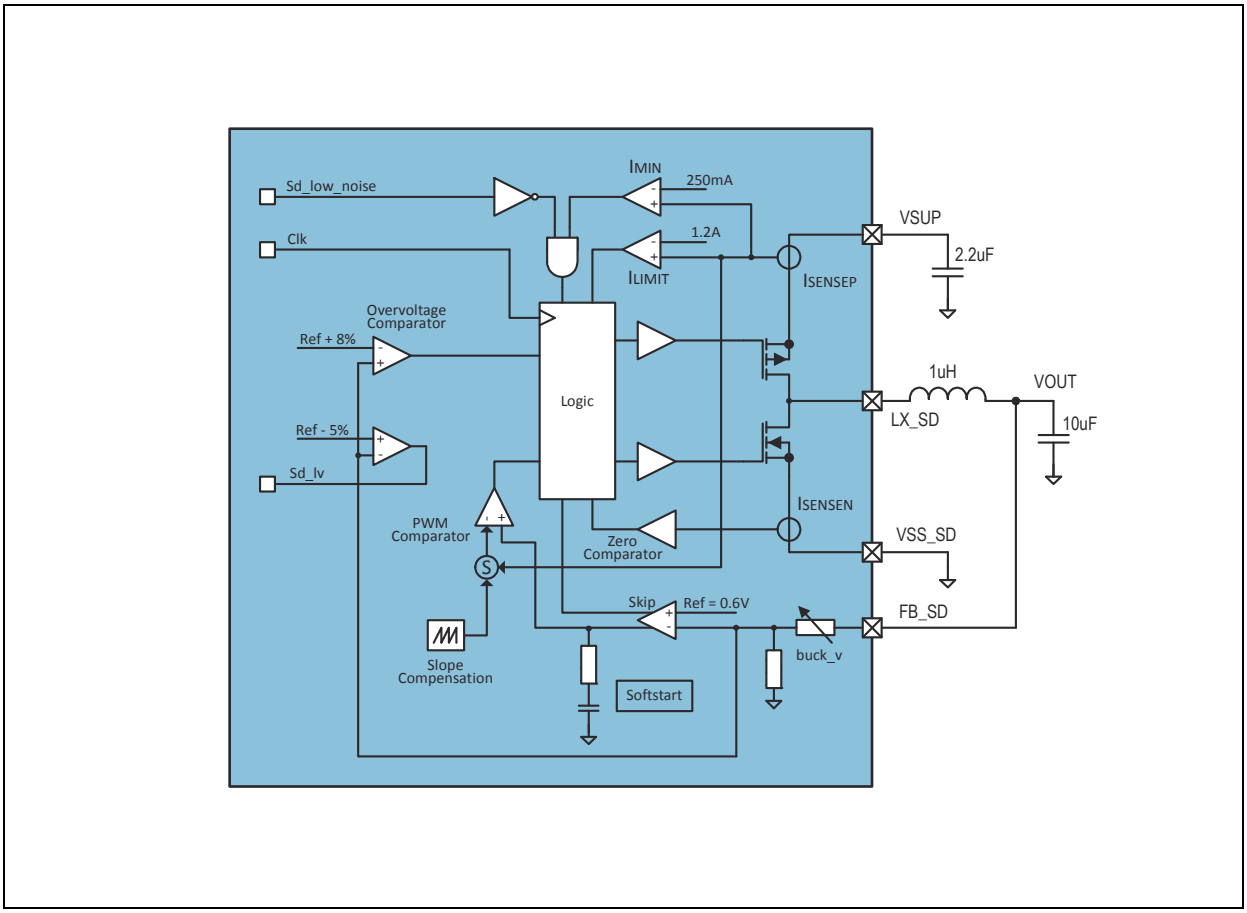
Electrical Characteristics: V_{SUP} = 3.7V, $V_{OUT} < V_{IN} - 0.5V$, T_A = -40°C to 85°C, typ. values @ T_A = 25°C (unless otherwise specified)

Detailed Description - Power Management Functions

Step Down DC/DC Converter

The step-down converter is a high-efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches, efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 1A, with an output capacitor of only 10µF. The implemented current limitation protects the DC/DC Converter and the coil during overload condition.

Figure 8:
Step Down DC/DC Converter Block Diagram



Mode Settings

To allow optimized performance in different applications, there are bit settings possible, to get the best compromise between high efficiency and low input/output ripple.

Low-Ripple, Low-Noise Operation

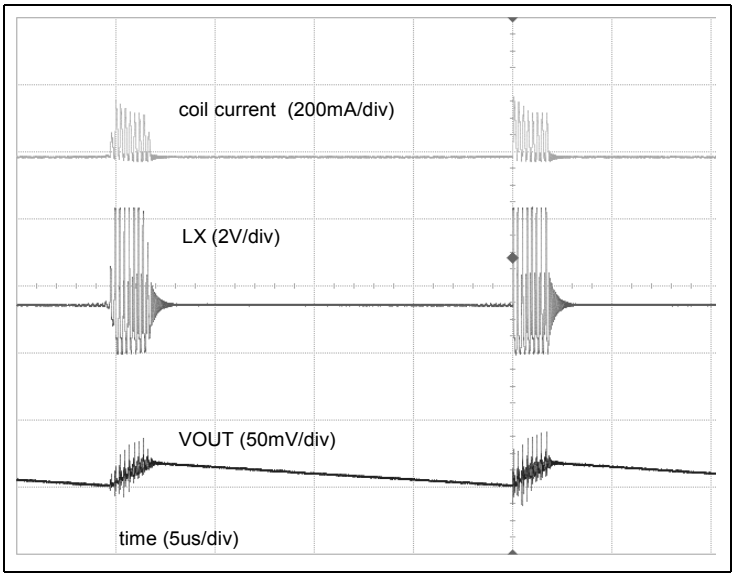
Low-ripple, low-noise operation can be enabled by setting bit *sd_low_noise* = 1.

In this mode there is no minimum coil current necessary before switching OFF the PMOS. As long as the load current is superior to the ripple current, the device operates in continuous mode. When the load current gets lower, the discontinuous mode is triggered. Resultant the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to t_{MIN_ON} to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency at light loads, especially at low input to output voltage differences.

Only in the case the load current gets so small, that less than the minimum on time of the PMOS would be needed to keep the loop in regulation, the regulator will enter low power mode operation.

The crossover point is about 15mA for V_{IN} = 3V, V_{OUT} = 1.2V, 1µH, 4MHz.

Figure 9:
DC/DC Buck Low Noise Mode



DC/DC Buck Low Noise Mode: Shows the DC/DC switching waveforms for low noise operation.

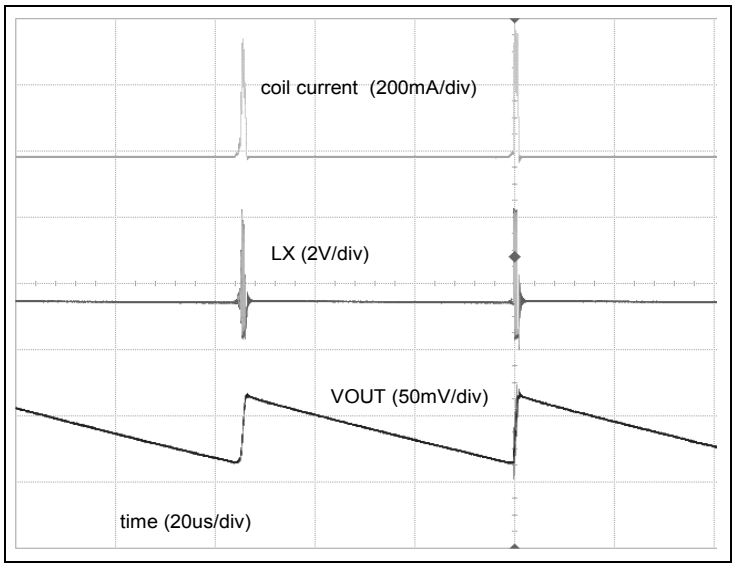
High-Efficiency Operation (Default Setting)

High-efficiency operation is enabled by setting bit *sd_low_noise* = 0.
In this mode there is a minimum coil current necessary before switching OFF the PMOS. Resultant there are less pulses necessary at low output loads, and therefore the efficiency increases. As drawback, this mode increases the ripple up to a higher output current.

The crossover point to low power mode is already reached at reasonable high output currents. (e.g. @110mA for V_{IN} = 3V, V_{OUT} = 1.2V, 1µH, 4MHz)

Figure 10:
DC/DC Buck High Efficiency Mode

DC/DC Buck High Efficiency Mode:
Shows the DC/DC switching waveforms for high efficiency operation



Low Power Mode Operation (Automatically Controlled)

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at ±5% of the target value to react quickly on large over/undershoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

DVM (Dynamic Voltage Management)

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

DVM can be selected for all step-down converters, but only for one at a time. (see *sd_dvm_select* and *dvm_time* description)

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs a 22µF output capacitor instead the 10µF one to guarantee the stability of the regulator.

The mode is enabled by setting *sd_fast* =1.

Selectable Frequency Operation

Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency. The frequency can be set to 2, 3 or 4MHz and this mode is selected by setting *sd_freq* and *sd_fsel* to the appropriate values.

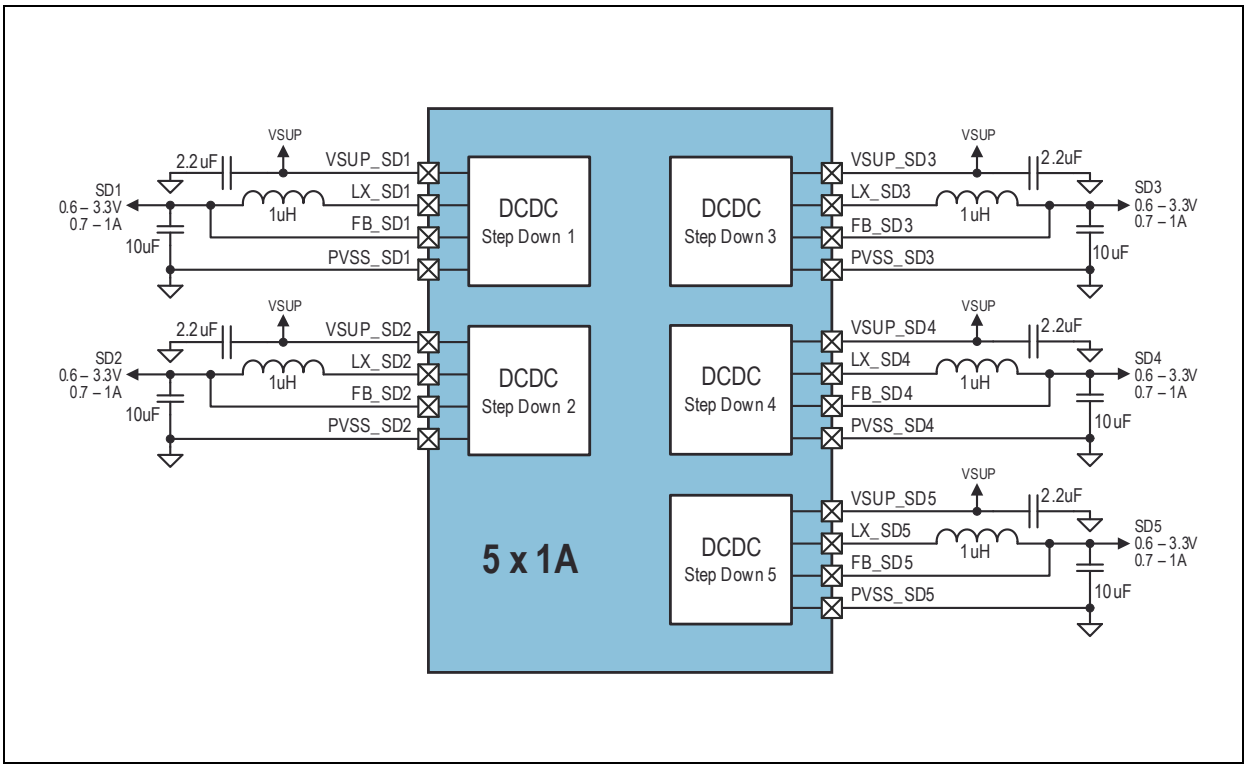
100% PMOS ON Mode for Low Dropout Regulation

For low input to output voltage difference the DC/DC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

Step Down Converter Configuration Modes

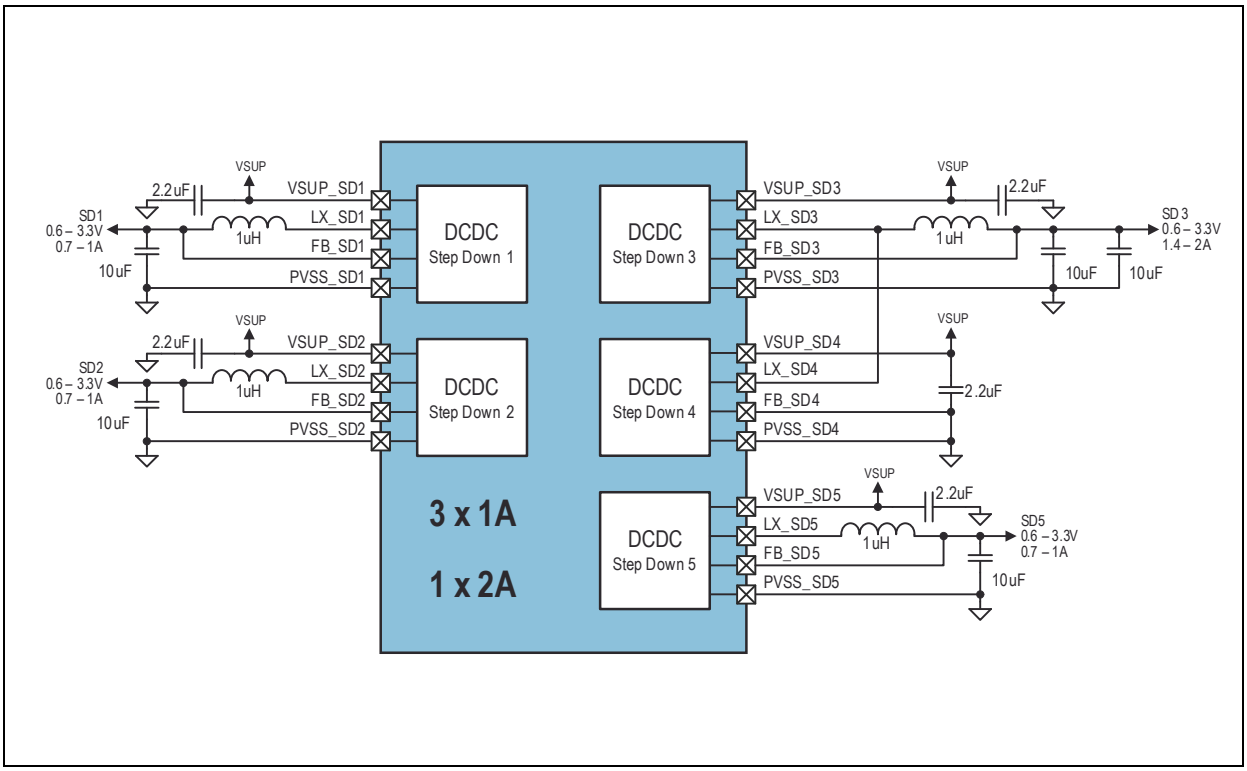
The step down dc/dc converters have two configuration modes to deliver different output currents for the applications. The operating mode is selected by setting the bit *sd2_slave*, *sd4_slave* and *sd5_slave* (the default is set by the Boot-OTP).

Figure 11:
DC/DC Step Down Normal Operating Mode



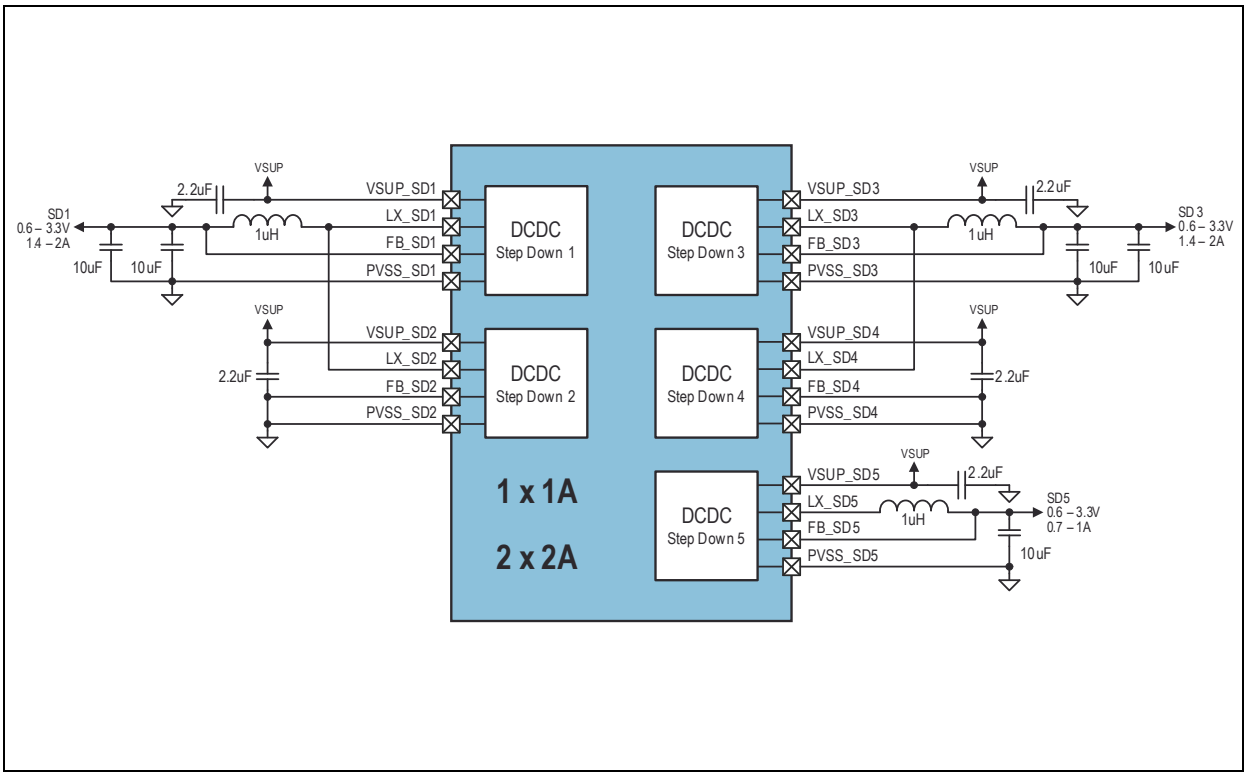
Normal Operating Mode: sd2_slave = 0, sd4_slave = 0, sd5_slave = 0

Figure 12:
DC/DC Step Down SD3/SD4 Operating Mode



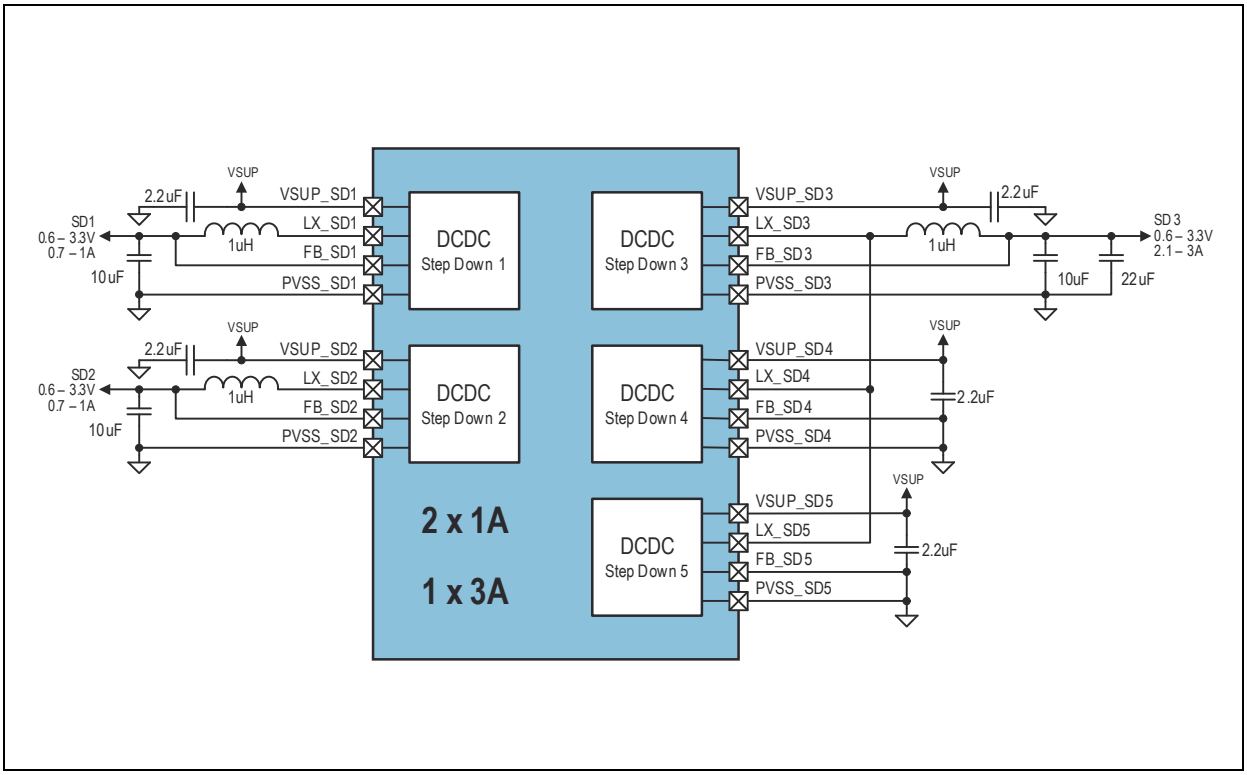
SD3/SD4 Operating Mode: sd2_slave = 0, sd4_slave = 1, sd5_slave = 0

Figure 13:
DC/DC Step Down SD1/SD2 & SD3/SD4 Operating Mode



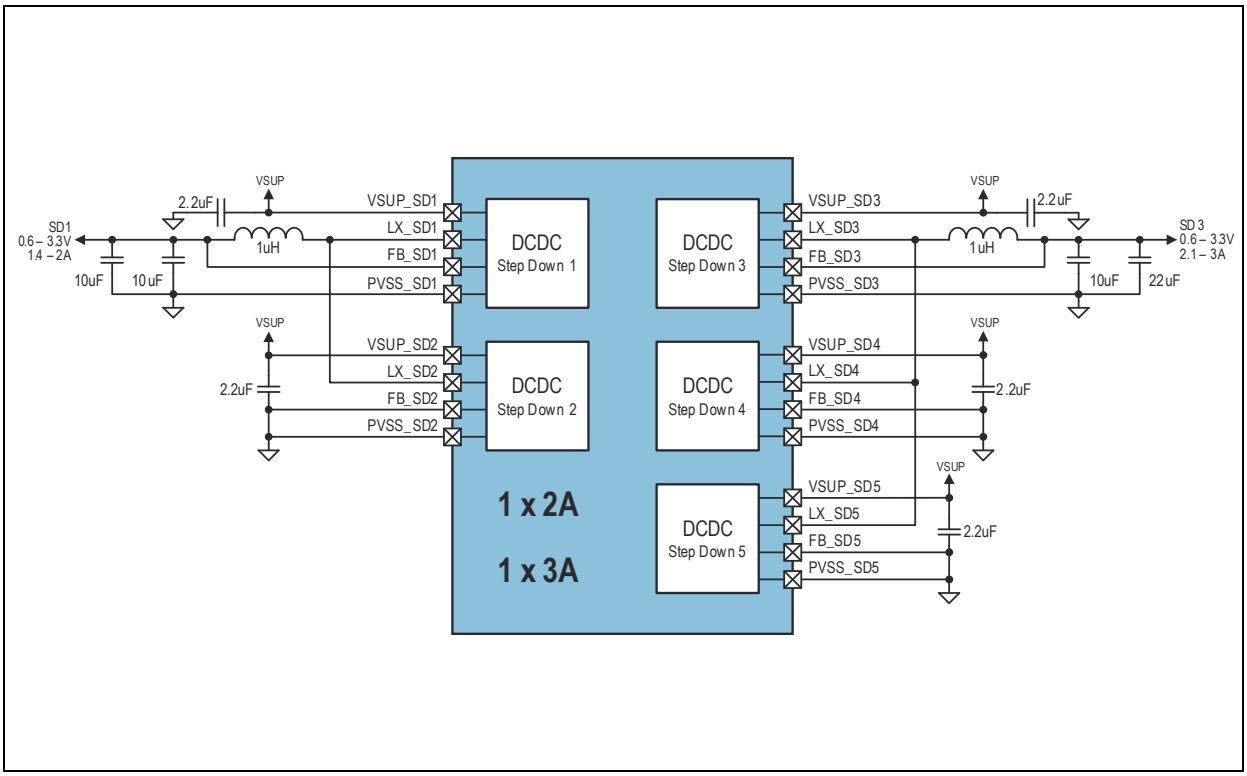
SD3/SD4 & SD4/SD5 Operating Mode: sd2_slave = 1, sd4_slave = 1, sd5_slave = 0

Figure 14:
DC/DC Step Down SD3/SD4/SD5 Operating Mode



SD3/SD4/SD5 Operating Mode: sd2_slave = 0, sd4_slave = 1, sd5_slave = 1

Figure 15:
DC/DC Step Down SD1/SD2 & SD3/SD4/SD5 Operating



SD1/SD2 & SD3/SD4/SD5 Operating Mode: sd2_slave = 1, sd4_slave = 1, sd5_slave = 1

Parameters

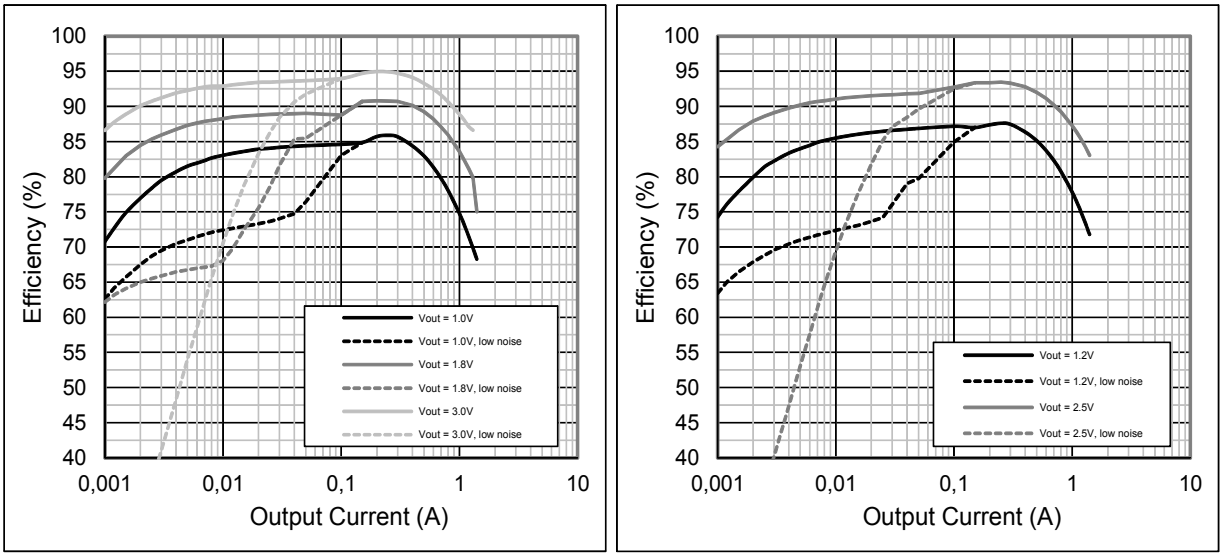
Figure 16:
Step Down DC/DC Converter Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage	Pin V_{SUP}	2.7		5.5	V
V_{OUT}	Regulated Output Voltage		0.6125		3.35	V
V_{OUT_TOL}	Output Voltage Tolerance	min. 40mV	-3		+3	%
I_{LIMIT}	Current Limit			1.2		A
R_{PMOS}	P-Switch ON Resistance			0.25	0.5	Ω
R_{NMOS}	N-Switch ON Resistance			0.25	0.5	Ω
f_{SW}	Switching Frequency	*sdX_frequ* = 1 *sdX_fsel* = 1 *fclk_int* = 4MHz		4		MHz
		sdX_frequ = 1 *sdX_fsel* = 0 *fclk_int* = 4MHz		3		MHz
		sdX_frequ = 0 *sdX_fsel* = 0 *fclk_int* = 4MHz		2		MHz
I_{LOAD}	Load Current	$V_{OUT} \leq 1.8V$	0		1	A
		$V_{OUT} > 1.8V$	0		0.7	
$I_{SUP\_DC/DC}$	Current Consumption	Operating current without load		60		µA
		Shutdown current		0.1		
t_{MIN_ON}	Minimum ON Time			40		ns
η_{EFF}	Efficiency	See figures below				%

Figure 17:
Step Down DC/DC External Components

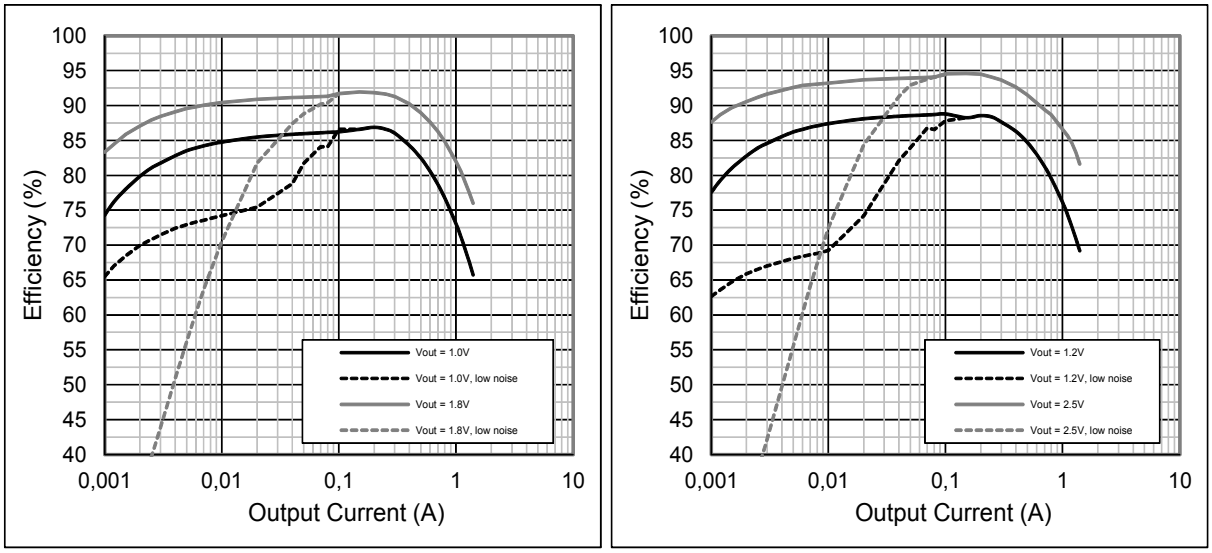
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{FB_SDx}	Output Capacitor	Ceramic X5R or X7R	8	10		µF
C_{VSUP_SDx}	Input Capacitor	Ceramic X5R or X7R		2.2		µF
L_{SDx}	Inductor	4MHz operation		1		µH
		3MHz operation		1		
		2MHz operation		2.2		

Figure 18:
DC/DC SD1 Efficiency vs. Output Current



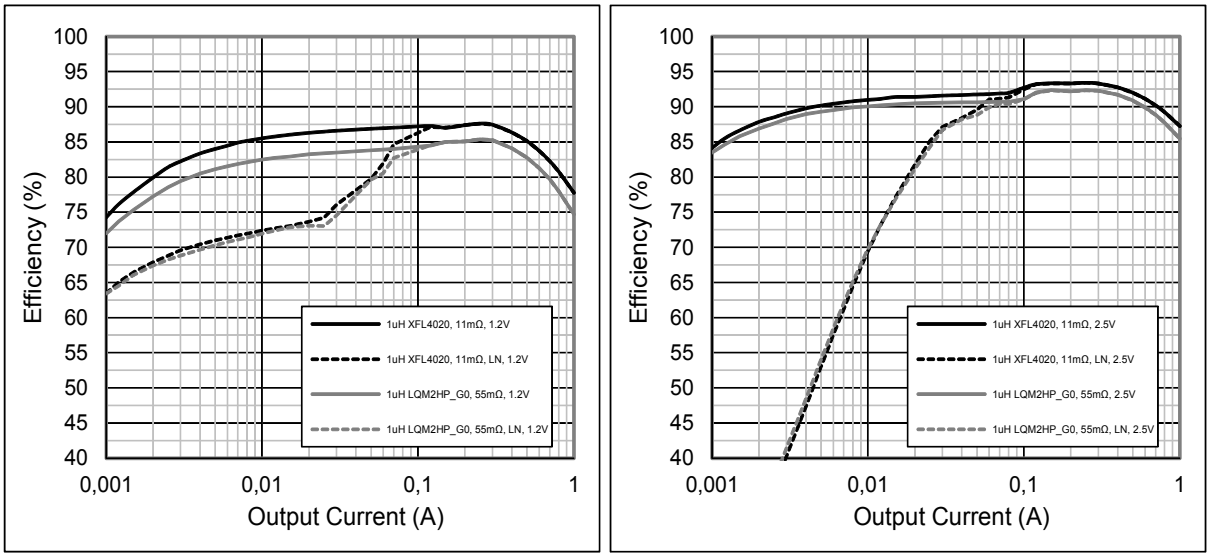
SD1 Efficiency vs. Output Current: V_{IN} = 3.7V, 3MHz operation, XFL4020 1µH coil, T_A = 25°C

Figure 19:
DC/DC SD1 Efficiency vs. Output Current



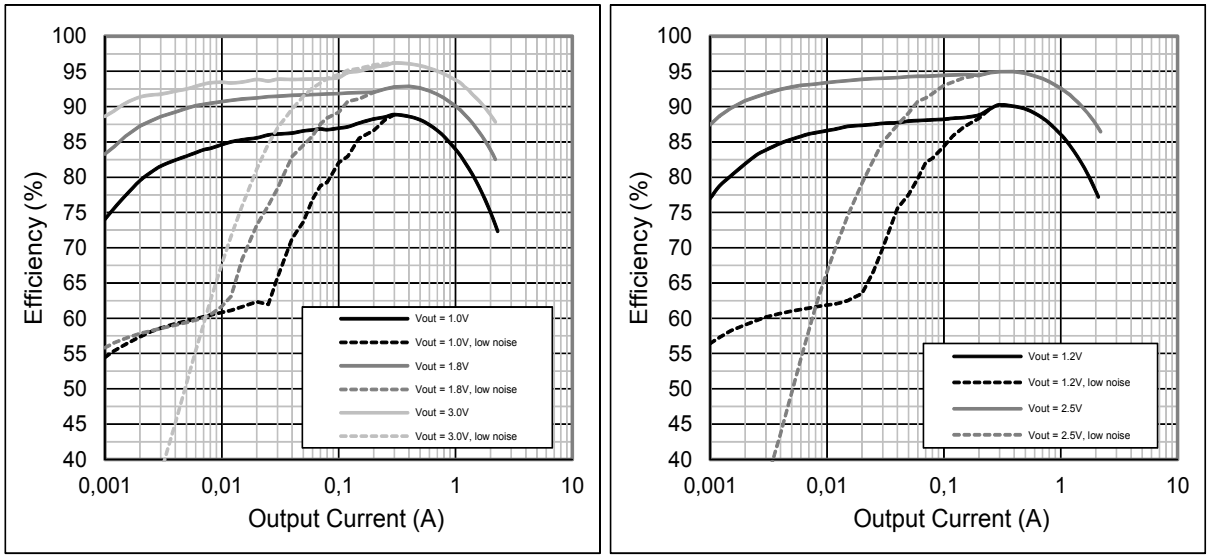
SD1 Efficiency vs. Output Current: V_{IN} = 3.0V, 3MHz operation, XFL4020 1µH coil, T_A = 25°C

Figure 20:
DC/DC SD1 Efficiency vs. Output Current



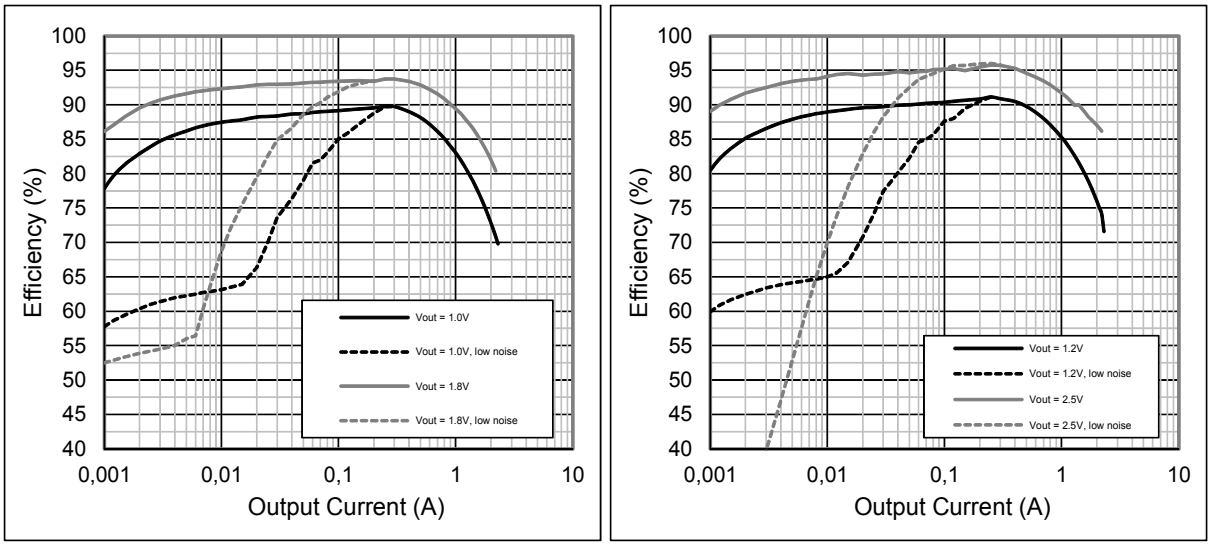
SD1 Efficiency vs. Output Current: V_{IN} = 3.7V, V_{OUT} = 1.2V/2.5V, 3MHz operation, T_A = 25°C

Figure 21:
DC/DC SD1 + SD2 Efficiency vs. Output Current



SD1 + SD2 Efficiency vs. Output Current: V_{IN} = 3.7V, 3MHz operation, XFL4020 1µH coil, T_A = 25°C

Figure 22:
DC/DC SD1 + SD2 Efficiency vs. Output Current



SD1 + SD2 Efficiency vs. Output Current: V_{IN} = 3.0V, 3MHz operation, XFL4020 1µH coil, T_A = 25°C

Figure 23:
DC/DC SD1 + SD2 Efficiency vs. Output Current

SD1 + SD2 Efficiency vs. Output Current: V_{IN} = 3.7V, V_{OUT} = 1.2V, 3MHz operation, T_A = 25°C

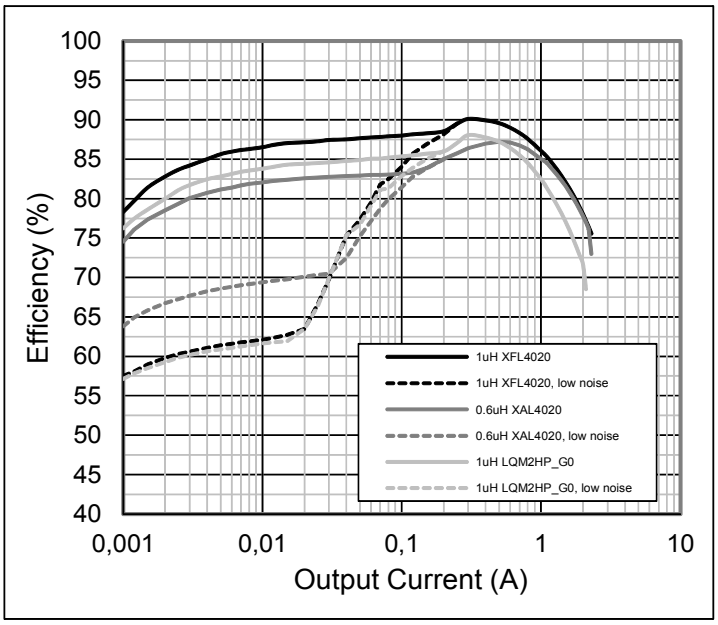
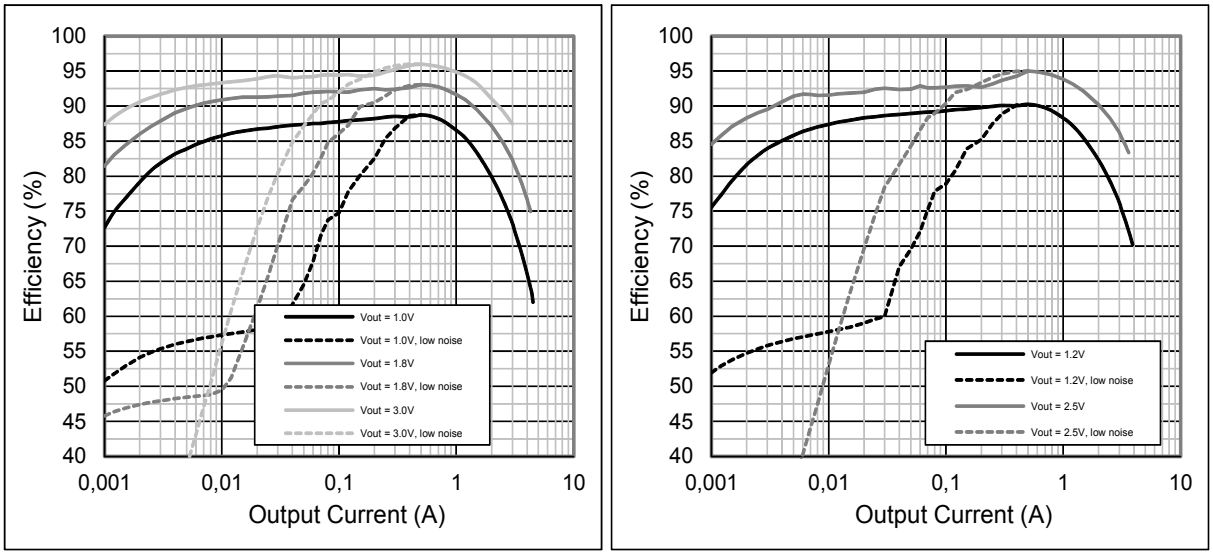
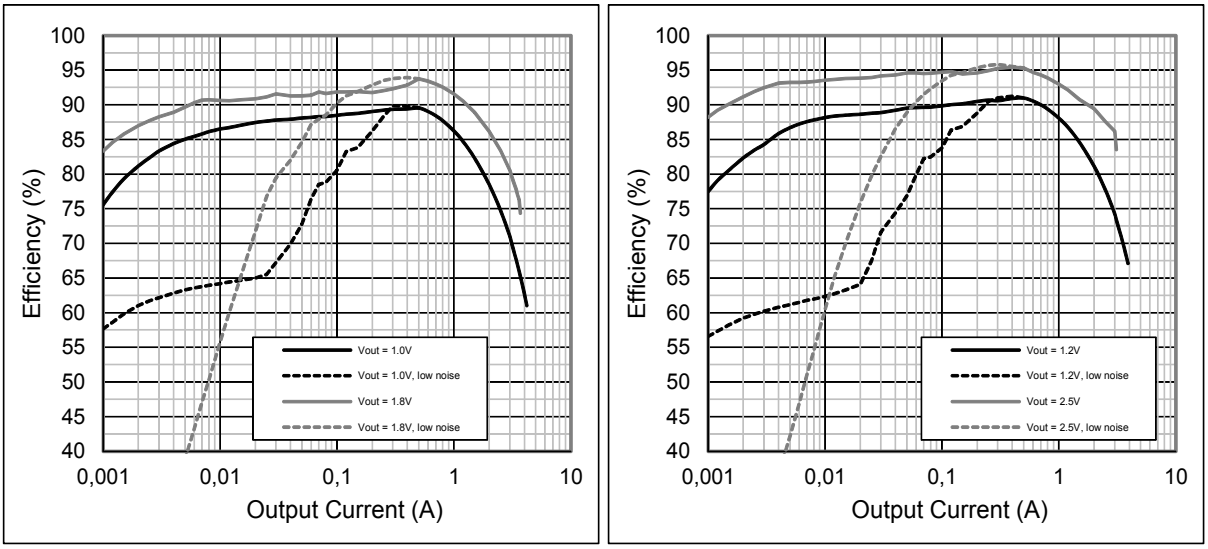


Figure 24:
DC/DC SD3 + SD4 + SD5 Efficiency vs. Output Current



SD3 + SD4 + SD5 Efficiency vs. Output Current: V_{IN} = 3.7V, 3MHz operation, XFL4020 1µH coil, T_A = 25°C

Figure 25:
DC/DC SD3 + SD4 + SD5 Efficiency vs. Output Current



SD3 + SD4 + SD5 Efficiency vs. Output Current: V_{IN} = 3.0V, 3MHz operation, XFL4020 1µH coil, T_A = 25°C

Figure 26:
DC/DC SD3 + SD4 + SD5 Efficiency vs. Output Current

SD3 + SD4 + SD5 Efficiency vs. Output Current: V_{IN} = 3.7V, V_{OUT} = 1.2V, 3MHz operation, T_A = 25°C

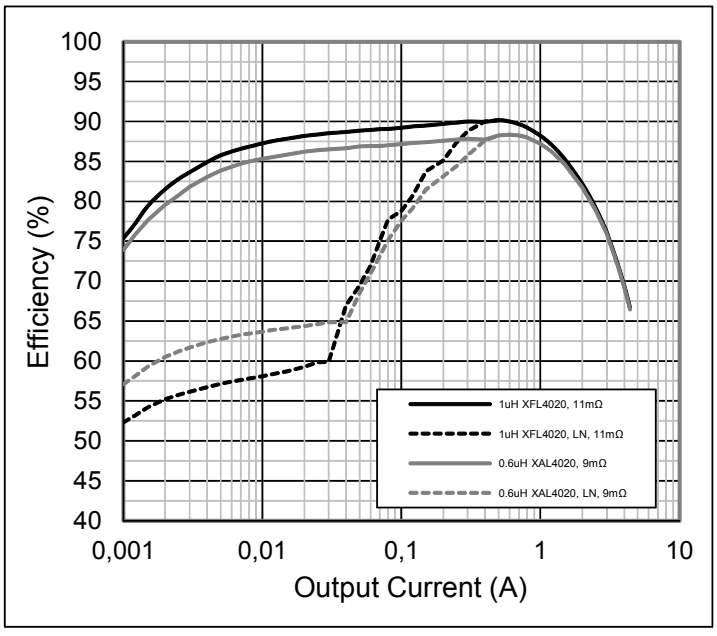
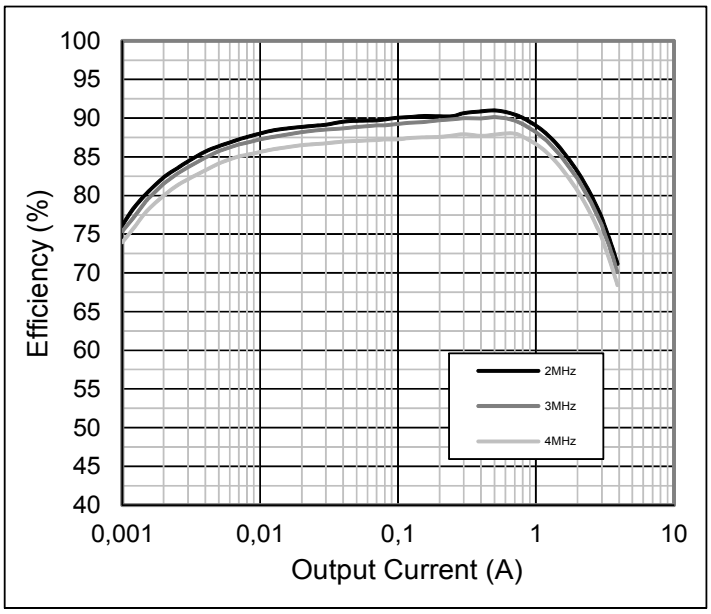


Figure 27:
DC/DC SD3 + SD4 + SD5 Efficiency vs. Output Current

SD3 + SD4 + SD5 Efficiency vs. Output Current: V_{IN} = 3.7V, V_{OUT} = 1.2V, XFL4020 1µH coil, T_A = 25°C

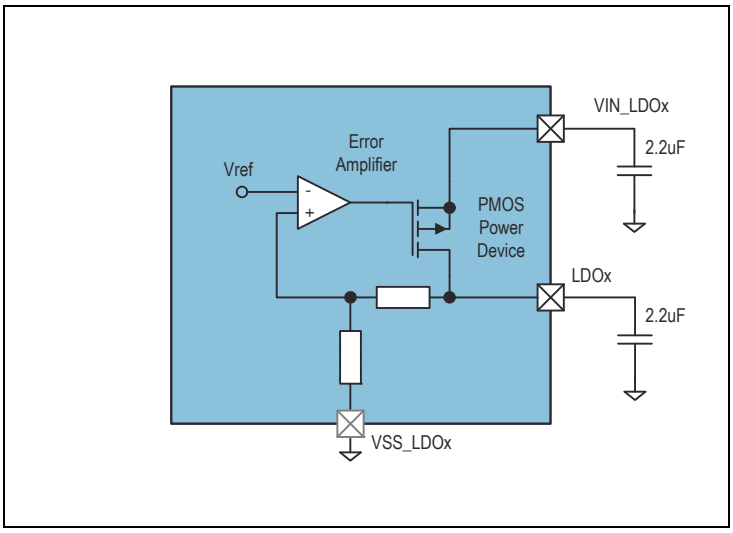


Universal IO LDO Regulators

2 universal IO range LDOs offer a wide input (1.8V to 5.5V) as well as a wide output (0.8 to 3.3V) voltage range to be used for general purpose peripheral supply. Up to 300mA possible output currents are offered with good noise and regulation performance and very low quiescent current even suitable for stand-by power supply.

Figure 28:
Universal IO LDO Block Diagram

AS3709 LDO: Shows the detailed Universal IO LDO Block Diagram



Parameter

Figure 29:
Universal IO LDO Electrical Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	Pin VIN_LDOx	1.75		5.5	V
V_{OUT_TOL}	Output Voltage Tolerance	Min. 40mV	-3		+3	%
V_{OUT}	Output Voltage Range	Pin LDOx I_{OUT} < 150mA, 25mV steps	0.825		3.3	V
I_{OUT_L}	Output Current (1)	ldoX_ilimit = 0 (150mA)	0		150	mA
I_{LIMIT_L}	Current Limit (1)			300		mA
I_{OUT_H}	Output Current (1)	ldoX_ilimit = 1 (300mA)	0		300	mA
I_{LIMIT_H}	Current Limit (1)			500		mA
R_{ON}	On Resistance	LDO1, LDO2		0.6		Ω
PSRR	Power Supply Rejection Ratio	f=1kHz	60			dB
		f=100kHz	30			
I_{OFF}	Shut Down Current			100		nA
I_Q	Quiescent Current	Without load		30	43	µA
t_{START}	Startup Time	Low current used during start-up			500	us
V_{LNR}	Line Regulation	Static		0.07		%/V
		Transient; Slope: tr=15µs; delta 1V		20		mV
V_{LDR}	Load Regulation	Static		0.014		%/mA
		Transient; Slope: tr=15µs; 1mA -> 300mA		30		mV

Note(s):

1. Guaranteed by design and verified by laboratory evaluation and characterization; not production tested

Figure 30:
Universal IO LDO Electrical Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{OUT_LDOx}	Output Capacitor	Ceramic X5R or X7R	0.7	2.2		µF
C_{VIN_LDOx}	Input Capacitor	Ceramic X5R or X7R	1	2.2		µF

Low Power LDO V2_5 Regulator

The low power LDO V2_5 is needed to supply the chip core (analog and digital) of the device. It is designed to get the lowest possible power consumption and still offering reasonable characteristics. To ensure high PSRR and stability, a low-ESR ceramic capacitor of min. 0.7µF must be connected to the output.

Parameter

Figure 31:
Low Power V2_5 LDO Electrical Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
	Supply Voltage Range	See V_{SUP}				
V_{OUT}	Output Voltage		2.4	2.5	2.6	V
R_{ON}	On Resistance	Guaranteed by design		50		Ω
I_{OFF}	Shut Down Current			100		nA
I_Q	Quiescent Current	Guaranteed by design, consider chip internal load for measurements		3		µA
t_{START}	Startup Time			200		µs

Figure 32:
Universal IO LDO Electrical Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{V2_5}	Output Capacitor	Ceramic X5R or X7R	0.7	1		µF

Detailed Description - System Functions

Start-Up

Normal Start-Up

During a normal reset cycle (e.g. after the battery is inserted), after V2_5 is above V_{POR} and V_{SUP} is above ResVoltRise a normal startup happens:

- Configuration of DC/DCs (combined mode or separated) is read from the Boot-OTP
- Startup state machine reads out the internal Boot-OTP
- Reset-Timer is set by the Boot-OTP
- The reset is released when the Reset-Timer expires (external pin XRES)

Parameter

Figure 33:
ON Input Start-Up Condition

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{ON_IL}	ON Low Level Voltage				0.4	V
V_{ON_IH}	ON High Level Voltage		1.4			V
I_{ON_PD}	ON Pull Down Current		4	12		µA