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AS3711

Quad Buck High Current PMIC with Charger

General Description

The AS3711 is a compact System PMU with integrated battery charger and back light driver.

The device offers advanced power management functions. All necessary ICs and peripherals in a battery powered mobile device are supplied by the AS3711. It features 3 DCDC buck converters as well as 8 low noise LDOs. The different regulated supply voltages are programmable via the serial control interface. 4MHz operation with 1uH coils are reducing cost and PCB space.

AS3711 further features a DCDC buck controller which is ideal to support processor core currents up to 3A.

The two step-up converter generate voltages for e.g.the backlight, classD amplifier, USB host support or LCD display supply. Both constant voltage (for e.g. OLED supply) as well as constant current (white LED backlight) operations with three current sinks are possible. An internal voltage protection is limiting the output voltage in the case of external component failures.

AS3711 contains a linear or switching mode Li-Ion battery charger with constant current and constant voltage. The maximum charging current is 1.5A. An integrated battery switch and an optional external switch are separating the battery during charging or whenever an external power supply is present. With this switch it is also possible to operate with no or deeply discharged batteries. A programmable current limit (100mA - 2.5A) can be used to control the maximum current used from a USB supply or charger input. Additional features are a 30V OV protection and battery temperature supervision.

The single supply voltage may vary from 2.7V to 5.5V.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3711, Quad Buck High Current PMIC with Charger are listed below:

Figure 1:
Added Value Of Using AS3711

Benefits	Features
Compact design due to small coils for IO and memory voltage generation	• 3 DCDC step down regulators (2-4MHz) - DVM (0.6V-3.3V;1×1.2-1.5A, 2×0.7-1A) - 60µA quiescent current - 2A with combined DCDC 2 & 3
High current generation for processor core	• DCDC step down controller - DVM (0.6V-3.3V; 2-3A)
Supply multiple independent voltage rails for general IO supplies	• 2 analog low noise LDOs, 6 digital LDOs - 2×1.2-3-3V, 6×0.9-3.3V; 150-300mA - 30µA quiescent current (low power mode) • 1 ultra low power always on LDO 2.5V, 10mA
Backlight boost controller for multiple display configurations or fixed voltage supplies	**HV Backlight Driver** • 2×step up with external transistor - e.g. 0.5-1A@5V; 40mA@50V • Voltage control mode and over-voltage protection • 3 programmable current sinks (max. 40mA) • Possible external PWM dimming input (DLS, CABC)
Self contained free configurable charger with stand alone supervisory functions	**Battery Charger** • Programmable trickle charging (25-220mA) • Programmable constant current charging (up to 1500mA) • Programmable constant voltage charging (3.9V-4.25V) • Charger time-out and temperature supervision • Selectable current limitation for USB mode • Integrated battery switch & ideal diode (linear mode) • External battery switch control (switching mode) • External 30V OV protection
Save supervision in HV which works also without a processor	**Supervisor** • Automatic battery monitoring with interrupt generation and selectable warning level • Automatic temperature monitoring with interrupt generation and selectable warning and shutdown levels
Very low current time keeping and alarm functions without the need of a processor	**Real Time Clock** • Ultra low power 32kHz oscillator • Sec and minute counter, auto wake-up • Programmable alarm • Repeating alarm (seconds, minutes, 2 minutes, or 8 minutes) • 32kHz clock output to peripheral • <1µA total power consumption

Benefits	Features
Flexible multi-purpose IOs for general control or measurement tasks	**General Purpose IOs** • 10-bit general purpose ADC input • Wake-up/sleep and DVM input • PWM (DLS, CABC) dimming input • Status output for: charger, low battery, power good and step-up over-current • Q32k clock output • Interrupt output • PWM output • Step-up feedback input
Flexible and fast adaptations to different processors/applications.	**OTP programmable BOOT Sequence** • Programmable regulator default voltages • Programmable start-up sequence
Enables the processor to check the system state in detail	**General Purpose ADC** • 10-bit resolution • Several internal / external sources - VUSB, VSUP, CHGIN, VBAT - GPIOx, CURRx - XOUT32K, SENSEN_SU1, LX_SD4 - Chip temperature
Easy control of all PMIC functions, Safety shutdown feature, without reset button.	**Control Interface** • I^2C control lines, including watchdog • ON input with 4/8s emergency shut-down • Bidirectional reset, with selectable delay • Ultra low power standby mode
No need for external POR or supervisory	**Power-On Reset Circuit**
Dedicated packages for specific applications. Optimization for PCB cost or size.	**Packaging** • QFN56 7×7mm 0.4mm pitch • CSP64 3.6x3.5mm 0.4mm pitch

Applications

The AS3711, Quad Buck High Current PMIC with Charger, is suitable for Portable Media Players, Portable Navigation Devices, E-Books, Mobile Internet Devices, and Tablet PCs.

Figure 2:
AS3711 Block Diagram for QFN56

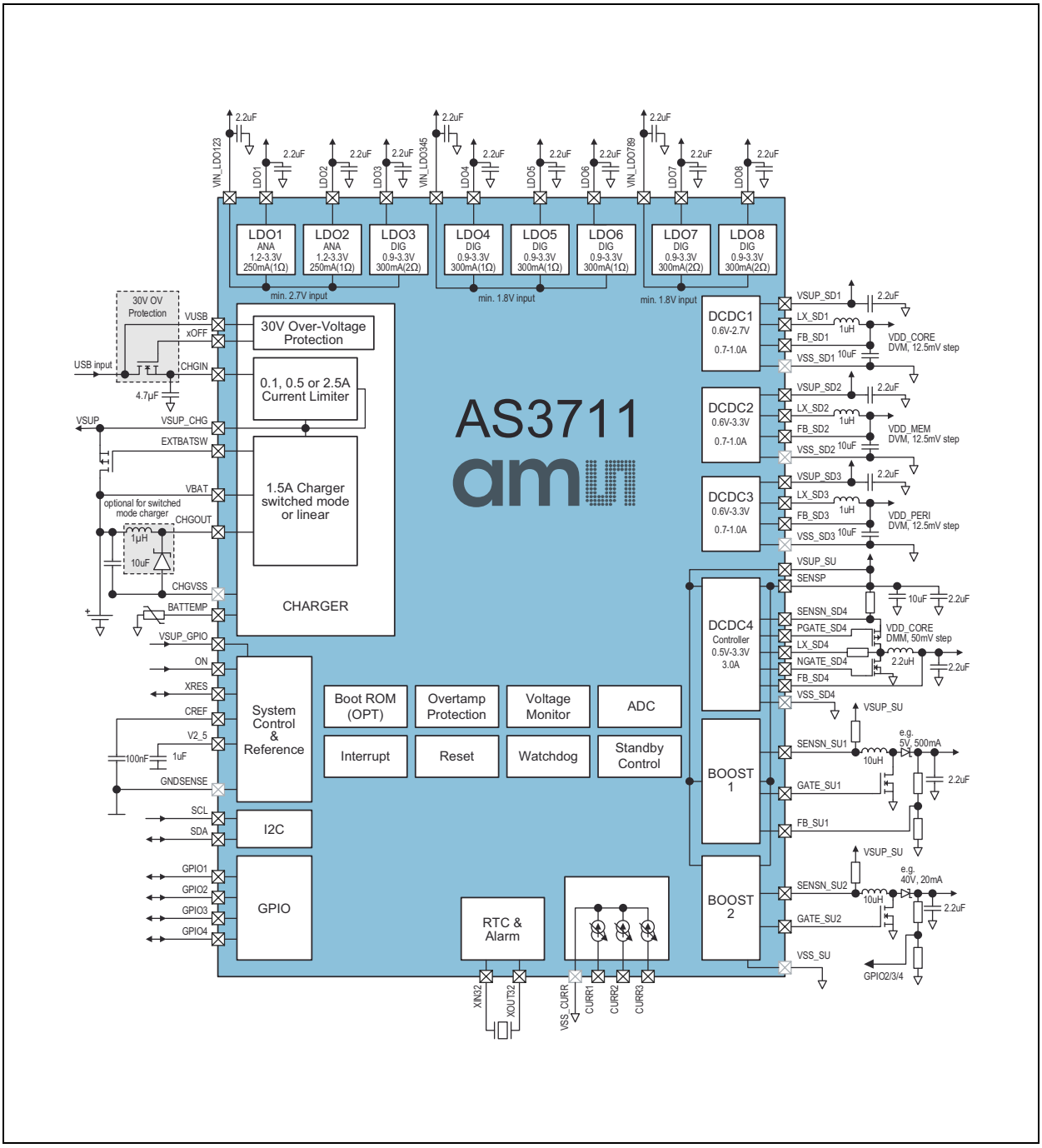
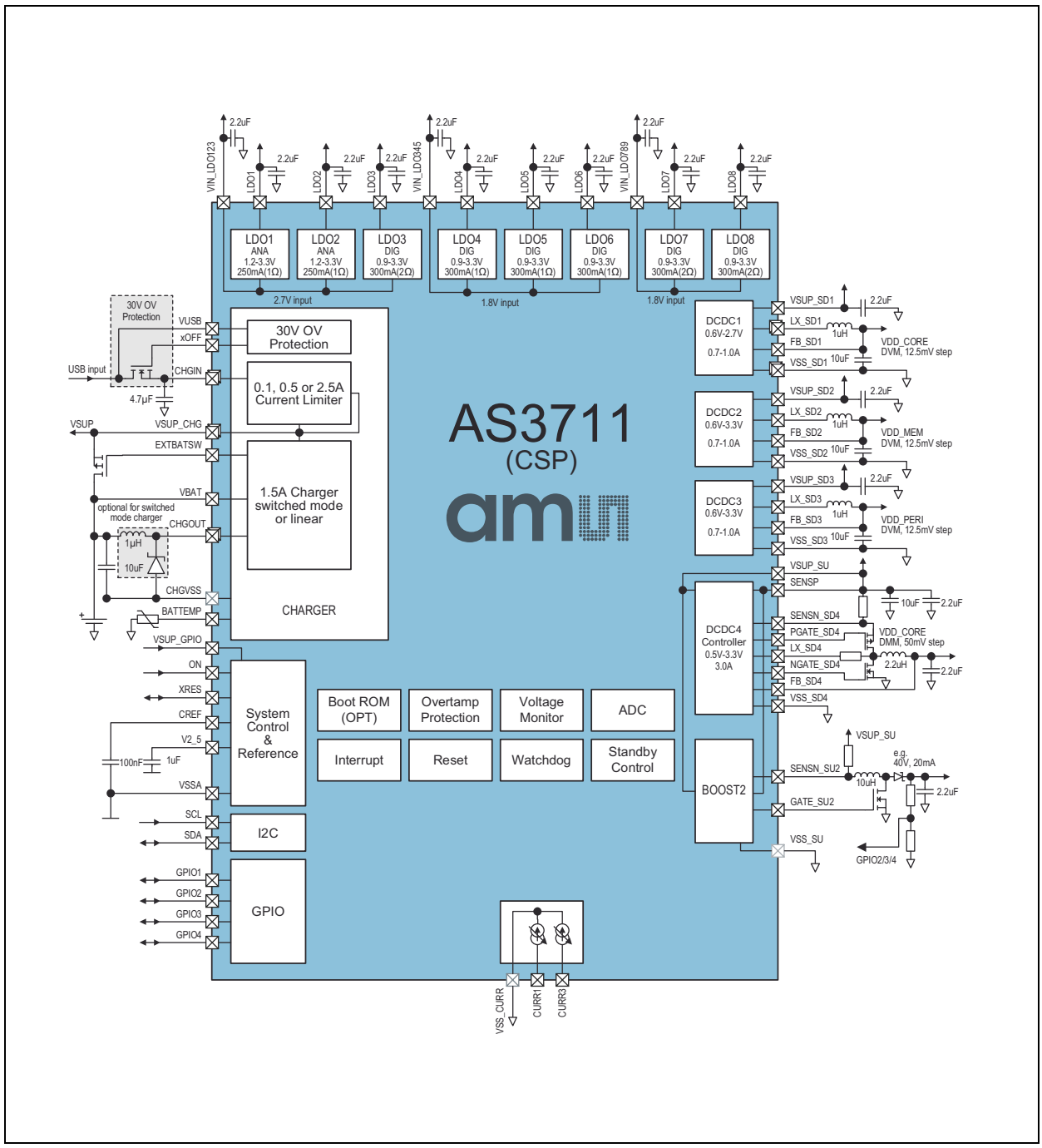


Figure 3:
AS3711 Block Diagram for CSP64



Pin Assignments

Figure 4:
Pin Assignment QFN56 (Top View)

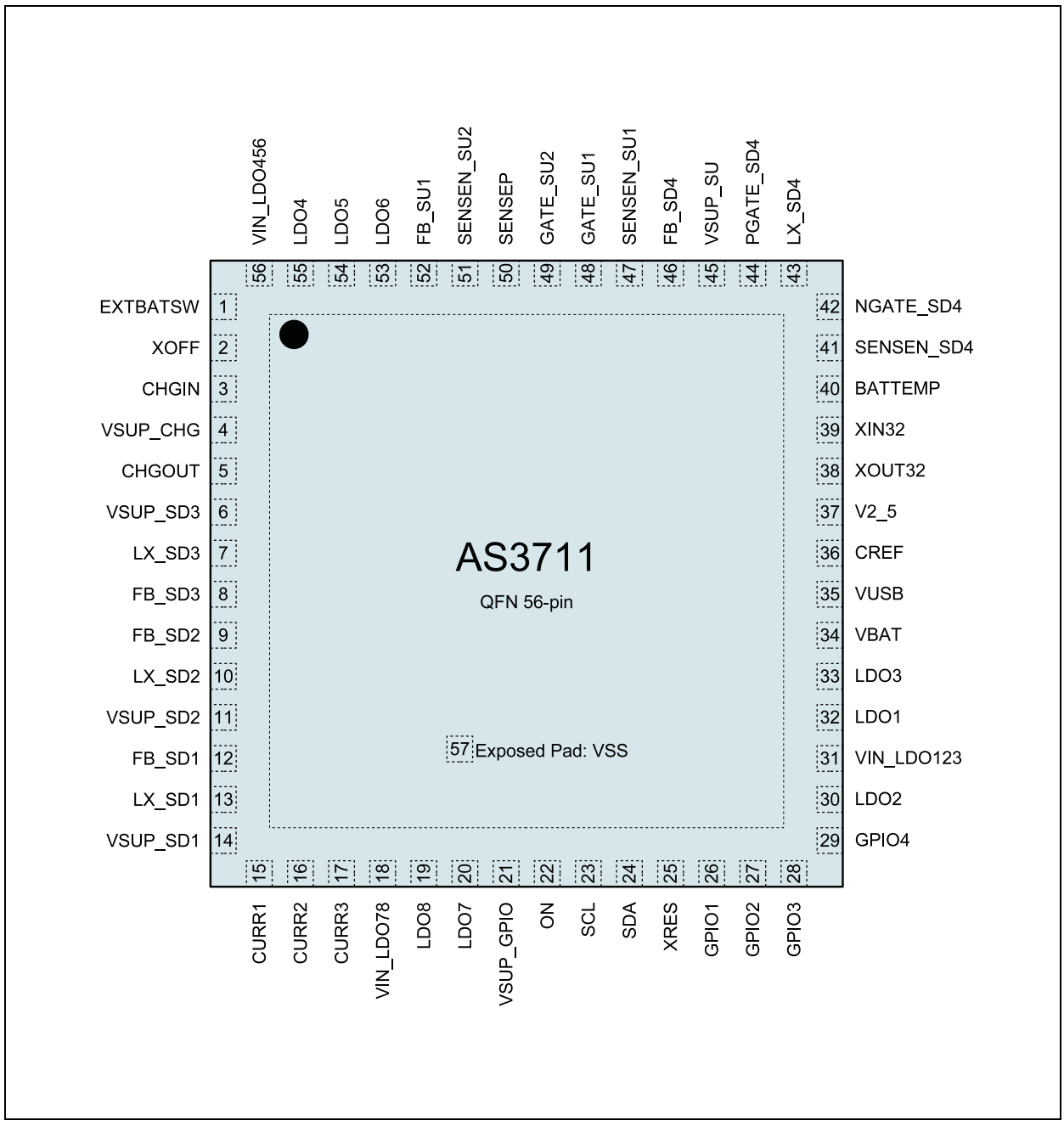


Figure 5:
Ball Assignment CSP64

	1	2	3	4	5	6	7	8
A	LX_SD4	VSS_SSD4	LDO6	LDO5	LDO4	EXTBATSW	CHGIN	CHGIN
B	PGATE_ SD4	FB_SU3	SENSP	VIN_ LDO456	VSSA	XOFF	VSUP_CHG	VSUP_CHG
C	GATE_SU3	VSUP_SU	SENSEN_ SU3	GATE_SU2	VSSA	CHGOUT	CHGOUT	VSUP_SD3
D	BATTEMP	V2_5	CREF	SENSEN_ SU2	GPIO2	FB_SD3	VSS_SD3	LX_SD3
E	VUSB	VBAT	VSSA	GPIO4	XRES	FB_SD2	VSS_SD2	
F	LDO3	LDO1	LDO2	GPIO1	CURR3	FB_SD1	VSUP_SD2	LX_SD2
G	VIN_ LDO123	GPIO3	SDa	ON	VSUP_GPIO	CURR1	VSS_SD1	VSS_SD1
H		SCL	VIN_LDO78	LDO7	LDO8	VSUP_SD1	LX_SD1	LX_SD1

Figure 6:
Pin Descriptions

Pin #		Pin Name	Pin Type	Description	If not used
CSP	QFN	AS3711			
A6	1	EXTBATSW	ANA OUT	External Battery Switch Gate Driver Output	open
B6	2	XOFF	ANA OUT	External OV NMOS Gate Driver Output	open
A7, A8	3	CHGIN	SUP IN	Wall adapter or USB Bus Power Input (after protection)	open
B7, B8	4	VSUP_CHG	SUP IO	Current Limiter Output, Charger Input, connect to VSUPx	always needed
C6, C7	5	CHGOUT	ANA OUT	Linear and DCDC Charger output	open
C8	6	VSUP_SD3	SUP IN	DCDC Step Down 3 Pos. Supply Terminal	always needed
D8	7	LX_SD3	DIG OUT	DCDC Step Down 3 Switch Output to Coil	open
D6	8	FB_SD3	ANA IN	DCDC Step Down 3 Feedback Pin	open
D7	-	VSS_SD3	ANA IO	DCDC Step Down 3 power GND	always needed
E7	-	VSS_SD2	ANA IO	DCDC Step Down 2 power GND	always needed
E6	9	FB_SD2	ANA IN	DCDC Step Down 2 Feedback Pin	open

Pin #		Pin Name	Pin Type	Description	If not used
CSP	QFN	AS3711			
F8	10	LX_SD2	DIG OUT	DCDC Step Down 2 Switch Output to Coil	open
F7	11	VSUP_SD2	SUP IN	DCDC Step Down 2 Pos. Supply Terminal	always needed
F6	12	FB_SD1	ANA IN	DCDC Step Down 1 Feedback Pin	open
G7, G8	-	VSS_SD1	ANA IO	DCDC Step Down 1 power GND	always needed
H7, H8	13	LX_SD1	DIG OUT	DCDC Step Down 1 Switch Output to Coil	open
H6	14	VSUP_SD1	SUP IN	DCDC Step Down 1 Pos. Supply Terminal	always needed
G6	15	CURR1	ANA IO	Load Current Sink 1 Terminal	open
-	16	CURR2	ANA IO	Load Current Sink 2 Terminal	open
F5	17	CURR3	ANA IO	Load Current Sink 3 Terminal	open
H3	18	VINLDO78	SUP IN	LDO 7 & 8 Positive Supply Terminal	always needed
H5	19	LDO8	ANA OUT	LDO8 Output	open
H4	20	LDO7	ANA OUT	LDO7 Output	open
G5	21	VSUP_GPIO	SUP IN	GPIO Positive Supply Terminal, connect to VSUP_CHG	always needed
G4	22	ON	DIG IN	Power Up Input	open
H2	23	SCL	DIG IN	2-wire Serial IF Clock Input	open
G3	24	SDA	DIG IO	2-wire Serial IF Data I/O	open
E5	25	XRES	DIG IO	Reset IO, open-drain (needs external pull-up)	open
F4	26	GPIO1	ANA IO	General Purpose IO 1	open
D5	27	GPIO2	ANA IO	General Purpose IO 2	open
G2	28	GPIO3	ANA IO	General Purpose IO 3	open
E4	29	GPIO4	ANA IO	General Purpose IO 4	open
F3	30	LDO2	ANA OUT	LDO2 Output	open
G1	31	VINLDO123	SUP IN	LDO 1, 2 & 3 Positive Supply Terminal, connect to VSUP_CHG	always needed
F2	32	LDO1	ANA OUT	LDO1 Output	open
F1	33	LDO3	ANA OUT	LDO3 Output	open
E2	34	VBAT	SUP IO	Li-Ion Battery Terminal	open

Pin #		Pin Name	Pin Type	Description	If not used
CSP	QFN	AS3711			
E1	35	VUSB	SUP IN	Wall adapter or USB Bus Power Input (before protection)	open
D3	36	CREF	ANA IO	Reference Bypass Capacitor Terminal	always needed
D2	37	V2_5	ANA OUT	Internal 2.5V Regulator Supply Output	always needed
-	38	XOUT32	ANA OUT	RTC 32kHz Crystal Drive Terminal	open
-	39	XIN32	ANA IN	RTC 32kHz Crystal Feedback Terminal	open
D1	40	BATTEMP	ANA IO	Li-Ion Battery Charger Temperature Sensor Input	open
C3	41	SENSEN_SD4	ANA IN	DCDC Step Down 4 Negative Sense Resistor Input	open
C1	42	NGATE_SD4	ANA OUT	DCDC Step Down 4 ext. NMOS Gate Driver Output	open
A1	43	LX_SD4	ANAIN	DCDC Step Down 4 Sense Input	open
B1	44	PGATE_SD4	ANA OUT	DCDC Step Down 4 ext. PMOS Gate Driver Output	open
A2	-	VSS_SD4	ANA IO	DCDC Step Down 4 power GND	always needed
C2	45	VSUP_SU	SUP IN	DCDC Step Down 4 Positive Supply Terminal, connect to VSUP_CHG	always needed
B2	46	FB_SD4	ANA IN	DCDC Step Down 4 Feedback Pin	open
-	47	SENSEN_SU1	ANA IN	DCDC Step Up 1 Negative Sense Resistor Input	open
-	48	GATE_SU1	ANA OUT	DCDC Step Up 1 ext. NMOS Gate Driver Output	open
C4	49	GATE_SU2	ANA OUT	DCDC Step Up 2 ext. NMOS Gate Driver Output	open
B3	50	SENSEP	ANA IN	DCDC Step Up 1, 2 & Step Down 4 Positive Sense Resistor Input	open
D4	51	SENSEN_SU2	ANA IN	DCDC Step Up 2 Negative Sense Resistor Input	open
-	52	FB_SU1	ANA IN	DCDC Step Up 1 Feedback Pin	open
A3	53	LDO6	ANA OUT	LDO6 Output	open

Pin #		Pin Name	Pin Type	Description	If not used
CSP	QFN	AS3711			
A4	54	LDO5	ANA OUT	LDO5 Output	open
A5	55	LDO4	ANA OUT	LDO4 Output	open
B4	56	VINLDO456	SUP IN	LDO 4, 5 & 6 Positive Supply Terminal	always needed
B5, C5, E3	-	VSSA	ANA IO	Analog GND input	always needed

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 7:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
	5V pins	-0.5	7.0	V	Applicable for pins VSUP_CHG, VSUP_SD1/2/3, VSUP_SU, VSUP_GPIO, VIN_LDO123/456/78, GPIO1/2/3/4, GATE_SU1/2, NGATE_SD4, PGATE_SD4, FB_SU1, SENSEP, SENSEN_SU1/2, SENSEN_SD4, VBAT, LDO1/2/3/4/5/6/7/8, FB_SD1/2/ 3/4, LX_SD1/2/3/4, XRES, SCL, SDA
	3V pins	-0.5	5.0	V	Applicable for pins V2_5, CREF, ON, BATTEMP, XIN32, XOUT32
	30V pins	-0.5	32	V	Applicable for pin VUSB, XOFF, CURR1/2/3
I_{SCR}	Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC JESD78
Continuous Power Dissipation (T_A = +70°C)					
P_T	Continuous power dissipation		1.4	W	P_T [(1)] for CSP64 package (R_{TH} ~ 40K/W)
			1.8	W	P_T [(1)] for QFN56 package (R_{TH} ~ 30K/W)
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM		±1.5	kV	Norm: JEDEC JESD22-A114F
Temperature Ranges and Storage Conditions					
T_{AMB}	Operating Temperature	-40	+85	°C	
T_J	Junction Temperature		+125	°C	for CSP64 package
			+150	°C	for QFN56 package
T_{STRG}	Storage Temperature Range	-55	+150	°C	

Symbol	Parameter	Min	Max	Units	Comments
T_{BODY}	Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020 (2) For QFN, the lead finish for Pb-free leaded packages is matte tin (100% Sn)
RH_{NC}	Humidity non-condensing	5	85	%	
MSL	Moisture Sensitive Level	1			For CSP64, represents an unlimited max. floor live time
		3			For QFN56, represents a max. floor life time of 168h

Note(s) and/or Footnote(s):

1. Depending on actual PCB layout and PCB used.
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices".

Electrical Characteristics

VSUPx=+2.7V to +5.5V, T_A =-40°C to +85°C. Typical values are at VSUPx=+3.6V, T_A=+25°C, unless otherwise specified.

The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 8:
Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VUSB	Charger HV Input		0	5	30	V
CHGIN	Charger LV Input		0	5	5.5	V
VSUPx	Supply Voltage VSUP_x		2.7	3.6	5.5	V
VINLDO123	Supply Voltage for LDO 1, 2 & 3		2.7	3.6	5.5	V
VINLDO456	Supply Voltage for LDO 4, 5 & 6		1.8	3.6	5.5	V
VINLDO78	Supply Voltage for LDO 7 & 8		1.8	3.6	5.5	V
V2_5	Voltage on Pin V2_5		2.4	2.5	2.6	V
I_{low_power}	Low Power current	@ VSUPx = 4.2V		220		µA
I_{power_off}	Power-Off current	All regulators OFF V2_5 ON		10		µA

Typical Operating Characteristics

Please see operating characteristics in the block description chapters.

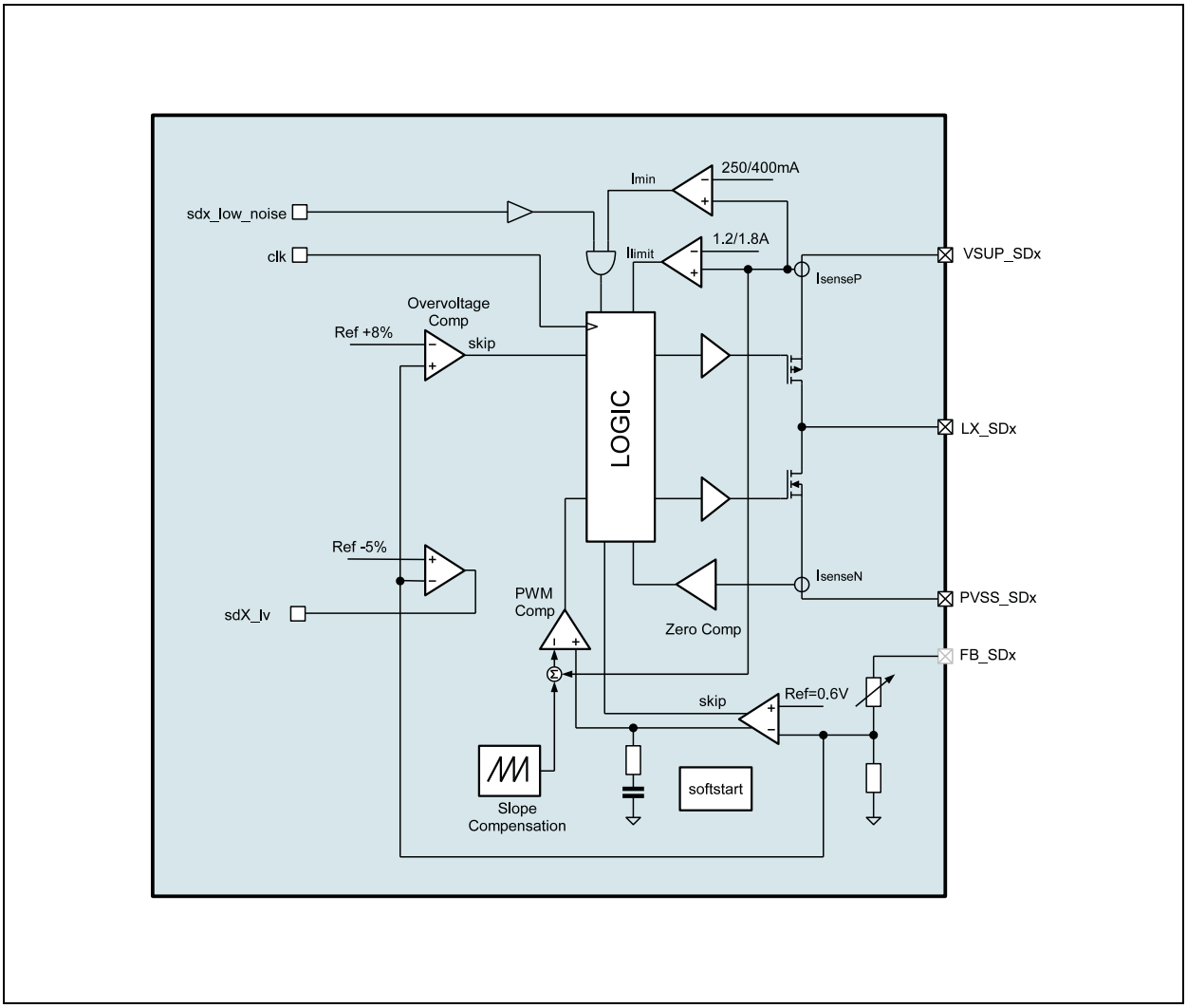
Detailed Description - Power Management Functions

DCDC Step-Down Converter

Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 1A (SD2, SD3) and 1.5A for SD1, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC and the coil during overload condition.

Figure 9:
Step Down DC/DC Converter Block diagram



Mode Settings

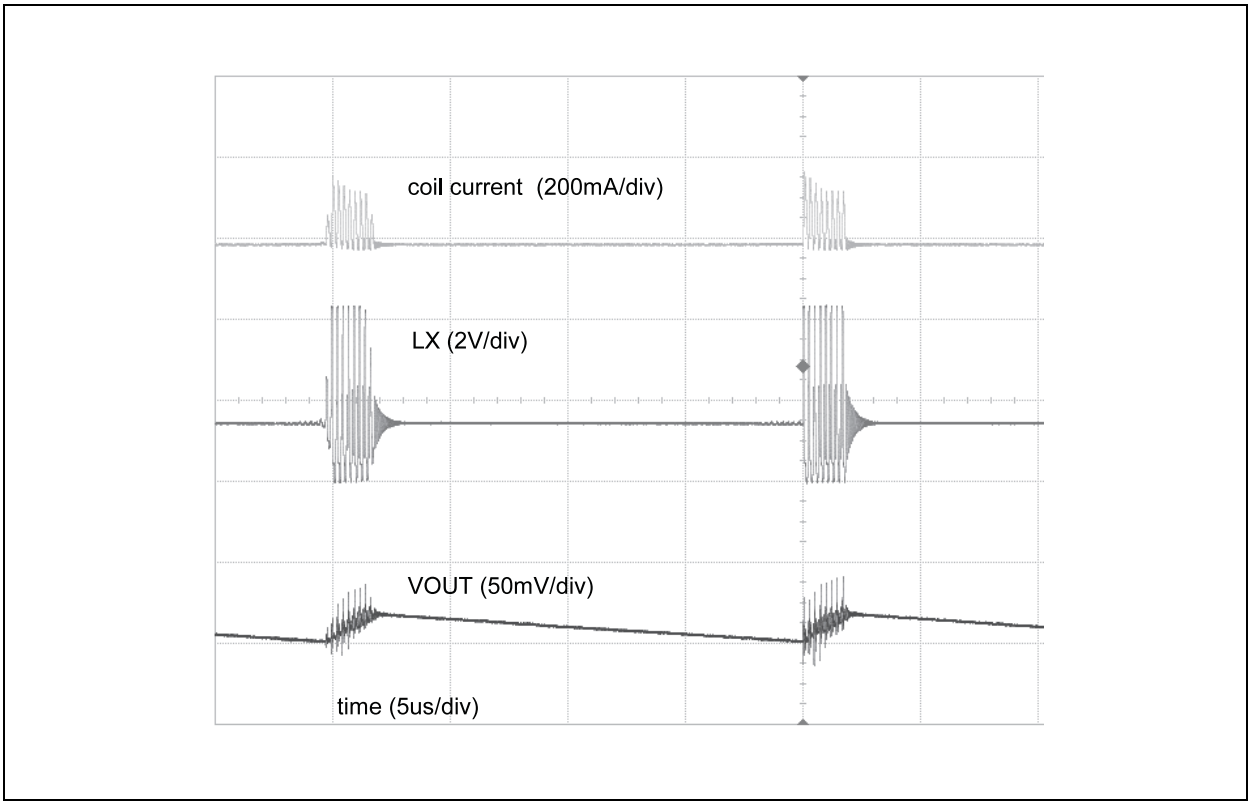
Low ripple, low noise operation:

Bit settings: sdX_low_noise=1

In this mode there is no minimum coil current necessary before switching OFF the PMOS. As long as the load current is superior to the ripple current the device operates in continuous mode. When the load current gets lower, the discontinuous mode is triggered. As result, the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to tmin_on to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences.

Only in the case the load current gets so small that less than the minimum ON-time of the PMOS would be needed to keep the loop in regulation the regulator will enter low power mode operation. The crossover point is about 15mA for Vin=3V, Vout=1.2V, 1uH, 4MHz.

Figure 10:
DCDC Buck with enabled Low Noise Mode



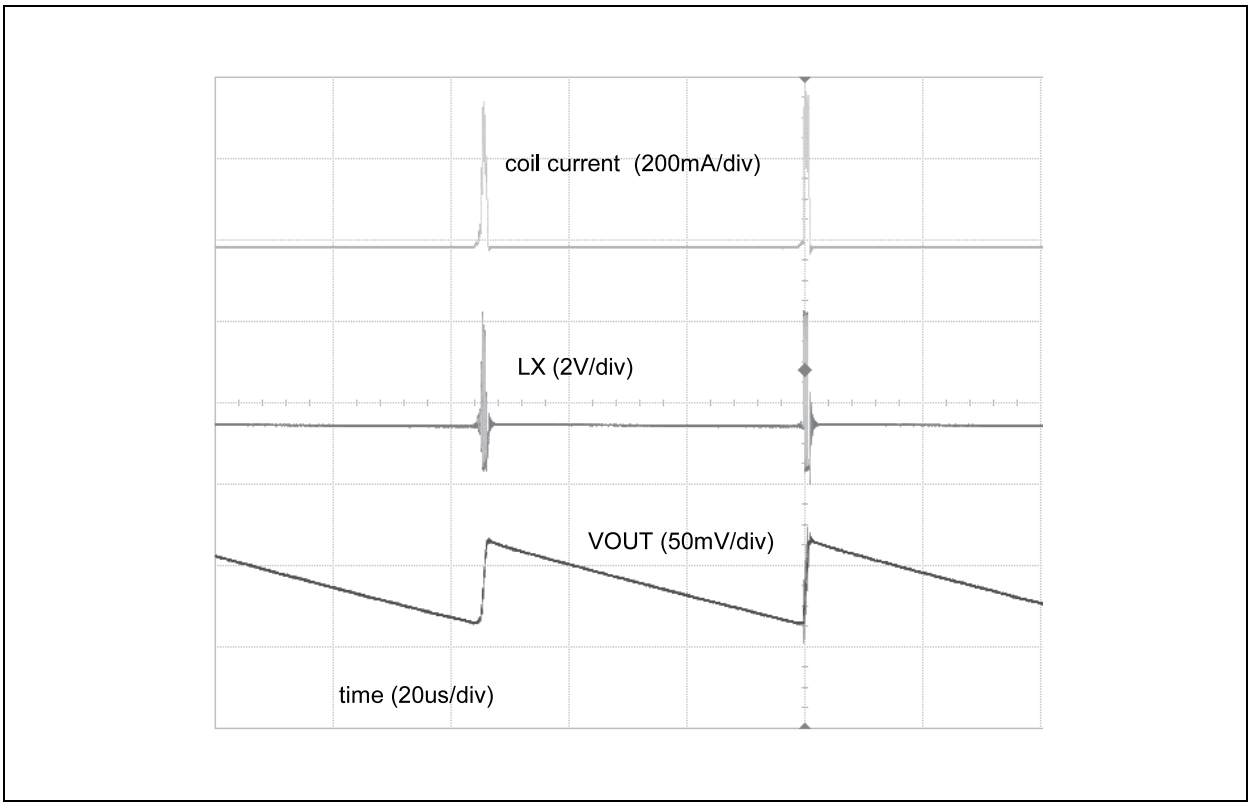
High efficiency operation (default setting):

Bit settings: sdX_low_noise=0

In this mode there is a minimum coil current necessary before switching OFF the PMOS. As a result there are less pulses necessary at low output loads, and therefore the efficiency at low output load is increased. As drawback this mode increases the ripple up to a higher output currents.

The crossover point to low power mode is already reached at reasonable high output currents. (e.g. @110mA for Vin=3V, Vout=1.2V, 1uH, 4MHz)

Figure 11:
DCDC Buck with disabled Low Noise Mode



It's possible to switch between these two modes during operation:

Low power mode operation (automatically controlled):

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at ±5% of the target value to react quickly on large over/undershoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

DVM (Dynamic Voltage Management)

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

DVM can be selected for all step-down converters, but only for one at a time. (see sd_dvm_select and dvm_time description)

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs an 22uF output capacitor instead the 10uF one to guarantee the stability of the regulator. The mode is enabled by setting sdX_fast =1.

Selectable Frequency Operation

Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency. The frequency for SD1, SD2 and SD3 can be set to 2, 3 or 4MHz. This mode is selected by setting sdX_freq and sdX_fsel to the appropriate values.

100% PMOS ON Mode for Low Dropout Regulation

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

Step-Down Converter Configuration Modes

The step down DCDC converters have two configuration modes to deliver different output currents for the applications. The operating mode is selected by setting the bit sd3_slave (the default is set by the Boot-OTP).

Figure 12:
DC/DC step-down SD1, SD2, SD3 Normal Operating Mode; sd3_slave = 0

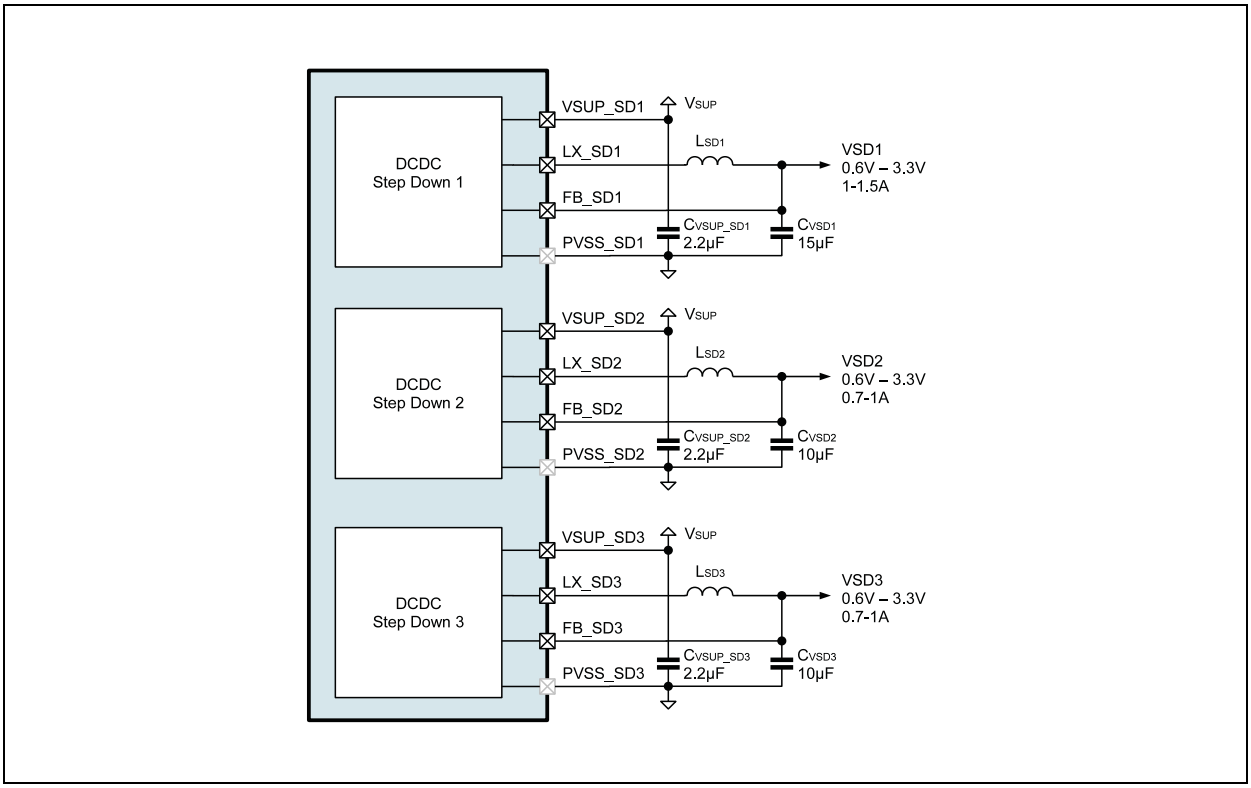
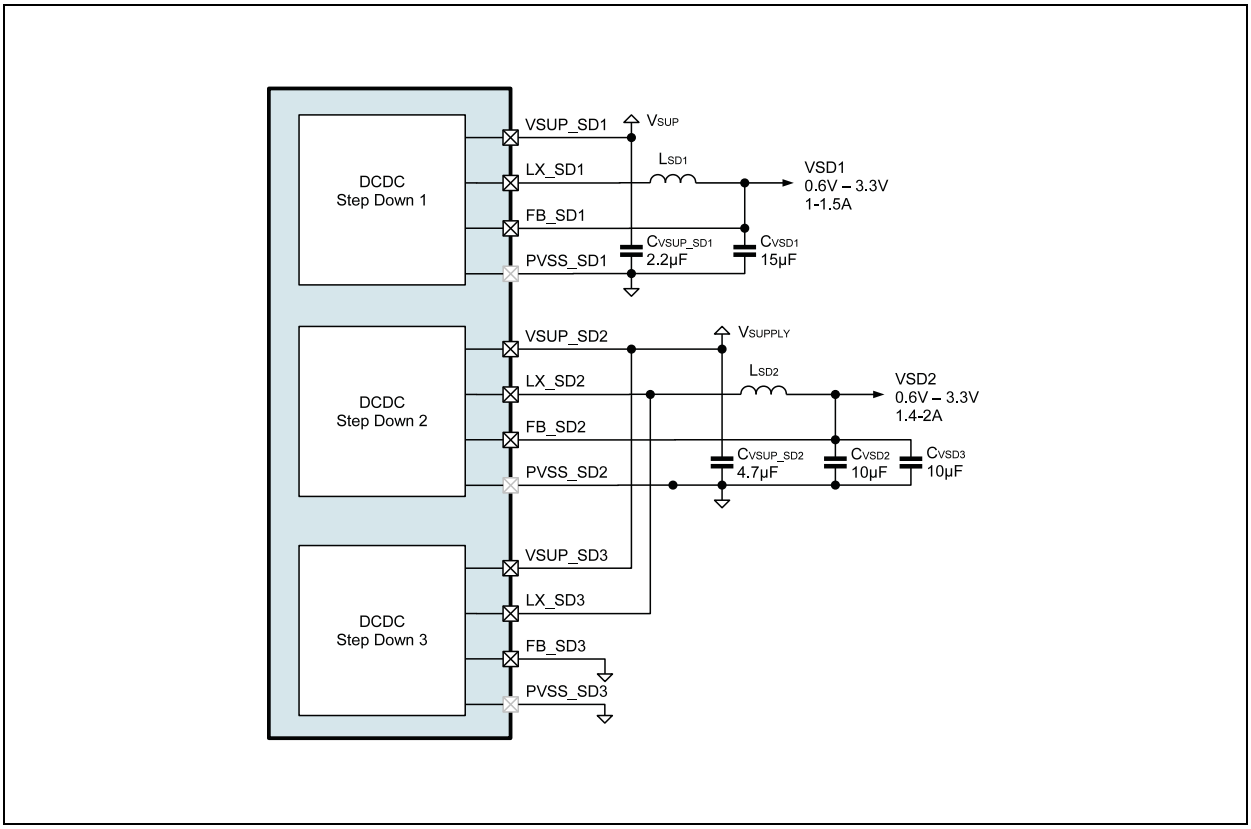


Figure 13:
DC/DC step-down SD1, SD2, SD3 2A Operating Mode; sd3_slave = 1



Parameter

Figure 14:
Step Down DC/DC Converter Parameters

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IN}	Input voltage	Pin VSUP_SDx	2.7		5.5	V
V_{OUT}	Regulated output voltage		0.6125		3.35	V
VOUT_tol	Output voltage tolerance	min. 40mV	-3		+3	%
I_{LIMIT}	Current limit	SD1		1.8		A
		SD2, SD3		1.2		A
RPSW	P-Switch ON resistance	SD1; VSUP_SDx=3.0V		0.17	0.4	Ω
		SD2, SD3; VSUP_SDx=3.0V		0.25	0.5	Ω
RNSW	N-Switch ON resistance	SD1; VSUP_SDx=3.0V		0.17	0.4	Ω
		SD2, SD3; VSUP_SDx=3.0V		0.25	0.5	Ω
I_{Load}	Load current	SD1	0		1.5	A
		SD2, SD3	0		1	A
f_{SW}	Switching frequency	sdX_frequ=1, sdX_fsel=1; fclk_int =4MHz		4		MHz
		sdX_frequ=1, sdX_fsel=0; fclk_int =4MHz		3		MHz
		sdX_frequ=0, sdX_fsel=0; fclk_int =4MHz		2		MHz
tmin_on	Minimum ON time			40		ns
ηeff	Efficiency	Iout=300mA, Vout=2V, VSUP=3.5V		92		%
I_{VDD}	Current consumption	Operating current without load		60		µA
		Shutdown current		0.1		

Figure 15:
Step Down DC/DC External Components

Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{FB_SD1}	Output capacitor	Ceramic X5R or X7R	10.0	15		µF
		Ceramic X5R or X7R, fast mode=1	20.0	30		µF
C_{FB_SD2-3}	Output capacitor	Ceramic X5R or X7R	8.0	10		µF
		Ceramic X5R or X7R, fast mode=1	16.0	20		µF
C_{VSUP_SD1-3}	Input capacitor	Ceramic X5R or X7R		2.2		µF
$L_{SD1-SD3}$	Inductor	4MHz operation		1		µH
		3MHz operation		1		
		2MHz operation		2.2		

All measurements where done with 55mΩ chip coils (Murata LQM2HPN1R0MG0). Using coils with lower on-resistance will increase the efficiency especially at higher output currents.

Figure 16:
Step Down DC/DC SD1 Efficiency vs. Output Current; V_{SUP} = 3.0V, 3MHz operation, T_A = +25°C

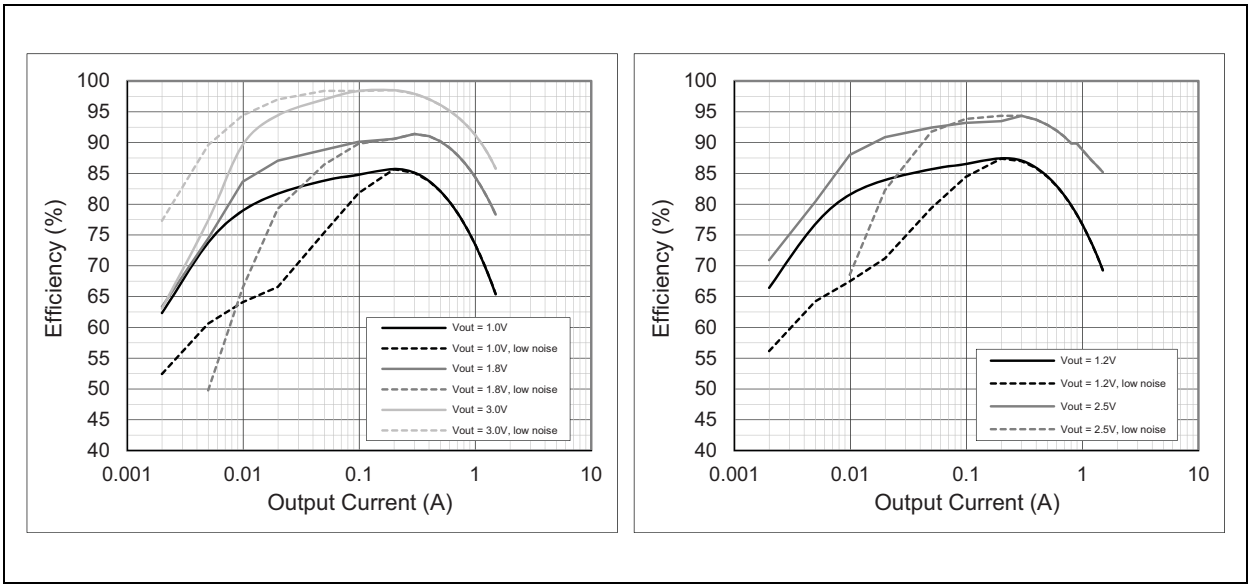


Figure 17:
Step Down DC/DC SD1 Efficiency vs. Output Current; V_{SUP} = 3.8V, 3MHz operation, T_A = +25°C

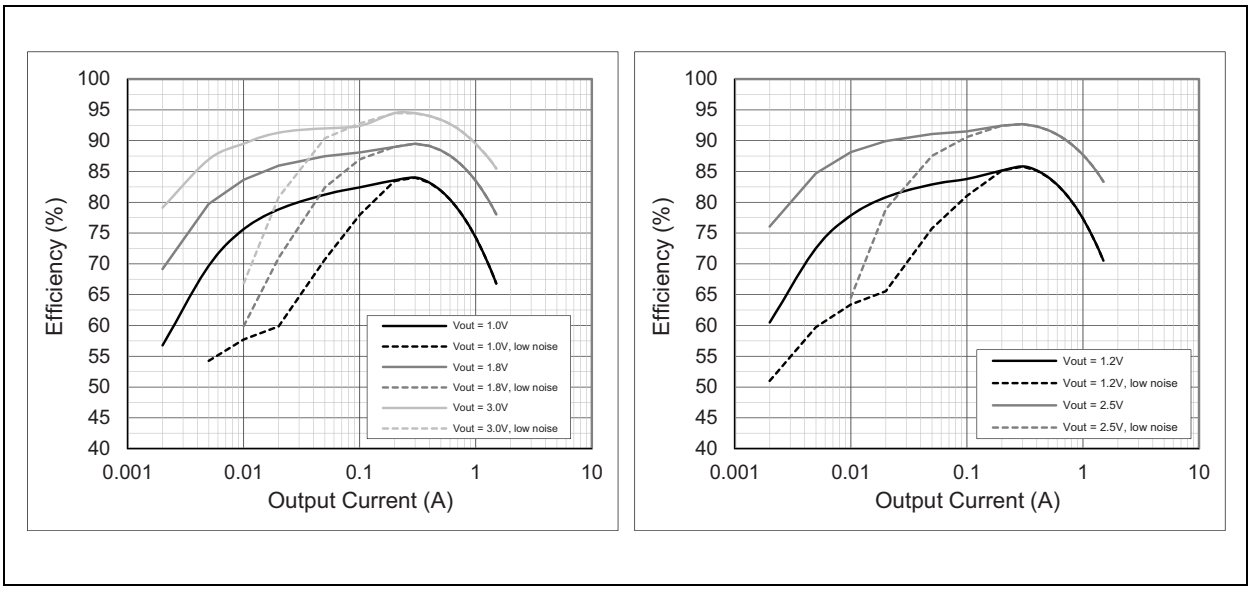


Figure 18:
Step Down DC/DC SD2 & SD3 Efficiency vs. Output Current; V_{SUP} = 3.0V, 3MHz operation, T_A = +25°C

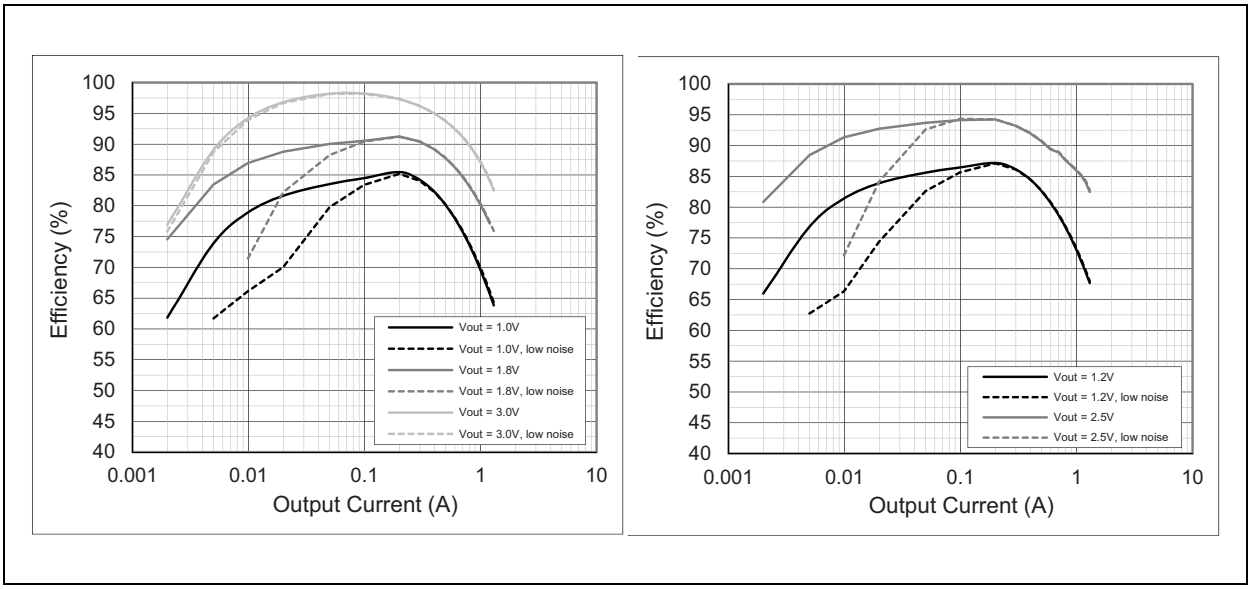
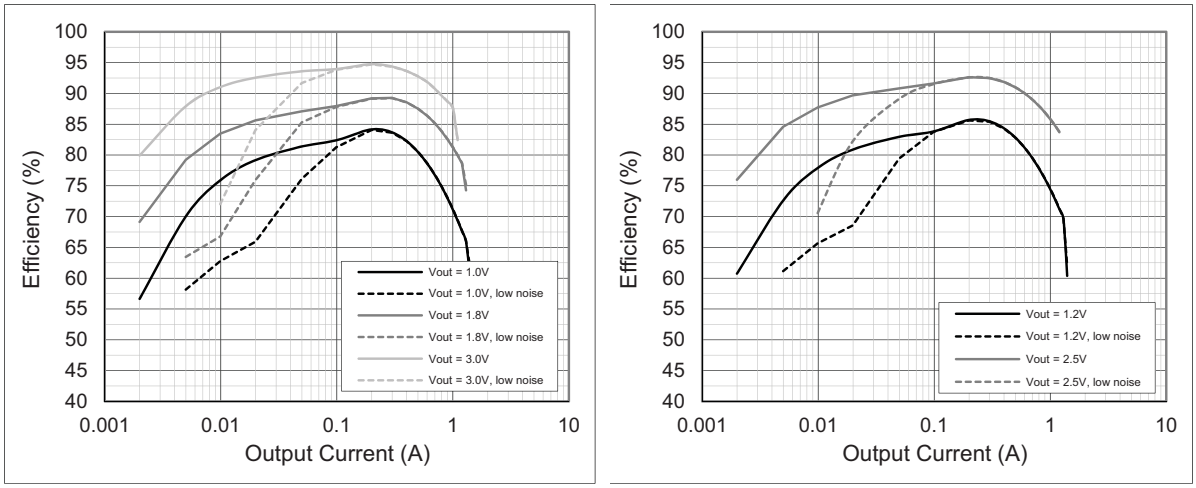


Figure 19:
Step Down DC/DC SD2 & SD3 Efficiency vs. Output Current; V_{SUP} = 3.8V, 3MHz operation, T_A = +25°C

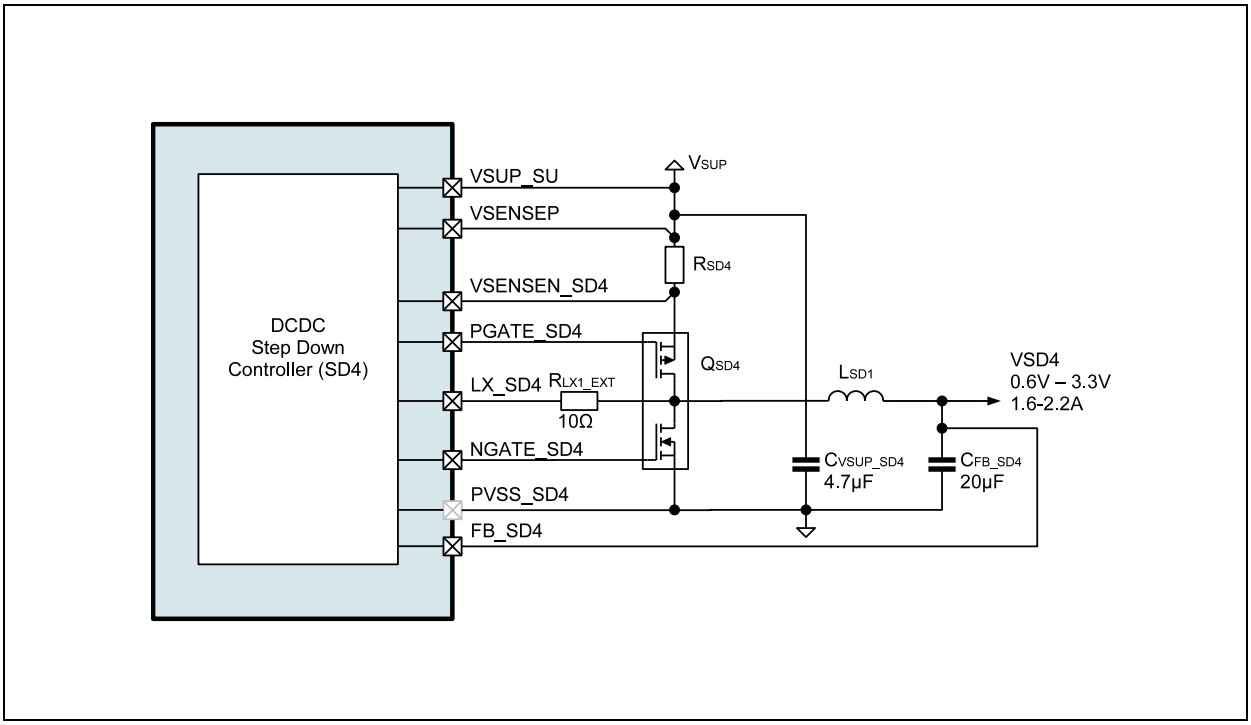


DCDC Step-Down Controller

Description

The Step-Down controller SD4 uses a paired external NMOS, PMOS to achieve higher output currents. the maximum output current is determined by the external transistor and shunt used.

Figure 20:
DC/DC step-down Controller



Parameter

Figure 21:
Step Down DC/DC Controller Parameters

Symbol	Parameter	Note	Min	Typ	Max	Unit
VIN	Input voltage	Pin VSUP_SDx	2.7		5.5	V
VOUT	Regulated output voltage		0.6125		3.3	V
VOUT_tol	Output voltage tolerance	min. 40mV	-3		+3	%
V_{rsense_max}	Current limit voltage at Rsense	E.g.: 2.6A for 0.033Ω sense resistor		100		mV
f_{SW}	Switching frequency	fclk_int = 4MHz		1		MHz

Figure 22:
Step Down DC/DC Controller External Components

Symbol	Parameter	Note	Min	Typ	Max	Unit
External Components 1.6A						
Q_{SD4}	Paired NMOS-PMOS	FDC6327C	PMOS: Ron=250mOhm, 1.6A NMOS: Ron=120mOhm, 2.7A			
R_{SD4}	Shunt	0.15W; ±1%		50		mΩ
C_{FB_SD4}	Output capacitor	Ceramic X5R or X7R	16.0	20		µF
		Ceramic X5R or X7R, fast mode=1	32.0	40		µF
C_{VSUP_SD4}	Input capacitor	Ceramic X5R or X7R		10		µF
L_{SD4}	Inductor	2A rated, 1MHz operation		2.2		µH
External Components 2.2A						
Q_{SD4}	Paired NMOS-PMOS	FDC6420C	PMOS: Ron=190mOhm, 2.2A NMOS: Ron=95mOhm, 3A			
R_{SD4}	Shunt	0.2W; ±1%		33		mΩ
C_{FB_SD4}	Output capacitor	Ceramic X5R or X7R	24.0	30		µF
		Ceramic X5R or X7R, fast mode=1	48.0	60		µF
C_{VSUP_SU}	Input capacitor	Ceramic X5R or X7R		10		µF
L_{SD4}	Inductor	2.5A rated, 1MHz operation		1.5		µH

Symbol	Parameter	Note	Min	Typ	Max	Unit
External Components 3A						
Q_{SD4}	paired NMOS-PMOS	NTHD3102C	PMOS: Ron=83mOhm, 4.2A NMOS: Ron=37mOhm, 5.5A			
R_{SD4}	Shunt	0.3W; ±1%		25		mΩ
C_{FB_SD4}	Output capacitor	Ceramic X5R or X7R	32.0	40		µF
		Ceramic X5R or X7R, fast mode =1	64.0	80		µF
C_{VSUP_SU}	Input capacitor	Ceramic X5R or X7R		10		µF
L_{SD4}	Inductor	3A rated, 1MHz operation		1		µH

All measurements where done with the 2.2A transistors (Fairchild FDC6420C) and 70mΩ chip coils (Murata LQM2HPN1R0MG0). Using coils with lower on-resistance will increase the efficiency especially at higher output currents.