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AS3713

Quad Buck High Current PMIC without Charger

1 General Description

The AS3713 is a compact System PMU with integrated battery charger and back light driver.

The device offers advanced power management functions. All necessary ICs and peripherals in a battery powered mobile device are supplied by the AS3713. It features 3 DCDC buck converters as well as 8 low noise LDOs. The different regulated supply voltages are programmable via the serial control interface. 4MHz operation with 1uH coils are reducing cost and PCB space.

AS3713 further features a DCDC buck controller which is ideal to support processor core currents up to 3A.

The two step-up converter generate voltages for e.g.the backlight, classD amplifier, USB host support or LCD display supply. Both constant voltage (for e.g. OLED supply) as well as constant current (white LED backlight) operations with three current sinks are possible. An internal voltage protection is limiting the output voltage in the case of external component failures.

The single supply voltage may vary from 2.7V to 5.5V.

2 Key Features

Voltage Generation

- 3 DCDC step down regulators (2-4MHz)
  - DVM (0.6V-3.3V;1x 1.2-1.5A, 2x 0.7-1A)
  - 60µA quiescent current
  - 2A with combined DCDC 2 & 3
- DCDC step down controller
  - DVM (0.6V-3.3V; 2-3A)
- 2 analog low noise LDOs, 6 digital LDOs
  - 2x 1.2-3-3V, 6x 0.9-3.3V; 150-300mA
  - 30µA quiescent current (low power mode)
- 1 ultra low power always on LDO 2.5V, 10mA
- Power supply supervision
- 4sec and 8sec emergency shut-down
- Stand-by function with voltage selection

HV Backlight Driver

- 2x step up with external transistor
  - e.g. 0.5-1A@5V; 40mA@50V
- Voltage control mode and over-voltage protection
- 3 programmable current sinks (max. 40mA)
- Possible external PWM dimming input (DLS, CABC)

Supervisor

- Automatic battery monitoring with interrupt generation and selectable warning level
- Automatic temperature monitoring with interrupt generation and selectable warning and shutdown levels

Real Time Clock

- Ultra low power 32kHz oscillator
- Sec and minute counter, auto wake-up
- Programmable alarm
- Repeating alarm (seconds, minutes, 2 minutes, or 8 minutes)
- 32kHz clock output to peripheral
- <1µA total power consumption

General Purpose IOs

- 10-bit general purpose ADC input
- Wake-up/sleep and DVM input
- PWM (DLS, CABC) dimming input
- Status output for: low battery, power good and step-up over-current
- Q32k clock output
- Interrupt output
- PWM output
- Step-up feedback input

OTP programmable BOOT Sequence

- Programmable regulator default voltages
- Programmable start-up sequence

General Purpose ADC

- 10-bit resolution
- Several internal / external sources
  - VUSB, VSUP, CHGIN, VBAT
  - GPIOx, CURRx
  - XOUT32K, SENSEN_SU1, LX_SD4
  - Chip temperature

Control Interface

- I2C control lines, including watchdog
- ON input
- Bidirectional reset, with selectable delay
- Ultra low power standby mode

Power-On Reset Circuit

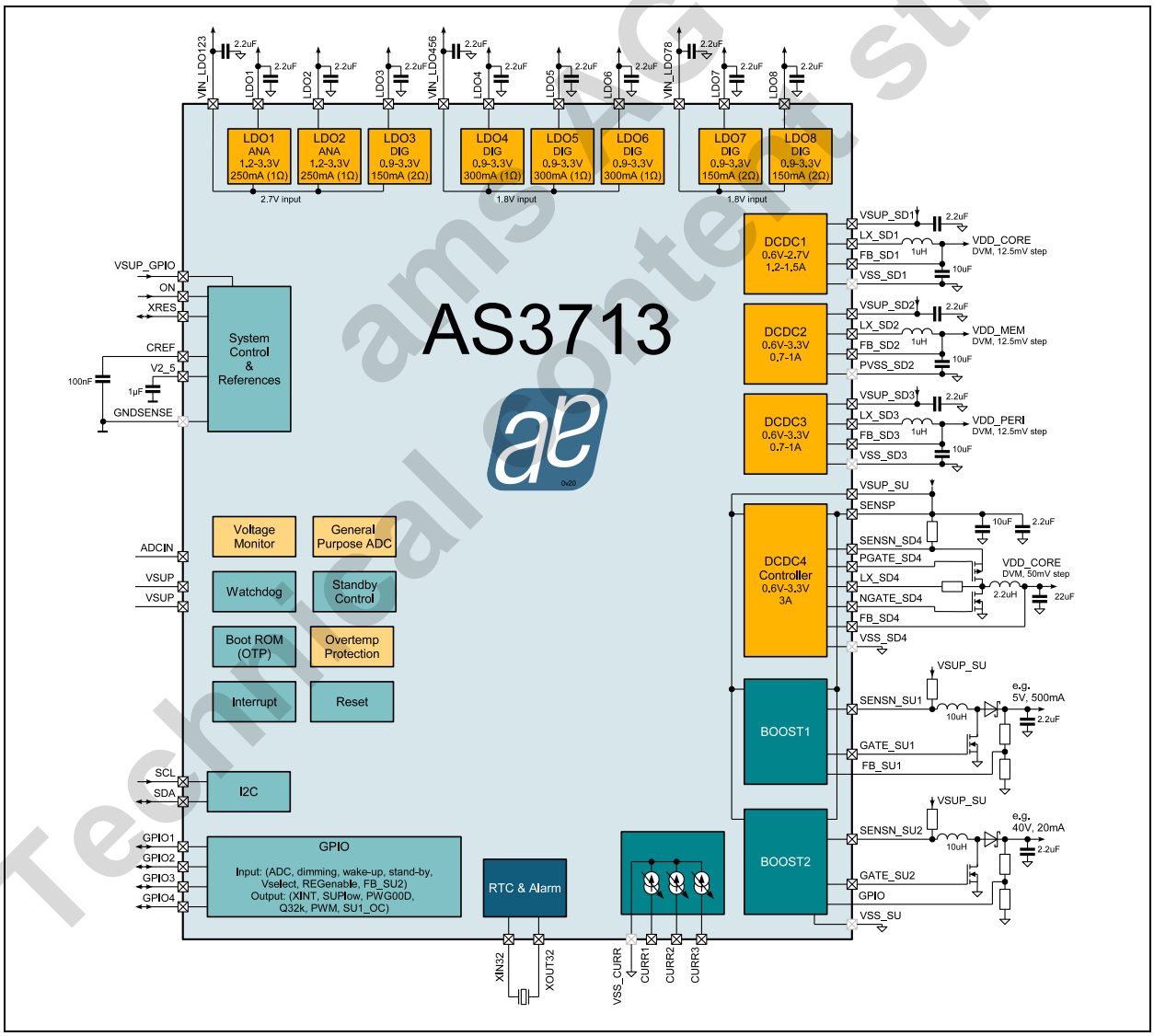
Packaging

QFN56 7x7mm 0.4mm pitch

3 Application

The device is suitable for Set-top Boxes, Portable Media Players, Portable Navigation Devices, E-Books, Mobile Internet Devices, and Tablet PCs. .

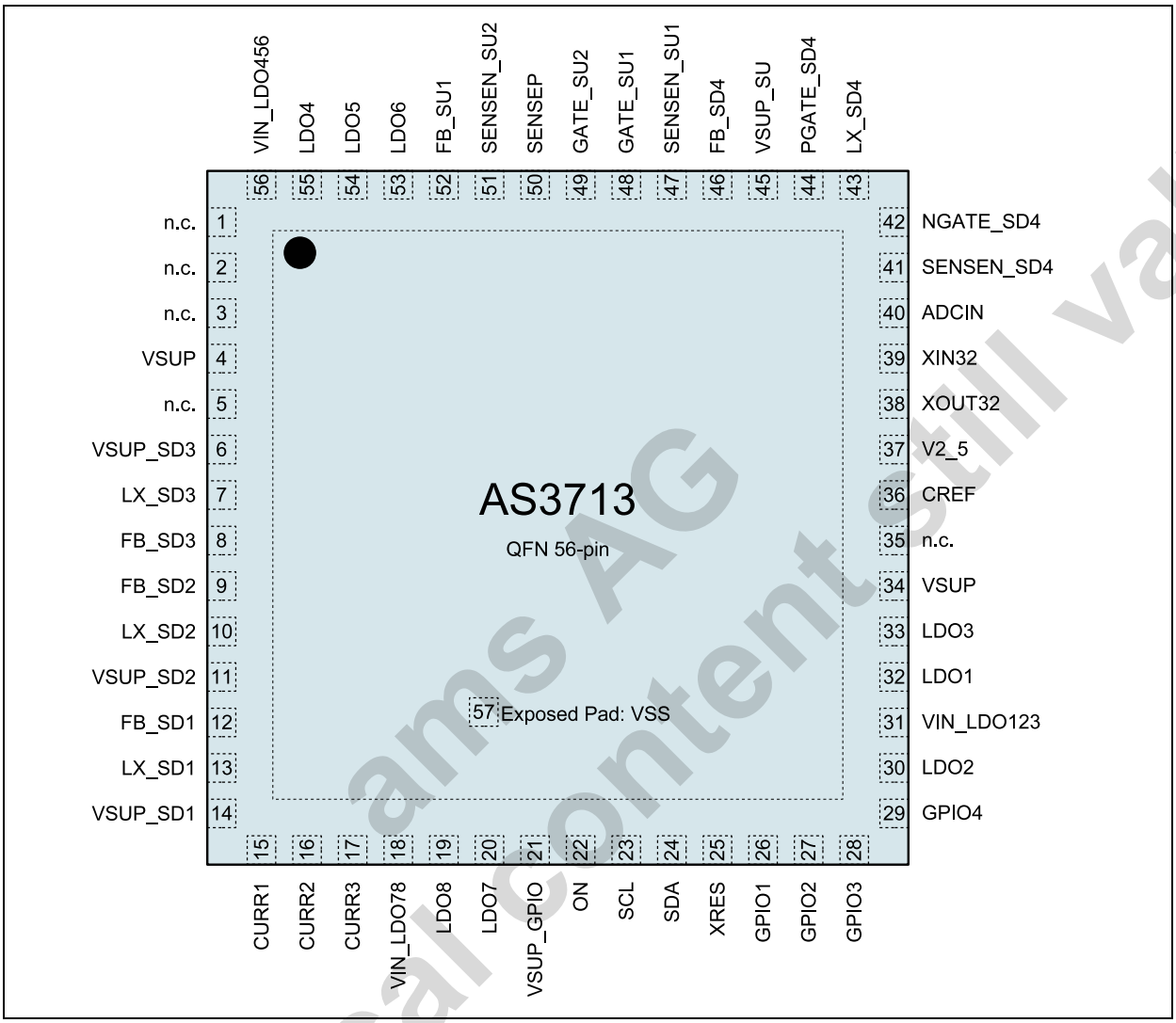
Figure 1. AS3713 *Block Diagram*



Contents

4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name AS3713	Pin Type	Description	if not used
1	n.c.	-	leave unconnected	open
2	n.c.	-	leave unconnected	open
3	n.c.	-	leave unconnected	open
4	VSUP	SUP IO	connect to VSUPx	always needed
5	n.c.	-	leave unconnected	open
6	VSUP_SD3	SUP IN	DCDC Step Down 3 Pos. Supply Terminal	always needed
7	LX_SD3	DIG OUT	DCDC Step Down 3 Switch Output to Coil	open
8	FB_SD3	ANA IN	DCDC Step Down 3 Feedback Pin	open
9	FB_SD2	ANA IN	DCDC Step Down 2 Feedback Pin	open
10	LX_SD2	DIG OUT	DCDC Step Down 2 Switch Output to Coil	open
11	VSUP_SD2	SUP IN	DCDC Step Down 2 Pos. Supply Terminal	always needed
12	FB_SD1	ANA IN	DCDC Step Down 1 Feedback Pin	open
13	LX_SD1	DIG OUT	DCDC Step Down 1 Switch Output to Coil	open
14	VSUP_SD1	SUP IN	DCDC Step Down 1 Pos. Supply Terminal	always needed
15	CURR1	ANA IO	Load Current Sink 1 Terminal	open
16	CURR2	ANA IO	Load Current Sink 2 Terminal	open
17	CURR3	ANA IO	Load Current Sink 3 Terminal	open
18	VINLDO78	SUP IN	LDO 7 & 8 Positive Supply Terminal, connect to VSUP	always needed
19	LDO8	ANA OUT	LDO8 Output	open
20	LDO7	ANA OUT	LDO7 Output	open
21	VSUP_GPIO	SUP IN	GPIO Positive Supply Terminal, connect to VSUP	always needed
22	ON	DIG IN	Power Up Input	open
23	SCL	DIG IN	2-wire Serial IF Clock Input	open
24	SDA	DIG IO	2-wire Serial IF Data I/O	open
25	XRES	DIG IO	Reset IO	open
26	GPIO1	ANA IO	General Purpose IO 1	open
27	GPIO2	ANA IO	General Purpose IO 2	open
28	GPIO3	ANA IO	General Purpose IO 3	open
29	GPIO4	ANA IO	General Purpose IO 4	open
30	LDO2	ANA OUT	LDO2 Output	open
31	VINLDO123	SUP IN	LDO 1, 2 & 3 Positive Supply Terminal, connect to VSUP	always needed
32	LDO1	ANA OUT	LDO1 Output	open
33	LDO3	ANA OUT	LDO3 Output	open
34	VSUP	SUP IO	connect to VSUPx	always needed
35	n.c.	-	leave unconnected	open
36	CREF	ANA IO	Reference Bypass Capacitor Terminal	always needed

Table 1. Pin Descriptions

Pin Number	Pin Name AS3713	Pin Type	Description	if not used
37	V2_5	ANA OUT	Internal 2.5V Regulator Supply Output	always needed
38	XOUT32	ANA OUT	RTC 32kHz Crystal Drive Terminal	open
39	XIN32	ANA IN	RTC 32kHz Crystal Feedback Terminal	open
40	ADCIN	ANAIO	ADC10 input	open
41	SENSEN_SD4	ANA IN	DCDC Step Down 4 Negative Sense Resistor Input	open
42	NGATE_SD4	ANA OUT	DCDC Step Down 4 ext. NMOS Gate Driver Output	open
43	LX_SD4	ANAIN	DCDC Step Down 4 Sense Input	open
44	PGATE_SD4	ANA OUT	DCDC Step Down 4 ext. PMOS Gate Driver Output	open
45	VSUP_SU	SUP IN	DCDC Step Down 4 Positive Supply Terminal, connect to VSUP	always needed
46	FB_SD4	ANA IN	DCDC Step Down 4 Feedback Pin	open
47	SENSEN_SU1	ANA IN	DCDC Step Up 1 Negative Sense Resistor Input	open
48	GATE_SU1	ANA OUT	DCDC Step Up 1 ext. NMOS Gate Driver Output	open
49	GATE_SU2	ANA OUT	DCDC Step Up 2 ext. NMOS Gate Driver Output	open
50	SENSEP	ANA IN	DCDC Step Up 1, 2 & Positive Sense Resistor Input	open
51	SENSEN_SU2	ANA IN	DCDC Step Up 2 Negative Sense Resistor Input	open
52	FB_SU1	ANA IN	DCDC Step Up 1 Feedback Pin	open
53	LDO6	ANA OUT	LDO6 Output	open
54	LDO5	ANA OUT	LDO5 Output	open
55	LDO4	ANA OUT	LDO4 Output	open
56	LDO456	SUP IN	LDO 4, 5 & 6 Positive Supply Terminal, connect to VSUP	always needed

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 8 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
	5V pins	-0.5	7.0	V	Applicable for pins VSUP, VSUP_SD1/2/3, VSUP_SU, VSUP_GPIO, VIN_LDO123/456/78, GPIO1/2/3/4, GATE_SU1/2, NGATE_SD4, PGATE_SD4, FB_SU1, SENSEP, SENSEN_SU1/2, SENSEN_SD4, CHGIN, VBAT, EXTBATSW, LDO1/2/3/4/5/6/7/8, FB_SD1/2/3/4, LX_SD1/2/3/4, XRES, SCL, SDA
	3V pins	-0.5	5.0	V	Applicable for pins V2_5, CREF, ON, ADCIN, XIN32, XOUT32
	30V pins	-0.5	32	V	Applicable for pin VUSB, XOFF, CURR1/2/3
	Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC JESD78
Continuous Power Dissipation (T_A = +70ºC)					
P_T	Continuous power dissipation		1.8	W	P_T[1] for QFN56 package (R_{TH} ~ 30K/W)
Electrostatic Discharge					
	Electrostatic Discharge HBM		±1.5	kV	Norm: JEDEC JESD22-A114F
Temperature Ranges and Storage Conditions					
T_{AMB}	Operating Temperature	-40	+85	ºC	
T_J	Junction Temperature		+125	ºC	
	Storage Temperature Range	-55	+150	ºC	
	Humidity non-condensing	5	85	%	
Temperature (soldering)					
T_{BODY}	Package Body Temperature		260	ºC	Norm IPC/JEDEC J-STD-020[2] The lead finish for Pb-free leaded packages is matte tin (100% Sn)
	Moisture Sensitive Level	3			Represents a max. floor life time of 168h

1. Depending on actual PCB layout and PCB used
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices”

6 Electrical Characteristics

VSUPx=+2.7V...+5.5V, T_A =-40ºC...+85ºC. Typical values are at VSUPx=+3.6V, T_A=+25ºC, unless otherwise specified.

The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VSUPx	Supply Voltage VSUP_x		2.7	3.6	5.5	V
VINLDO123	Supply Voltage for LDO 1, 2 & 3		2.7	3.6	5.5	V
VINLDO456	Supply Voltage for LDO 4, 5 & 6		1.8	3.6	5.5	V
VINLDO78	Supply Voltage for LDO 7 & 8		1.8	3.6	5.5	V
V2_5	Voltage on Pin V2_5		2.4	2.5	2.6	V
I_{low_power}	Low Power current	@ VSUPx = 4.2V		220		µA
I_{power_off}	Power-Off current	All regulators off V2_5 on		10		µA

7 Typical Operating Characteristics

please see operating characteristics in the block description chapters.

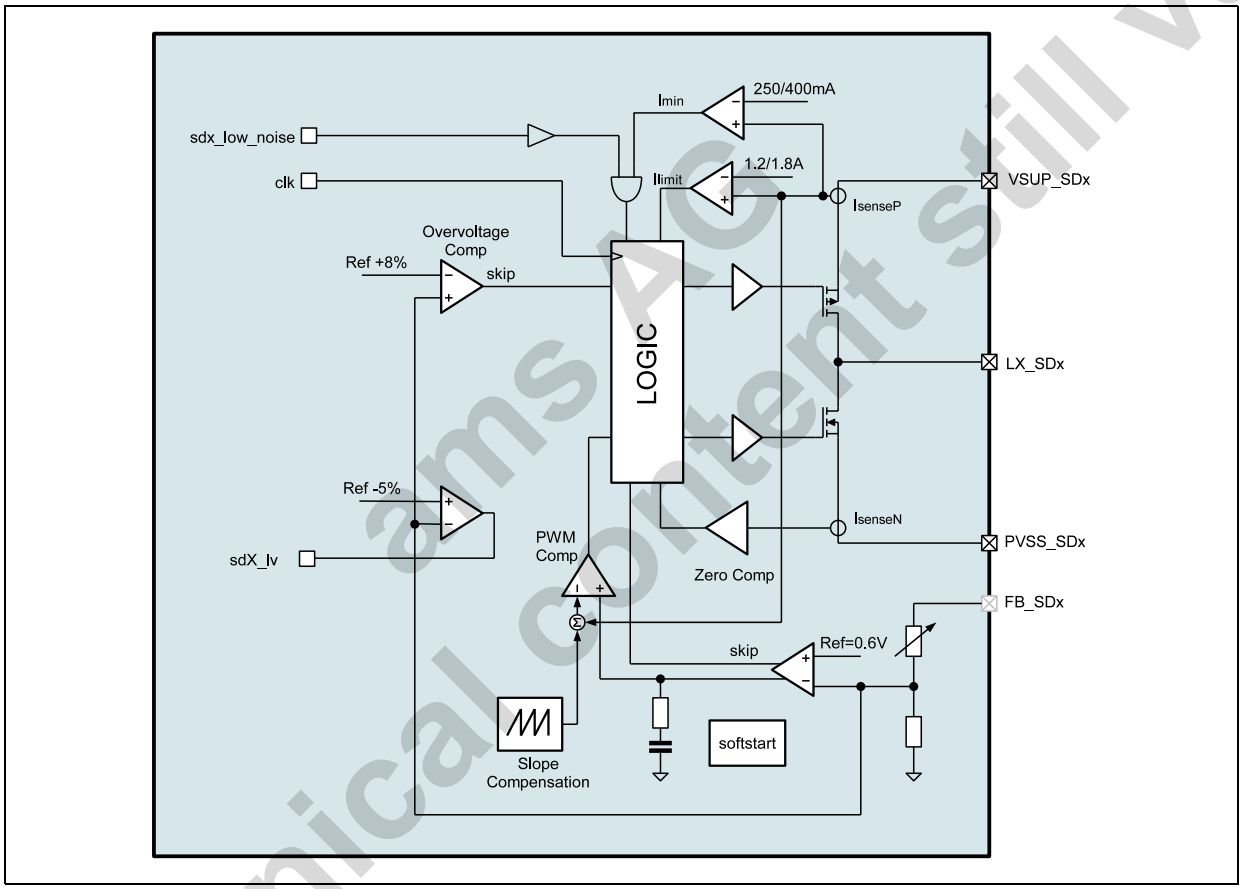
8 Detailed Description - Power Management Functions

8.1 DCDC Step-Down Converter

8.1.1 General Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 1A (SD2, SD3) and 1.5A for SD1, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC and the coil during overload condition.

Figure 3. Step Down DC/DC Converter Block diagram



8.1.2 Mode Settings

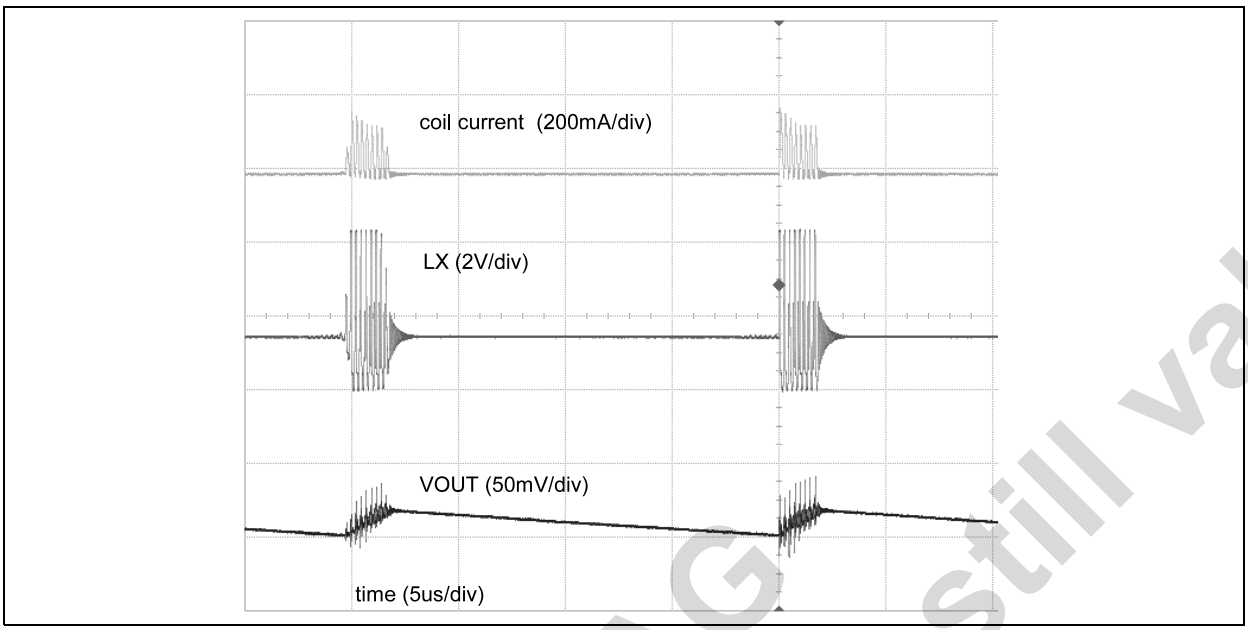
Low ripple, low noise operation:

Bit settings: sdX_low_noise=1

In this mode there is no minimum coil current necessary before switching off the PMOS. As long as the load current is superior to the ripple current the device operates in continuous mode. When the load current gets lower, the discontinuous mode is triggered. As result, the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to tmin_on to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences.

Only in the case the load current gets so small that less than the minimum on-time of the PMOS would be needed to keep the loop in regulation the regulator will enter low power mode operation. The crossover point is about 15mA for Vin=3V, Vout=1.2V, 1uH, 4MHz.

Figure 4. DCDC Buck with enabled low noise mode



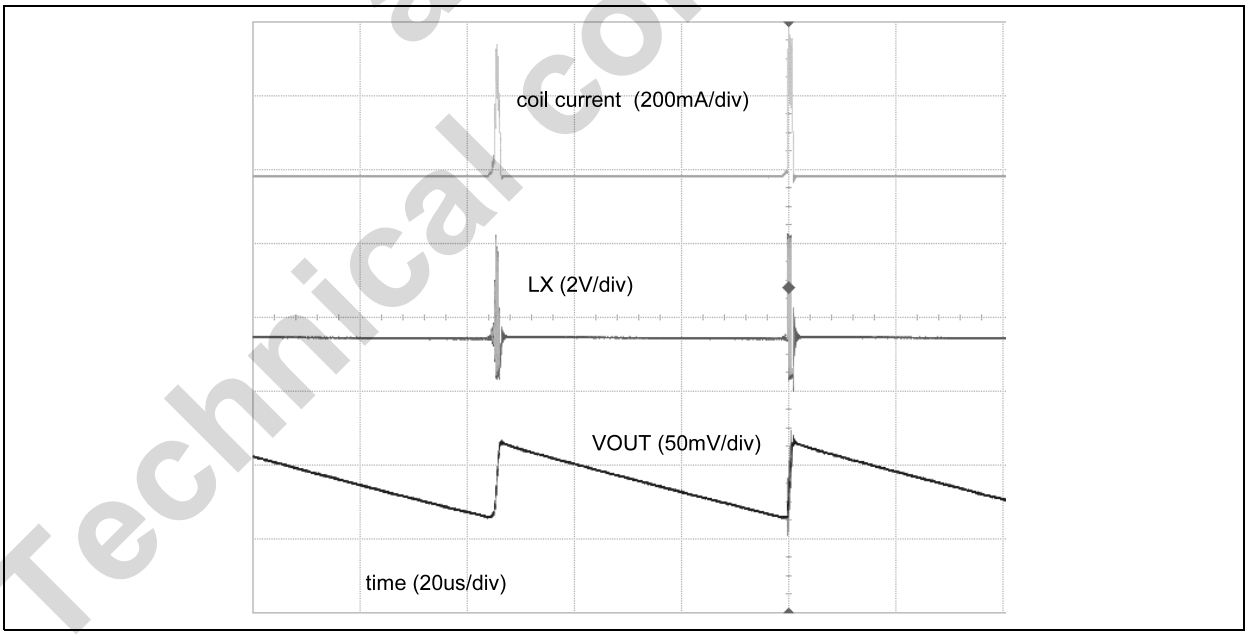
High efficiency operation (default setting):

Bit settings: sdX_low_noise=0

In this mode there is a minimum coil current necessary before switching off the PMOS. As a result there are less pulses necessary at low output loads, and therefore the efficiency at low output load is increased. As drawback this mode increases the ripple up to a higher output currents.

The crossover point to low power mode is already reached at reasonable high output currents. (e.g. @110mA for Vin=3V, Vout=1.2V, 1uH, 4MHz)

Figure 5. DCDC Buck with disabled low noise mode



It's possible to switch between these two modes during operation:

Low power mode operation (automatically controlled):

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at +/-5% of the target value to react quickly on large over/undershoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

DVM (Dynamic Voltage Management)

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

DVM can be selected for all step-down converters, but only for one at a time. (see **sd_dvm_select** and **dvm_time** description)

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs an 22uF output capacitor instead the 10uF one to guarantee the stability of the regulator. the mode is enabled by setting sdX_fast =1.

Selectable Frequency Operation

Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency. The frequency for SD1, SD2 and SD3 can be set to 2, 3 or 4MHz. This mode is selected by setting sdX_freq and sdX_fsel to the appropriate values.

100% PMOS ON Mode for Low Dropout Regulation

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

8.1.3 Step-Down Converter Configuration Modes

The step down DCDC converters have two configuration modes to deliver different output currents for the applications. The operating mode is selected by setting the bit **sd3_slave** (the default is set by the Boot-OTP).

Figure 6. DC/DC step-down SD1, SD2, SD3 Normal Operating Mode; ***sd3_slave*** *= 0*

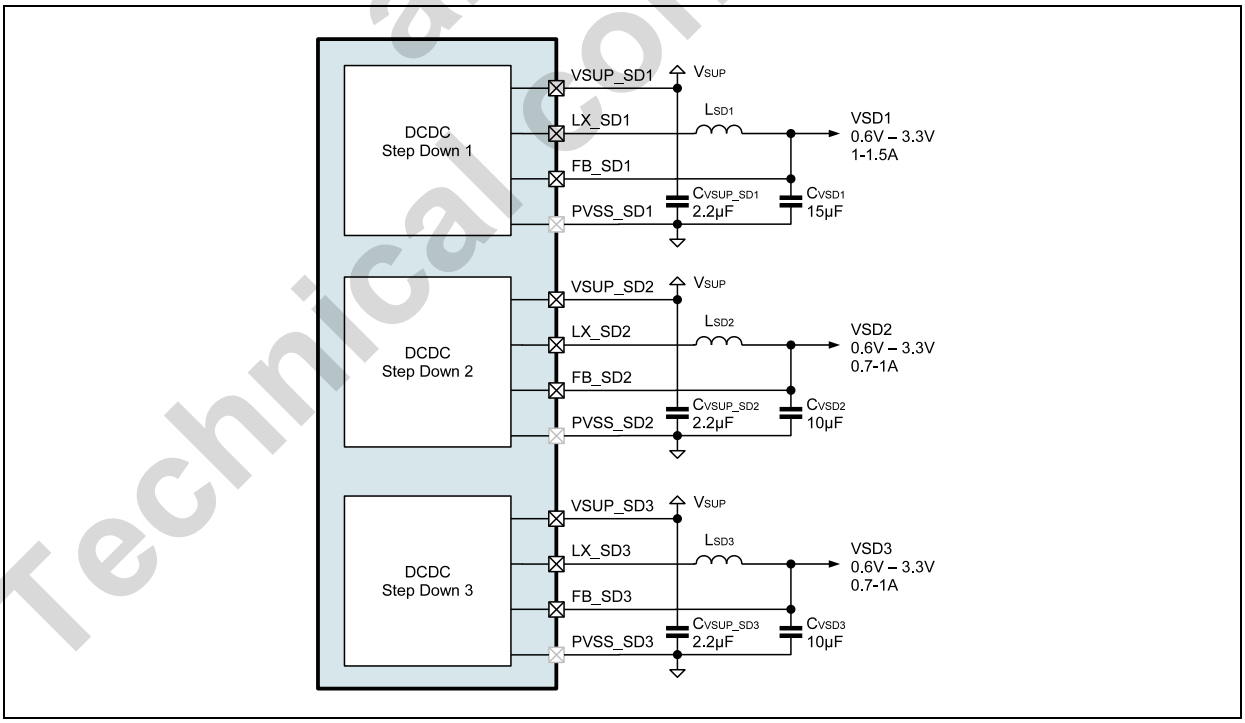
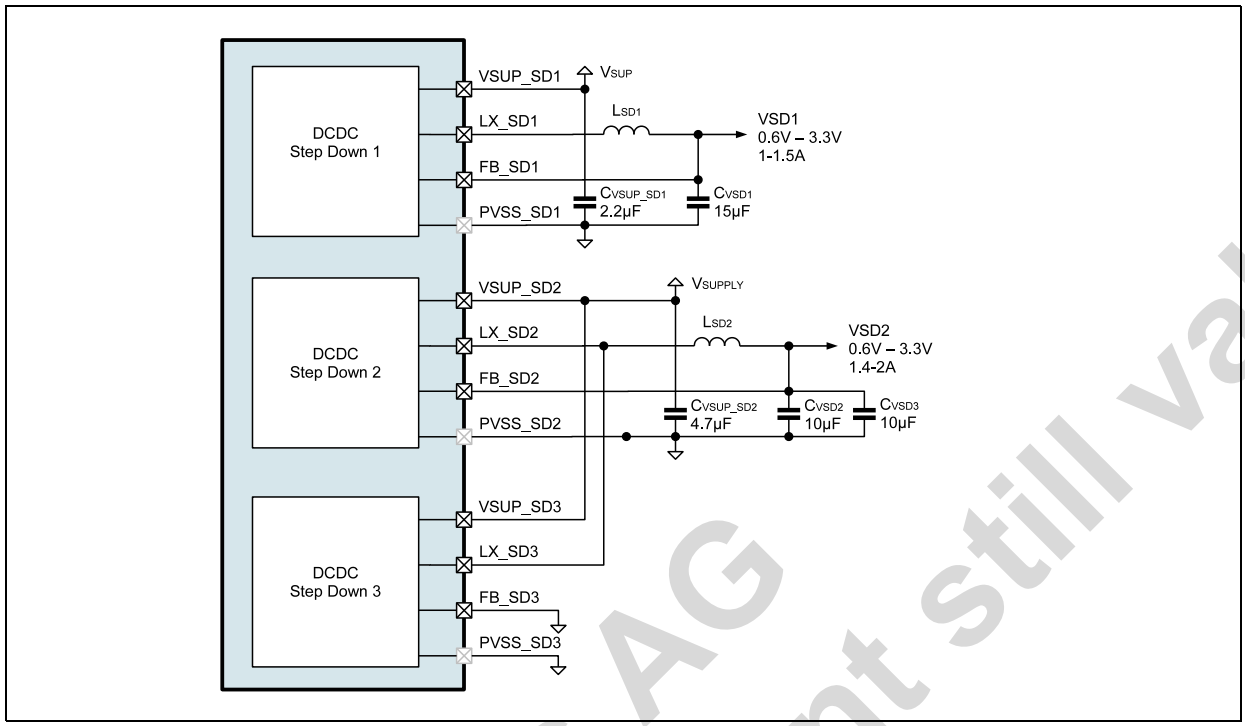


Figure 7. DC/DC step-down SD1, SD2, SD3 2A Operating Mode; **sd3_slave** *= 1*



8.1.4 Parameter

Table 4. Step Down DC/DC Converter Parameters

Symbol	Parameter	Note	Min	Typ	Max	Unit
VIN	Input voltage	Pin VSUP_SDx	2.7		5.5	V
VOUT	Regulated output voltage		0.6125		3.35	V
VOUT_tol	Output voltage tolerance	min. 40mV	-3		+3	%
ILIMIT	Current limit	SD1		1.8		A
		SD2, SD3		1.2		A
RPSW	P-Switch ON resistance	SD1; VSUP_SDx=3.0V		0.17	0.4	Ω
		SD2, SD3; VSUP_SDx=3.0V		0.25	0.5	Ω
RNSW	N-Switch ON resistance	SD1; VSUP_SDx=3.0V		0.17	0.4	Ω
		SD2, SD3; VSUP_SDx=3.0V		0.25	0.5	Ω
Iload	Load current	SD1	0		1.5	A
		SD2, SD3	0		1	A
f_{SW}	Switching frequency	sdX_frequ=1, sdX_fsel=1; fclk_int =4MHz		4		MHz
		sdX_frequ=1, sdX_fsel=0; fclk_int =4MHz		3		MHz
		sdX_frequ=0, sdX_fsel=0; fclk_int =4MHz		2		MHz
tmin_on	minimum on time			40		ns
ηeff	Efficiency	Iout=300mA, Vout=2V, VSUP=3.5V		92		%
IVDD	Current consumption	Operating current without load		60		µA
		Shutdown current		0.1		

Table 5. Step Down DC/DC External Components

Symbol	Parameter	Note	Min	Typ	Max	Unit
CFB_SD1	Output capacitor	Ceramic X5R or X7R	10.0	15		µF
		Ceramic X5R or X7R, fast mode=1	20.0	30		µF
CFB_SD2-3	Output capacitor	Ceramic X5R or X7R	8.0	10		µF
		Ceramic X5R or X7R, fast mode=1	16.0	20		µF
CVSUP_SD1-3	Input capacitor	Ceramic X5R or X7R		2.2		µF
LSD1-SD3	Inductor	4MHz operation		1		µH
		3MHz operation		1		
		2MHz operation		2.2		

All measurements where done with 55mΩ chip coils (Murata LQM2HPN1R0MG0). Using coils with lower on-resistance will increase the efficiency especially at higher output currents.

Figure 8. Step Down DC/DC SD1 Efficiency vs. Output Current; VSUP = 3.0V, 3MHz operation, TA = +25ºC

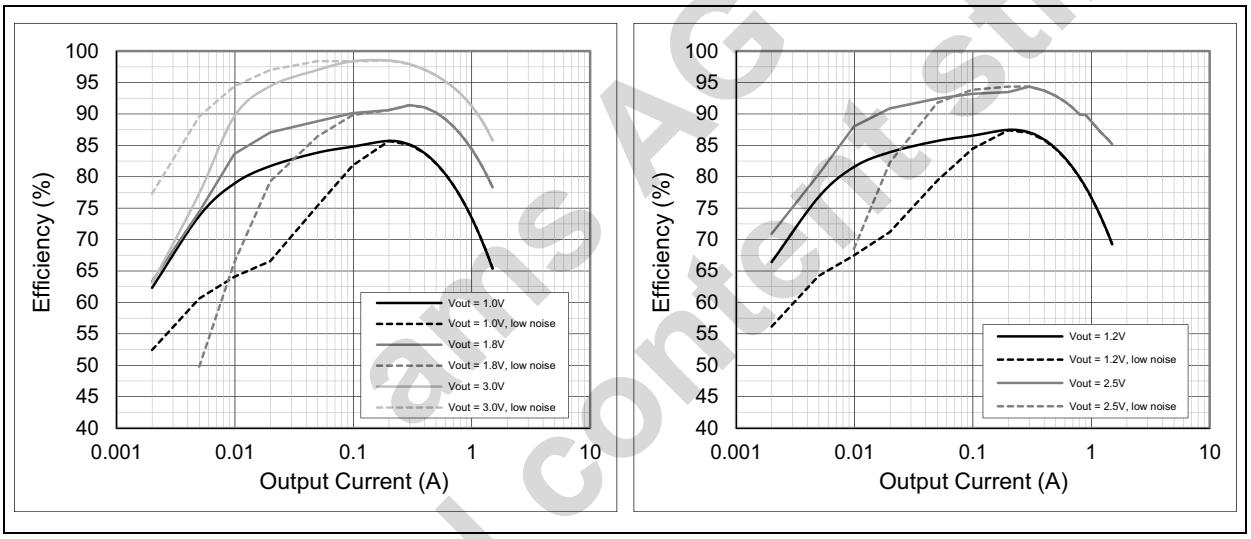


Figure 9. Step Down DC/DC SD1 Efficiency vs. Output Current; VSUP = 3.8V, 3MHz operation, TA = +25ºC

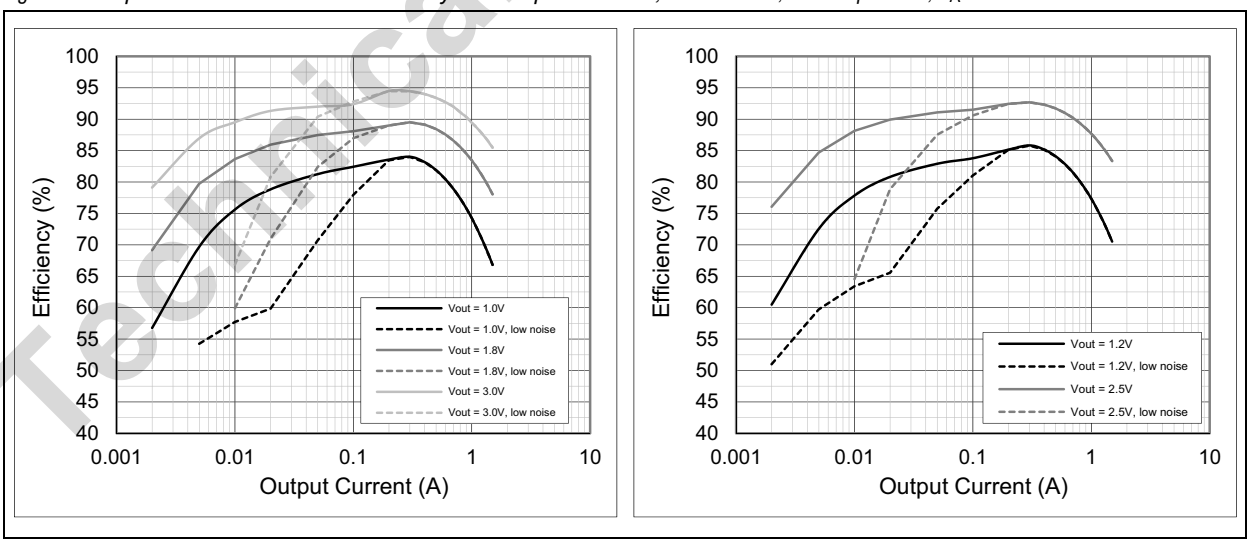


Figure 10. Step Down DC/DC SD2 & SD3 Efficiency vs. Output Current; V_{SUP} = 3.0V, 3MHz operation, T_A = +25ºC

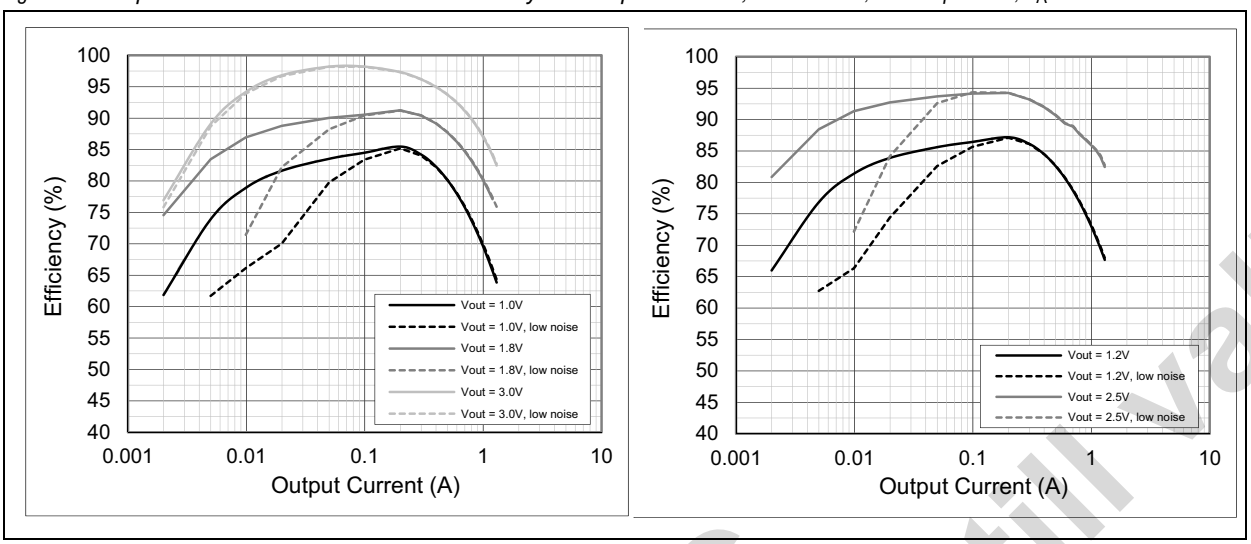
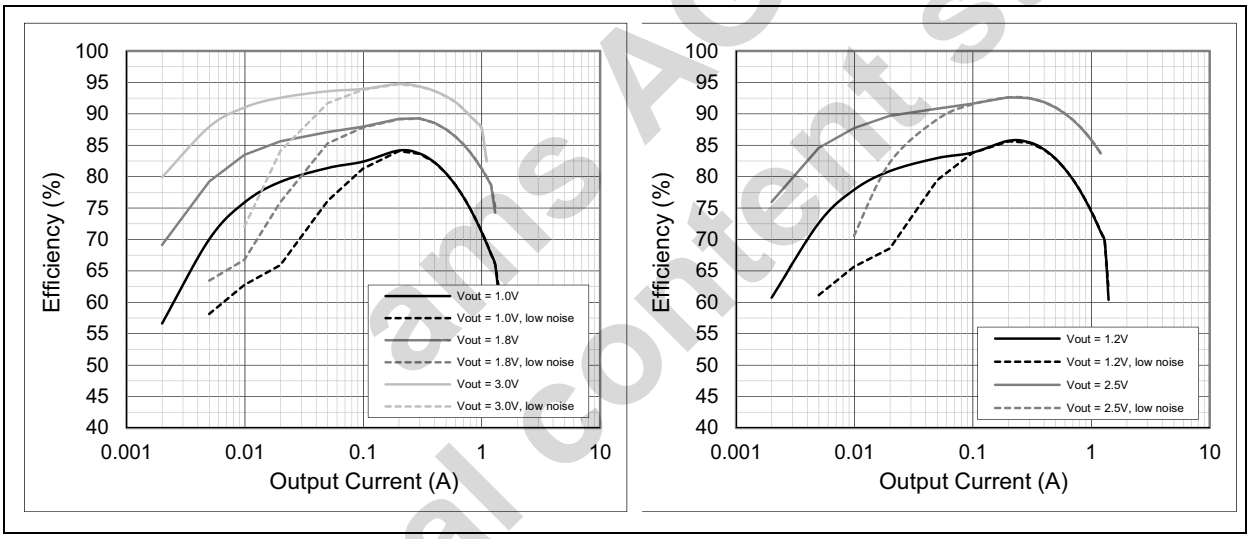


Figure 11. Step Down DC/DC SD2 & SD3 Efficiency vs. Output Current; V_{SUP} = 3.8V, 3MHz operation, T_A = +25ºC

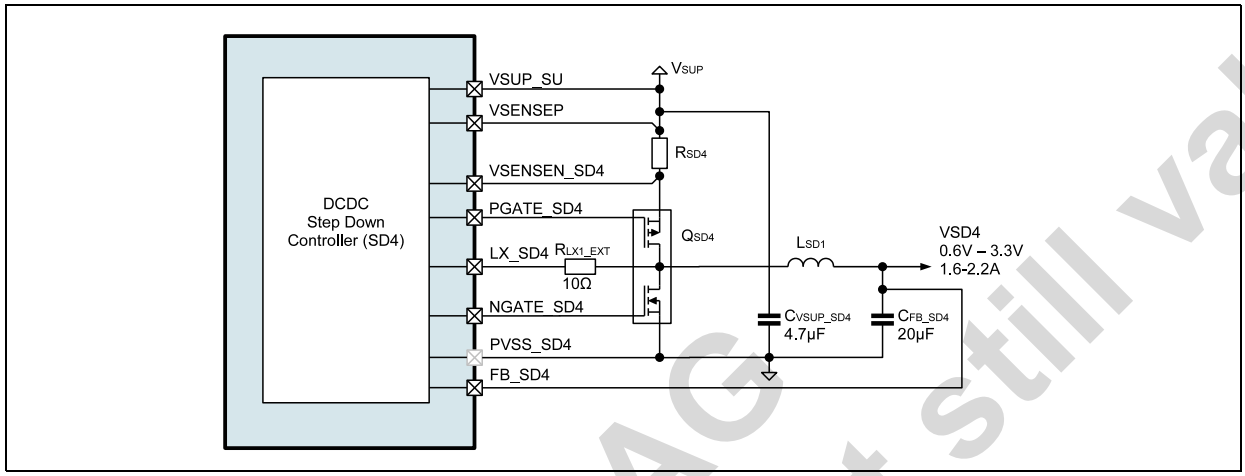


8.2 DCDC Step-Down Controller

8.2.1 General Description

The Step-Down controller SD4 uses a paired external NMOS, PMOS to achieve higher output currents. the maximum output current is determined by the external transistor and shunt used.

Figure 12. DC/DC step-down Controller



8.2.2 Parameter

Table 6. Step Down DC/DC Controller Parameters

Symbol	Parameter	Note	Min	Typ	Max	Unit
VIN	Input voltage	Pin VSUP_SDx	2.7		5.5	V
VOUT	Regulated output voltage		0.6125		3.3	V
VOUT_tol	Output voltage tolerance	min. 40mV	-3		+3	%
V_{rsense_max}	Current limit voltage at Rsense	E.g.: 2.6A for 0.033Ω sense resistor		100		mV
f_{SW}	Switching frequency	fclk_int = 4MHz		1		MHz

Table 7. Step Down DC/DC Controller External Components

Symbol	Parameter	Note	Min	Typ	Max	Unit
External Components 1.6A						
QSD4	paired NMOS-PMOS	FDC6327C	PMOS: Ron=250mOhm, 1.6A NMOS: Ron=120mOhm, 2.7A			
RSD4	shunt	0.15W; +/- 1%		50		mΩ
CFB_SD4	Output capacitor	Ceramic X5R or X7R	16.0	20		µF
		Ceramic X5R or X7R, fast mode=1	32.0	40		µF
CVSUP_SD4	Input capacitor	Ceramic X5R or X7R		10		µF
LSD4	Inductor	2A rated, 1MHz operation		2.2		µH
External Components 2.2A						
QSD4	paired NMOS-PMOS	FDC6420C	PMOS: Ron=190mOhm, 2.2A NMOS: Ron=95mOhm, 3A			
RSD4	shunt	0.2W; +/- 1%		33		mΩ

Table 7. Step Down DC/DC Controller External Components

Symbol	Parameter	Note	Min	Typ	Max	Unit
CFB_SD4	Output capacitor	Ceramic X5R or X7R	24.0	30		µF
		Ceramic X5R or X7R, fast mode=1	48.0	60		µF
CVSUP_SU	Input capacitor	Ceramic X5R or X7R		10		µF
LSD4	Inductor	2.5A rated, 1MHz operation		1.5		µH
External Components 3A						
QSD4	paired NMOS-PMOS	NTHD3102C	PMOS: Ron=83mOhm, 4.2A NMOS: Ron=37mOhm, 5.5A			
RSD4	shunt	0.3W; +/- 1%		25		mΩ
CFB_SD4	Output capacitor	Ceramic X5R or X7R	32.0	40		µF
		Ceramic X5R or X7R, fast mode =1	64.0	80		µF
CVSUP_SU	Input capacitor	Ceramic X5R or X7R		10		µF
LSD4	Inductor	3A rated, 1MHz operation		1		µH

All measurements where done with the 2.2A transistors (Fairchild FDC6420C) and 70mΩ chip coils (Murata LQM2HPN1R0MG0). Using coils with lower on-resistance will increase the efficiency especially at higher output currents.

Figure 13. Step-Down DC/DC SD4 Controller Efficiency vs. Output Current; V_{SUP} = 3.0V, T_A = +25ºC

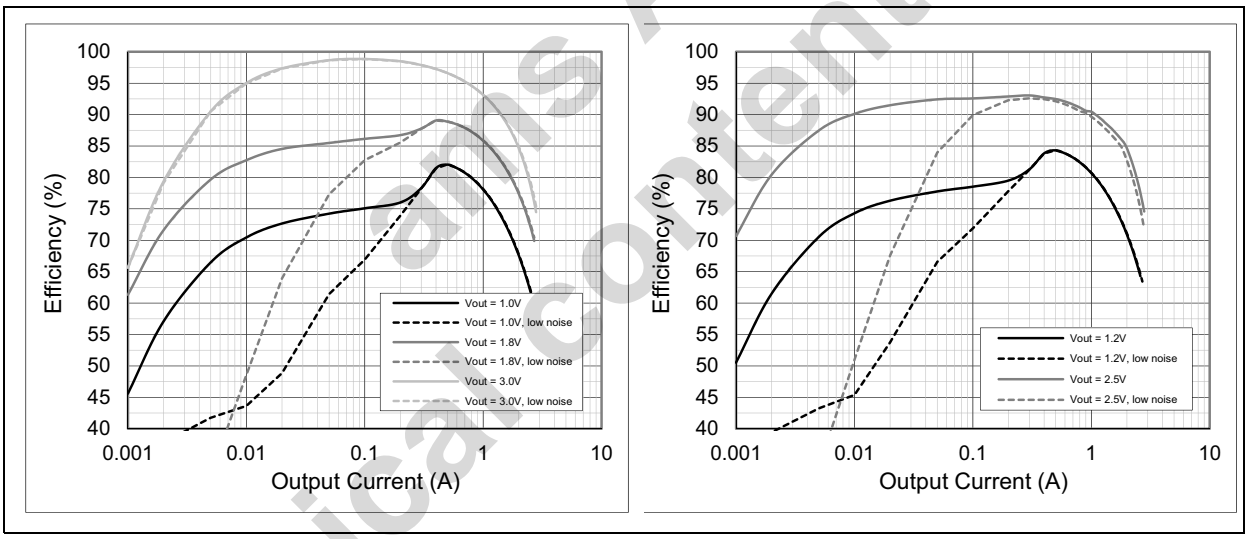
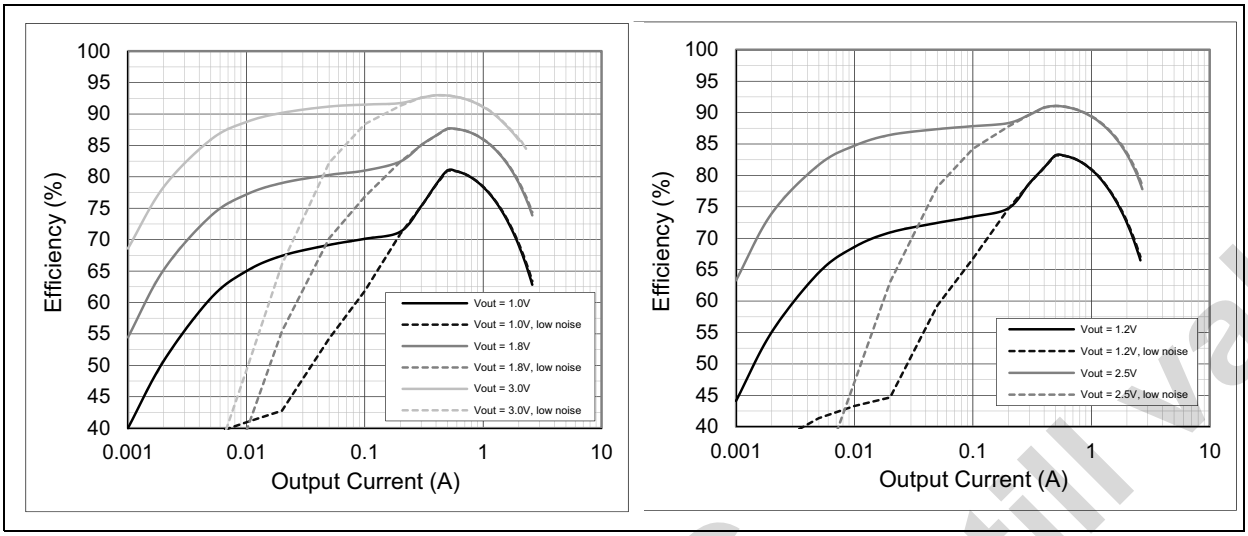


Figure 14. Step-Down DC/DC SD4 Controller Efficiency vs. Output Current; V_{SUP} = 3.8V, T_A = +25ºC



8.3 Analog LDO Regulators

8.3.1 General description

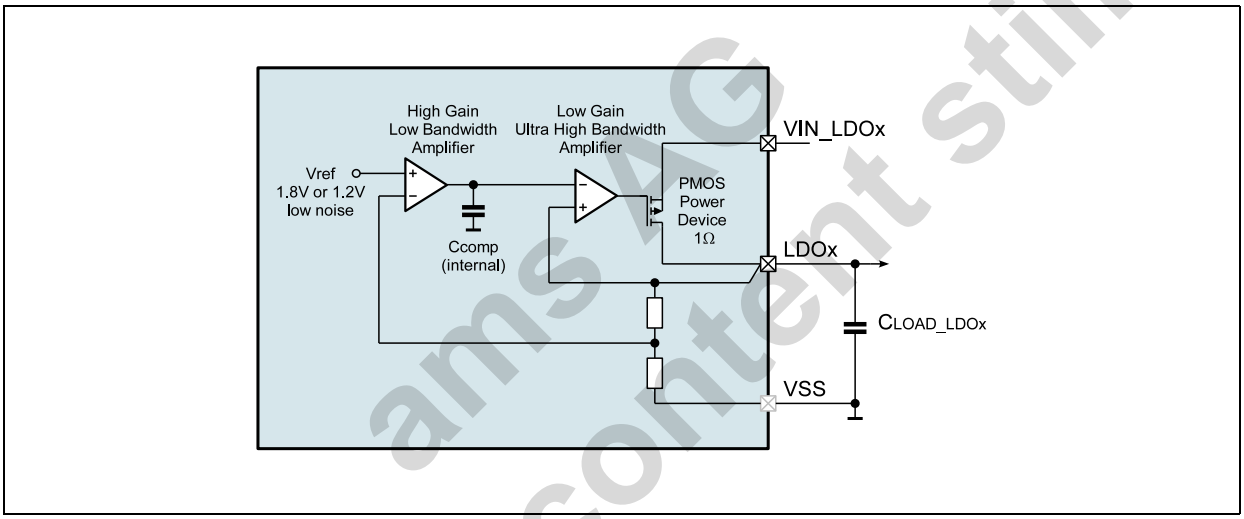
LDO1 and LDO2 are designed to supply sensitive analogue circuits like LNA's, Transceivers, VCO's and other critical RF components of cellular radios. Another application is the supply of audio devices or as a reference for AD and DA converters. The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of 1µF ±20% (X5R) or 2.2µF +100/-50% (Z5U). The low ESR of these caps ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress the PA-ripple on the battery in TDMA systems at the output. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power device enables the device to deliver up to IOUT current even at nearly discharged batteries without any decrease of performance.

The default guaranteed operating current during start-up is 150mA, but can be set to 250mA with ldoX_ilimit = 1.

To save power in low-power states where the full performance is not needed the bias current can be reduce by setting **reg_low_bias_mode**=1.

Figure 15. Analog LDO Block diagram



8.3.2 Parameter

Table 8. Analog LDO (LDO1, LDO2) Characteristics
VLDO123_IN=3.7V; ILOAD=150mA; Tamb=25ºC; CLOAD =2.2µF (Ceramic); unless otherwise specified

Symbol	Parameter	Note	Min	Typ	Max	Unit
VLDO123_IN	Supply voltage range		2.7		5.5	V
IOUT	Output current[1]	ldoX_ilimit = 0	0		150	mA
		ldoX_ilimit = 1	0		250	
R_{ON}	On resistance	LDO1, LDO2			1	Ω
PSRR	Power supply rejection ratio	f=1kHz	70			dB
		f=100kHz	40			
I_{OFF}	Shut down current				100	nA
I_{VDD}	Supply current	without load		50		µA
		without load, **reg_low_bias_mode**=1		30		µA
Noise	Output noise	10Hz < f < 100kHz			50	μV_{rms}
t_{start}	Startup time	low current limit used during start-up			200	µs

Table 8. Analog LDO (LDO1, LDO2) Characteristics
VLDO123_IN=3.7V; ILOAD=150mA; Tamb=25ºC; CLOAD =2.2µF (Ceramic); unless otherwise specified

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{out}	Output voltage		1.2		3.3	V
Vout_tol	Output voltage tolerance	min. 40mV	-3		3	%
$V_{LineReg}$	Line regulation	Static	-1		1	mV
		Transient; Slope: t_r=10µs	-10		10	
$V_{LoadReg}$	Load regulation	Static	-1		1	mV
		Transient; Slope: t_r=10µs	-10		10	
$I_{LIMIT\_LDO1,2\_L}$	low current limit	ldoX_ilimit = 0		300		mA
$I_{LIMIT\_LDO1,2\_H}$	high current limit	ldoX_ilimit = 1		500		mA
$C_{LOAD\_LDO1,2\_L}$	Ceramic load capacitor	LDO1 / LDO2; ldoX_ilimit = 0	1		5	µF
$C_{LOAD\_LDO1,2\_H}$	Ceramic load capacitor	LDO1 / LDO2; ldoX_ilimit = 1	2		5	µF

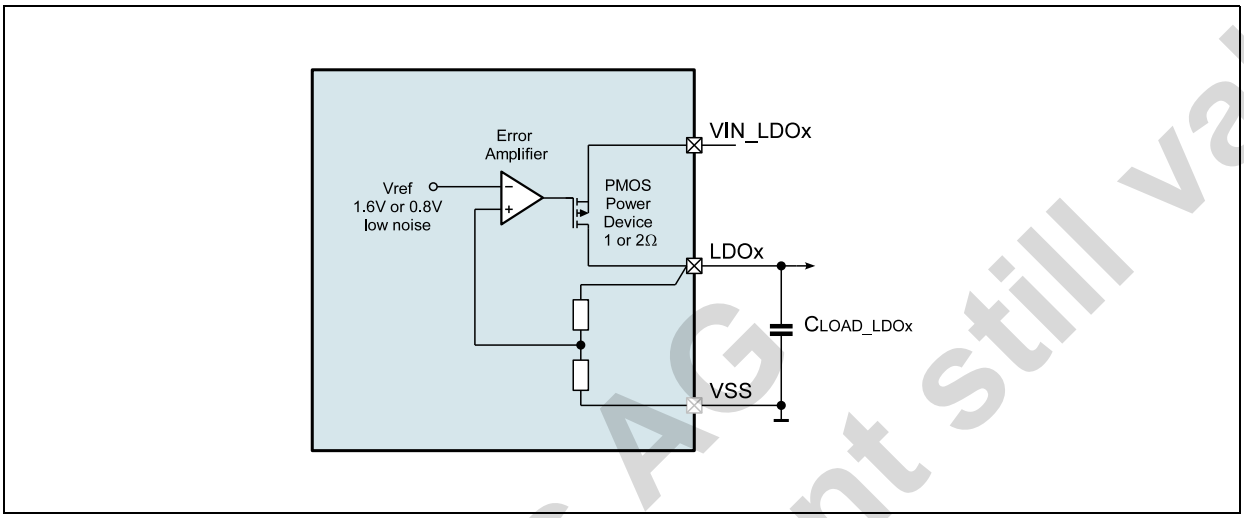
1.Guaranteed by design and verified by laboratory evaluation and characterization; not production tested.

8.4 Digital LDO Regulators

8.4.1 General Description

Digital LDOs offer a wide input (1.8V to 5.5V) as well as a wide output (0.9 to 3.3V) voltage range to be used for general purpose peripheral supply. Up to 300mA possible output currents are offered with good noise and regulation performance and very low quiescent current even suitable for stand-by power supply.

Figure 16. Digital LDO Block diagram



8.4.2 Parameter

Table 9. Digital LDO (LDO3, LDO4, LDO5, LDO6, LDO7, LDO8) Characteristics
VLDOx_IN=3.7V; ILOAD=150mA; Tamb=25ºC; CLOAD =1µF (Ceramic); unless otherwise specified

Symbol	Parameter	Note	Min	Typ	Max	Unit
VLDO123_IN	Supply voltage range		2.7		5.5	V
VLDO456_IN	Supply voltage range		1.75		5.5	V
VLDO78_IN	Supply voltage range		1.75		5.5	V
IOUT	Output current[1]	ldoX_ilimit = 0	0		150	mA
		ldoX_ilimit = 1	0		300	mA
RON	On resistance	LDO4, LDO5, LDO6			1	Ω
		LDO3, LDO7, LDO8			2	Ω
PSRR	Power supply rejection ratio	f=1kHz	60			dB
		f=100kHz	30			
IOFF	Shut down current			100		nA
IVDD	Supply current	without load		30	43	µA
tstart	Startup time	low current used during start-up			200	µs
Vout	Output voltage	Vsupply>3.0V, VCP=5.2V, Iout<200mA	0.9		3.3	V
Vout_tol	Output voltage tolerance	min. 40mV	-3		3	%
VLineReg	Line regulation	Static		0.07		%/V
		Transient; Slope: tr=15µs; delta 1V		20		mV
VLoadReg	Load regulation	Static		0.014		%/mA
		Transient; Slope: tr=15µs; 1mA->300mA		30		mV

Table 9. Digital LDO (LDO3, LDO4, LDO5, LDO6, LDO7, LDO8) Characteristics
VLDOx_IN=3.7V; ILOAD=150mA; Tamb=25ºC; CLOAD =1µF (Ceramic); unless otherwise specified

Symbol	Parameter	Note	Min	Typ	Max	Unit
ILIMIT_LDO3-8_L	low current limit	ldoX_ilimit = 0		300		mA
ILIMIT_LDO3-8_H	high current limit	ldoX_ilimit = 1		500		mA

1.Guaranteed by design and verified by laboratory evaluation and characterization; not production tested

8.5 Low power LDO V2_5 Regulators

8.5.1 General Description

The low power LDO V2_5 is needed to supply the chip core (analog and digital) of the device. It is designed to get the lowest possible power consumption, and still offering reasonable regulation characteristics. The regulator has two supply inputs selecting automatically the higher one. This gives the possibility to supply the chip core either with the battery or with the charger depending on the conditions. Bulk switch comparators are used to avoid any parasitic current flow. To ensure high PSRR and stability, a low-ESR ceramic capacitor of min. 1µF must be connected to the output.

8.5.2 Parameter

Table 10. Low power LDO (V2_5) Characteristics, V_{BAT} *=3.7V; ILOAD_ext=0; Tamb=25ºC; CLOAD =1 µF (Ceramic); unless otherwise specified*

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{BAT}	Supply voltage rage		2.7		5.5	V
V_{USB}			4.2		5.5	
R_{ON}	On resistance	Guaranteed per design		50		Ω
I_{OFF}	Shut down current			100		nA
I_{VDD}	Supply current	Guaranteed per design, consider chip internal load for measurements.		3		µA
t_{start}	Startup time			200		µs
V_{out}	Output voltage		2.4	2.5	2.6	V

8.6 DCDC Step-Up Converter

8.6.1 General Description

The DC/DC Step Up converter is a high efficiency current mode PWM regulator, which provides an output voltage dependent on the maximum VDS voltage of the external transistor, and maximum load current selectable by the external shunt resistor.
For Example:

- 5V, 0.5-1A @ 1Mhz
- 25V, 50mA @ 1MHz
- 40V, 20mA @ 500kHz

A constant switching frequency results in a low noise on supply and output voltage.

Figure 17. DC/DC step-up Converter 1